Chapter 2

Resonant Tunneling and Two-dimensional Gate Transistors

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Additional information is available at the end of the chapter

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Abstract

In this chapter, a new type of field-effect transistors is considered with a gate and a channel on a basis of two-dimensional systems of carriers. The key point of the device is that the systems are different. In particular, they are formed in different quantum wells or valleys of the carriers spectrum. Due to this difference, the coherent tunneling is reduced and inelastic tunneling requires additional excitations with significant momentum and energy. This decreases the tunneling rate significantly. For example, the intervalley tunneling rate is less than intravalley that in 9 orders of magnitude in GaAs/AlAs heterostructures. The two-dimensional character also can decrease the tunnel probability in a wide voltage range. Influence of further miniaturization will be discussed for the new types of the transistors.

Keywords: field-effect transistor (FET), two-dimensional system of carriers, resonant tunneling

1. Introduction

Size-shrinkage as a main trend of the electronics development has already brought not only cut-off frequency but also energy consumption increase. In addition, a current leakage of the field-effect transistor (FET) has also increased. The leakage current consists of a current from the drain to the source (I_{sd}) due to overlapping of the p-n transition regions in the contacts and a tunneling current from the gate to the channel (I_g). Moreover, in the FET size-shrinkage, the I_g part becomes more important; for example, at 130 nm technology, it takes less than 5% of whole leakage, at 90 nm, it takes 40%, and at 65 nm, it takes 90%, respectively [1]. To decrease the I_{sd}, SOI substrates and vertical orientations of the FET are used. This effectively decreases the width of the cross section for the I_{sd}. Note that this accompanies the two-dimensional character of the FET channel. To diminish the I_g, high-k dielectrics are used as the gate insulators. This increases the capacity between the gate and the channel and decreases the pinch-off voltage or energy of

the tunneling carriers. Another way is to use quantum well for the FET channel, for example, InSb layer [2]. This also diminishes gate voltage because the band inversion is not required. As a result, the cut-off frequency can be increased up to 300 GHz. One can see that two-dimensional systems of carriers (2DSC) are inherent to the modern nanoFET.

In this chapter, an application of the 2DSC in a FET gate is considered for further leakage reducing.

2. Resonant tunneling of carriers

Tunneling has been revealed by Esaki [3] and studied mainly in semiconductor diodes since 1958. Several years before, Shriffer had proposed size-quantization of the carriers in semiconductor films [4] that was observed by Tsui in InAs tunneling diode [5]. Then Esaki [6] and Kazarinov and Suris [7] proposed carriers resonant tunneling (CRT) in semiconductor heterostructures. In 1974, this effect was observed [6]. On the base CRT, a resonant-tunneling diode (RTD) [8] and resonant-tunneling transistor (RTT) [9] are realized as highest-frequency solid-state devices up to date. Carriers tunneling is well-known to play a negative role in modern c CMOS transistors made on the base technology of 45 nm or less. However, the instances of the RTD and RTT give us a hope that a proper application of the CRT can improve the situation in the FET. To clarify this, let us consider the CRT in detail.

Usually, the CRT is observed in a double-barrier heterostructure, the conduction band profile of which is shown in **Figure 1**. In a thin layer of a narrow band gap semiconductors, the localized states are forming and called subband states or levels. The ground subband state has energy E_{z0}. As a result, the barriers transparency has sharp peaks up to 1 in its energy dependency when the incident-electron energy along z direction E_z approaches to E_{z0} and, what is more important to this chapter, it decreases down to $T_z = 10^{-4}$ at intermediate energy [6].

To calculate current-voltage characteristics, one can consider model of sequential tunneling [10]. In this model, tunneling of the electron can be described as sequential quantum transition perturbed by tunnel Hamiltonian T [11]. In first term of the perturbation theory, one can expect to find the probability of the transition as follows:

$$W_{if} = \frac{2\pi}{\hbar}|\Psi_i|T|\Psi_f|^2\delta(E_f - E_i) \tag{1}$$

where $\hbar$ is Planck constant, $\Psi_{i,f}$ are electron wave functions, $E_{i,f}$ are energy of initial and final states. Since the potential is in the one z direction, the electron wave functions are as follows:

$$\Psi_{i,f} = \chi_{i,f}(z)\exp\left(\frac{i}{\hbar}[p_{xi,f}x + p_{yi,f}y]\right) \tag{2}$$

Then the matrix element of T is as follows:

$$\Psi_i|T|\Psi_f = T_{if}\delta(p_{xf} - p_{xi})\delta(p_{yf} - p_{yi}) \tag{3}$$

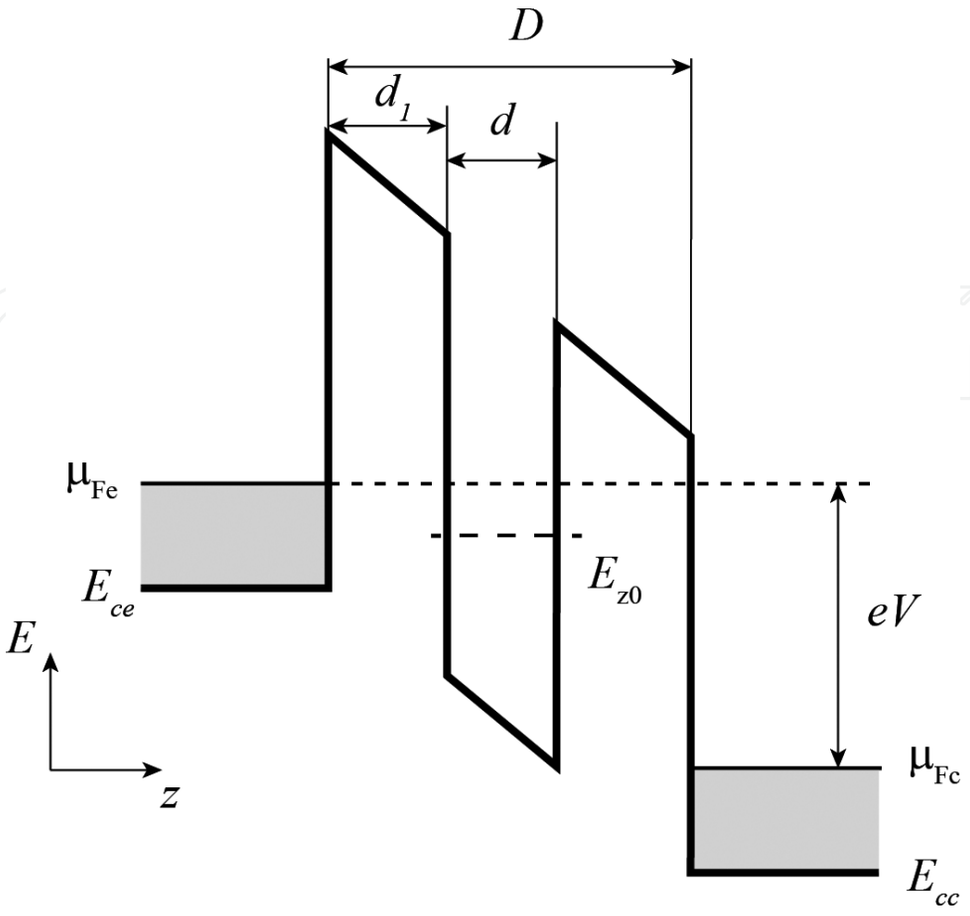

Figure 1. Energy profile of the conduction band bottom of the two barrier heterostructure.

where $T_{if} = \chi_i|T|\chi_f$. As one can see from Eqs. (1) and (3), the tunneling electrons save its energy and planar components of the momentum. Since the electron effective mass is equal on both sides of the barrier, the tunneling electron also saves E_z energy. To calculate current, one should sum transition probabilities timed on electron charge from given equation:

$$I = \sum_{i,f} eW_{if}(f_i - f_f) \tag{4}$$

where $f_{i,f,}$ Fermi-Dirac distribution functions of electrons in initial and final states. Let us suppose that T_{if} is a constant, then $T_{if} = \tau^{-1}$, where τ is a tunneling rate of the electrons. According to Eqs. (1) and (3), one can get the following:

$$I = \frac{e}{\tau} \sum_{i(E_{z0}), f(E_{z0})} (f_i - f_f) = \frac{e}{\tau}(N_i(E_{z0}) - N_f(E_{z0})) \tag{5}$$

where $i(E_{z0})$ and $f(E_{z0})$ are the initial and final states which have the same energy E_{z0} of motion in z direction; $N_i(E_{z0})$ and $N_f(E_{z0})$ are the number of electrons populating the initial and final states. Using low-temperature limit that is $kT << E_F$ and $kT << E_{z1} - E_{z0}$ and also supposing final states as empty that is $N_f(E_{z0}) = 0$ as usual, one can calculate $N_i(E_{z0})$ as a number of filled states

on a Fermi-hemisphere intersection disk taking at a momentum p_{z0} in the phase space (see gray disc in **Figure 2**) where $E_{z0} = (p_{z0})^2/2m^*$ and m* is an electron effective mass. Thus, the tunnel current can be found as follows:

$$I = \frac{e(p_F^2 - p_{z0}^2)S}{(2\pi\tau\hbar^2)} = eg_{2D}S(E_{Fe} - E_{z0})/\tau \tag{6}$$

where e is an electron charge, p_F is a Fermi momentum of electrons, g_{2D} is a density of two-dimensional states of electrons, and S is a sample area.

Let us suppose the emitter grounded, i. e., $\mu_{fe} = \text{const}$, then the voltage dependence of $E_{z0}(V)$ determines the I-V curve. If the barriers width D is greater than the quantum well (QW) width d, then $E_{z0}(V)$ can be found from linear Stark effect:

$$E_{z0}(V) = E_{z0}(0) - eV/\alpha \tag{7}$$

where α is a leverage factor, i.e., $\alpha = D/(d_1 + d_2)$. Since usually $E_{z0}(0) > \mu_{fe}$, there is a threshold voltage V_{th} higher than a resonant current I that has appeared when $E_{z0}(V_{th}) = \mu_{fe}$. Then combining Eqs. (6) and (7), one can get the following expression for the current I:

$$I = e^2 g_{2D} S(V - V_{th})/\alpha\tau \tag{8}$$

Eq. (8) is justified when $\mu_{fe} > E_{z0}(V) > E_{ce}$. At the current peak voltage $V_{p,}$ the subband energy E_{z0} approaches to E_{ce}, i.e., $E_{z0}(V_p) = E_{ce}$, and after that the resonant current drops down to zero.

As a result, the I-V curve of the RTD is shown in **Figure 3** as solid line. It is worth noting that Eq. (8) describes only resonant part of the current. Nonresonant current usually is monotonic

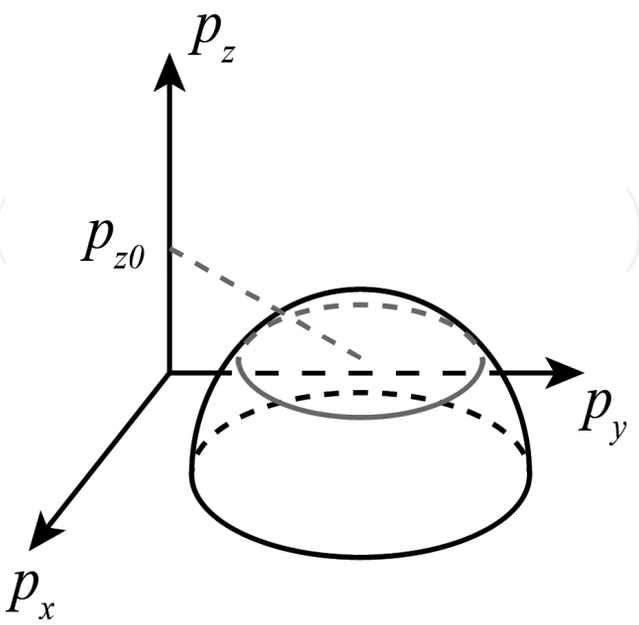

Figure 2. Momentum space of the emitter and states available for resonant tunneling.

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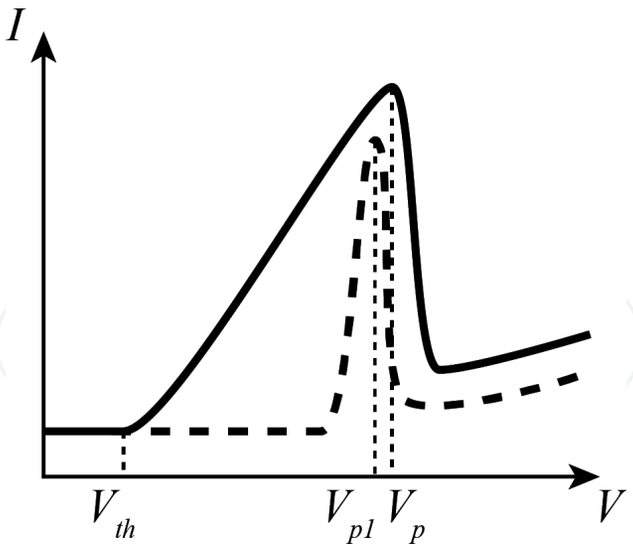

Figure 3. Current-voltage characteristics of RTD with a single quantum well between barriers (solid line) and a double quantum wells (dashed line).

function of the voltage and includes scattering tunneling and tunneling across all barriers. This provides nonzero current at any nonzero voltage. Thus, one can see that two-dimensional state in the QW produces the resonant tunneling in a finite resonant voltage range from V_{th} to V_{p} and depresses the resonant tunneling at other voltages. This resonant voltage range can be further shrunk if another QW will be used (see **Figure 4**). In this case, the resonant tunneling is possible only at resonant voltage V_{p1} when $E_{01}(V_{\text{p1}}) = E_{02}(V_{\text{p1}})$. This decreases significantly the width of the current peak in the I-V curve (see **Figure 3** dashed line).

Thus, the application of 2DSCs could significantly decrease the carriers tunneling in a wide range of the applied voltage. This means there is a new way to decrease carriers tunneling between a

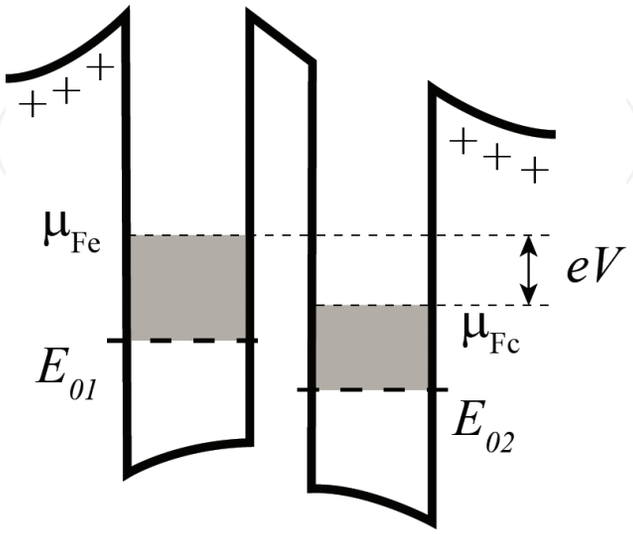

Figure 4. Energy profile of the conduction band bottom of the heterostructure with two quantum wells.

gate and a channel that is application 2DSCs in them. Semiconductor heterostructures with two 2DSCs separated by a tunnel barrier have been studied and demonstrated their properties [11].

3. Resonant tunnel transistors

As can be seen from **Figure 3**, tunneling current strongly depends on the energy of quantum level in the QW, so if you create a third electrical contact to control this energy, it is possible to obtain a transistor with a large transconductance value, and even with a negative transconductance. Several types of such transistors have been investigated and are shown in **Table 1**. They differ by base contact making as it is shown in **Figure 5**.

3.1. Bipolar resonant-tunneling transistor with QW

In this case, double-barrier heterostructure is located inside a vertical bipolar transistor in a thin layer being in connection with base contact [12]. One example implementation of such a heterostructure is shown in **Figure 6(a)** in the form of the band structure. QW layer is considerably doped with impurities of p-type, which allows change in the potential of QW almost independently of the potentials of the source and drain. Resonant tunneling through the QW starts at finite drain-source voltage (see **Figure 6(b)**). **Figure 7(a)** presents source-drain characteristics of the transistor at different values of voltage on the base. As one can see from **Figure 7(b)**,

	Unipolar transistors	**Bipolar transistors**
Base pin contacts to the QW	Unipolar RTT with contact to the QW	Bipolar RTT with QW contact
Base pin contacts layer close to the QW	Unipolar RTT on hot-electrons effect	Light-emitting RTT

Table 1. Resonant-tunneling transistors.

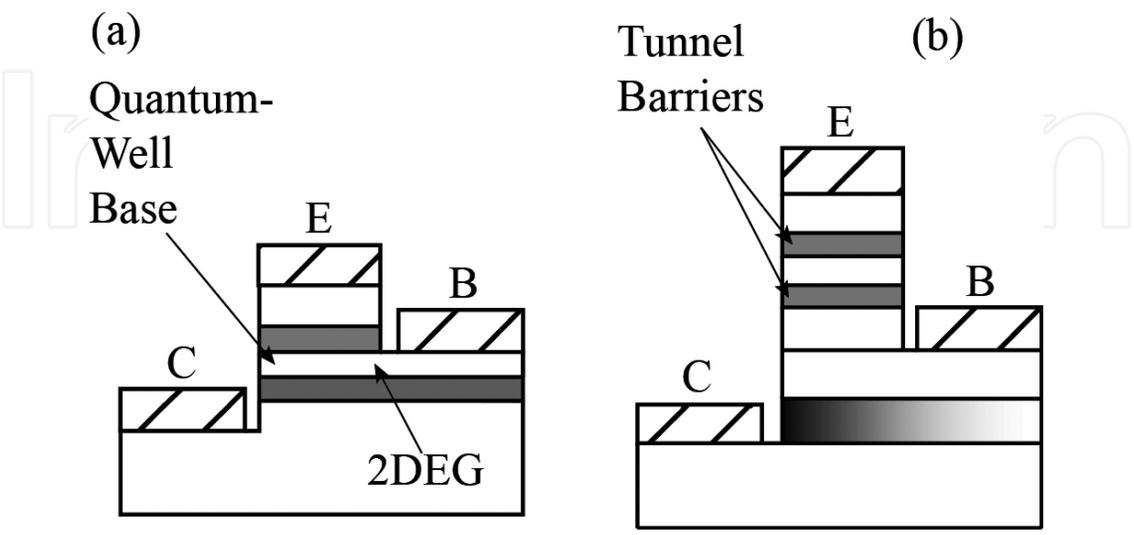

Figure 5. Topology of resonant-tunneling transistors. (a) RTT is shown where the base contact is connected directly to the QW and (b) RTT is shown where the base contact is connected to layer adjacent to the QW.

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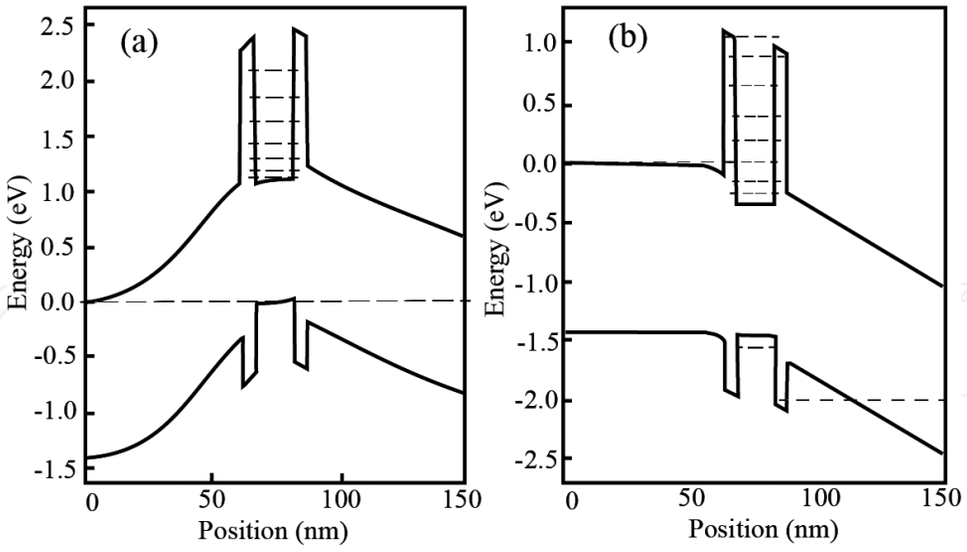

Figure 6. Band diagrams of the bipolar RTT with QW at zero drain-source voltage (a) and at finite applied voltage (b).

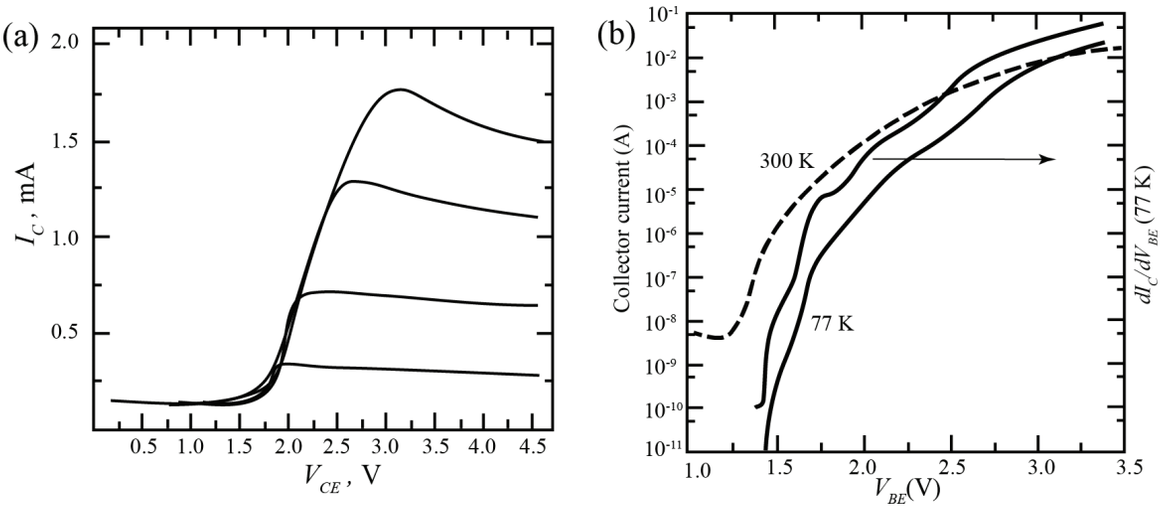

Figure 7. Characteristics of the bipolar RTT with QW taken from Ref. [12]. (a) Drain-source characteristics at different base voltages at 300 K and (b) source-base and transconductance characteristics at different temperatures.

the resonant tunneling provides just weak features in the transconductance of the transistor, which appears to be associated with a strong broadening of the levels of dimensional quantization in the QW, due to its disorder induced by doping impurities. The usage of modulated doping could significantly improve the situation, but further research in this direction is not followed. Perhaps because in the transistor the doped layer is placed outside the quantum well and the contact to the layer outside the quantum well.

3.2. Light-emitting resonant-tunneling transistor

In the case of a bipolar contact or p-n junction, the flow of electric current accompanied by the light emission resulted from the electron-hole recombination. Similar radiation was recorded

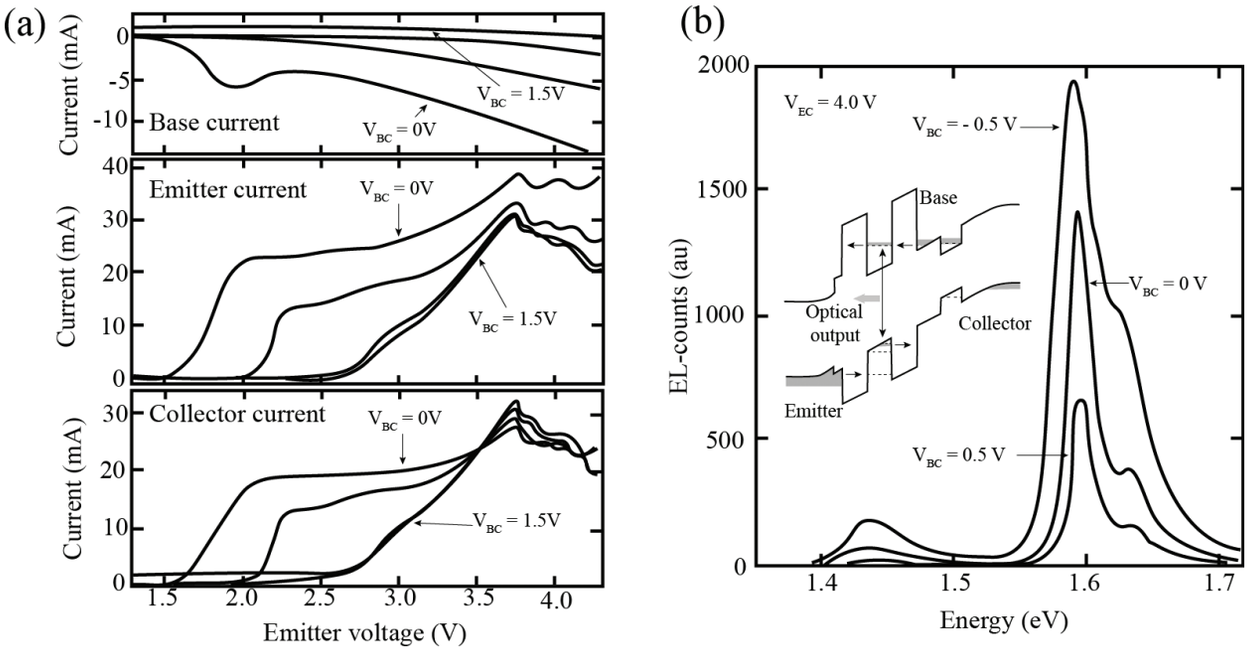

Figure 8. Electrical and optical characteristics of the bipolar RTT with base contact separated from active region taken from Ref. [14]. (a) Source or emitter, drain or collector and base currents are plotted versus applied source-drain voltage at different base voltages and (b) optical spectra at different base voltages.

in a bipolar RTD [13] and bipolar RTT [14]; in this sense, the third electrode can be considered as controlling not only current but also radiation. The presence of the region of negative differential conductance (NDC) allows to create not only an oscillator but also an optical pulsar with a clock frequency up to the THz range. One of the options for band structure of these transistors is shown in the insert in **Figure 8**. In this case, the base layer is doped by donors, but the contact is placed out from the side of the structure. This helped to maintain the quality of the QW between the tunneling barriers that has led to a significant effect of resonant tunneling. As a result, the region of the negative conductance and transconductance was present in all transistor characteristics (see **Figure 8(a)**).

3.3. Resonant-tunneling transistor with base contact to two-dimensional electron system

It is possible to make a deep QW between the tunneling barriers. The QW will be filled by carriers from adjacent layers, if a ground subband has energy E_0 below Fermi level [14]. Such QW can be connected via remote contact and has no disorder originated from doping (see **Figure 9**). In this case, the base contact is located remotely from active region on the side of the emitter and controls the potential of the QW (see **Figure 9**). Resonant tunneling of electrons through the level E_1 or through the first excited two-dimensional subbands. Source-drain current-voltage characteristics are shown in **Figure 10(a)**. It is seen in **Figure 10(b)** that, despite the observed NDC saturation current is not observed and there is a large nonresonant current. This behavior is expected because when tunneling takes place in the first excited subband, electrons tunnel with emission of a wide range of excitations, such as phonons, plasmons, and photons. These excitations transfer the electrons to the ground subband.

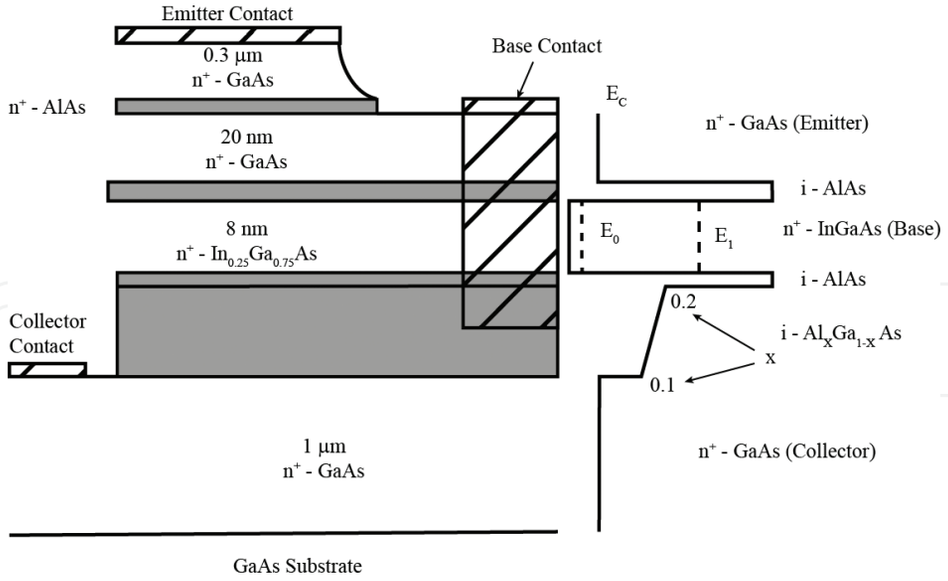

Figure 9. Resonant-tunneling transistor with deep QW. Topology of layers and contacts and conduction band bottom diagram of the active region of the RTT.

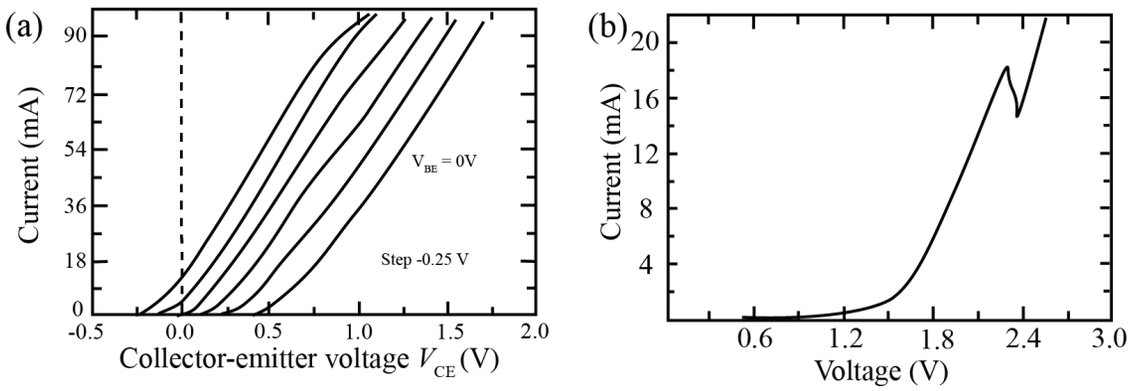

Figure 10. Electrical characteristics of the RTT with deep QW. (a) Source-drain current-voltage characteristics at different base voltage and (b) source-drain current-voltage characteristic at floating base potential.

3.4. Resonant-tunneling transistor on hot electrons

The removal of the base layer outside the quantum well improves the work of RTT, as demonstrated in Refs. [9, 15]. The topology of the transistor and its diagram of the conduction and composition of the layers is shown in **Figure 11**. In this case, the heavily-doped disordered base layer does not much influence the quality of the QW and bright NDC features are observed in all electrical characteristics. **Figure 12** shows transistor characteristics obtained. The thickness of the base layer is 50 nm (a) and 25 nm (b). From **Figure 12**, one can see that the wide-base layer degrades characteristics of NDC and increases the base current, decreasing the width of the layer characteristics improves characteristic and the gain current increases. It is worth noting that at low voltage, the current is very low because the ground subband has energy considerably higher the Fermi energy and only high energy electrons or hot electrons can tunnel.

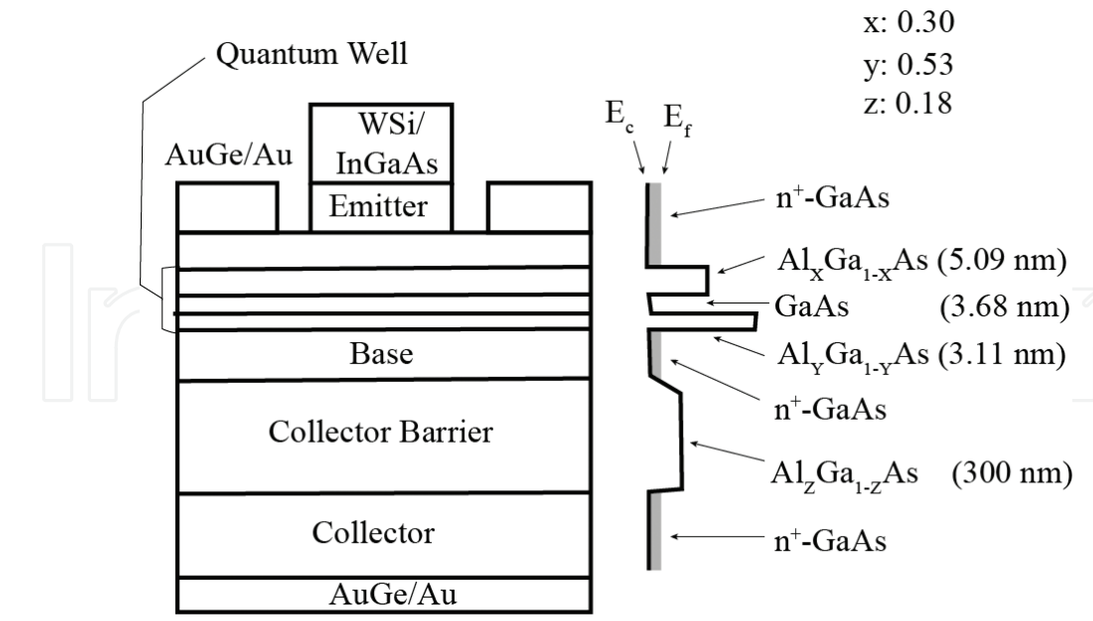

Figure 11. Resonant-tunneling transistor on hot electrons. Topology of layers and contacts and conduction band bottom diagram of the active region of the RTT.

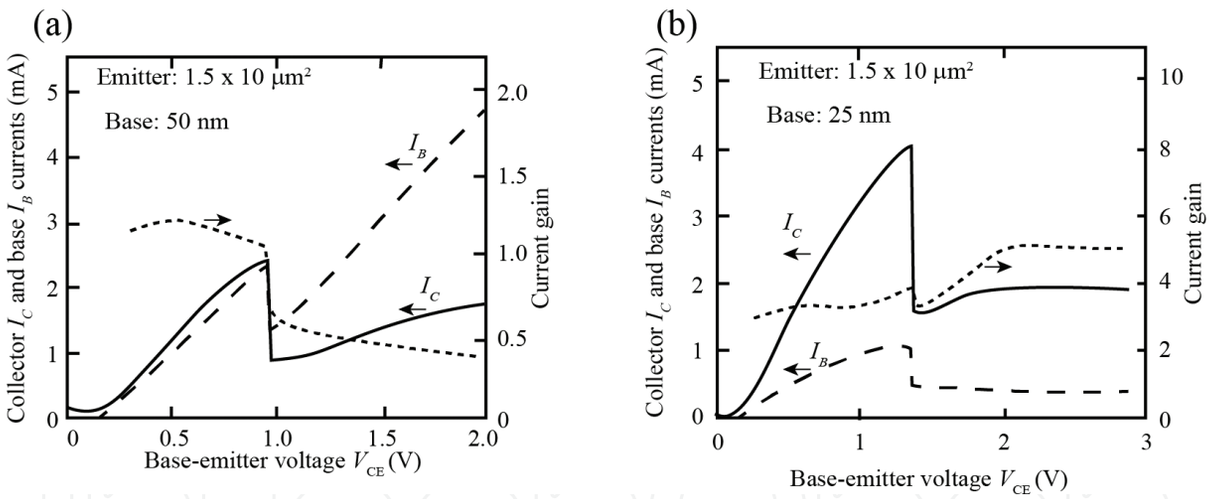

Figure 12. Electrical characteristics of the RTT on hot electrons. (a) Characteristics obtained on RTT with base layer of 50 nm thickness and (b) the same for 25 nm thickness.

4. Field-effect transistors with two-dimensional systems of carriers

Previously studied resonant-tunneling transistors have considerable disadvantages such as the tunnel current is very low and high frequency application is possible only in the region of NDC. However, the resonant tunneling can be used in conventional FET to shrink gate-voltage range where it takes place [16]. As already mentioned in Section 2, the situation can be significantly improved by using a structure with two quantum wells. In this case, the gate 2DCS has a carrier concentration different from the 2DCS concentration in the channel (see **Figure 13(a)**). To create such transistor, it requires an entire system of gates. The problem is

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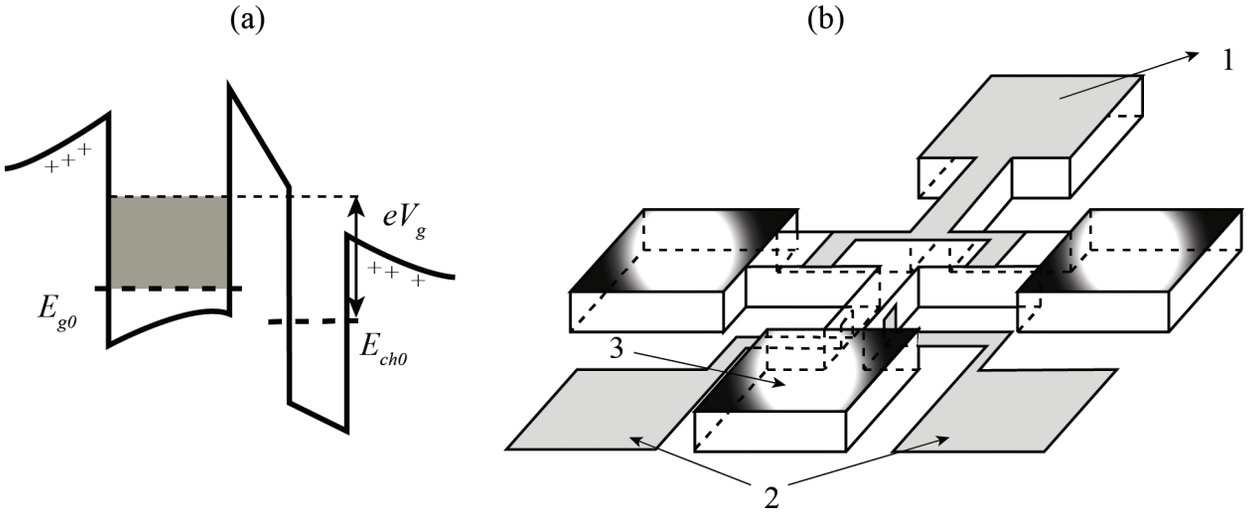

Figure 13. Field-effect transistor with QWs. (a) Conduction band bottom diagram of the active region of the FET and (b) topology of the contacts of the FET.

that two conductive layers are in close proximity to each other, which significantly complicates the creation of separate ohmic contacts to each layer. In this case, ohmic contacts to the both layers are made, and then, additional gates (1, 2 in **Figure 13(b)**) deplete one of the layers. So, gate 1 can be used by applying a negative voltage to the depletion of the upper layer and double gate 2 is used for the depletion of the lower layer. Due to the difference of the energies the resonant tunneling between the layers will be suppressed and the leakage current from the gate to channel will be low. It should be noted that when using this transistor to completely eliminate the resonant tunneling which is impossible as to deplete the channel, one must pass through the resonance voltage V_r, in which $E_{g0}(V_r) = E_{ch0}(V_r)$. However, even in this case, the current will not exceed the maximum current observed when the resonant tunneling takes place between a three-dimensional contact and QW (see **Figure 3**).

Another possibility of a FET is proposed in Ref. [17] with a gate and a channel on the basis of 2DSC in different valleys. The key point of the device is that the 2DSCs are different. In particular, they are formed in different valleys of the carrier spectrum (see **Figure 14(a)**). Due to this difference, the carrier tunneling requires additional excitations with significant momentum and energy. This decreases the tunneling rate significantly. For example, the intervalley tunneling rate is less than intravalley that in 9 orders of magnitude in GaAs/AlAs heterostructures [18]. Application of 2DSCs in the gate and channel in different valleys can significantly decrease the tunnel leakage and allow further cut-off frequency to increase. Moreover, in the case of low intervalley carriers scattering, the dielectric layer can be removed which increases the transconductance of the FET. Some realization of the conduction band bottom profile can be found in **Figure 14(b)**. The heterostructure is modulation-doped by Si donors. The AlAs is an indirect semiconductor where X-valley has lower energy than Γ-one. Hence, in the layer 2, a quantum well (XQW) is formed in the X-valley that is shown by long-dashed line in the profile. The XQW can be used as a FET gate. A GaAs quantum well is formed in Γ-valley (ΓQW) and can be used as a FET channel. A topology of the FET can be the same as in **Figure 13**. The source and drain are contacted to the ΓQW and the gate is contacted

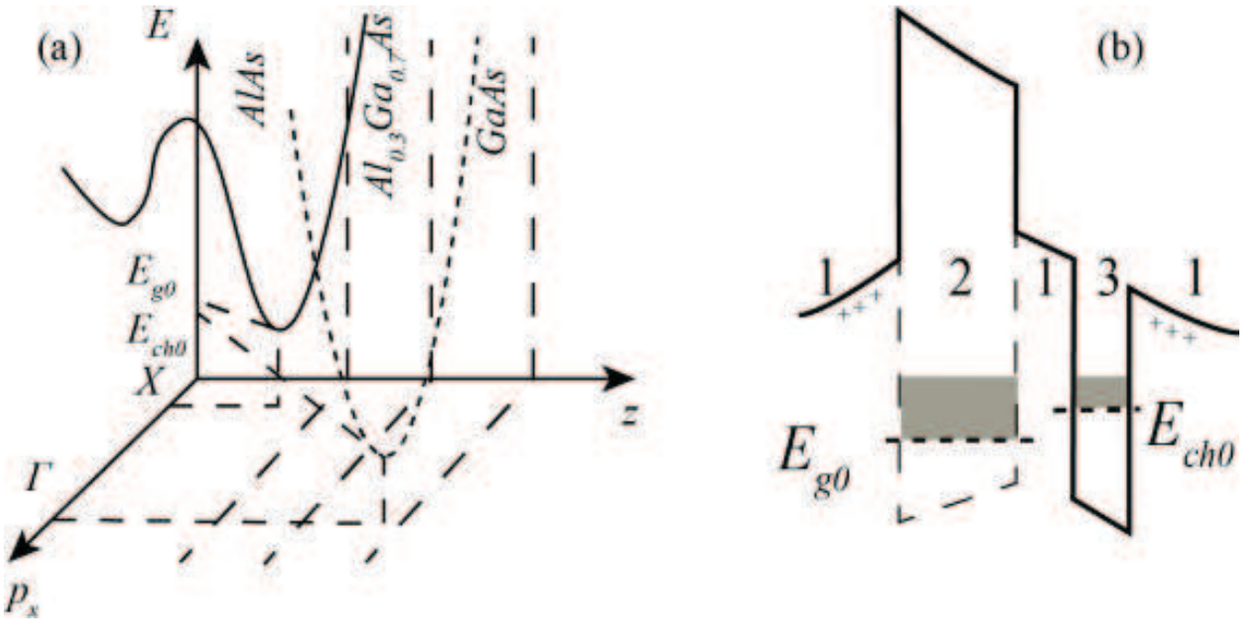

Figure 14. Electrons spectra in active region of the FET with QW in different valleys. (a) Electron dispersion curves in the XQW (solid curve) and ΓQW (dotted curve) and (b) conduction band bottom diagram of the proposed FET heterostructure.

to the XQW (see arrow 3 in **Figure 13**). The electric characteristics of the proposed FET are still under investigation. However, some discussion about their miniaturization is possible and follows in the next section.

5. Miniaturization of the field-effect transistors with two quantum wells

5.1. Cut-off frequency of the FET

As mentioned in Section 1, miniaturization of transistors is the main direction of development of microelectronics for more than 50 years and the reason is not only the attraction of investments or the usability of electronic devices. The main reason for miniaturization is to increase the cut-off frequency of semiconductor devices. Let us consider how the size reduction leads to an increase in the operating speed of a FET. In **Figure 15(a)**, one can see a typical topology of a FET with metal electrodes. The FET is plugged in the bias circuit through the contacts 1 (source) and 2 (drain). Offset E_c is necessary for the current saturation that one can see in the source-drain characteristics of the FET as shown in **Figure 15(b)**. The saturation velocity of the carriers in the channel (in gray in **Figure 15(a)**) does not change with applied voltage and it is possible to obtain the following expression for current:

$$I_{sd} = nevS_{ch} \tag{9}$$

Here, n is the carrier concentration in the channel, v is the velocity of the carriers, S_{ch} is a cross-sectional area in the channel. To change the concentration, the gate is used (see in **Figure 15(a)**). When voltage V_{in} is applied the carrier concentration n(V) is changed due to the finite capacitance between channel and gate Cp as follows:

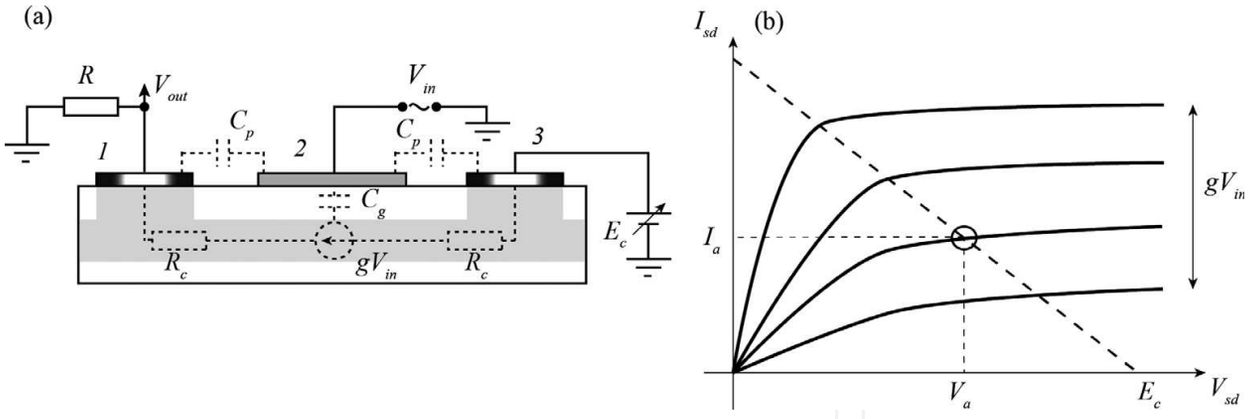

Figure 15. Topology and characteristics of the field effect transistor. (a) Topology of a field-effect transistor and the plug-in circuit. The dotted line shows the elements of the equivalent circuit of the transistor. (b) Source-drain characteristics of FET for different gate voltages V_{in}. The inclined straight line corresponds to the load straight line, its intersection with the source-drain characteristic corresponds to the operating point of the transistor, i.e., determines the current I_{a} and voltage V_{a}.

$$n(V) = n_0 + C_g V/(W_{ch}e) \tag{10}$$

where n_0 is the carrier concentration in the channel at zero gate voltage, $W_{\text{ch}} = S_{\text{ch}}L_{\text{ch}}$ is a volume of the channel, L_{ch} is a length of the gate or channel (see **Figure 15(a)**). Substituting the Eq. (10) in Eq. (8), one can get the following expression for the current:

$$I_{sd} = I_0 + \frac{vC_g V}{L_{ch}} = I_0 + gV \tag{11}$$

where g is a transconductance of the FET. In **Figure 15(a)**, dashed line presents the elements of the equivalent circuit of the transistor, i.e., elements for which the transistor can be modeled. In this case, the behavior of the semiconductor channel can be modeled by a current source dependent on the gate voltage V_{in}. Let us now consider the AC signal V_{in}, then there is a bias current δI_{c} through the parasitic capacitance of C_{p} and gate capacity C_{g}. The current through the capacitance is increased by increasing the frequency of the alternating voltage V_{in}, so there is a cut-off frequency at which the current through the capacitance is compared with the current in the semiconductor channel δI_{a} and then one can get the following equation:

$$\delta I_c = \omega(C_p + C_g)V = gV = \delta I_{sd} \tag{12}$$

Then taking into account Eq. (11), one can get the following expression for the cut-off frequency:

$$\omega = \frac{v}{L_{ch}(1 + C_p/C_g)} \tag{13}$$

This shows that by increasing the value of C_{g} and decreasing the value of C_{p} and L_{ch}, it is possible to increase the cut-off frequency of the transistor. To increase C_{g}, one can reduce the distance between the channel and the gate, i.e., d. By the way, the use of gate high-k dielectrics

is another way of increasing C_g. The reduction in C_p may also be obtained by decreasing a width of the gate contact and increasing the distance between the contacts and gate contacts. However, the increase in the distance between electrodes is limited by increase of the serial resistance R_c. Actually, Eq. (13) describes the cut-off frequency of the active region of the transistor, i.e., the channel region under the gate, the output AC signal is measured when the current flows through the load resistance R. Resistance R_c is shunted by a capacitance of C_p, therefore, the cut-off frequency of AC signals cannot exceed $\omega_1 = 1/(R_c C_p)$. Since R_c increases with increasing interelectrode distance, the effect of increasing this distance is significantly reduced.

5.2. Size-quantization and its effect on resonant tunneling

Thus, reducing the size of the active area of the transistors leads to an increase in the cut-off frequency, which is the main physical reason for the miniaturization. However, as mentioned in Section 1, miniaturization of transistors has led to the increase in the leakage current, which significantly increases energy consumption and reduces the prospects for further development in this direction to zero. The use of resonant tunneling can significantly reduce leakage currents, but it is necessary to use a carrier system with reduced dimensions. These systems which appear in semiconductor nanoheterostructures, recently also actively studied the carbon nanomaterials. Here, there is a new problem with miniaturization. When reduction of L_{ch} size occurs up to 20 nm, lateral size-quantization takes place in the two-dimensional gate and channel. This significantly degrades the resonant nature of tunneling, and nullifies efforts to suppress it, as demonstrated in the study of RTD of nanometer sizes [8]. However, to date, it has been shown that a RTD with a transverse size of 5 μm, is capable of operating at frequencies above 4 THz, which is 2 orders of magnitude higher frequencies of modern high-frequency transistors. A major obstacle to the wide use of RTD is the high cost of producing semiconductor nanoheterostructures, which requires the involvement of molecular beam epitaxy. However, the development of relatively cheap methods of obtaining carbon nanomaterials creates serious prospects of using such materials for the creation of RTD. RTD have already been successfully created on the base of graphene films [19, 20], but their quality is inferior to semiconductor films.

6. Conclusion

In summarizing, we can state that application of resonant tunneling can significantly increase the operating speed of the FET and reduce leakage currents. However, the application of 2DCS systems imposes new restrictions on the miniaturization, reducing her prospects to almost zero. However, even relatively large RTD already working on the frequencies exceeding the frequencies of the transistors. It is shown that devices based on resonant tunneling are able to replace the conventional FET. The main problem of widespread use of such devices today is a significant high cost of the technology of molecular-beam epitaxy. Possible further development of technology toward a carbon nanomaterials. Carbon nanomaterials might allow high-quality RTD, which is significantly cheaper than semiconductor materials. In this case, we

should expect serious changes in the architecture of classical computers and the emergence of new solutions in the field of quantum computing.

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