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# Solution-Processable Nanowire Field-Effect Transistors

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Maxim Shkunov, Grigorios Rigas and  
Marios Constantinou

Additional information is available at the end of the chapter

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## Abstract

Solution-processable single-crystalline inorganic semiconducting nanowires are excellent building blocks for printable electronics requiring high performance of semiconducting components. Excellent charge carrier mobilities of crystalline nanowires combined with solvent-based nanowire processing open up possibilities for low-cost nanowire electronics targeting a variety of applications ranging from flexible circuits to chemical and biological sensors. Nanowire field-effect transistors are key devices for most of such applications. Recent developments in controllable nanowire positioning and orientation on the substrates and electrical property selection provide the necessary technological breakthroughs enabling the fabrications of reproducible nanowire transistors. In this chapter, we discuss the nanowire assembly methods and high-spatial-resolution scanning probe microscopy techniques towards scalable fabrication of high-performance printable nanowire field-effect transistors.

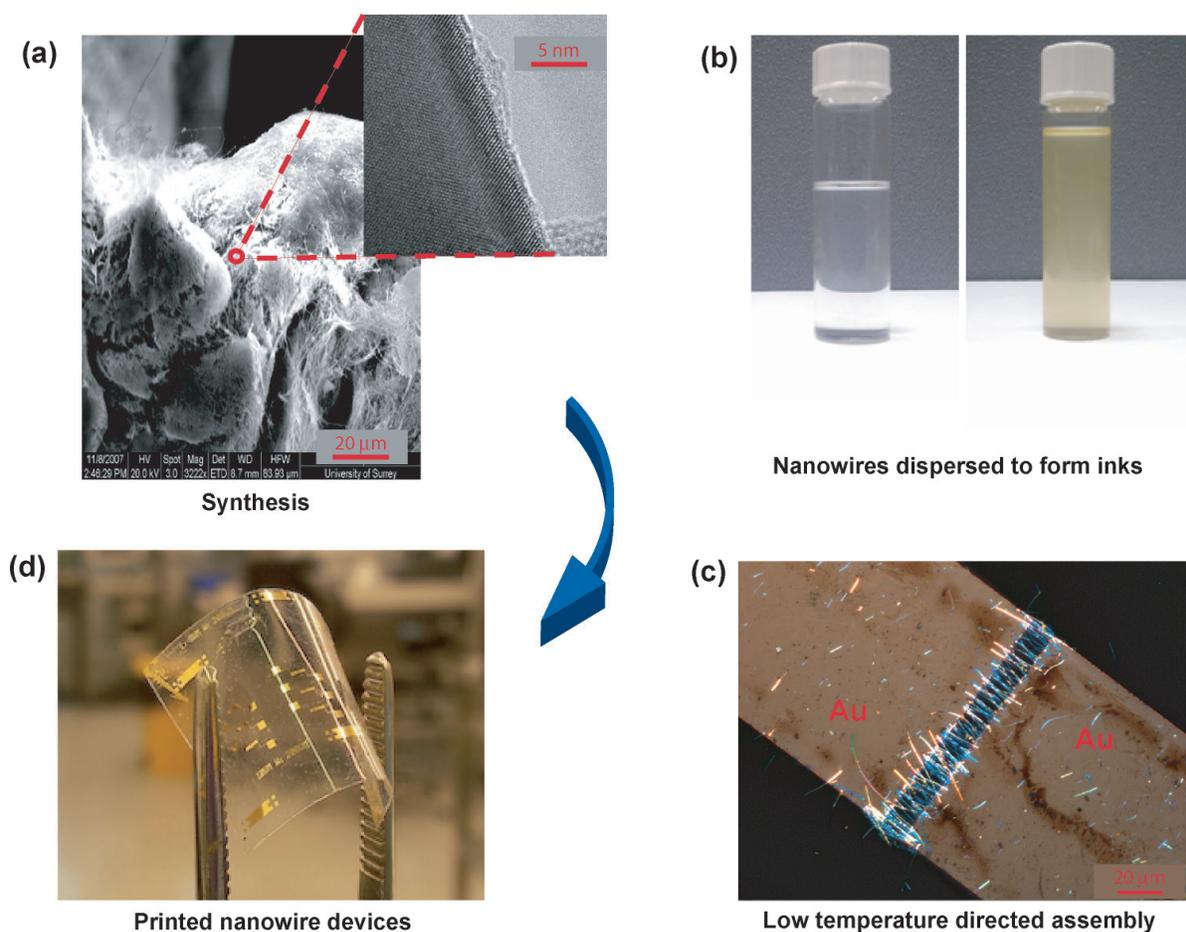
**Keywords:** inorganic semiconducting nanowires, printed electronics, field-effect transistors, solution processability

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## 1. Introduction

The growing interest for printed electronics using functional nanomaterials is due to a plethora of conventional and novel applications that can be generated at a fraction of the cost as compared to conventional microelectronic device fabrication involving multiple photolithographic and etching steps. These applications include flexible circuits [1], biological and chemical sensors [2–4], photovoltaic and piezo energy harvesting [5–7], low-dissipation power electronics [8], terahertz detectors [9, 10], memory storage devices [11], artificial e-skin sensors [12], flexible displays [13] and optoelectronic devices [14] including lasers [15, 16]. One-dimensional inorganic semiconductors in the form of single-crystalline nanowires

(NWs) hold most of the promise to act as a backbone for these applications. This is due to nanowires' excellent charge transport properties, the availability of both direct and indirect bandgap semiconducting materials, high aspect ratios allowing nanowires to bridge typical device electrode gaps, solution processability, chemical stability, room temperature deposition capabilities and compatibility with a variety of substrates including both rigid and flexible substrates such as plastics and paper. Separation of nanowire growth from the device assembly allows to employ low-temperature, bottom-up device fabrication approach utilising solution processing of nanowire devices. General nanowire device fabrication process flow is illustrated in **Figure 1**, where synthesised nanowires are dispersed in organic solvents for form functional inks, and then solution-based deposition is used to assemble nanowires on substrates, ideally with a good degree of nanowire orientation and positioning in respect to device electrodes. Density of nanowires after solvent-based disposition is defined by the type of the device and can vary significantly from monolayer coverage for transistor devices to very dense layers intended as energy storage electrodes in, for example, Li-ion batteries [17]. The devices are then finished by depositing the required counter-electrodes, dielectric



**Figure 1.** A concept of printable nanowire electronics on flexible substrates, where NW powder (a) is dispersed to form semiconducting nanowire inks (b), followed by aligned deposition of nanowires between device electrodes (c), and finished device can be fabricated at low-temperature process compatible with plastic substrates (d). (b) shows example of ZnO NW ink on the left and Si NW ink on the right.

layers and conducting tracks and also encapsulation layers, if devices need protection from the environment.

Reproducible positioning and alignment of nanowires with respect to device electrodes have been one of the key challenges in solution-processed nanowire electronics and has attracted a significant research effort. Advances toward nanowire assembly from liquid-based 'inks' onto device substrates are discussed in Section 3, paying attention to positioning, alignment and orientation. Recent progress toward selective nanowire deposition using dielectrophoresis is discussed in relation to separation of nanowires with different physical dimensions, such as lengths, and also selection based on their electrical properties and types of nanowires.

Nanowire surface states play an important role in the corresponding device electrical characteristics, and large surface-to-volume ratio of nanowires opens, on one hand, enormous opportunities for surface receptor functionalisation toward chemical and biological sensors and, on the other hand, can lead to undesirable electrical hysteresis effects due to the presence of surface trap states that need to be eliminated. Further discussion of nanowire surface functionalisation and passivation methods towards stable, hysteresis-free device operation is described in Section 4.

Multiple nanowire channel devices raise particular characterisation challenges associated with both good contact formation between the nanowires and electrodes and also the need to identify nanowires which fully connect the device electrodes and those that do not participate in the conduction mechanism. Characterisation methods based on conducting scanning probe microscopy techniques are discussed in Section 5 in relation to conducting and semiconducting nanowires to probe their positioning, morphology, conductivities and other physical parameters.

## 2. Nanowire transistor device structures

Field-effect transistors (FETs) are key building blocks for modern electronics as they provide a variety of functions essential for analogue and digital electronics. Printable electronic fabrication approach is highly beneficial for a variety of sensor transistor applications, including chemical and biological sensing and tensile and optical sensing, where extremely dense transistor integration is not required, and in many cases, sensors need to be positioned some distance apart from each other to allow, for example, transistor functionalisation with chemical or biological receptors.

Traditional microelectronic fabrication involves mainly top-down processes, such as masking; etching; stripping; ion implantation, with multiple photolithographic steps; and high-temperature annealing (often around 900°C), resulting in high amount of chemical waste required for the processing and very significant amount of energy use.

Printable electronics is based around the concept of bottom-up fabrications with additive manufacturing steps aimed at building the devices by functional inks printing and deposition techniques involving consecutive printing of conducting, semiconducting, and dielectric lay-

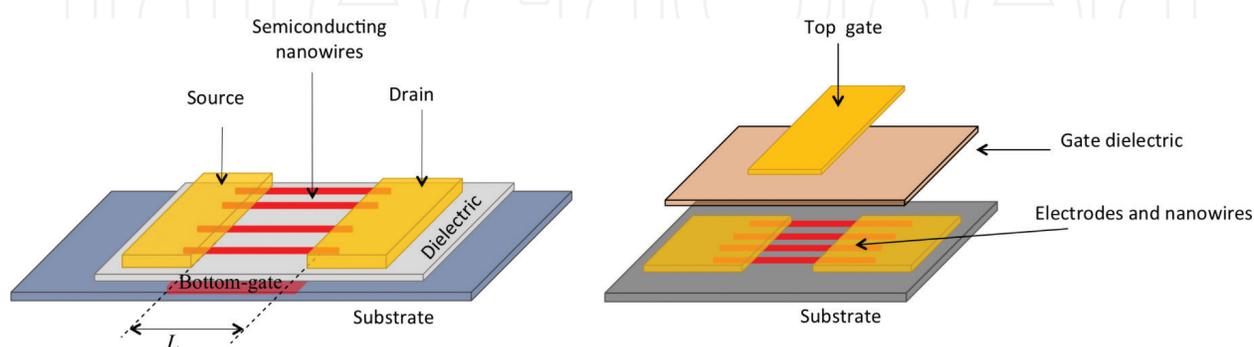
ers and components. These functional inks thus need to contain nanoparticles and/or material providing the necessary properties. Examples include semiconducting nanowire inks, metal nanoparticle inks and polymer dielectric inks. Printable nanowire FETs can be fabricated by various deposition techniques, with specifics related to the particular conductor, semiconductor, or dielectric materials. Metal nanoparticle ink deposition for nanowire FET electrodes, for example, can be performed by ink-jet printing [18], whereas popular gate dielectric deposition for NW FETs is by spin-coating polymer insulator materials [19]. Semiconductor nanowire transistor channel plays a defining role in the FET operation, so more attention will be devoted to the NW assembly as discussed in the next section.

FET device structures that are fully compatible with solution-based printing fabrication belong to thin-film transistor family and are represented by bottom-gate FETs and top-gate FETs. **Figure 2** is showing schematics for both types of NW FETs.

Top- and bottom-gate NW FET structures each have particular advantages: Bottom-gate structure is ideal for sensing applications, where NW channel area is fully exposed on the top to chemical or biological analytes. Additionally, bottom-gate design offers straightforward device prototyping when using commercially available oxidised silicon ( $\text{Si}/\text{SiO}_2$ ) wafers, which can be directly used as the substrate, incorporating conducting common gate, highly doped Si and gate dielectric  $\text{SiO}_2$ . Such substrates are also highly amenable for ink-jet printing for electrode deposition.

Top-gate transistor architecture allows better gate control over nanowire channel due to wrap-around gate dielectric geometry, naturally occurring after the dielectric deposition. Importantly, top-gate FETs demonstrate improved environmental stability due to nanowire channel encapsulation provided by the gate dielectric together with metal gate electrode covering the channel, thus protecting nanowires from atmospheric exposure [20].

Main challenges in printable NW FET fabrication (Section 3) are due to deposition and controllable alignment of nanowires, which need to bridge the device electrodes; reproducible number of nanowires in FETs; and solvent-based deposition and alignment compatible with large-scale printing.



**Figure 2.** Schematics of bottom-gate (a) and top-gate (b) nanowire FETs.

Surface states are always present in nanomaterials due to their high surface area, and they play an important role in nanowire device performance. Thus, interface properties of nanowires need to be controlled to eliminate unwanted electrical hysteresis effects as discussed in Section 4.

### 3. Nanowire assembly

The bottom-up fabrication approach for nanowire transistors relies on the availability of grown nanowire materials and also on the efficient assembly methods for nanowire solvent-based deposition. The NW synthesis has been demonstrated using various methods, including supercritical fluid-liquid-solid growth (SFLS) for Si and Ge NWs [21], vapour liquid solid (VLS) growth for Si nanowires and the laser ablation for SnO<sub>2</sub> nanowires [22]. For the preparation of the NW formulations, the as-synthesised NWs are typically dispersed in various organic solvents using low-power sonication process for short periods of time to gently remove nanowires from the growth substrates and to promote homogeneous distribution of nanowire materials in the solvent.

Nanowire deposition and alignment on device substrates represent the next fabrication step. Several self-assembly techniques have been developed in the past for transferring the NWs onto the microelectrode structures to form the conducting channels of the FET devices. The main challenges in self-assembly are the precise alignment and positioning of the nanowires on predefined electrode areas and the purification and selection of nanowires with desired electrical properties. Most of the reported assembly techniques, apart from dielectrophoresis (DEP) provide no or very limited control of NW lateral alignment and no electrical properties selection. In this section, various NW deposition methods are discussed, and more attention is paid to the DEP process enabling electrical and morphological properties' selectivity.

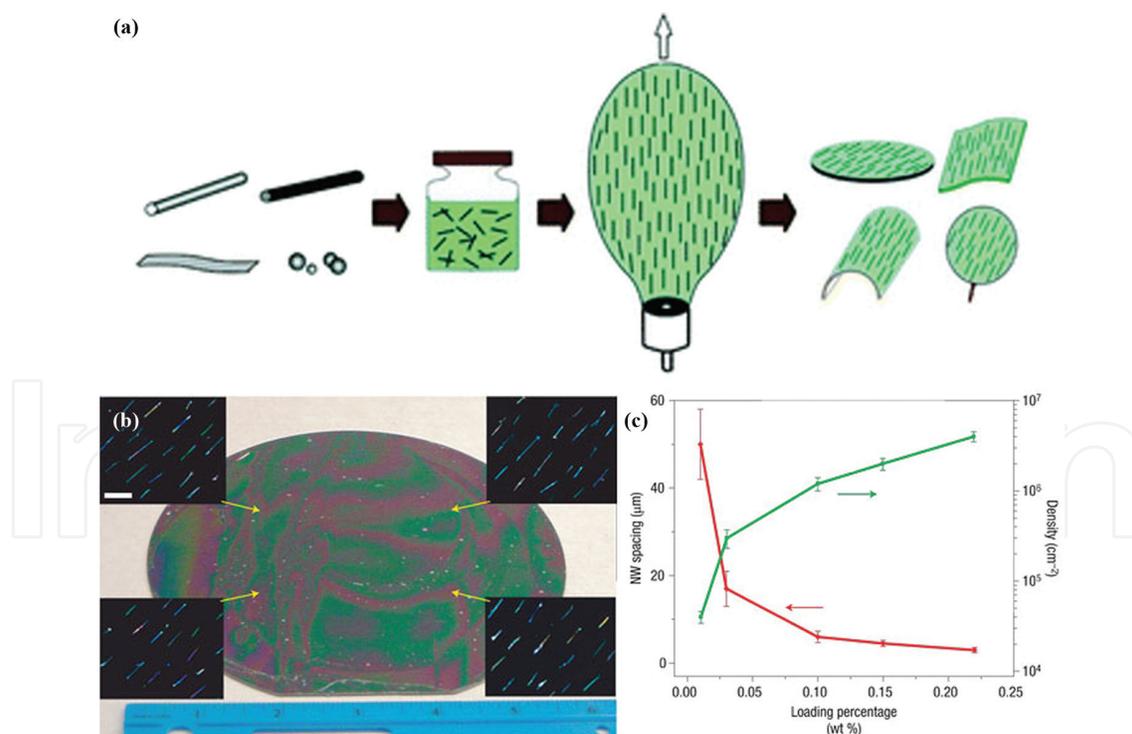
#### 3.1. Nanowire alignment techniques

A number of techniques have been developed for the alignment and deposition of NWs on the substrates, including Langmuir-Blodgett (LB), blown-bubble films (BBF), flow-directed assembly, electrostatic interactions, mechanical shear forces and electric field-assisted assembly with dielectrophoresis.

The Langmuir-Blodgett deposition is a very powerful technique for the alignment of high-density arrays of parallel nanostructures over large areas with a precise spacing between nanoparticles from  $\mu\text{m}$  down to nm scale. The method was first reported for barium chromate nanorods [23], with inspiration taken from centuries-old technique for timber-floating on rivers [24]. The technique has been adapted and developed to assemble a variety of nanowires from metallic silver NWs [25] to semiconducting nanowires, including silicon [26]. In the LB technique, the surfactant-wrapped NWs (e.g. 1-octadecylamine) are dispersed on the water surface of a Langmuir-Blodgett trough. Due to the impartial surfactant's solubility in water, the NWs are floating on the surface of the trough. Then, computer-controlled barriers, positioned at the edges of the LB trough, slowly compress the NWs to a higher density at the

surface. The density of the monolayer, which depends on NW-to-NW stacking, is mainly limited by the amount of the suspended NWs, and their direction of alignment is dictated by the barrier orientation of the LB trough. Barrier compression causes NWs to reorient and to align parallel to the trough barrier edge, forming a highly dense monolayer. Then the NW layer can be transferred to a substrate, such as silicon wafer; however, some degree of misalignment can occur during the transfer of nanowire from the surface of the trough onto the solid substrate. This LB technique is compatible with large-area electronic fabrication; however, it is difficult to control the NW alignment yield and reproducibility of the alignment on top of the FET source-drain electrode structures [25, 26], and no lateral nanowire alignment is typically obtained.

The blown-bubble film assembly technique is able to provide uniformly aligned and controlled density of NW by utilising a bubble expansion process [27]. The surface of nanomaterials is chemically functionalised, and then, nanowires are mixed with epoxy resin. For example, Si NWs are modified using 5,6-epoxyhexyltriethoxysilane, dispersed into tetrahydrofuran and then homogeneously mixed with a known mass of epoxy resin. Afterward, a bubble is expanded from the epoxy-nanomaterial viscous formulation at a controlled direction and speed, and then bubble surface is touched by a substrate to transfer the nanowires resulting in well-defined nanomaterial-incorporated thin films. The alignment of the nanomaterials is mainly attributed to the shear stress present in the epoxy fluid during the bubble expansion



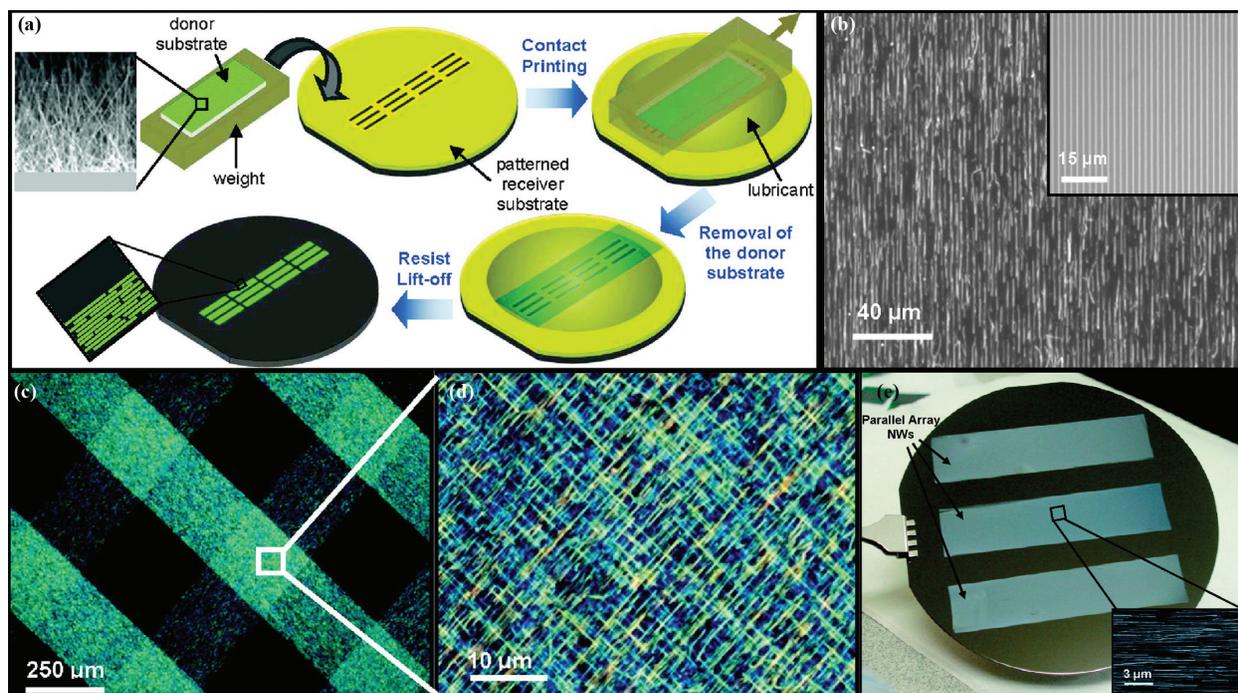
**Figure 3.** (a) Schematic of the BBF technique. The nanomaterials are dispersed in polymer solution, the solution is expanded as a bubble using a die, and then the uniformly aligned nanomaterials are transferred to different substrates including plastics. (b) Optical image of 6 inch Si wafer with aligned Si NWs (scale bar, 10  $\mu\text{m}$ ). (c) Density vs. concentration curve, indicating the density can be controlled by loading a percentage of nanomaterials [27]. © The Royal Society of Chemistry 2008.

process (**Figure 3a**). The viscosity of the homogeneous solution is the key parameter for the uniform distribution of nanomaterials in the resulting bubble films (**Figure 3b–c**). This technique provides a dense and uniform NW distribution suitable for large-area applications, and it is applicable to both rigid and flexible substrates. Although, it requires a large sample volume of NWs, the residual epoxy resin needs to be removed in order to define electrical contacts for NW FET applications, and it is difficult to control the number of the aligned NWs across the source-drain FET electrodes [27]

Highly aligned and dense nanowire packing was demonstrated by flow-directed assembly of nanowires in a microfluidic channel structure formed between poly(dimethylsiloxane) (PDMS) mould and a flat substrate (Si/SiO<sub>2</sub> modified with amine functionality). Assembled arrays of NWs, formed by passing the suspended NWs through the microfluidic channels, were aligned along the flow direction. The shear flow near the surface of the substrate immobilised the NWs and aligned them along the flow. At high flow rates, larger shear forces were produced and led to better alignment. This technique provided a controlled NW density and a flexibility to meet complex device configurations. However, the alignment process was attainable only for NWs with diameter <15 nm, it required the fabrication of microfluidic channels, it was challenging to scale up the process to large wafers, it was difficult to control the number of the aligned NWs across the source-drain FET electrodes and no lateral nanowire alignment was achievable [28, 29].

The electrostatic interaction method for nanowire assembly was developed by Heo et al. [30], and it relied on the electrostatic interactions of the positively charged surfaces of the semi-conducting nanomaterials with the negatively charged surface of the substrate. Si NWs were functionalised with amine-terminated aminopropyltriethoxysilane (APTS) self-assembled monolayer (SAM) and well dispersed in aqueous solution. Then Si NWs were deposited on negatively charged substrates (i.e. SiO<sub>2</sub>) with hydrophobic octadecyltrichlorosilane patterns. Therefore, the positively charged NWs were attracted and aligned by the negatively charged APTS surface regions of the substrate. This technique was able to prepare arbitrarily shaped patterns using conventional microfabrication facilities; nonetheless it required the removal of the APTS SAM on the Si NWs with buffer oxide etching process.

A nanowire contact printing method was developed by et al. [31] which utilises the shear forces generated by mechanically sliding two solid surfaces, giving a high degree of order of assembled NWs. In this method two substrates are needed, namely, the donor and the receiver substrate. The donor substrate is covered with a dense “lawn” of NWs, while the receiver is coated with lithographically patterned resist. The method is based on a contact printing process by sliding the surfaces of the two substrates against each other under gentle pressure (**Figure 4a**). Also, lubricant is used to minimise the NW-NW mechanical friction and their uncontrolled breakage during the sliding process. During printing, NWs are transferred from the donor substrate to the receiver substrate by the van der Waals interactions, resulting in the direct alignment of a dense monolayer array of NWs (**Figure 4b–e**). This technique offers the ability to transfer monolayer arrays of NWs on both rigid and flexible substrates with a controllable density. The disadvantage of this technique is the lack of control of the number of the aligned NWs across the source-drain FET electrodes, and NWs tend to break during the transfer process [29, 31].

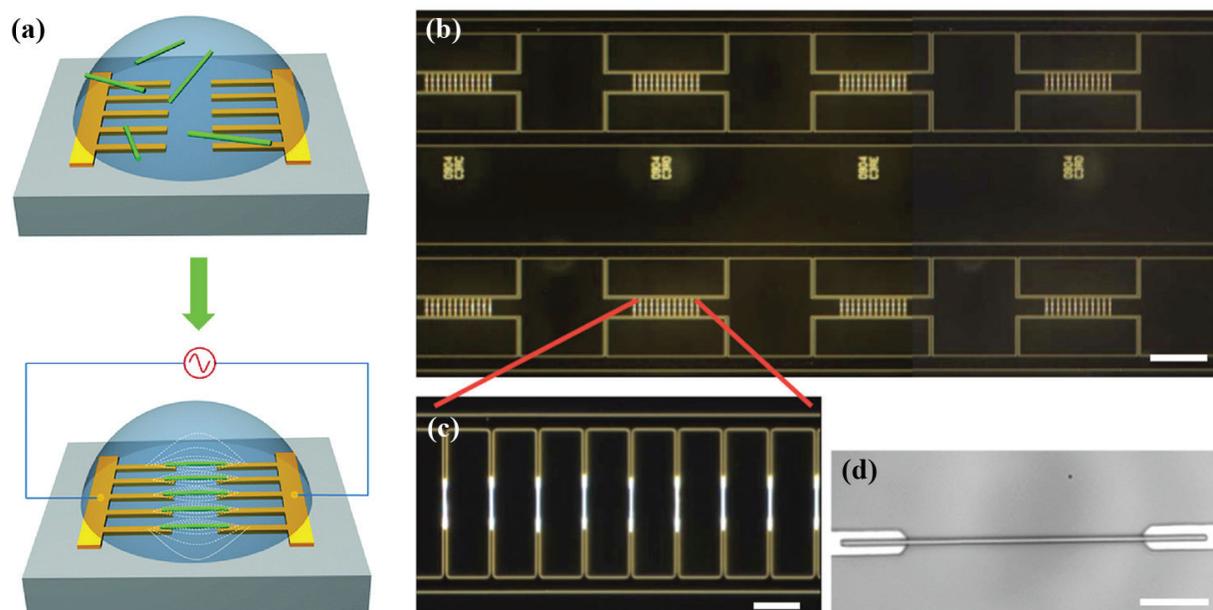


**Figure 4.** (a) A schematic illustration of the contact printing method. (b) Optical image of the assembly of Ge NWs on a Si/SiO<sub>2</sub> substrate. (c–d) Optical images of a cross assembly printing of Si NWs. (e) Printed Ge NWs on a 4 inch Si/SiO<sub>2</sub> wafer, including an inset SEM image of the printed NWs [31]. © 2008 American Chemical Society.

The electric field-assisted assembly known as dielectrophoresis (DEP) is currently the most promising nanowire assembly technique for the self-alignment of nanomaterials. During a DEP process, a polarisable nanoparticle, suspended in a liquid, is subjected to a non-uniform alternating electric field (AC), and its charges separate and accumulate at the surface, forming a dipole, which experiences the force dependent on the gradient of the electric field resulting in NW self-assembly across the electrode gap [32, 33]. The working principle of DEP is based on the balancing of NW-NW interaction and dielectrophoretic and opposing hydrodynamic drag forces. When the NW “ink” (nanowire dispersion) flows over the electrode gap with applied AC electric field, it gets polarised and attracted to the regions with the strongest electric field gradient, resulting in nanowire deposition across the electrode gap by means of dielectrophoretic forces ( $F_{\text{DEP}}$ ), as illustrated in **Figure 5a**. The deposition of NWs across the FET source-drain electrodes mainly depends on the difference in the dielectric properties ( $\epsilon$ ) of the nanomaterial and the medium, based on the Clausius-Mossotti factor (CMF) and the electric field gradient. As opposed to previously mentioned nanowire assembly techniques, the DEP method requires very small volumes of NW dispersion (a few  $\mu\text{L}$  per DEP alignment), and it offers a precise, dense and controllable deposition of NW monolayer arrays on predefined electrode structures with a high degree of orientation control as shown in **Figure 5b–d**. The NW density can be controlled by tailoring the NW concentration in the formulation and the applied DEP signal voltage [33, 34].

### 3.2. Self-assembly and purification of nanowires

Some of the key challenges in solution-processed NW applications are the simultaneous purification, selection, and alignment of NWs on the desired substrate areas, which have attracted



**Figure 5.** (a) Graphical illustration of dielectrophoretic assembly [1]. © 2012 American Chemical Society. (b) Optical image of NW assembly on eight multi-finger electrode arrays of total 96 sites (scale bar, 200  $\mu\text{m}$ ). (c) Precision alignment of NWs on a single sense array (scale bar, 20  $\mu\text{m}$ ). (d) Deep ultraviolet image of a NW aligned on a single electrode (scale bar, 4  $\mu\text{m}$ ) [34]. © 2010 Macmillan Publishers Limited.

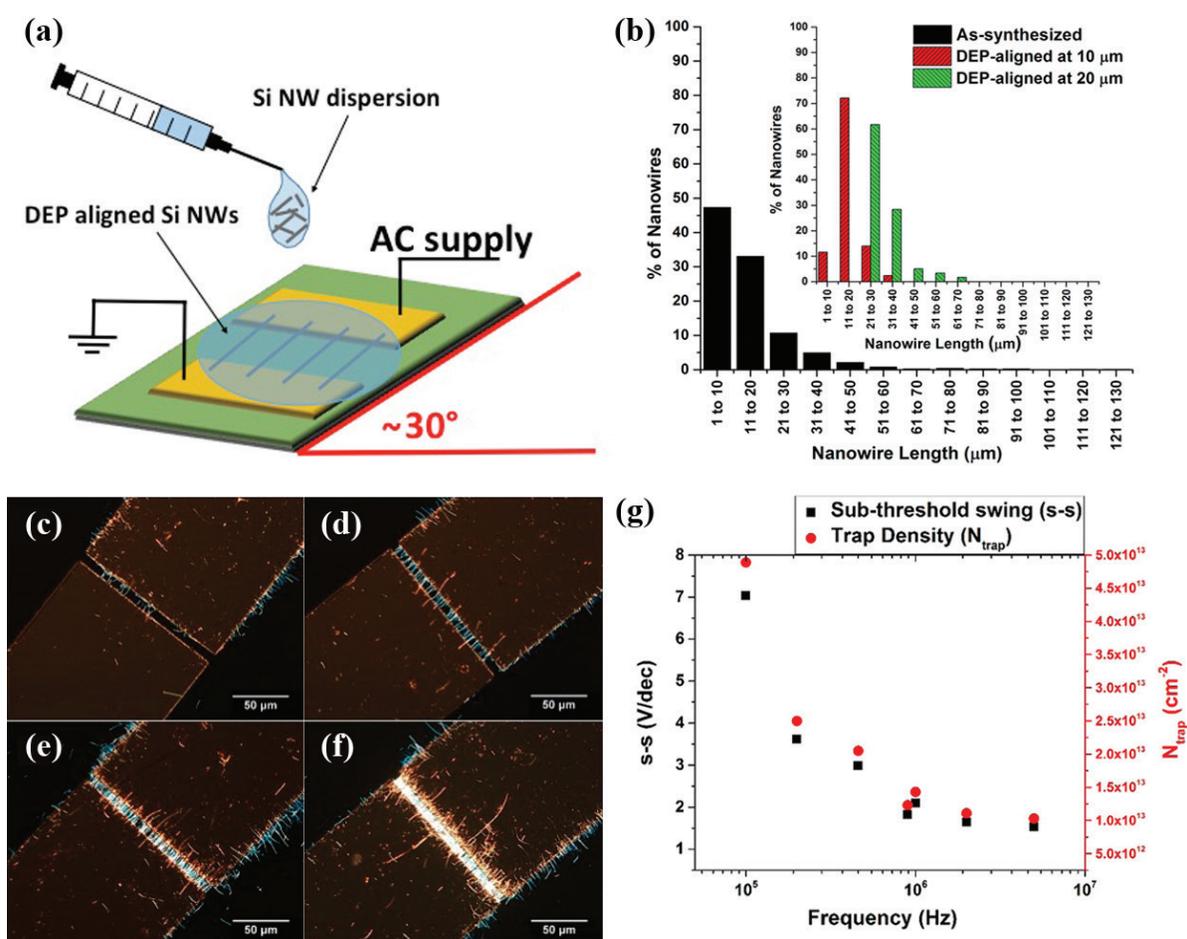
a significant research effort. Despite the substantial progress in NW assembly demonstrated with LB, BBF, flow-directed assembly, electrostatic interactions and mechanical shear forces, the simultaneous precise deposition of NWs with respect to device electrodes and the selective deposition of NWs based on morphological or electrical properties received little attention, and NWs were typically deposited as-synthesised, which affected device reproducibility, performance and reliability.

The first precise orientation positioning, selective deposition and separation of single Si NWs based on their electrical quality from a mixture of other types of nanowires were demonstrated using DEP with capillary assembly by Collet et al. [35]. The combination of both DEP and capillary assembly involved dragging the liquid meniscus of the NW solution on top of the substrate, with a controlled velocity and temperature which led to the trapping of single NWs by the DEP forces on predefined locations coupled with the capillary force acting to align the nanowires. The DEP force trapped the NWs and also adjusted their orientation at the surface of the electrodes followed by the liquid evaporation. A mixture of monodispersed Si, ZnO and InAs nanowires dispersed in isopropanol was used in this study.

The precise orientation of the NWs was achieved by employing stronger electronic polarisation along the long NW axis as compared to the short axis under the application of the AC electric field. In the case of Si NWs, the optimum capture frequency was obtained at 50 kHz and for InAs and ZnO were 500 kHz and 2 MHz, respectively. The authors argued that each NW exhibits its own specific signature based on their electrical properties, which leads to the assembly of different nanostructures at different frequencies. As a proof of concept, the authors provided separation and precise alignment of single Si and InAs nanowires from NW mixture containing both types of nanowires, into alternating columns on the substrate, by

switching the applied frequency between 50 and 500 kHz in each column of DEP electrodes, once the meniscus of the NW solution reached the desired set of electrodes. This work has successfully demonstrated a separation of nanowires with different electrical conductivities by examining their optimum capture frequency, which is influenced by the conductivity and level of doping.

Key progress in DEP nanowire selection and purification was demonstrated by Constantinou et al. [33] by developing a scalable one-step solution process for the selection, collection and ordered assembly of Si NW arrays (**Figure 6a**) with desired electrical properties from a poly-disperse as-synthesised NW dispersions. The method was applied to SFLS-grown Si NWs with various lengths, diameters and electrical conductivities. The technique utilised the fluidic shear forces coupled with DEP self-alignment to position high-quality NWs with the lowest level of traps across the electrode gap and to remove weakly interacting NWs and



**Figure 6.** (a) Graphical illustration of the fluidic shear force with DEP technique used for the NW deposition and DEP alignment. The substrate was tilted at approximately  $30^\circ$  angle (versus horizontal plane) to provide gravity-assisted flow of NW dispersion. (b) Length histogram of NWs collected by DEP across two different electrode gaps, 10 and 20  $\mu\text{m}$ . Controllable DEP alignment of SFLS Si NWs across parallel electrode bas with 10  $\mu\text{m}$  spacing at (c) 5 V, (d) 10 V, (e) 15 V and (f) 20 V. (g) Subthreshold swing (s-s) and NW trap density ( $N_{\text{trap}}$ ) data extracted from transfer characteristics of FETs for NWs collected from 100 kHz to 5 MHz [33]. © 2016 American Chemical Society.

impurities from the device channel region. The DEP assembly process employed a drop-cast method on an inclined substrate to provide a gravity-assisted slow flow of NW formulations perpendicular to the pre-patterned DEP electrode gap after the DEP sinusoidal signal was applied (**Figure 6c–f**). The DEP selectivity based on the NW electrical parameters was controlled by altering the frequency dependence of the DEP force. The DEP method coupled with fluidic shear forces offered a high degree of flexibility for NW positioning with NWs being oriented along the channel and perpendicular to the electrode edges. Importantly, the DEP also served as a nanowire length selection tool by providing the strongest interactions for the NWs with lengths at least the same size as the electrode gap or slightly longer opening the possibility for a sequential separation of NWs by length (**Figure 6b**). Main advancement of the method was in systematical examination of the electrical response of the Si NWs aligned at various DEP signal frequencies. It was highlighted that the  $F_{\text{DEP}}$  is frequency dependent and the level of polarisability is related to the conductivity of the nanostructure, allowing the selection of highly conducting NWs by altering the applied DEP frequency. Thus, lower frequency range collects NWs with various qualities including poor quality that may contain defects and associated traps, while high frequencies induce the collection of only the highest quality, low-defect semiconducting Si NWs, with higher conductivity. The electrical properties of the NWs aligned at various frequencies were compared using FET devices by extracting both subthreshold swing (s-s) and trap density ( $N_{\text{trap}}$ ) data as shown in **Figure 6g** and via conducting atomic force microscopy analysis. As a proof of concept, high-performance Si NW FETs with excellent performance were demonstrated with high FET on-currents in the mA range and low subthreshold swing (s-s) and trap density.

The proposed methodology enables the effective selection and assembly of heterogeneous nanowires of any type and provides a printed electronic fabrication approach that can be scaled up for industrial applications.

#### 4. Surface modification approaches for nanowire FETs

The undesirable electrical hysteresis effect in NW FETs is one of the main sources for performance instabilities, which affects the reproducibility and potential applications of NW FETs such as sensors, circuits elements and logic gates, that causes a shift in the threshold voltage ( $V_{\text{TH}}$ ) during normal device operation under gate bias stress. In most FET applications, besides memory devices, even a small degree of hysteresis is unwanted.

The hysteresis behaviour mainly originates from electron or hole trapping/detrapping at the semiconductor/insulator interface due to dielectric surface functionalities and adsorbed small molecules (e.g. oxygen and water). Typically such interface trapping is very strongly pronounced in bottom-gate NW FETs with  $\text{SiO}_2$  gate dielectric [36], where silanol groups trap charges at the interfacial layer between the semiconductor material and the gate dielectric [37]. In NW FETs, the hysteresis also originates from the NW surface traps, and it is observed in moisture-free environments and ambient air conditions, highlighting the demand for NW passivation. In this section, we describe NW surface passivation methods with an oxide shell for minimising hysteresis effects.

#### 4.1. Silicon nanowire surface passivation methods

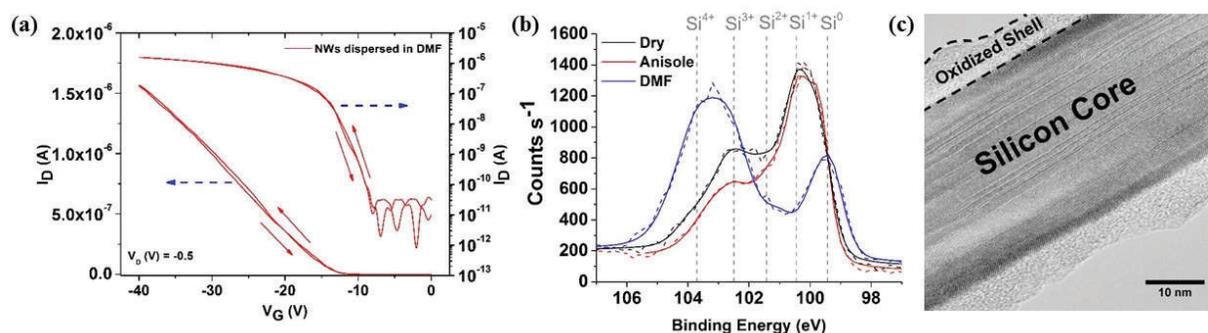
The majority of the NW surface passivation methods include high-temperature annealing which is not suitable for plastic electronic applications. However, successful passivation results for Chemical Vapour Deposition grown Si NWs have been demonstrated by Kawashima et al. [38] and Wang et al. [39]. Both approaches focused on the synthesis of core-shell Si NWs with the core acting as a channel and the shell acting as a gate dielectric.

Kawashima et al. [38] investigated the growth of a 24-nm thermal oxide layer on the surface of Si NWs (forming a core-shell structure) using rapid thermal processing in an oxygen atmosphere at 1100°C for 2–6 min. The authors compared the I–V characteristics of bare and core-shell Si NW FETs, although hysteresis appeared in both cases with a much smaller effect on the core-shell Si NW FETs than the bare Si NW FETs. The results proved that the hysteresis is drastically reduced by the formation of the oxide shell around the Si NW core, effectively passivating the Si NW surface and preventing the adsorption of oxygen and moisture which cause hysteresis. In a similar approach by Wang et al. [39], a silicon nanowire core was covered with a 10-nm-thick SiO<sub>2</sub> shell at lower annealing temperature (700°C) but for a much longer time duration (4 h), also resulting in near-zero hysteresis in devices.

A different approach [40] demonstrated thermal oxidation using ozone for forming a good quality 5-nm-thick SiO<sub>2</sub> shell layer obtained at 600°C processing temperature. However, such high-temperature annealing is not fully suitable for printed electronic applications, and a low-temperature process is still required.

A very efficient method for nanowire passivation that results in a dramatic reduction of surface trap states on Si NWs was demonstrated by Constantinou et al. [41]. This method is ideally suited for nanomaterials intended for printed electronic applications, as it is quick, fully solution based and conducted at room temperature and normal pressure. The passivation phenomenon was directly linked to the interfacial mild oxidation effect induced by the processing solvent.

Dimethylformamide (DMF) solvent treatment was used to directly reduce the hysteresis effect in solution-processed SFLS-grown Si NW FET devices [41]. The choice of solvents for the NW dispersion had a dramatic impact on the NW surface trap density and on the hysteresis effect. The undoped Si NWs were dispersed in both anisole and DMF, with DMF solvent-processed FETs exhibiting significantly low hysteresis of ~3 V, with the lowest reported hysteresis value being 0.1 V (**Figure 7a**), whereas the average hysteresis values of FETs based on nanowires dispersed in anisole were 25–32 V. Thus, DMF passivation effect of the Si NW shell resulted in a drastically suppressed NW FET hysteresis with up to 300 times (from 32 to 0.1 V) reduction as compared to anisole dispersion solvent [41]. For the investigation of the NW surface passivation, high-resolution X-ray photoelectron spectroscopy (XPS) technique was used to analyse the surface of the DMF- and anisole-treated Si NWs. It was observed that DMF-treated Si NWs showed a significant 35% increase of SiO<sub>2</sub> composition of NW shell around the core compared to the reference sample (dry NWs) as shown in **Figure 7b**. The formation of a SiO<sub>2</sub>-rich shell passivates the Si core channel area and provides stability against environmental ageing and prevents the adsorption of water molecules that are responsible for the hysteretic behaviour of the Si NW FETs (**Figure 7c**). As a further study, the DMF-treated devices were exposed to



**Figure 7.** (a) I–V characteristics of DMF-treated Si NW FET showing a very low hysteresis of 0.1 V. (b) XPS high-resolution spectrum of the Si2p region of SFLS-grown Si NWs dispersed in anisole and DMF. (c) HRTEM image of Si NW dispersed in DMF showing a single crystal silicon core with 30 nm diameter and 5–8-nm-thick amorphous oxidised polyphenylsilane shell [41]. © 2015 American Chemical Society.

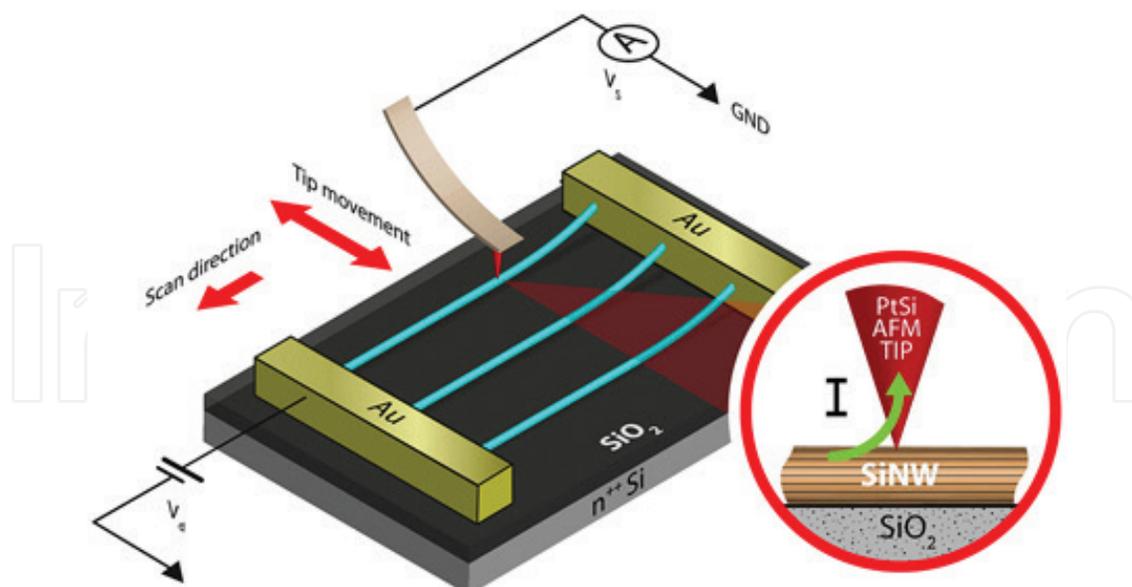
ambient conditions for 1000 h showing environmental stability, with a marginal increase of the hysteresis. In summary, the simplicity and effectiveness of solution-based mild oxidation methods offer fast passivation technological solution for printable nanowire-based electronics.

## 5. Scanning probe microscopy techniques for the characterisation of nanowires and devices

### 5.1. Introduction to conducting atomic force microscopy

Scanning probe microscopy (SPM) techniques evolved quite rapidly over the last two decades for incorporating additional modes beyond conventional topography [42, 43] and were able to provide additional characterisation information in comparison with traditional nanomaterial electron microscopy techniques such scanning electron microscopy. Driven by the introduction of novel one-dimensional conducting and semiconducting nanomaterials, SPM coupled with electrical modes became an integral part for the development and further understanding of these materials due to the unique capability of extracting critical information about the electrical properties of nanoparticles with a spatial resolution comparable to their nanoscale size [44, 45]. By combining this new level of information with conventional topography data [46], a correlation between structural and electrical properties can be established, thus enabling further optimisation of nanoparticles' growth and device integration mechanisms. In this section, the discussion will focus on recent advances in the field of conductive atomic force microscopy (c-AFM) for nanowire characterisation.

c-AFM is a current-based sensing technique for mapping the conductivity variations in samples. It utilises a conductive AFM tip which is brought in contact with a biased sample. During the scan, any current flowing through the sample and into the tip is recorded, forming a current map of the scanned surface (**Figure 8**). c-AFM can simultaneously map the topography and current distribution of a sample (**Figure 9**), thus making it ideal for evaluating defects formed during the fabrication of functional devices made with conducting or semiconducting NW networks.



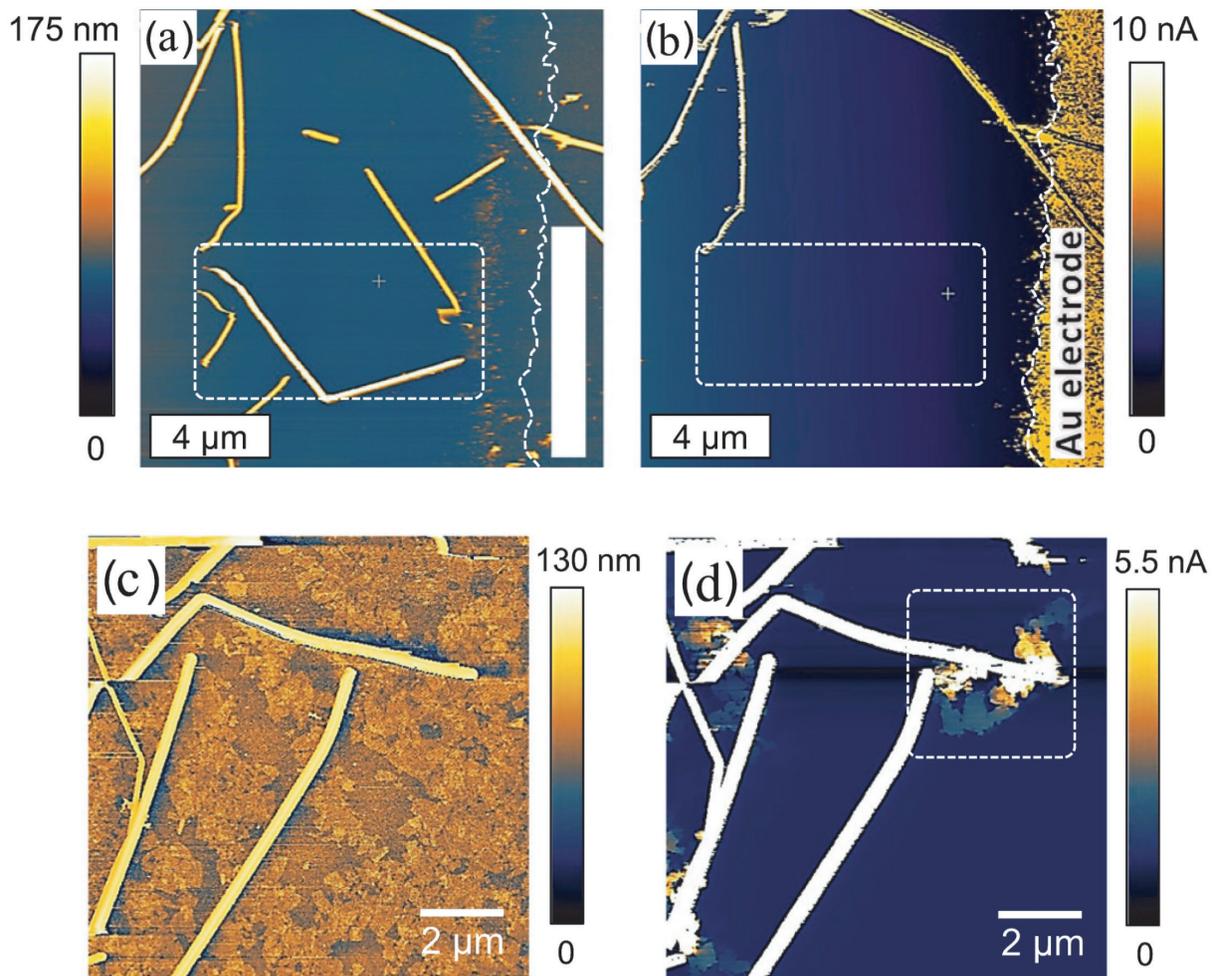
**Figure 8.** Schematic of c-AFM operating principle [33]. © 2016 American Chemical Society.

In the pursuit of solution processed, high conductivity and transparent alternatives to the ITO electrodes, commonly used in optoelectronic devices, metallic NWs were extensively studied [47–49]. One of the main fabrication challenges was the ability of the entire NW network to conduct and thus to minimise the effective sheet resistivity. Bridging the naturally occurring gaps between isolated nanowires during deposition (**Figure 9**) was considered of high importance, and several optimisation approaches were suggested [48, 50, 51]. While conventional measurement techniques can be employed for evaluating the conductivity improvement of these methods on the macroscopic scale, nanoscopic evaluation of the nanowire-to-nanowire connections requires a special approach. One of recent examples was based on using reduced graphene oxide (rGO) as a way of connecting discontinuities in silver nanowire (AgNW) networks [51]. c-AFM was successfully used for imaging these junctions and for proving the bridging effect induced by rGO flakes.

Example of metallic NWs acting as the electrode layer represents one of the most straightforward systems to be examined with c-AFM. Solution-processed nanowire electronics relies heavily on the active layers of the devices consisting of semiconducting NWs. Thus, efficient characterisation of nanowires, including FET device components and any defects on nanowires or contact areas, is essential for the advancement of printed electronics.

## 5.2. c-AFM characterisation of nanowires with high spatial resolution

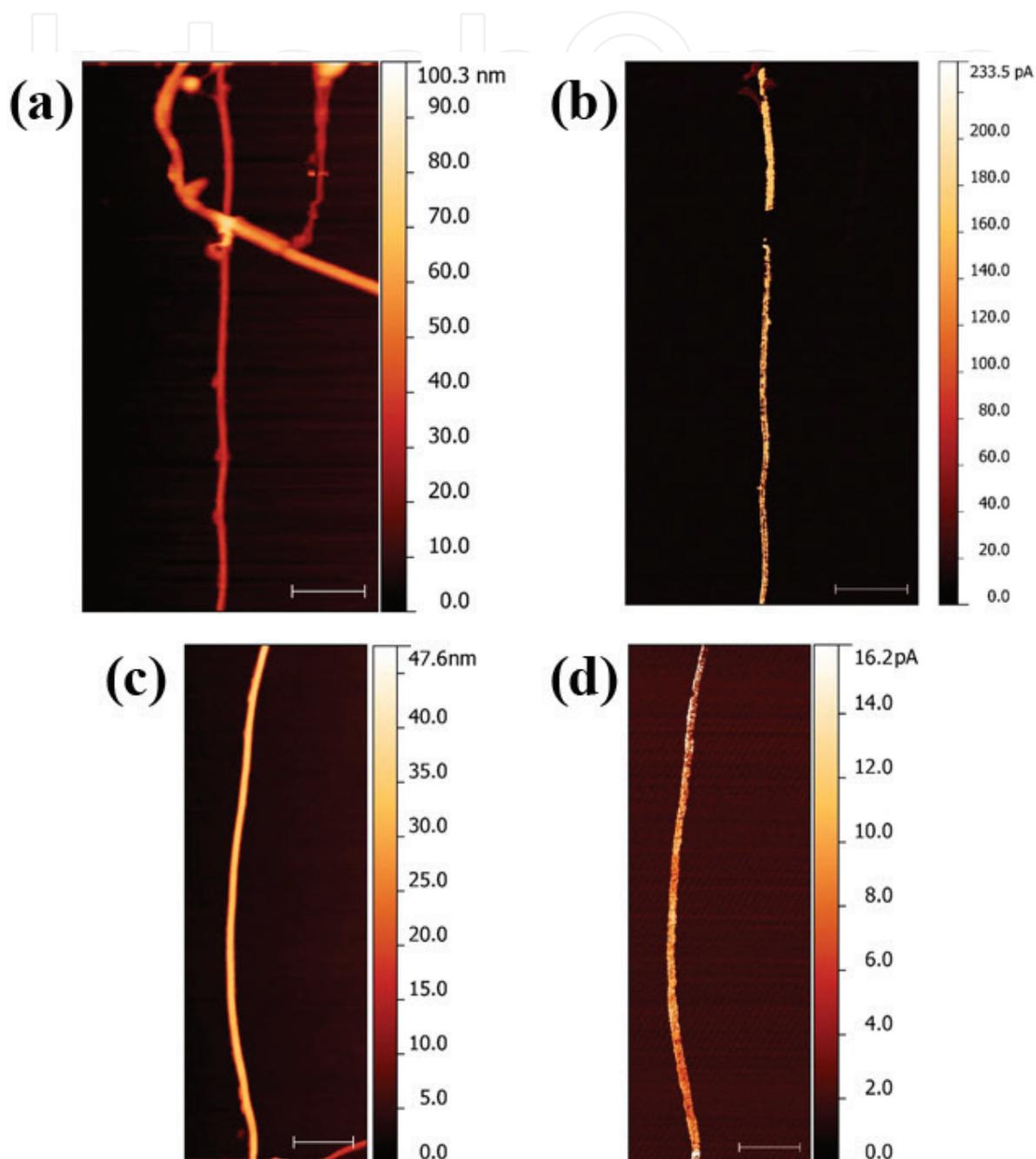
As discussed in Section 3, the purification of NWs based on their electrical properties is essential for their efficient incorporation in functional devices. Establishing a relation between the nanowire deposition methods and the properties of assembled nanowires, with very high spatial resolution, is key for high-performance printable nanowire-based FETs. Recently, c-AFM technique was employed for probing the electrical properties of polydispersed Si NWs, after selection processes using different dielectrophoretic signal frequencies [33]. In order to



**Figure 9.** (a–b) c-AFM images including topography (a) and current maps (b) obtained for an AgNW network at a tip bias of 1.6 V. As deposited NWs may result in discontinuities which affect the sheet resistance of the layer. (c–d) Topography (c) and current maps (d) of isolated AgNWs, electrically connected using rGO [51]. © 2016 AIP Publishing.

investigate the conductivity of the low- and high-DEP frequency-selected NWs, c-AFM measurements were conducted with Si NW channels in real FETs. The devices were prepared with Si NWs assembled at DEP frequencies of 220 kHz and 5 MHz. The samples were biased at the drain electrode of the structure, as shown in **Figure 8**, with the conductive platinum-silicide AFM tip being in contact with the Si NWs to act as a ground electrode. Such two-terminal current measurement allows probing the NW conductivity directly, as a function of position. The material for the tip was chosen in order to reduce the contact resistance with the underlying semiconducting nanostructures, without increasing the cantilever deflection and thus allowing soft contact with the sample. By keeping the bias constant at 0.5 V and maintaining constant force applied to the AFM tip, the current maps for NW samples deposited at various DEP signal frequencies were obtained by scanning the samples in contact mode in the direction perpendicular to the NWs. Both conducting AFM current data and AFM topological data were collected at the same time allowing to differentiate the NWs deposited in the channel, but not electrically connected to the contacts, from NWs that were fully electrically connected.

**Figure 10** demonstrates typical images obtained for both height (AFM mode) and current (conducting mode) measurements of Si NWs aligned at different DEP frequencies. During the measurement, a common trend was observed that NWs collected using a high, 5 MHz, DEP signal showed  $\sim 14$  times higher current than the ones collected at low, 220 kHz, frequency. Current levels up to 233 pA were obtained for the NWs aligned at 5 MHz (**Figure 10b**), while peak

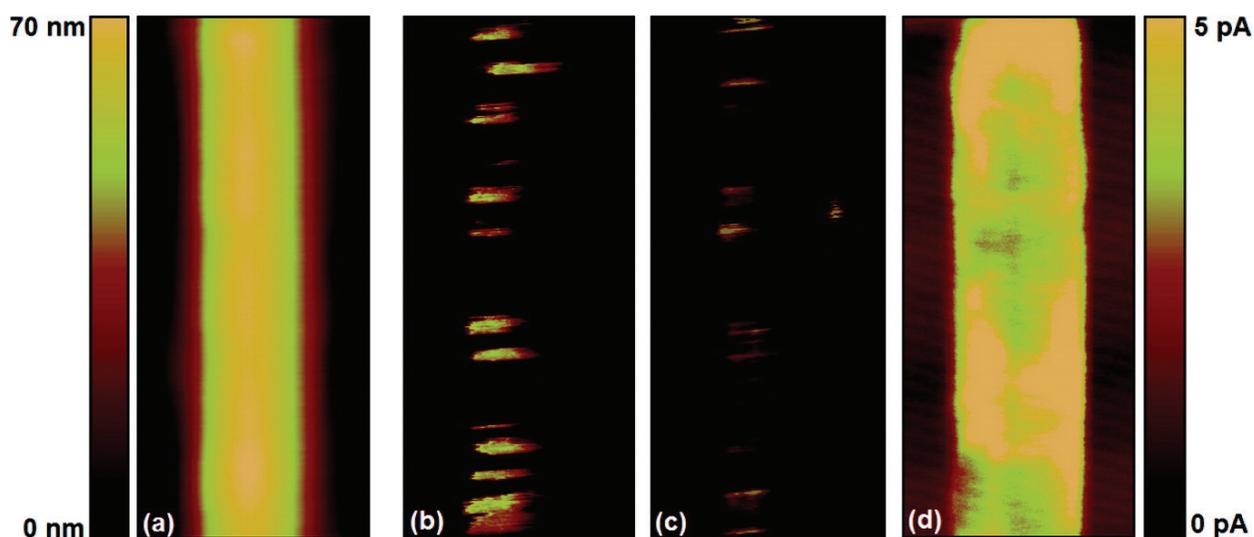


**Figure 10.** c-AFM data. (a) Height map of Si NWs aligned at 5 MHz and (b) the corresponding current map. Only one straight, fully electrically connected NW is visible in the image. (c) Height map of a NW aligned at 220 kHz and (d) its current map. Scale bars are 1  $\mu\text{m}$ . Conducting Si NWs have similar diameters, (a) 33 nm and (c) 34 nm. All the images were obtained in the trace mode with a pixel size of 5.9 nm. NWs aligned at higher frequency showed higher peak currents up to 233 pA (b), compared to the 16-pA peak current found in the lower frequency assembled NWs (d) [33]. © 2016 American Chemical Society.

current values of 16 pA were measured for the ones assembled at 220 kHz (**Figure 10d**). These current differences between the NWs collected at high and low DEP signal frequencies were fully consistent with the transistor measurements, demonstrating that selective nanoparticle assembly at various dielectrophoretic frequencies is directly correlated with the conductivity of the NWs.

Incorporation of semiconducting NWs into functional devices requires to consider surface oxide properties as well, to enable the efficient coupling of these nanowires with the rest of the device components [52]. In Si NWs, for example, native or intentionally grown surface oxide can act as an insulator or as a poor charge transport medium with limited conduction [53]. In such cases, the uniformity of this oxide layer can be of fundamental importance for the overall functionality of the device. Conventional approaches for imaging any defects in the oxide shell, such as transmission electron microscopy, rely on the observed structural uniformity only and may lead to incorrect assumptions regarding its electrical characteristics.

In a work published in 2008, Stratakis et al. [54] compared the differences between oxide grown on planar Si and Si NWs, in an attempt to evaluate the reliability of these nanostructures for future applications. By examining several nanowires, it was found that the interface barrier for electron injection from silicon core into the oxide shell was similar to planar oxides. Trap density however was susceptible to the non-uniformities of the oxide shell, which, despite appearing to be planar under conventional topography or TEM, had localised weaknesses (**Figure 11**). These weakness areas did not appear to lower substantially the threshold for current leakage through the oxide, but they were potential reliability hazards in nanowire-based devices. This work demonstrated quite successfully that electrical characteristics in NWs may vary significantly depending on the growth conditions of the shell layer. It can also serve as an example of the level of information that can be extracted using advanced SPM techniques.



**Figure 11.** c-AFM current through NW oxide. (a) AFM topography image of part of a NW. Images b, c and d are current maps of the same part of the wire. At the pristine state of this wire, current was first detected at a bias of 13 V (b). Emission is inhomogeneous. Reduced average current in the second scan (c) is attributed to electron trapping in the oxide. At a higher voltage (16 V), increased current density appears from the entire surface of the nanowire (d) [54]. © 2008 American Chemical Society.

## 6. Conclusions

Solution-processed nanowire field-effect transistors have reached the threshold of being commercially viable due to the developments in nanowires controllable assembly. The main criticism for nanowire-based electronics was linked in the past to the lack of control of a number of nanowires between the device electrodes, thus limiting the devices reproducibility. Recent developments in the field, focusing on solvent-based reproducible and controllable positioning, orientation and placement of nanowires on predefined substrate locations, also coupled with nanowires' purification and selection methods, have provided the necessary breakthroughs to enable scalable fabrication of nanowire devices, including FETs.

For some time, the main target in NW assembly was to reach a high deposition yield and well-aligned nanostructures over large areas as an attempt to achieve superior device performances and reproducibility. However, more precise control of nanowire properties in fabricated devices can only be achieved by full integration of separation and purification processes for nanomaterials, based on their electrical and morphological properties. Currently, the only assembly technique offering all of these features is electric-field-assisted dielectrophoresis. This method is scalable and can be applied in large-area device deposition. Scanning probe microscopy characterisation techniques, such as conductive AFM, capable of simultaneous topological and conductivity measurements of nanowire active channels in electronic devices with high spatial resolution, have helped to optimise the nanowire properties and the corresponding selection and deposition methods.

In summary, solution-processed nanowire field-effect transistors represent a powerful technological platform with high potential for low-cost large-area electronics with applications targeting chemical, biological and tensile sensing; flexible circuits; memory; displays; and photonic devices.

### Author details

Maxim Shkunov\*, Grigorios Rigas and Marios Constantinou

\*Address all correspondence to: m.shkunov@surrey.ac.uk

Advanced Technology Institute, Electrical and Electronic Engineering, University of Surrey, Guildford, UK

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