Chapter 3

Cascaded H-Bridge Converters Based on Current-Source Inverters: Analysis, Design, and Application on AC Drives

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Abstract

This chapter reviews the cascaded H-bridge (CHB) based on current-source inverter (CSI) topology. First, the description of power topology is presented from the point of view of the current-source single-phase inverter and it connection in series with others inverters. Then, modulation of the single-phase inverter is studied, including the use of multi-level modulation techniques and their use in the proposed power topology are reviewed and simulated. Next, key design guidelines of the output capacitor and the DC inductor are reviewed. Finally, an application example for AC drives simulated in PSIM is presented. From the study, it can be concluded that the main advantage of the topology is the quality of both input currents and load voltage, while its main drawback is the use of a bulky DC inductor because of the use of current-source inverters and the oscillating power drained by the inverter from the DC side. In the same way of classic cascaded H-bridge topologies, the use of the proposal topology allows us to use semiconductors and passive components with lower voltage and current rating than the voltage and current required by the load.

Keywords: single-phase current-source inverter, cascaded H-bridge converter based on current-source inverter, oscillating power compensation

1. Introduction

Limited voltage and current rating of semiconductors are the main limitations of the different static power converter topologies [1–4]. Diodes and thyristors are the power devices with the

higher voltage blocking levels and conduction current levels, but diodes work with natural commutation while thyristors can only be communed to conduction condition. The above operation conditions do not allow one to control the electrical power transferred by the power converter—in diode-based topologies—or have poor power quality, increasing not only the input harmonic but also injecting unwanted reactive power—thyristor-based topologies - . On the other hand, force-commuted power semiconductors allow controlling the electrical power transferred and increase the power quality in both input and output of the power converter. The device's voltage and current ratings are lower than diodes and thyristors, and so in order to reach higher voltage and current levels, the devices connection in series or in parallel are typically used. From this kind of connection, and gating the devices in a convenient way, it is possible to increase further the current and voltage quality, allowing reducing losses and the size of the filter components.

The cascaded H-bridge (CHB) topologies are born under the next concept: to reach higher voltage levels using power valves with lower voltage rating, while a high power quality is keeping in the load and the power source [5–7]. Classical topology is based on H-bridge voltage-source inverters, where the series connection is natural because each inverter works as a controlled voltage source. Because of the series connection, each inverter can be disconnected from the whole array without this implying that the equipment should get offline, which is highly convenient when an inverter fails, increasing the reliability of the equipment. On the other hand, an array of nC cells per phase in a three-phase system allows dividing the load power on 3nC cells [8] so that the electrical stress in each cell is lower than other power topologies as three-phase inverters and their extension to multilevel topologies—as neutral point clamped, for example. A drawback of the cascaded connection is the power device losses which are mainly a function of the current level; in a cascaded connection, this current level is equal in all the power devices. On the other hand, for current-source converter, the natural multilevel connection is using inverters in a parallel connection. This allows summing the current injected by each converter, increasing the current waveform capability. A drawback is that the voltage rating in all the semiconductors is equal to half of the load voltage, while the capacitive filter voltage rating is equal to the load voltage.

Cascaded H-bridge based on current-source inverter (CSI) is an emerging power topology that uses a current-source inverter and a capacitive filter to synthetize a controlled voltage source that can be connected in series with other controlled voltage sources in order to reach higher voltage levels. It has been proposed for the first time in 2008 [9] for AC drive applications, and its study has been focused mainly in reducing the size of the DC inductor, the use of control techniques [10] and the compensation of using cells that are magnetically coupled [11–14], the control of the inverters using linear control and non-linear control [15–17], and the modulation and design of the power topology [18, 19].

This chapter study the cascaded H-bridge topology, without using any DC inductor reduction technique, focusing the study in operation of the power topology, the series connection of several current-source inverters in series, the use of multilevel modulation techniques, and how it defines the size of the capacitive filter required for each inverter. Also, the effect of the oscillating power drained by the inverter is described, including how it defines the size of the

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DC inductor is studied. Finally, the application in an AC drive computing the operation region and the key waveform of the power topology for both steady states and step changes in the DC current are studied.

2. Power topology

2.1. Power cell based on single-phase current-source inverter

Each power cell based on a single-phase current-source inverter fed by an isolated DC current source is shown in **Figure 1**. In the single-phase current-source inverter, each power valve requires symmetric blocking capabilities in order to block the AC voltages which have positives or negative values. For the abovementioned requirement, power valves can be implemented using gate turn-off thyristor (GTO) with insulated-gate bipolar transistor (IGBT) with reverse blocking capability or an IGBT with a diode in series, in order to get the reverse blocking capability. Also, new semiconductor technologies such as wide bandgap semiconductors can be used, allowing increases in the switching frequency of the power converter.

In order to simplify the power cell analysis, let's assume that we can use an ideal DC current source. This DC current source fed the single-phase inverter and, jointly, they injected a pulse width modulated current to the capacitor C_o and the load Z_L. If the modulation functions s_i of the CSI are given by

$$s_i = s_1 s_2 - s_3 s_4, \tag{1}$$

then the current injected by the CSI and the voltage in the DC side are

$$i_o = i_{dc} s_i, \tag{2}$$

and

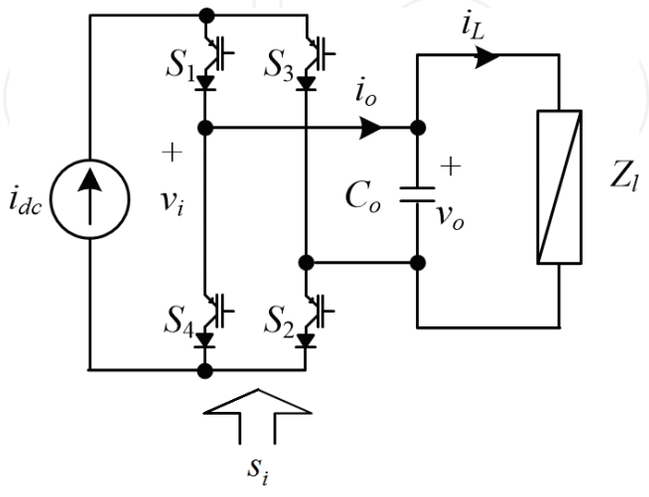

Figure 1. A power cell for CHB-CSI.

$$v_{\mathrm{i}} = v_{\mathrm{o}} s_{\mathrm{i}}. \tag{3}$$

The modulation function s_{i} can be approximated to its fundamental component; then,

$$s_{\mathrm{i}} \approx m_{\mathrm{i}} \sin(\omega_{\mathrm{s}} t + \alpha), \tag{4}$$

and the injected current and the DC voltage v_{i} can be defined as a function of this simplification

$$i_{\mathrm{o}} = i_{\mathrm{dc}} m_{\mathrm{i}} \sin(\omega_{\mathrm{s}} t + \alpha), \tag{5}$$

and

$$v_{\mathrm{i}} = v_{\mathrm{o}} m_{\mathrm{i}} \sin(\omega_{\mathrm{s}} t + \alpha). \tag{6}$$

Using the above equations, the load voltage is equal to the capacitor voltage, v_{o}, and both are given by

$$v_{\mathrm{o}} = v_{\mathrm{L}} = i_{\mathrm{o}} \left(\vec{z}_{\mathrm{L}} || \vec{x}_{\mathrm{Co}} \right) \approx i_{\mathrm{dc}} m_{\mathrm{i}} \sin(\omega_{\mathrm{s}} t + \alpha) Z_{\mathrm{L}}. \tag{7}$$

The simplification can be made only if $\vec{z_{\mathrm{L}}} << \vec{x_{\mathrm{Co}}}$ so that all the fundamental components circulate through the load. This consideration must be included in the design requirement of the output capacitor.

2.2. Modulation and harmonic compensation on CHB-CSI

Because of the use of single-phase current-source inverter, two conditions must be avoided—(i) the electrical circuit of the DC current—typically based on an inductor—must not be open and (ii) the AC side must not be shortcircuited. The first case is because of the use of an inductor to synthetize the DC current source, and if it is open, the voltage on the power valves will theoretically become infinity; the second case is because the use of a capacitor is on the AC side. Then, if the capacitor is shortcircuited, the current on the semiconductor will be infinity. Both conditions can destroy the semiconductors used to implement the power valves.

Single-phase current-source inverter has four valid conditions (**Table 1**). Each state avoids the above conditions and allows transfer of electrical power to the load—state #1 and state #2—or disconnects the load from the DC current source—state #3 and state #4—also called zero states.

State	S1	S2	S3	S4	Io	Vi
#1	1	1	0	0	Idc	Vo
#2	0	0	1	1	−Idc	−Vo
#3	1	0	0	1	0	0
#4	0	1	1	0	0	0

Table 1. Single-phase current-source inverter states.

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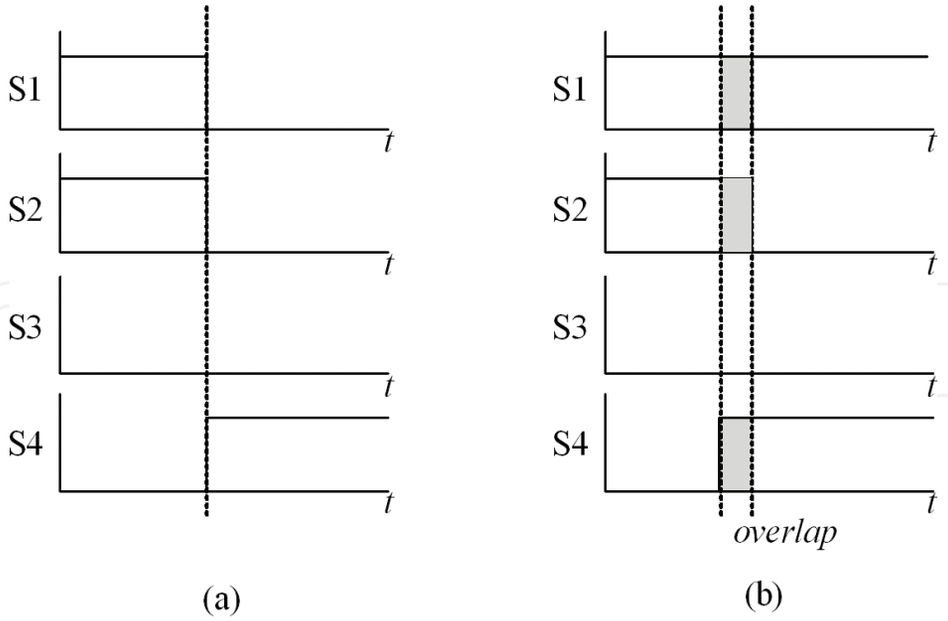

Figure 2. Transition between single-phase CSI states and overlap: (a) transitions without overlap and (b) transitions using overlap.

On the other hand, on transitions between states—**Figure 2**—it is necessary to ensure that the electrical circuit of the current source is not open. For the above, an overlap must be implemented when the inverter state is changed. The overlap should last long enough for the power valve to complete the switch. In the example, the first state is #1 and final state is #4 and in the transition between the states, the overlap is implemented.

Because of the use of a capacitive filter in each power cell, CHB-CSI topology is not a multilevel power topology but in the same way as that of multilevel topologies, the use of an appropriate modulation technique allows compensating some harmonics among inverters. In a typical current-source multilevel topology, these harmonics will be harmonic currents; in a CHB-CSI topology, the compensated harmonics will be voltage harmonics in the capacitive filter.

Sinusoidal pulse width modulation (SPWM) will be studied as an example of a modulation technique which can be used in CHB-CSI topologies. SPWM has the following advantages: it is easy to implement using both analogic circuit and digital circuit, it has the facility to modify SPWM techniques to use it in a multilevel application and the fundamental gain of the modulation technique, which in single-phase inverters, is unitary. In SPWM, a reference signal called modulator is compared with a triangular signal, also called carrier. Comparison generates a Boolean signal which is used to commutate the power valves. The inverters output signal is a pulse width modulated signal which has a wanted fundamental component and several unwanted harmonics which are the functions of the modulator frequency and the carrier fundamental frequency, so, higher carrier frequencies not only displace the unwanted harmonic to higher frequencies but also increase the commutations per period of the semiconductor devices. In multilevel topologies, the connection of the power converters in series—in the case of voltage-source converters—or parallel—in the case of current-source converters—allows to sum up the DC voltage/current levels and compensate the unwanted harmonics if

they are generated and phase-shifted among them in an appropriate way. In case of phase-shifted carrier (PSC) sinusoidal pulse width modulation, the switching signals are generated comparing n_C carriers phase-shifted at $180°/n_C$, among them with a common modulator signal. An example simulated in MATLAB is shown in **Figure 3**. In the first case, the modulator signal is compared with the carrier, generating the pulse width modulation signal shown below (**Figure 3a**). Multilevel cases are **Figure 3b** and **Figure 3c** for $n_C = 2$ and $n_C = 3$, respectively, where the resulting waveform is of 5 levels for $n_C = 2$ and 7 levels for $n_C = 3$. Computing and comparing the total harmonic distortion (THD) of the three PWM signals presented, these values are 46, 25, and 14% for $n_C = 1$, $n_C = 2$, and $n_C = 3$, respectively, showing the reduction of the distortion of the resulting pulse width modulated waveform without increasing the commutation frequency. The above is valid for multilevel topologies. The effects of using PSC SPWM in a CHB-CSI topology—which is not a multilevel topology—will be analyzed in the next section.

2.3. Cascaded connection of single-phase CSI

Inverters with their isolated and controlled DC current source and their capacitive filter can be connected in a series array because each power cell is working as a controlled AC voltage source (**Figure 4**). With the above, the voltage of the array is the sum of all power cells connected to it, allowing (i) to use components with lower voltage ratings than the voltage of the application and (ii) to divide the power of the application in multiple power cells. **Figure 4** shows multiple power cells—which will be named as $3n_C$—feeding a common three-phase load. Each cell injects a controlled current to the load. Defining $\vec{i}^{j}_{oi,1}$ as the fundamental current of the $i = 1, 2, \ldots, n_C$ cell feeding the j = u,v,w phase and $\vec{i}^{j}_{L,1}$ as the fundamental component of the load current of the same j phase, then

$$\vec{i}^{j}_{L,1} = \vec{i}^{j}_{o1,1} = \vec{i}^{j}_{o2,1} = \ldots = \vec{i}^{j}_{onc,1}, \tag{8}$$

while the load voltage is the summation of the cell output voltage, each one is given by the voltage on the capacitor filter so

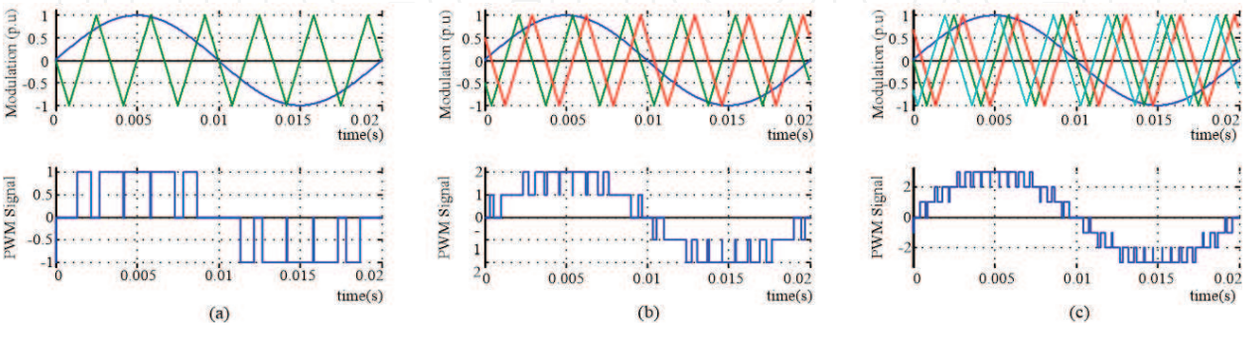

Figure 3. Sinusoidal pulse width modulation and phase-shifted carrier sinusoidal pulse width modulation with a modulation signal equal to 50 Hz; (a) modulator, carrier signals, and 3 levels of pulse modulation signal, (b) modulator, carrier signals, and 5 levels of pulse modulation signal, and (c) modulator, carrier signals, and 7 levels of pulse modulation signal.

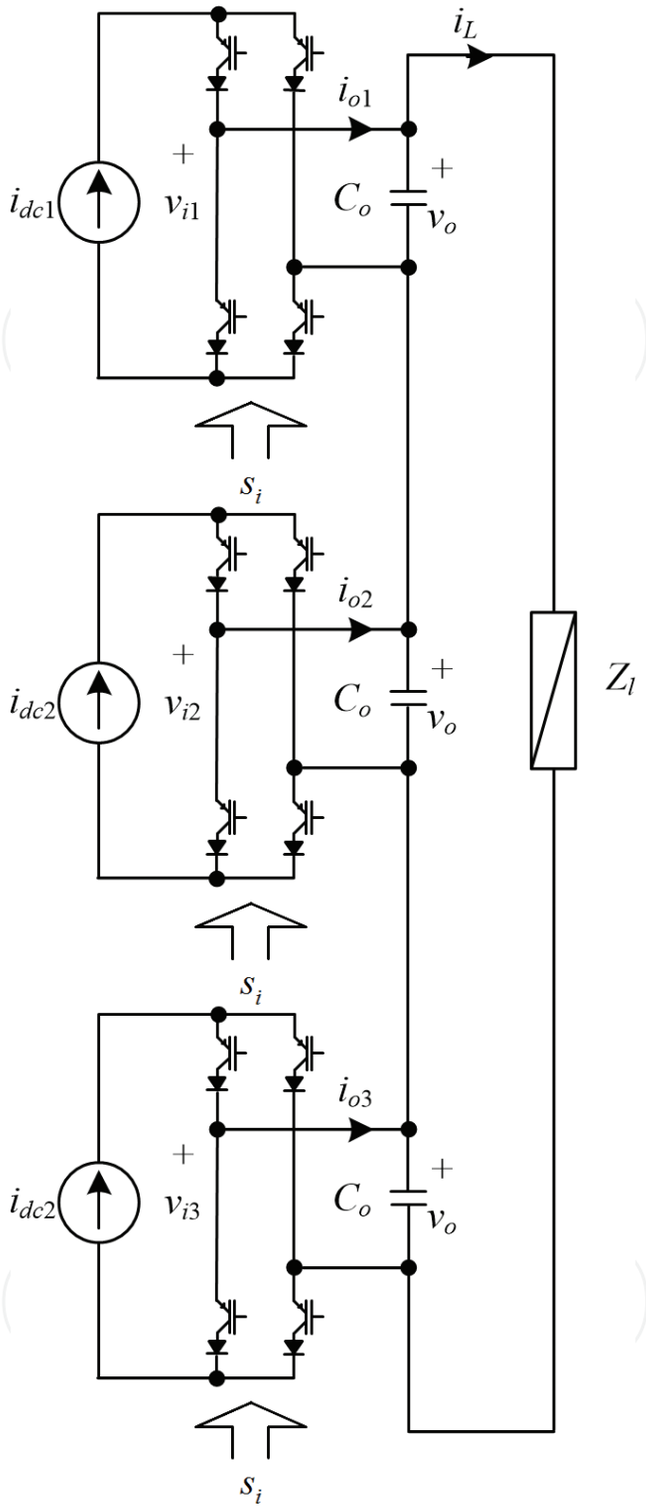

Figure 4. Three-phase applications of CSC-CHB ($n_C = 3$).

$$\vec{v}_{\mathrm{L},1}^{\,j} = \vec{v}_{\mathrm{N\,j},1} = \sum_{i=1}^{n_C} \vec{v}_{\mathrm{oi},1}^{\,j} = \vec{i}_{\mathrm{L},1}^{\,j}\,\vec{z}_{\mathrm{L},1}. \tag{9}$$

From the equations, it is clear that the connection of single-phase inverters in a cascaded array allows dividing the load voltage *in N* cells, allowing the use of a semiconductor with lower

voltage rating than the required load voltage, but the current in each cell is equal to the other, increasing semiconductor losses.

An advantage of the topology is the quality of the voltage waveform at the load. Because of the use of a capacitive filter, the sum of all cell output voltages is not a multilevel voltage, but through the multilevel modulation technique that is used in each inverter connected in series, it is possible to compensate the dominant harmonic among cells. An example of the above is shown in **Figure 5**, where the topology has been simulated using PSIM in order to obtain the load voltage waveform for $n_C = 1$, $n_C = 2$, and $n_C = 3$. For $n_C = 2$ and $n_C = 3$, a multilevel modulation technique—specifically phase-shifted carried pulse width modulation—is used. For $n_C = 1$, one has THD = 28.2% which is reduced to THD = 9.6% in $n_C = 3$. The above is because dominant harmonic presented in each capacitor is phase shifted with the dominant harmonic in the other capacitor. Each capacitor voltage for N = 2 and $n_C = 3$ can be seen in **Figure 5d** and **e**, where each waveform is similar to the voltage capacitor in $n_C = 1$.

2.4. Isolated DC current source for power cells

Each power cell requires an isolated DC current source and there are several options to implement the DC current source. For example, a controlled rectifier in series with a DC

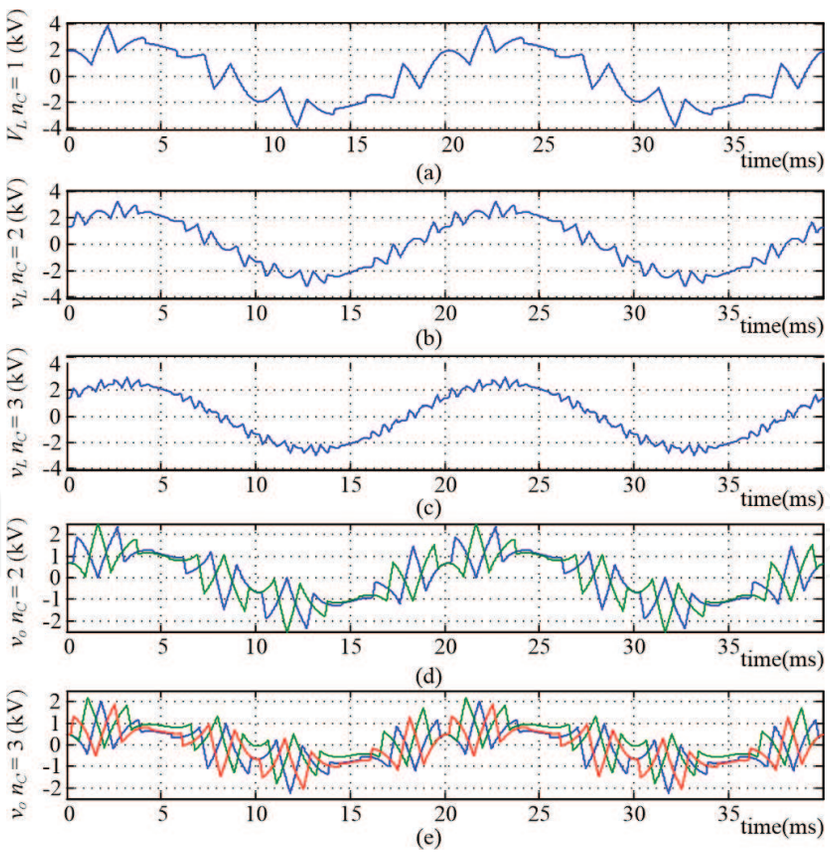

Figure 5. Voltage features for $n_C = 1$, $n_C = 2$, and $n_C = 3$, $C_o = 17\mu F$; (a) load voltage for $n_C = 1$ (THD = 28.2%), (b) load voltage for $n_C = 2$ (THD = 14.2%), (c) load voltage for $n_C = 3$ (THD = 9.6%), (d) capacitor voltage for $n_C = 2$, and (e) capacitor voltages for $n_C = 3$.

reactor can be used to get, from the viewpoint of the inverter, a controlled DC current source. In order to isolate this DC current source from other DC current sources that feed other power cells, a power transformer is required. With the above, the rectifier stage can be implemented using single-phase or three-phase controlled rectifiers based on thyristor or force-commuted semiconductors as IGBT or silicon carbide (SiC). Both cases require a DC reactor on the DC side; in thyristor rectifier cases, it can be connected directly to the secondary transformer while in force-commuted semiconductor rectifiers, an LC filter is required between the secondary transformer and the rectifier. Another option is to use a diode rectifier and a DC/DC converter on the DC stage. This case limits the power that can be transferred to the inverter stage but is a good option for non-conventional renewable power source. Also, if the source is a DC power source type, a DC/DC to regulate the DC current to the inverter stage can be used. This is the case of photovoltaic arrays and fuel cells. A third case is when the inverters are directly connected to the power grid. In this case, the DC current source can be implemented with the single-phase inverter and the DC inductor. The DC current regulation must be implemented in the inverter control scheme.

3. DC Reactor on cascaded H-bridge based on current source inverters

3.1. Oscillating power on single-phase current-source inverter

Using single-phase inverters involving the occurrence of an oscillating and continuous power, it can be described as

$$p_{\mathrm{o}} = S_{\mathrm{o}}\left[\cos\left(\phi_{\mathrm{m}}\right) - \cos\left(2\omega_{\mathrm{i}}t + 2\alpha_{\mathrm{i}} + \phi_{\mathrm{m}}\right)\right], \tag{10}$$

where $S_{\mathrm{o}} = \frac{1}{2} Z_{\mathrm{m}} {I_{\mathrm{dc}}}^2 {M_{\mathrm{i}}}^2$ is the load apparent power, M_{i} is the inverter modulation index—considering fixed for this case—and Z_{m} is the equivalent impedance of the load in parallel with the inverter output capacitor as is shown in **Figure 6**. Then, the power drained from the cell can be written in terms of the cell energy, and the charge and discharge of the DC inductor current is

$$P_{cell} = \frac{\Delta E_{cell}}{\Delta t} = \frac{L_{\mathrm{dc}}\left[{i_{\mathrm{dc}}(t_2)}^2 - {i_{\mathrm{dc}}(t_1)}^2\right]}{2(t_2 - t_1)} = p_{\mathrm{o}}(t_2) - p_{\mathrm{o}}(t_1), \tag{11}$$

where $i_{\mathrm{dc}}(t_1) = I_{\mathrm{dc}}$ e$i_{\mathrm{dc}}(t_2) = I_{\mathrm{dc}} k_{\mathrm{dc}}$, and a k_{dc} near to 1 means that there is no variation in the DC current level. With the above, one can write

$$4\omega_{\mathrm{i}}\pi^{-1} L_{\mathrm{dc}} {I_{\mathrm{dc}}}^2 \left[{(k_{\mathrm{dc}})}^2 - 1\right] = S_{\mathrm{o}}. \tag{12}$$

Then, the DC current variation, in per unit, can be written as

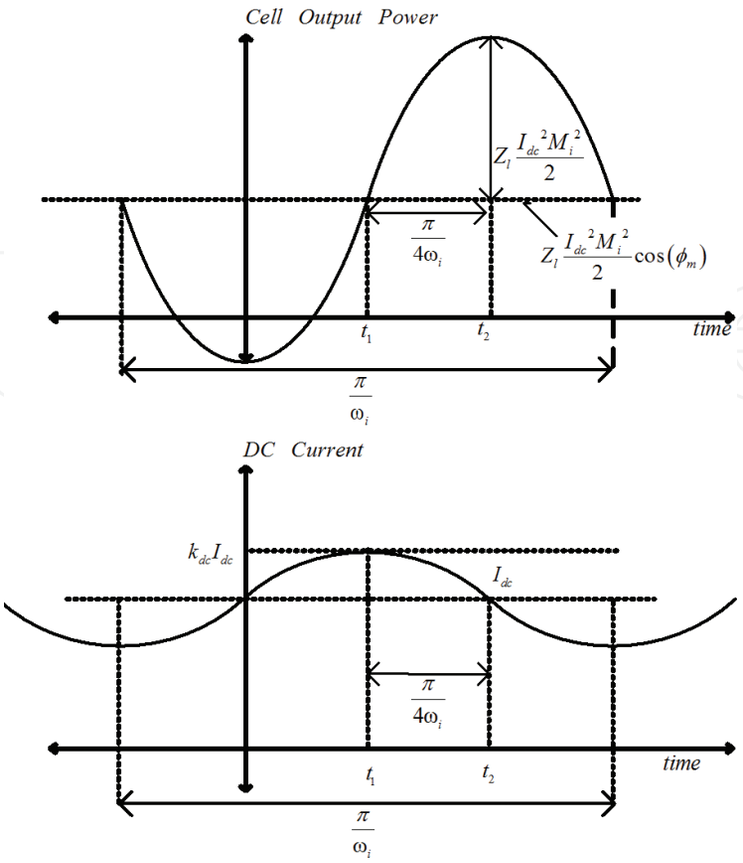

Figure 6. Oscillating power and its effects in the DC current.

$$k_{\mathrm{dc}} = \sqrt{\frac{\pi}{8\omega_{\mathrm{i}}} \frac{Z_{\mathrm{m}} M_{\mathrm{i}}^2}{L_{\mathrm{dc}}} + 1}. \tag{13}$$

Considering that the power converter that feeds the DC inductor and the single-phase inverter only injects to the DC side, the continuous power drained by the inverter—corresponding to the active power delivered by the inverter to the load—and that the voltage imposed by power converter in the DC side has mainly a DC component, another element must provide the oscillating power so that it does not disturb the DC current.

The easier solution to avoid the DC current variation due to the oscillating power is to increase the size DC inductor. This increases the losses in the DC link, along with the size of the inductor and increases the cost of each cell. Other options consider the use of active compensators in the DC side, tuned passive filters, or neutral leg. Specifically, for the case of an AC drive, the active compensation adds complexity to the topology, adding semiconductors and additional accumulators to DC link, besides requiring additional controllers to manipulate the semiconductors incorporated, but it is a good option when the inverters are directly connected to the electrical grid or when the CHB-CSI topology is used in photovoltaics application. On the other hand, the passive techniques are mainly applied to cases where the frequency inverter is fixed, making a complex application for AC drives.

3.2. DC inductor design

The main objective of the DC inductor is to limit the DC current variation. Due to the oscillating power drained by the single-phase inverter and its effects on the load current and load voltage, the lower frequency that the DC inductor must limit to is the second harmonic of the inverter frequency. Then, using Eq. (11) and defining k_{dc} in Eq. (13), the DC inductor can be computed with

$$L_{dc} = \frac{\pi}{8\omega_i} \frac{Z_m {M_i}^2}{\left({k_{dc}}^2 - 1\right)}. \tag{14}$$

4. Capacitive filter

4.1. Capacitive filter design as a function of the load voltage THD, $n_C = 1$

For $n_C = 1$, the inverter output voltage v_o is equal to the load voltage. Also, the output voltage total harmonic distortion is given by

$$THD_{Vo} = \frac{\sqrt{\sum_{i=2}^{\infty} {V_{o,h}}^2}}{V_{o,1}}, \tag{15}$$

where fundamental output voltage is defined by

$$V_{o,1} = I_{dc} M_i G_{ac} Z_m, \tag{16}$$

with M_i as the modulation index and

$$Z_m = |\vec{z}_M| = |\vec{x}_{Co}||\vec{z}_L|. \tag{17}$$

On the other hand, output voltage harmonics are defined by the inverter current harmonics that flow through the capacitor. Then

$$V_{o,h} = I_{dc} f_{iac,h} X_{Co}. \tag{18}$$

Hence, Eq. (15) can be written as

$$THD_{Vo} = \frac{\sqrt{\sum_{i=2}^{\infty} {V_{o,h}}^2}}{V_{o,1}} = \frac{X_{Co}\sqrt{\sum_{i=2}^{\infty} \left(\frac{f_{iac,h}}{h}\right)^2}}{Z_m M_i G_{ac}}. \tag{19}$$

Eq. (19) shows that the output voltage THD is a function of the filter reactance, impedance Z_m, and modulation techniques, including the modulation index. Grouping the terms defined by the modulation technique, F_{iac} can be defined as

$$F_{\text{iac}} = \frac{\sqrt{\sum_{i=2}^{\infty}\left(\frac{f_{\text{iac,h}}}{h}\right)^2}}{M_i G_{\text{ac}}}. \tag{20}$$

Considering Eq. (17) on Eq. (15) and solving for C_o, it can be found that

$$C_o = \left(\omega_i{}^2 L_{\text{L}} \pm \omega_i \sqrt{\left(\frac{THD_{Vo}{}^2}{F_{\text{iac}}{}^2}\right)\left((R_{\text{L}})^2 + (\omega_i L_{\text{L}})^2\right) - R_{\text{L}}{}^2}\right)^{-1}, \tag{21}$$

where two solutions for C_o can be computed due to the ± sign in the denominator.

4.2. Capacitive filter design for n_C inverters

The fundamental load voltage is the summation of each capacitor's fundamental voltage (Eq. (9)) and this voltage will not change for $n_C \neq 1$ in order to keep the performance of the array, that is, there is a symmetrical distribution of the load voltage among cell output capacitors. The voltage in each capacitor is the function on the fundamental current injected by the inverter, the load impedance, and the number of inverters connected in series, while the current harmonics generated by the inverters must flow across the capacitive filter of each cell, which will generate voltage harmonics in each capacitor and, therefore, the sum of these voltage harmonics will be in the load voltage. Then, it is possible to write Eq. (15) as

$$THD_{V_{\text{L}}} = \frac{X_{\text{Co}}\sqrt{\sum_{i=2}^{\infty}\left(\sum_{j=1}^{n_{\text{C}}}\frac{f_{\text{iacj,h}}}{h}\right)^2}}{M_i G_{\text{ac}}\sum_{j=1}^{n_{\text{C}}}\frac{Z_{\text{M}}}{n_{\text{C}}}} = \frac{X_{\text{Co}}}{Z_{\text{M}}} F_{i\text{acM}}, \tag{22}$$

where the terms by the modulation technique can be summarized in one term defined by

$$F_{i\text{acM}} = \frac{\sqrt{\sum_{i=2}^{\infty}\left(\sum_{j=1}^{n_{\text{C}}}\frac{f_{\text{iacj,h}}}{h}\right)^2}}{M_i G_{\text{ac}}}. \tag{23}$$

Finally, C_o can be found solving Eqs. (22) and (23) for an RL load as shown in Eq. (24). Then, with n_C inverters in a cascaded device, n_C capacitors are needed, one for each inverter, and they can be computed using

$$C_{\text{o}} = \left(\omega_i{}^2 L_{\text{L}} \pm \omega_i \sqrt{\left(\frac{THD_{Vo}{}^2}{F_{i\text{acM}}{}^2}\right)\left((R_{\text{L}})^2 + (\omega_i L_{\text{L}})^2\right) - R_{\text{L}}{}^2}\right)^{-1}. \tag{24}$$

Due to the series connection of the current-source inverters, it is not possible to sum up the current level and obtain a multilevel current waveform—multilevel current source topologies

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must be connected in a parallel array to sum up currents levels, but it is possible to compensate voltage harmonic among the capacitor voltage. These harmonics are generated by the current harmonic injected by the inverters and are a function of the switching function—see Eq. (22)—therefore, if a multilevel modulation technique is used with the aim of generating current harmonics that are phase shifted, the DC current level in each inverter is the same and all outputs filters have the same capacitor value; some capacitor voltage harmonics will be phase shifted and can be compensated among cells. The amplitude of the voltage harmonic in each cell is a function of the capacitor value—see Eqs. (21) and (24)—so by increasing the capacitor size, the voltage harmonic will be increased and, at the same time, the capacitor voltage rating.

As examples, values of F_{iac} and F_{iacM} are computed for PSC-SPWM using MATLAB and they are presented in **Figure 7**, considering modulation indexes $0.5 \leq M_i \leq 1$ and different carrier frequencies for each case. For $n_C = 2$ and $n_C = 3$, if a multilevel modulation technique is not

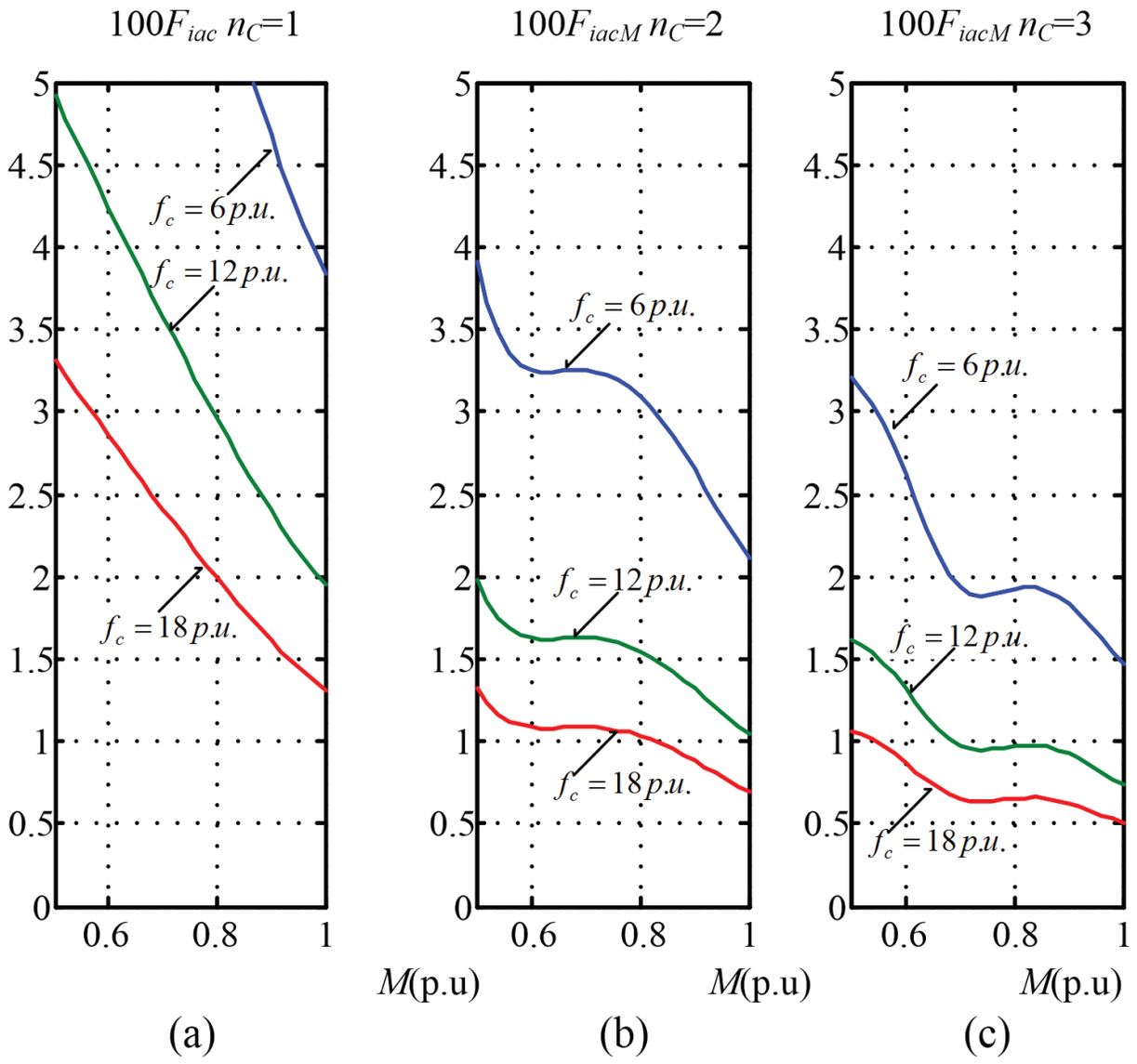

Figure 7. F_{iac} and F_{iacM} as functions of the inverters number and carrier frequency (a) F_{iac} for $n_C = 1$, 3 levels, (b) F_{iacM} for $n_C = 2$, 5 levels, and (c) F_{iacM} for $n_C = 3$, 7 levels.

used, then F_{iacM} is equal to n_C times F_{iac}. For example, a CHB-CSI with a unitary modulation index ($M_i = 1$), three cells per phase ($n_C = 3$), and a 6 p.u. carrier frequency ($F_{iacM} \approx 0.038$) shows $F_{iacM} \approx 0.114$.

5. AC drive application

5.1. Description

An example of the use of the CHB-CSI topology is AC Drive, where the power converter is connected in series to each phase of an electrical AC machine. In this case, a three-phase machine is fed by n_C cells by phase, so the AC drive has $3n_C$ cells as is shown in **Figure 8**. For this example, each cell is fed by a three-phase rectifier based on a current-source rectifier which is connected to the AC grid through a power transformer. This power transformer typically is a multistep transformer in classical CHB-CSI topology but can be simplified when active front ends are used, as in this case. Due to the use of a current-source rectifier, an LC filter is required at the cell input stage.

In the same way, the multicell topology is based on voltage-source inverters; the multicell topology based on current-source inverters is designed to increase the load voltage, which is the sum of the voltage on each cell. Due to the series connection, the current in each cell is the same. Then, the fundamental load current shown in **Figure 8** is given by

$$\vec{i}^{\,j}_{\mathrm{L},1} = \vec{i}_{\mathrm{oj1},1} = \vec{i}_{\mathrm{oj2},1} = \ldots = \vec{i}_{\mathrm{ojn_C},1}. \tag{25}$$

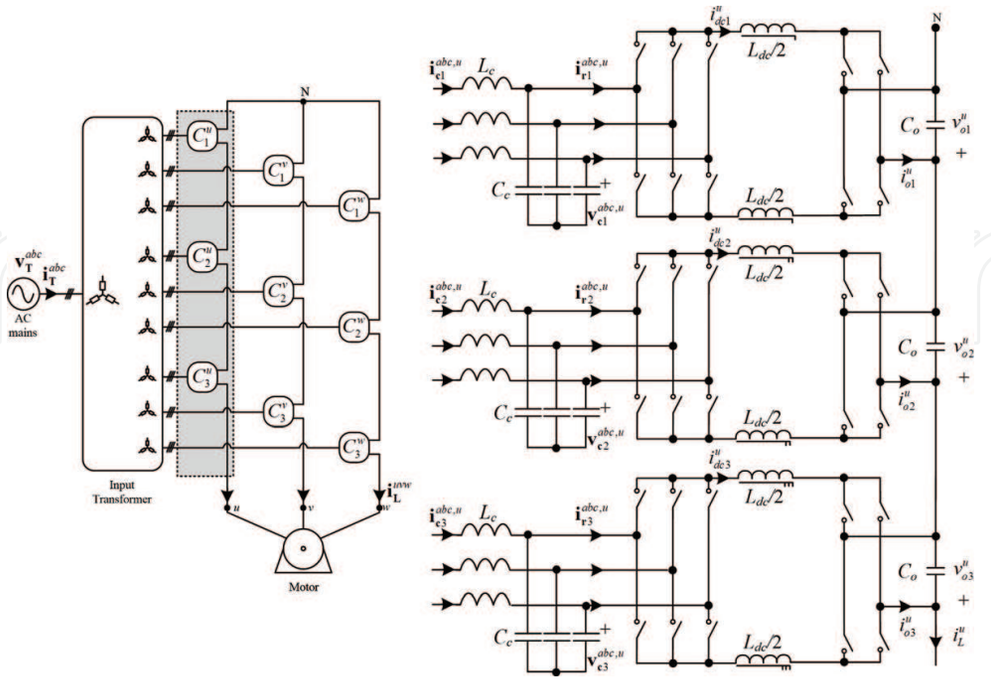

Figure 8. Cascaded H-bridge topology based on current-source inverter in an AC drive application.

The load voltage can be written in terms of the fundamental load current; thus,

$$\vec{v}_{\mathrm{L},1}^{\,j} = \vec{v}_{\mathrm{Nj},1} = \sum_{i=1}^{n_C} \vec{v}_{\mathrm{ji},1} = \vec{i}_{\mathrm{L},1}^{\,j}\,\vec{z}_{\mathrm{L},1}. \tag{26}$$

For the transformer input current, if there is not a phase shift between the primary and the secondary, one can write

$$\mathbf{i}_{\mathbf{T}}^{abc} = \frac{1}{n_T} \sum_{\substack{i=1 \\ j=u,v,w}}^{n_C} i_{\mathrm{cji}}^{\mathrm{abc}}, \tag{27}$$

and the cell input voltage is defined as

$$\mathbf{v}_{\mathbf{sji}}^{\mathrm{abc}} = \frac{1}{n_{\mathrm{T}}} \mathbf{v}_{\mathbf{T}}^{\mathrm{abc}}. \tag{28}$$

Every cell is built up by a current source active front end which feeds a single-phase inverter through the DC link inductor. In order to obtain several controlled voltage sources connected in series array to the load, single-phase inverters and their respective capacitors are connected in series, achieving with this that each inverter-capacitor set behaves like a voltage source controlled through their DC currents. Then, each cell, as is shown in **Figure 9**, can be modeled in *dq* axis; thus

$$\mathbf{v}_{\mathbf{r}}^{dq} = L_{\mathrm{C}} \left[\dot{\mathbf{i}}_{\mathbf{r}}^{dq} + \mathbf{W} \mathbf{i}_{\mathbf{r}}^{dq} \right] + \mathbf{v}_{\mathbf{C}}^{dq}, \tag{29}$$

$$\mathbf{i}_{\mathbf{r}}^{dq} = C_{\mathrm{C}} \left[\dot{\mathbf{v}}_{\mathbf{C}}^{dq} + \mathbf{W} \mathbf{v}_{\mathbf{C}}^{dq} \right] \mathbf{v}_{\mathbf{C}}^{dq} + G_r \mathbf{m}_{\mathbf{r}}^{dq} i_{\mathrm{dc}}, \tag{30}$$

$$\left[G_{\mathrm{r}} \mathbf{m}_{\mathbf{r}}^{dq} \right]^{\mathrm{T}} \mathbf{v}_{\mathbf{C}}^{dq} = L_{\mathrm{dc}} \dot{i}_{\mathrm{dc}} + s_{\mathrm{i}} i_{\mathrm{dc}}, \tag{31}$$

$$v_{\mathrm{o}} = R_{\mathrm{l}} i_{\mathrm{o}} + L_{\mathrm{s}} \frac{d}{dt} i_{\mathrm{o}}, \tag{32}$$

where

$$\mathbf{W} = \begin{bmatrix} 0 & -2\pi f_{\mathrm{r}} \\ 2\pi f_{\mathrm{r}} & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\omega_{\mathrm{r}} \\ \omega_{\mathrm{r}} & 0 \end{bmatrix}, \tag{33}$$

with f_{r} as the network frequency. Using the *dq* model, it is possible to define a control strategy for the rectifier stage. A control scheme must ensure the regulation of the DC current level in each cell (see **Figure 10**), allowing the use of a fixed modulation pattern in the inverter stage. The control scheme controls the active and reactive power using the currents at the input of the cell. An active power controller is used to control the DC current and, through the DC current, the cell output voltage, using the DC component of the output power of the cell. A reactive power controller can be used to compensate the reactive power of the LC filter. The control is

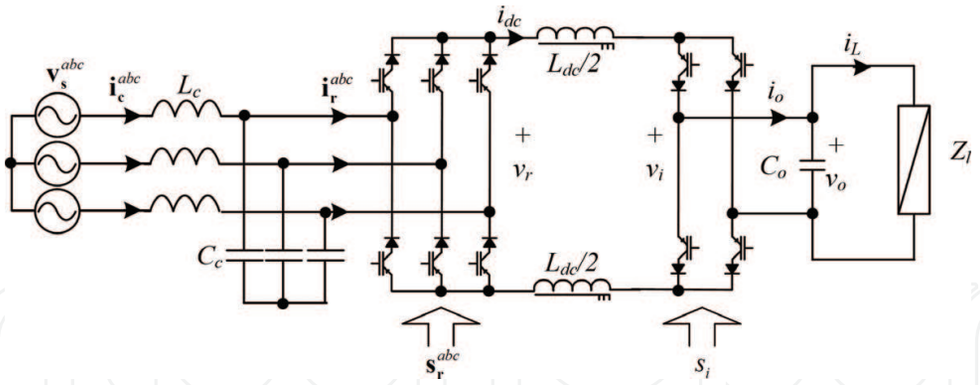

Figure 9. A power cell with an active front end stage.

replicated in each cell and the references of the output voltage, frequency, and cell reactive power are common to those controllers.

On the other hand, *dq* model allows to calculate the operation region of the topology and defines the active power P_{MC}, reactive power Q_{MC} and load voltage in terms of the number of cells n_C, the LC filter, the modulation at the rectifier stage, and the transformer voltage and its ratio; so

$$P_{MC} = V_T^d I_T^d = 3n_C \underbrace{\frac{V_T^{d2}}{n_T} \frac{K_{dc} M_r^d}{\left(1 - \omega_r{}^2/\omega_{LC}{}^2\right)^2}}_{P_C} \approx P_{Load}, \tag{34}$$

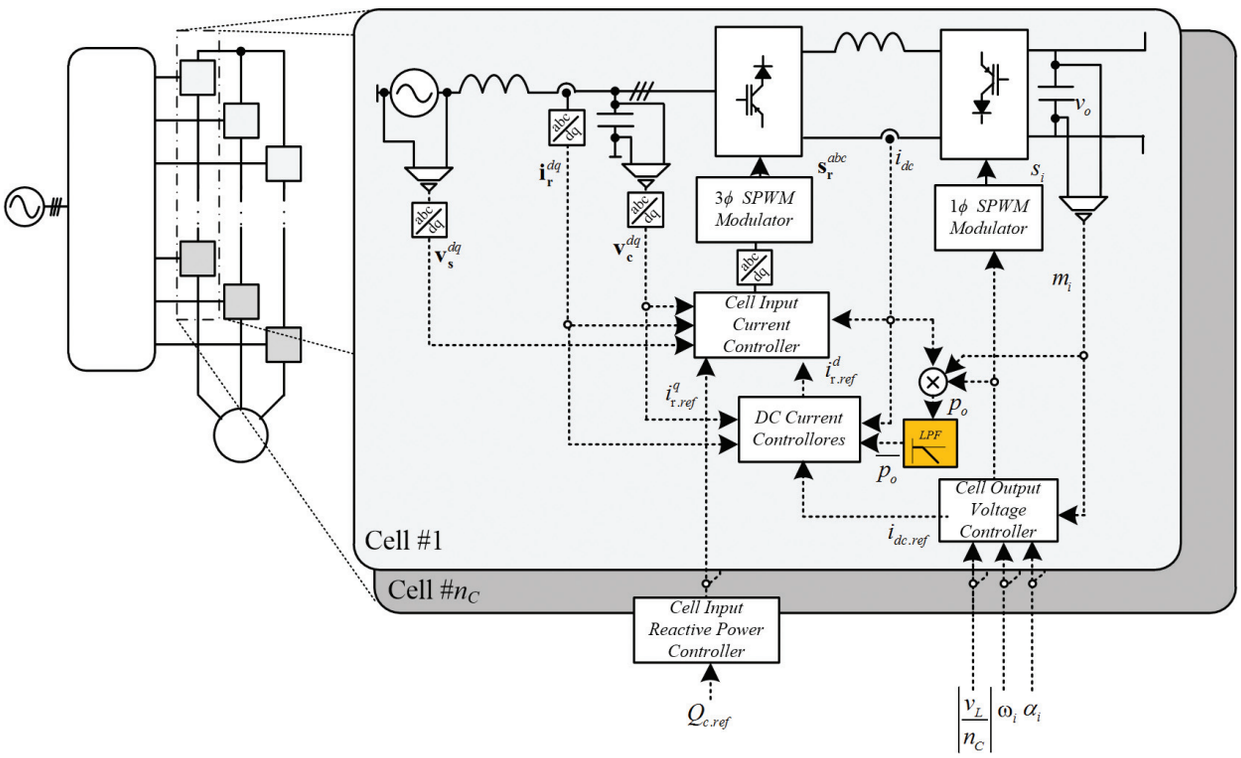

Figure 10. A control scheme for an AC drive based on CHB-CSI.

$$Q_{MC} = V_T^q I_T^d = 3n_C \underbrace{\frac{V_T^{d^2}}{n_T}\left[\frac{\frac{{G_r}^2}{R_{dc}+R_i(\omega_i)}M_r^d M_r^q}{\left(1-{\omega_r}^2/{\omega_{LC}}^2\right)^2}+\frac{\omega_r C_c}{1-{\omega_r}^2/{\omega_{LC}}^2}\right]}_{Q_C}, \tag{35}$$

where P_c and Q_c are the active power and reactive power in each power cell, G_r is the gain of the modulation technique for the fundamental component, R_{dc} can be used to simulate the losses on the cell, and ω_{LC} is the resonance of the LC input filter given by

$$\omega_{LC} = \frac{1}{\sqrt{L_C C_C}}. \tag{36}$$

While the load voltage can be defined as

$$V_L(\omega_i) = n_C \frac{V_T^d}{n_T}\frac{M_r^d Z_m(\omega_i)\left(\frac{{G_r}^2}{R_{dc}+R_i(\omega_i)}\right)}{4G_r\left(1-{\omega_r}^2/{\omega_{LC}}^2\right)}, \tag{37}$$

and $R_i(\omega_i)$ is defined by

$$R_i(\omega_i) = \frac{1}{2n_C} Z_m(\omega_i){M_i}^2 cos\left(\phi_m(\omega_i)\right). \tag{38}$$

from Eqs. (34) and (35), it is possible to notice that for a required active power on the load ($P_{MC} = P_{Load}$ only if $R_{dc} = 0$), it can be divided into $3n_C$ cells, and the same for the load voltage can be divided into n_C cells. On the other hand, from Eq. (36), it is possible to notice that the cell input voltage (i.e., the voltage at the secondary transformer) can be reduced when the cell number, n_C, is increased.

5.2. Examples

In order to show the performance of the CHB-CSI topology, an AC Drive is simulated using PSIM with the parameters shown in **Table 2**, considering a 9.33 MVA load per phase and a 0.8 inductive power factor, using one cell per phase (n_C= 1) and two cells per phase (n_C= 2).

Figure 11 shows the operating region for n_C= 1 and n_C= 2 as functions of the DC current level, including active and reactive power per cell (**Figure 11a**) and load voltage and inverter voltage per cell (**Figure 11b**), where the RMS cell input voltage for $n_C = 1$ is equal to 4 kV and, in order to get the same load voltage level, for n_C= 2, the RMS cell input voltage is reduced to 2 kV—reducing the semiconductor voltage rating with respect to $n_C = 1$).

In terms of steady-state performance, **Figure 12** shows the key waveform $n_C = 1$ and $n_C = 2$ using a DC current level equal to 500 A per cell (**Figure 12a**) and a load frequency equal to 50

Parameter		Value		Value p.u.
Load	R_l	20	Ω	0.804
	L_l	47	mH	0.593
Voltage at the transformer primary	V_{Trms}	8	kV	
Transformer ratio for $n_C = 1$	nT	2		
Transformer ratio for $n_C = 2$	nT	4		
Lc Filter at the cell input	L_c	12	mH	0.15
	C_c	40	μF	3.2
DC inductor	L_{dc}	15·36	mH	6.82
Output capacitor	C_o	20	μF	6.4
Switching frequency for rectifier stage		750	Hz	15
Switching frequency for inverter stage		500	Hz	10

Table 2. AC drive parameters.

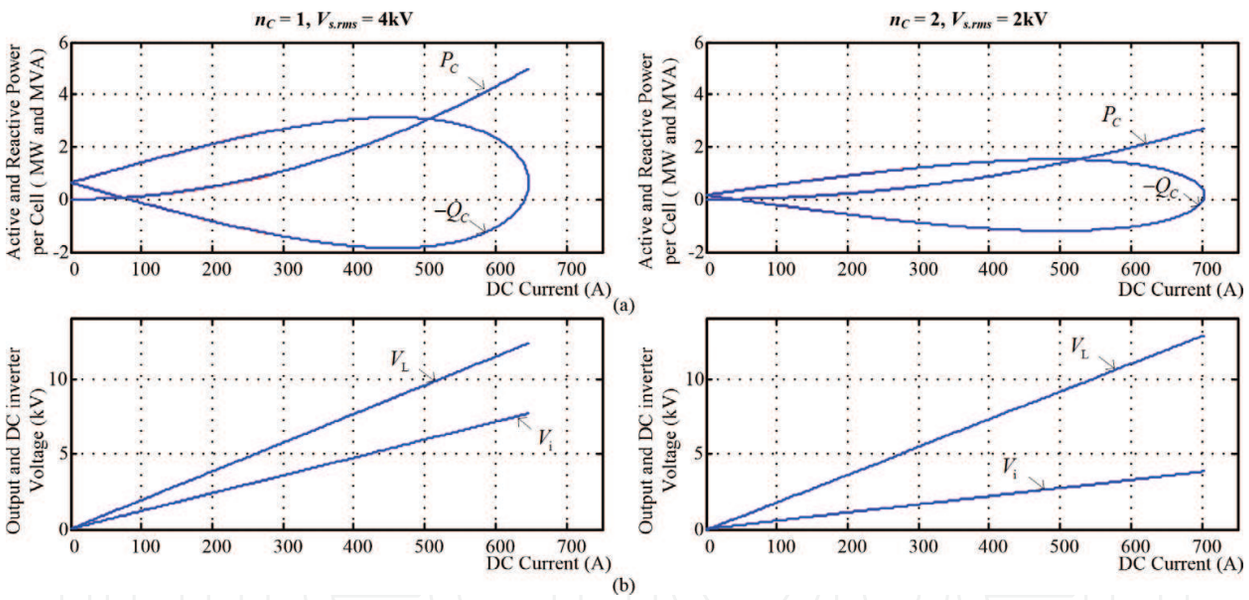

Figure 11. Operation region for $n_C = 1$ and $n_C = 2$ (a) input active and reactive power, per cell and (b) load voltage and inverter output voltage.

Hz. For this case, unitary displacement power factor at the input of the power converter has been set in order to get input current in phase with the input voltage. It is possible to notice that, for the same DC inductor parameters, the ripple by the oscillating power is lesser in $n_C = 2$ than in $n_C = 1$—near to 50% less, while in both cases, the average value of the DC current is 500 A. About the load voltage, **Figure 12b** shows that both cases reach similar voltage levels, but the harmonic distortion in $n_C = 2$ is lesser than $n_C = 1$ because of the use of a multilevel modulation technique. About the quality in the input of the cell and the input of the power

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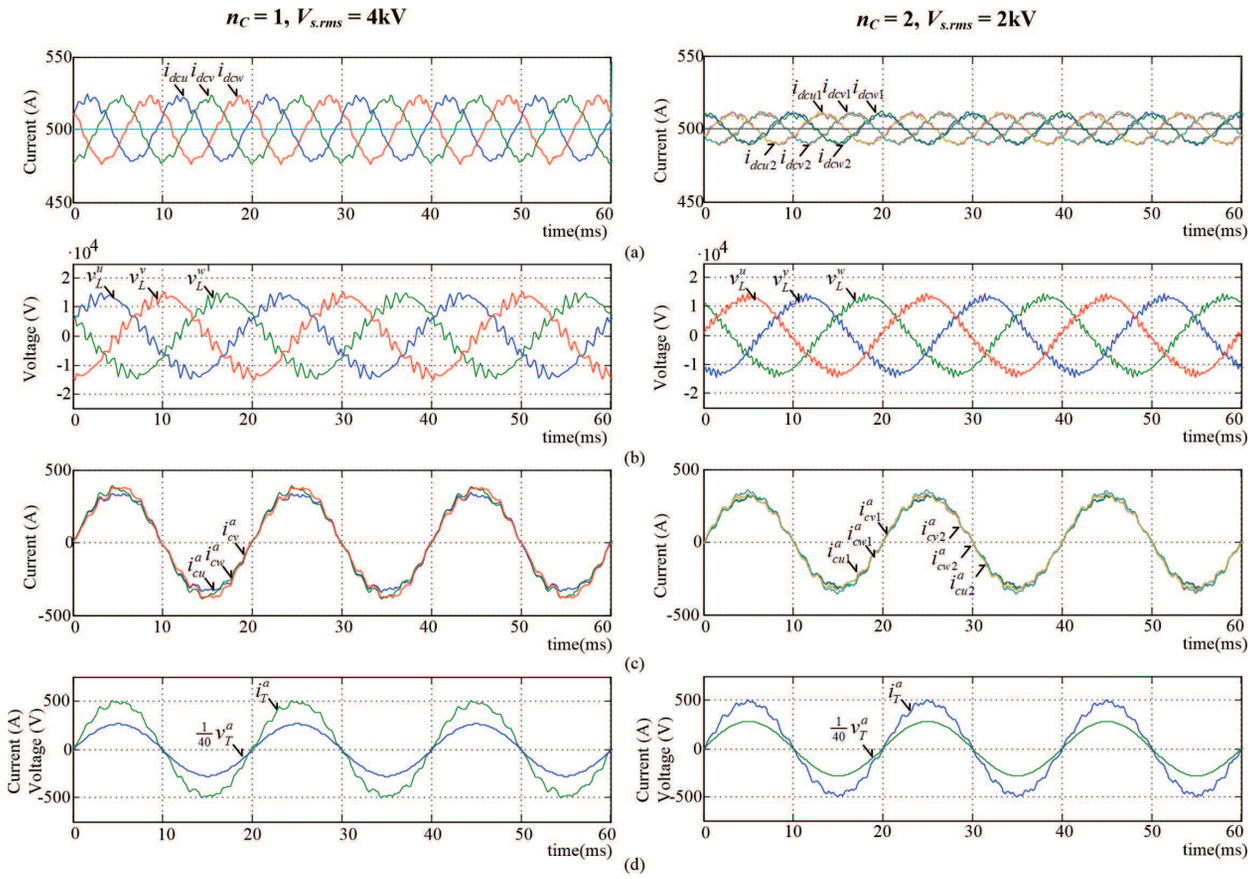

Figure 12. Steady state key waveform for $n_C = 1$ and $n_C = 2$ (a) DC current in the cells, (b)load voltage, (c)cell input currents, and (d) transformer input current and transformer primary voltage.

transformer, **Figure 12c** and **d** shows voltage and current for both cases, where one can see the low distortion in the input current—typically in current-source rectifier topologies.

Figure 13 shows the frequency spectra for the DC current (**Figure 13a**), load voltage (**Figure 13b**), and cell input current (**Figure 13c**). From the DC current frequency spectra, a second harmonic can be noticed due to the oscillating power drained by the single-phase inverter limited by the DC inductor design. This component is lesser in the $n_C = 2$ than $n_C = 1$, but the effect in the load voltage—third harmonic—is similar. Finally, at the cell input current, there is a third harmonic caused by the second harmonic in the DC current. This harmonic does not exist at the transformer input current because it is compensated among cells that feed different phases of the load.

Finally, for $n_C = 1$ and $n_C = 2$, the performance under load frequency changes and DC current level change has been tested (**Figures 14** and **15**, respectively). For these tests, a non-linear control has been implemented in order to control the load voltage using the DC current level, which is controlled by the rectifier stage. In the first case, under frequency changes from 20 to 70 Hz (**Figure 14b**), the power topology is able to impose it on the load. For lower frequencies, the amplitude of the second harmonic in the DC current increases because the DC inductor has been designed to limit it at 50 Hz (**Figure 14a**) and decreases for higher frequencies. On the

other hand, at the input current (**Figure 14c**), it is possible to notice the effect of the second harmonic in the DC current. This oscillation is not presented in the current at the primary transformer because of the compensation of these components among cells that feed different load phases.

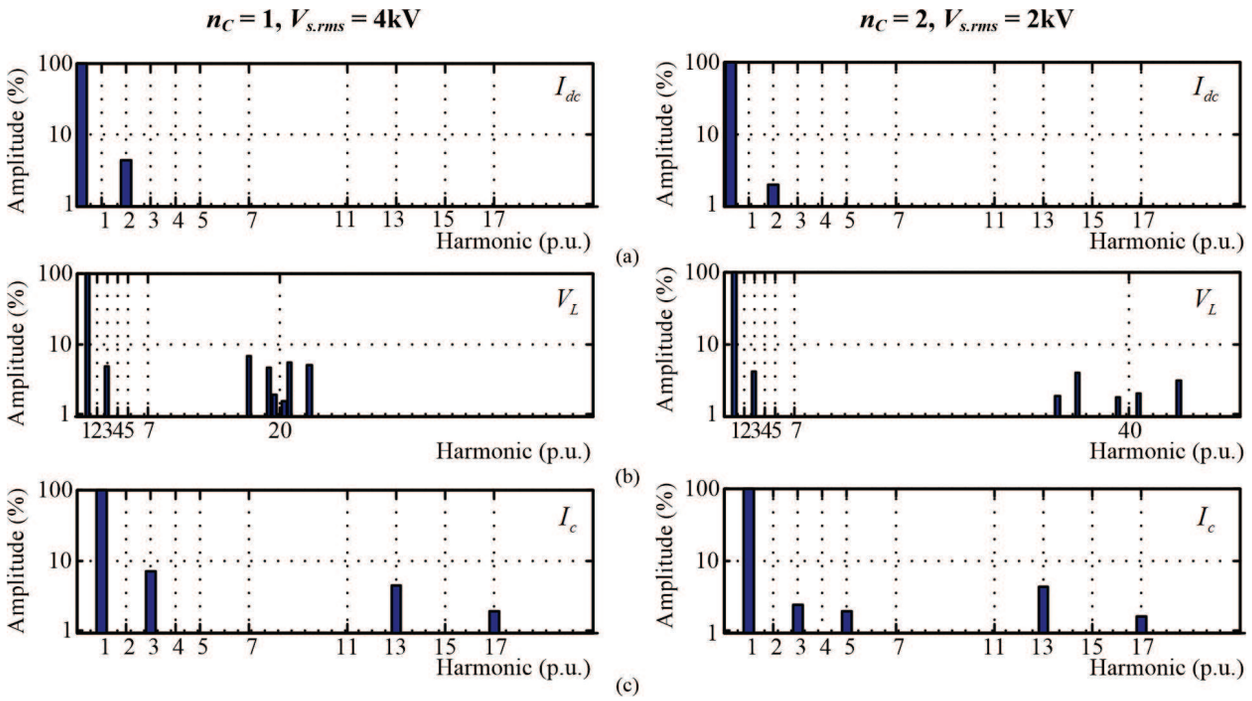

Figure 13. Frequency spectra for $n_C = 1$ and $n_C = 2$ (a) DC current, (b) load voltage, and (c) cell input current.

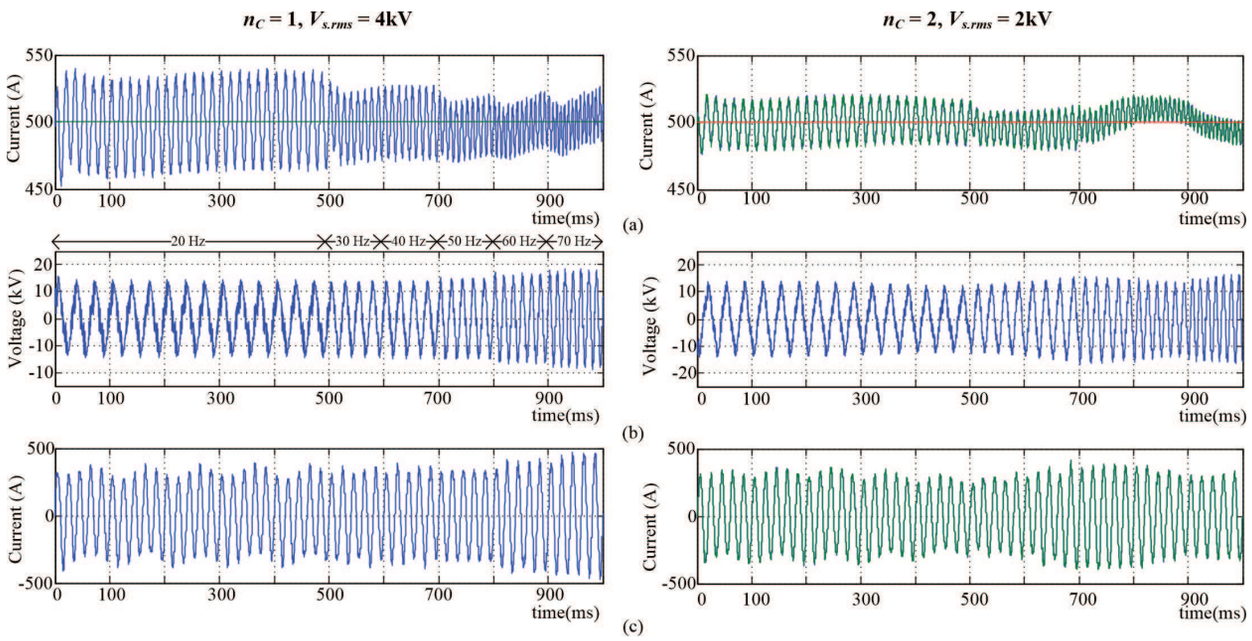

Figure 14. Response for load voltage frequency changes (a) DC current, (b) load voltage, and (c) cell input current.

About the DC current step change, **Figure 15a** shows a 10% step in t = 100 ms. In both cases, it can be notice that the load voltage increases by 10% (**Figure 15b**), while the input current increases in the same rate due the increases in the load power (**Figure 15c**). In this case, the dynamic is defined by the controller parameters and can be specified in the controller design process.

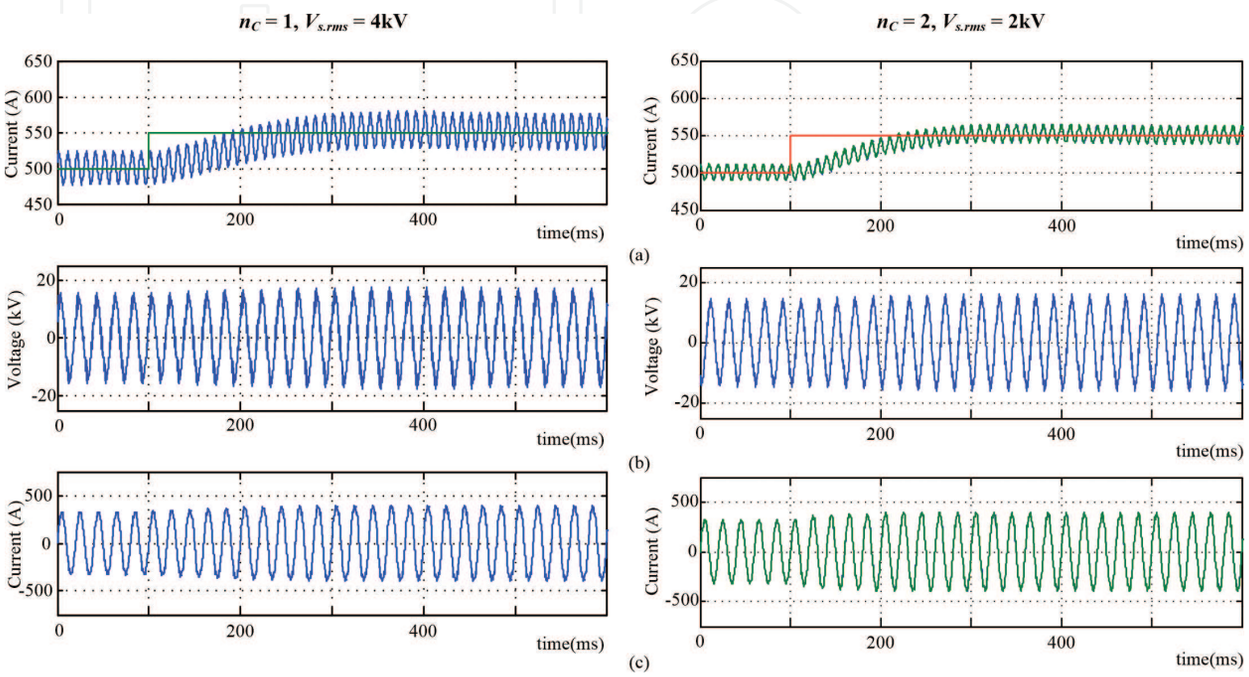

Figure 15. Key waveform for 10% DC current step (a) DC current, (b) load voltage, and (c) cell input current.

6. Conclusions

Cascaded H-bridge topologies based on CHB-CSI are emerging topologies that use the same principle of a cascaded H-bridge converter, allowing to divide the required load voltage level and power into several single-phase inverters connected in series. Advantages of the proposed topology are (i) high quality of voltage and current waveforms using lower switching frequencies and (ii) inherent short-circuit protection because of the use of current-source inverter, while its main drawbacks are (i) the use of a bulky DC inductor because of the use of current-source inverters and (ii) the oscillating power drained by the inverter on the DC side, because the use of single-phase inverters. With an appropriate control scheme, the CHB-CSI is able to impose a desire frequency and load voltage level. In case of AC drive applications, an increase in the number of cells allows reducing the voltage rating of the components without reducing the operation region of the whole converter. At the same time, the DC current variation in each cell decreases when the number of cells increases. On the other hand, load voltage can be regulated through the DC current control, allowing the use of a fixed modulation index for the inverter stage. The above allows designing the capacitive filter with the minimum F_{iacM} required for a given modulation technique and switching frequency.

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Nomenclature

n_C	Number of cells in a series array
Z_L	Load impedance
s_i	Modulation function of the inverter
v_o	Cell output voltage
$\mathbf{v_l}$	Load voltage
i_o	Cell output current
$\mathbf{i_L}$	Load current
i_{dc}	DC current
s_o	Cell apparent output power
$\mathbf{v_s}$	Cell voltage supply
$\mathbf{i_c}$	Cell input current
$\mathbf{s_r}$	Modulating vector of the rectifier
$\mathbf{i_c}$	Cell input current
abc	Stationary coordinates for three-phase input
uvw	Stationary coordinates for three-phase output
dq	Rotating coordinates

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