Chapter 9

Silicon Growth Technologies for PV Applications

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Additional information is available at the end of the chapter

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Abstract

Crystalline silicon is the most used semiconductor material for solar cell applications accounting for more than 90% of the market share. Nowadays, multicrystalline and monocrystalline silicon are mainly produced from directional solidification and Czochralski method, respectively. Solar cells made of these two types of material have shown efficiencies below the theoretical limit due to the presence of impurities in the silicon feedstock, challenges during the solidification process and issues in the different solar cell flowchart steps. This book chapter focuses on the solidification of the silicon photovoltaic value chain and corresponding growth technologies. A detailed description of the directional solidification and Czochralski method apparatus is initially presented. The several types of defects generated during the solidification as well as the source of impurities incorporation into the ingots are described in detail. Among different defects, dislocations and grain boundaries are presented for directional solidification and voids and oxygen-related defects for the Czochralski method. At the end, alternative methods to grow silicon substrates from both liquid and gaseous phase at lower cost and moderate qualities compared to standard processes are presented. These methods are still not considered to be cost-effective compared to more traditional ones due to the higher defect density.

Keywords: silicon, growth, monocrystalline, multicrystalline, Czochralski method, directional solidification, ribbons, impurities, defects, solar cells

1. Introduction

Crystalline silicon has been the dominant semiconductor material used in the fabrication of solar cells with a market share of over 90%. Silicon is abundant in earth crust and presents unique physical and chemical properties. Associated with the strong technological developments of its purification and solidification as well as advanced solar cell concepts, silicon is an interesting candidate to remain the foremost photoactive substrate for photovoltaic (PV)

applications over the next decades. In 2016, multicrystalline silicon and monocrystalline silicon solar cells have reached maximum efficiencies of 21.3 and 25%, respectively [1]. These values are still far from the theoretical efficiency limit of about 31% for homojunction solar cells. It gives rise to the fact that optimization of the first steps of the PV value chain is needed. **Figure 1** shows the flowchart of the PV value chain where it can be divided into six main categories, from silicon feedstock to the final system installed outdoors. In order to obtain a silicon ingot from the feedstock, several growth processes can be used, namely Czochralski process for monocrystalline silicon (Cz-Si) and directional solidification for multicrystalline silicon (mc-Si). The silicon feedstock is initially molten at 1414°C in a crucible and subsequently solidified according to the corresponding method. The solidification step determines the quality of the ingot, where both impurities can be incorporated and defects generated and will impact the solar cell performance. Therefore, this step of the silicon PV value chain is of high importance to the cost effectiveness of the technology and needs to be carefully studied and optimized.

The production of mc-Si solar cells dominates the market share, as mc-Si technologies accounted over 60% of all module produced in 2014 [2]. Mc-Si materials are mainly formed by directional solidification, achieved in Bridgman or vertical gradient freeze (VGF) type of furnaces. The material produced in this way is relatively cheaper than monocrystalline silicon. It has, however, much higher densities of crystalline defects compared to singe crystals, and consequently, lower energy conversion efficiencies are obtained. Mc-Si ingots contain a variety of impurities, in dissolved and precipitated form. Some of them are intentionally added to the melt (dopants) to increase and control the conductivity of the silicon material. N- and p-type ingots are usually doped with phosphorus and boron, respectively. Other impurities are unintentionally incorporated into the crystal and drastically affect the material electrical properties. These are referred as contaminants and originate from the silicon feedstock, the crucible and coating, and the furnace environment. Among them, metallic impurities (e.g., iron and chromium) and light elements (e.g., carbon) are usually found.

In 2014, Cz-Si market share was well below the mc-Si one, accounting for approximately 34% [2]. It is, however, expected that this technology will have a significant increase over the next years due to expected improvements and enhanced productivity. Although with lower amount of defects compared to mc-Si solar cells, Cz-Si is still facing important challenges with the incorporation of impurities and their interaction with defects. The main source of unintentionally added impurities is the crucible and feedstock. The silica crucible dissolves during the process feedstock melting and subsequent steps of the process. Oxygen is released into the melt and transported toward the solid-liquid interface, which together with point defects generated at the interface, form oxygen-related defects. These are nowadays the type of defects that have the most detrimental impact on solar cell efficiency [3]. Carbon is normally found in much lower amounts compared to oxygen, but still with high contribution to the efficiency degradation even at low concentrations.

These processes waste very high amounts of material during sawing with important impact on the final module cost. Wires with nearly the same thickness of the desired wafer thickness are used, and thus, a large amount of material is wasted (commonly referred as kerf losses). A possible solution will be to develop low cost techniques by using lower energy budgets compared to standard processes and avoid the wafering step. At the same time, a reasonable

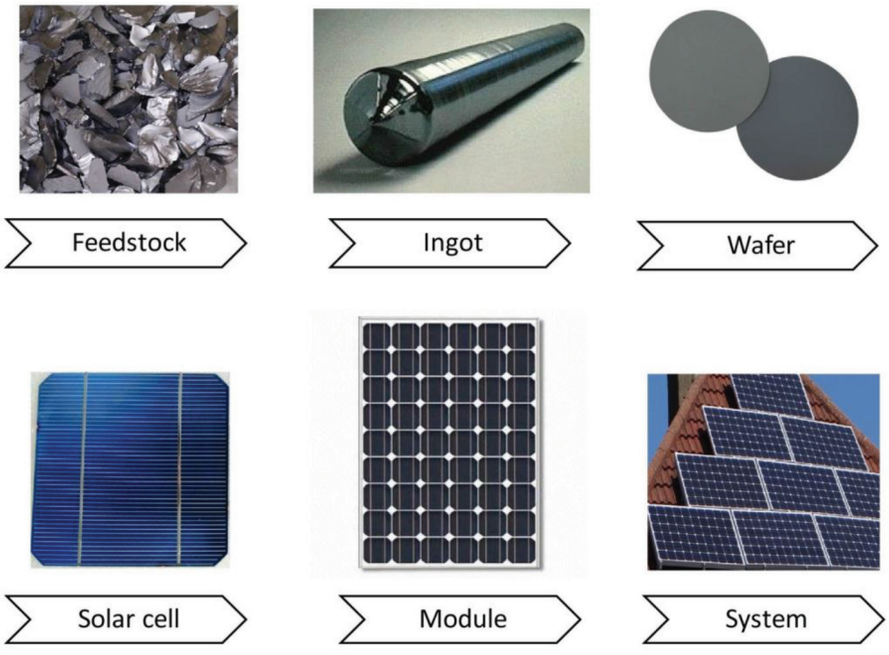

Figure 1. Flowchart of the silicon PV value chain.

performance of these materials is expected in order for the technique to become cost effective. Alternative techniques that short-circuit the ingot and wafering step have been developed and used to produce thin films and ribbons [4].

Next section describes the apparatus of standard processes for the production of silicon for solar cells, namely directional solidification for mc-Si and Cz method for monocrystalline silicon. The main impurities and their incorporation mechanisms as well as the most common defects found in both type of materials are described. In addition, alternative methods to produce and grow Si substrate materials from both liquid and gaseous phase feedstock are presented.

2. Growth techniques

2.1. Directional solidification

2.1.1. Process details

Silicon feedstock is placed in silicon nitride coated silica crucible. The coating layer prevents the silicon to stick to the crucible wall. Sticking points generate stresses in the ingot leading to plastic deformation and therefore to the development of crystalline defects such as dislocations. It also increases the level of oxygen contamination. The silicon nitride coating is applied to the inner walls by spraying a water-based slurry. It is then dried and oxidized by firing at 1100°C. This oxidation step is necessary to avoid the silicon melt to wet the coating layer. The silica crucible is a consumable as it cracks during the cooling of the ingot.

The feedstock is then melted in a controlled argon atmosphere. A near vertical temperature gradient is established in the hot zone, and directional solidification occurs from bottom to top.

The temperature ramp-down is achieved while maintaining a relatively high vertical temperature gradient of approximately 500–1000 K/m in order to (1) keep a near-planar solidification interface and (2) obtain good mixing conditions in the melt. The importance of point (2) will be developed in Section 3. Cooling can technically be performed either by:

- Controlled heat extraction from the bottom of a crucible. In such a case, the crucible is immobile and the process is often referred to as "Bridgman."
- Downward movement of the crucible through the vertical temperature gradient. The process is then often referred to as vertical gradient freeze (VGF).
- A combination of the two first methods.

The melt surface is flushed with argon during the entire process to remove the oxygen evaporating from the silicon melt. The chosen growth rates are low (typically 1 cm/h) in order to maintain favorable solidification conditions—that is, an effective mixing of the melt, and a near-planar solidification interface. Once the solidification step is over, the ingot is cooled down progressively to limit the development of stresses.

Industrial mc-Si ingots solidified in Bridgman/VGF furnaces have square horizontal cross sections and weigh up to 1 ton. The larger ingots are referred as "G6," as they will later in the solar cell process be cut into 6 × 6 bricks of 120 × 120 mm^2 top surfaces. The trend is toward larger ingot size, which gives a higher yield and lowers the price of the produced material.

2.1.2. Defects in mc-Si ingots

As mentioned in the previous section, mc-Si ingots crystallized by directional solidification methods contain more crystalline imperfections than single-crystalline ingots. Extended defects—as opposed to point defects—constitute the most important category, as they are found in high densities in mc-Si materials and have a considerable impact on solar cell properties. They are also responsible for the occurrence of *internal gettering*, where mobile impurities diffuse in the material and precipitate at defects. This phenomenon occurs when the ingot cools down during the directional solidification process and continues during the high-temperature steps of the solar cell process. Extended defects can be separated in two categories:

- *Surface defects*—that is, mostly *grain boundaries*—correspond to the interfaces separating grains of different crystalline orientations;
- *Line defects*—that is, *dislocations*—correspond to a line in the crystal lattice around which atoms are misaligned;

2.1.2.1. Grain boundaries

Multicrystalline silicon ingots are typically composed of elongated grains extending through its height, with diameters ranging from a few millimeters to a few centimeters. This multicrystalline structure is the result of the initial multiplicity of nucleation points on the silicon nitride coating layer. The grains composing an ingot have different crystalline orientations and

are separated by interfaces referred as *grain boundaries*. Depending on the misorientation between the grains, the boundaries can have different degrees of coherency and consequently different impacts on the output solar cell performances. A boundary with a higher degree of coherency is generally considered to have a lower impact on the material electrical properties, and a lower ability to internally getter impurities by precipitation. Grain boundaries can be classified into two main categories, according to their misorientation angle and the arrangement of atoms at their interface:

- A specific type of grain boundaries with defined misorientations shows low interfacial energies and high degrees of coherency. These boundaries correspond to particular atom arrangements, where the two adjacent grains share coincident sites. They are referred as *coincident site lattice (CSL) grain boundaries*. A Σ-value defines the degree of fit, corresponding to the reciprocal density of coincident sites. For example, two grains separated by a perfect Σ27 grain boundary share one coincident site each 27 atoms. Σ3 grain boundaries—or *twins*—are a particular case of CSL boundary. They have a very high degree of coherency and an extremely low interfacial energy. Σ3 boundaries are in their majority formed during the growth of the ingot by a phenomenon called *twinning*. CSL boundaries are very common in silicon, in particular Σ3 boundaries. Twins of higher degrees $\Sigma 3^n$—Σ9, Σ27, for example—are also often found in mc-Si materials.
- Any deviation from the ideal coincident site lattice misorientations is accommodated by the introduction of line defects—or *intrinsic dislocations*—in the CSL grain boundary. *Random grain boundaries* are boundaries deviating considerably from the CSL configurations. They consequently have low degrees of coherency and high interfacial energies.

2.1.2.2. Dislocations

One of the main drawbacks of directional solidification when compared to single-crystal solidification methods is the invariable incorporation of numerous dislocations in the ingot. Dislocations are formed during the crystal growth and the cooling of the ingot and are found in densities ranging from 10^4 to 10^8 cm^{-2}. As opposed to grain boundaries, dislocations are mobile in silicon material. This means that once generated, a dislocation will have the ability to migrate and potentially multiply, annihilate or rearrange in energetically favorable structures. They have drastic impacts on the material electrical properties and heavily getter mobile impurities. Research has been conducted in order to limit the development of dislocations in the ingot, and multiplication mechanisms and dislocation interaction processes are necessary for this purpose.

As mentioned in the previous section, a dislocation is a linear defect. A line vector therefore defines each dislocation. A displacement vector—also referred as burgers vector **b**—characterizes in addition the nature of the dislocation. The edge and screw dislocations are special cases where the angle between the line direction and **b** is 90° and 0°, respectively (see **Figure 2**). All other types of dislocations are mixed cases, with both edge and screw components. In silicon, dislocations tend to align along the <1 1 0> dense direction, and the most common Burgers vector is ½ <110> **a**, being **a** the lattice vector.

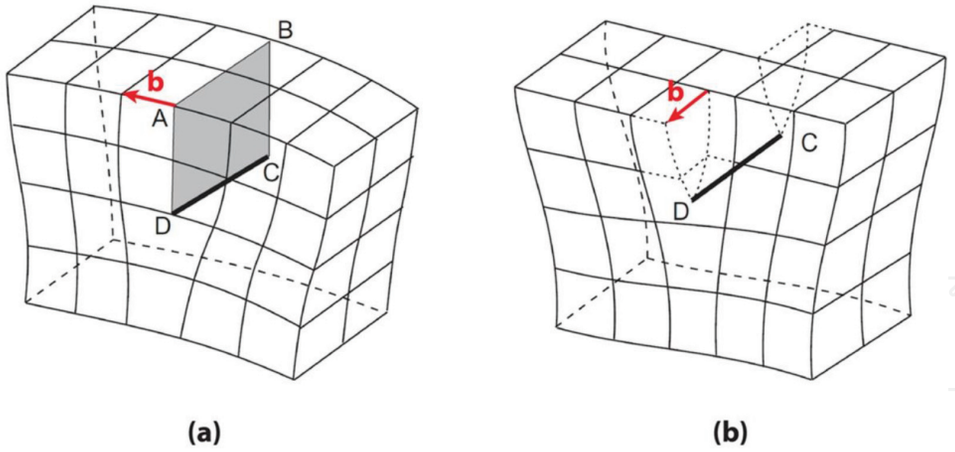

Figure 2. (a) Model of an edge dislocation (line DC), perpendicular to the Burgers vector (b) Model of a screw dislocation (Line DC), parallel to the Burgers vector **b**. Modified from Ref. [5].

In mc-Si, dislocations are mostly generated at grain boundaries, where the energy barrier for plastic deformation and dislocation emission is lowered. Grain boundary topological imperfections particularly trigger dislocation emission, as they act as stress concentrators. Semicoherent grain boundaries—or near-CSL boundaries—have the highest ability to generate dislocations, where incoherent boundaries tend to accommodate for stresses developing in the ingot. Precipitates and inclusions also generate dislocations, mainly on the bottom, sides and top of the ingot. In silicon, dislocations move only at temperatures close to the melting point. When the motion occurs within a surface that contains both the dislocation line and **b**, it is referred as *gliding*. Dislocations glide in the so-called slip planes, and along specific slip directions. In silicon, the most favorable slip planes are the {1 1 1} densely packed planes, and the <1 1 0> dense directions are the slip directions. As each of the four {1 1 1} planes contains three distinct <1 1 0> vectors, 12 slip systems are available for dislocations in silicon. When the motion occurs within a plane that does not contain **b**, it is referred as *climbing*. This mechanism is controlled by the presence of point defects. Multiplication phenomena are responsible for the formation of so-called *dislocation clusters*, containing very high densities of dislocations. The multiplication mechanisms are not yet clear, but it has been demonstrated that clusters are formed during the growth of the crystal. The dislocations generated during the cooling of the ingot are sparser as they do not have the same ability to move in the crystal. Dislocations in silicon tend to rearrange by alignment in arrays perpendicular to the slip planes, by a recovery mechanism called polygonization. A high fraction of the dislocations present in clusters is polygonized. These dislocation arrays form low-energy structures and define low-angle grain boundaries.

2.1.2.3. Structure control

Much effort is currently put on research focusing on techniques to control the structure of the mc-Si ingots solidified by directional solidification. The objective is to produce material with lower densities of extended defect. Two main directions are pursued:

- One of them focuses on obtaining ingots with larger grains, the objective being to eliminate grain boundaries and to approach single crystalline materials. The most common

approach is to control the structure by seeded-growth: monocrystalline seeds are preplaced on the bottom of the crucible and partially melt before solidification. The orientation of the growing crystal is imposed by this mean, and large grains grow from bottom to top. This technology faces several technical challenges, as (1) parasite grains can tend to grow from the side-walls of the crucible, (2) dislocations originating from the seed-joints spread into the crystals, and (3) a domain of bad electrical properties is observed right above the seeds. The recent development has been, however, very successful to hinder these problems, and results on the solar cell level show a great potential;

- The second direction focuses on lowering the average dislocation density. The objective is to obtain a more random structure in order to favor the development of random grain boundaries, less likely to generate dislocations. This random structure is achieved by a better control of the nucleation step, or by seeding, using a bed of silicon particles. Mc-Si solidified using this method is typically composed of smaller grains and contains almost no dislocation cluster. This material shows also great results on the solar cell level and is now widely implemented industrially;

2.1.3. Incorporation of Impurities

2.1.3.1. Contaminants

Although carbon and oxygen can be found in mc-Si ingots in concentrations ranging from 5 to 10 ppma, metallic impurities are the contaminants with the most dramatic effects on the mc-Si electrical properties. Metallic impurities are typically found at ppb levels in the middle of mc-Si ingots, which is often enough to extensively limit the solar cell performances. Dissolved metallic impurities are often mobile in silicon and tend therefore to be internally gettered by precipitation at extended defects. Metallic impurities originate from several sources: The silicon feedstock contains invariably metallic impurities that will be later partially incorporated in the crystal. The feedstock purity is, however, very high, up to 6N for polysilicon. In addition, directional solidification being a very effective purification process (see Section 2.1.3.2), the amount of metallic impurities typically found in mc-Si ingots, cannot be solely attributed to the silicon feedstock. The silica crucible and the silicon nitride coating contain both typically 10–50 ppm of metallic impurities and are therefore important contamination sources. Impurities originating from the crucible/coating are incorporated in the melt during the growth of the crystal, and in the ingot, once solidification is finished. The effect of the solid contamination is visible on vertical ingot cuts when mapping minority carrier lifetime. A region of lower performance—often referred as red zone—is found on the bottom and the sides, close to the crucible. This region extends typically 2–5 cm in the ingot and corresponds to the diffusion of metallic impurities from the crucible/coating, in the solidified ingot (see **Figure 3**).

2.1.3.2. Impurity segregation

The solid solubility of impurities in silicon is higher than their liquid solubility. It implies that foreign elements are segregated at the solid-liquid interface during the silicon solidification. A

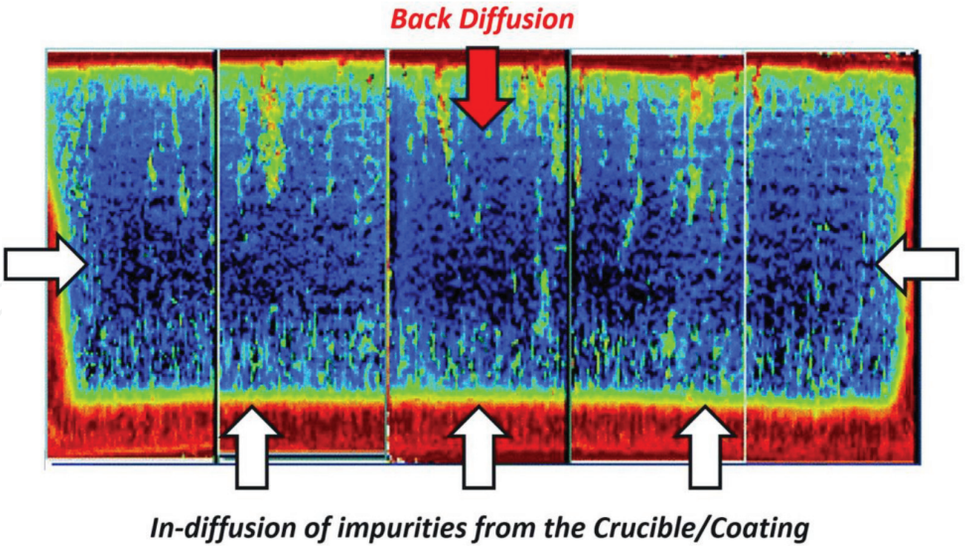

Figure 3. Minority carrier lifetime map of a vertical cross-section of a mc-Si ingot. The region of lower performance appears close to the crucible wall as a result of the in-diffusion of impurities from the crucible and coating. The top part of the ingot is influenced by the back-diffusion of segregated impurities. Modified from [6].

thermodynamic partition ratio k_0 is defined for each element and characterizes its ability to be incorporated in the growing crystal:

$$k_0 = C_s/C_l \tag{1}$$

C_s is the solid solubility and C_l is the liquid solubility. Equilibrium partition ratios of selected impurities are listed in **Table 1**. Metallic elements typically have very low segregation ratio, which makes directional solidification an efficient purification process. Carbon, oxygen and doping elements are less segregated as their equilibrium partition ratios are closer to unity.

Once the solidification is finished, the impurity distribution over the height of the ingot is commonly described by the Scheil-Gulliver equation:

$$C_s = k_0 \times C_0(1 - z/H)^{k_0 - 1} \tag{2}$$

where C_S is the impurity concentration at the vertical position z and H is the total ingot height. Examples of segregation profiles are given in **Figure 4**. The Scheil-Gulliver equation assumes no diffusion in the solid and a homogeneous liquid. In real cases, this last assumption does not hold, as all elements have a limited diffusivity in liquid silicon, and the stirring driven by natural or forced convection cannot lead to a perfectly homogeneous liquid. Impurities rejected in the liquid during solidification have therefore a tendency to build up and form a boundary layer of higher concentration close to the solid-liquid interface. This phenomenon is accounted for by the introduction of a so-called *effective partition ratio k*, where $k > k_0$.

The segregation of impurities with low partition ratios results in higher concentration in the top of the ingot (see **Figure 4**). During the ingot cooling, the impurity will then tend to back-

Element	Equilibrium partition ratio, k_0
Fe	8×10^{-6}
Ti	3.6×10^{-4}
Cr	1.1×10^{-5}
Cu	4×10^{-4}
Ni	8×10^{-6}
B	0.8
P	0.35
O	0.25^{-1}
C	0.07

Table 1. Equilibrium partition ratio of selected impurities in silicon. From Ref. [7].

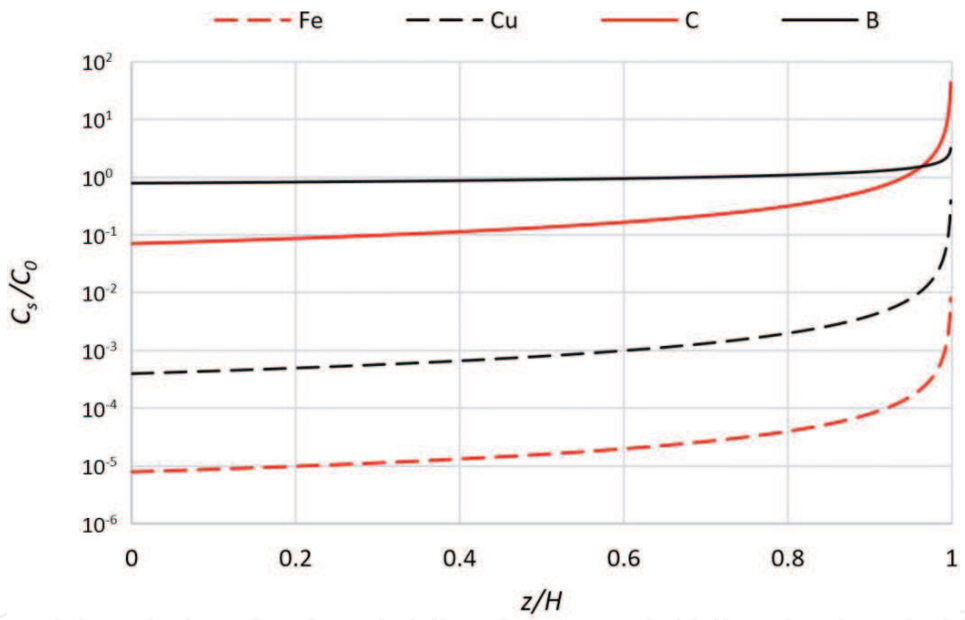

Figure 4. Examples of segregation profiles, as given by the Scheil-Gulliver equation using the equilibrium partition ratio k_0.

diffuse in the material, while it is still warm. This phenomenon is not captured by the Scheil-Gulliver equation due to the "no solid-diffusion assumption," but is visible on minority carrier lifetime maps as it affects the quality of the ingot over distances of several centimeters. The Scheil-Gulliver equation finally assumes that there is no outer-source of impurity—that is, the final concentration profile is the only result of the segregation of impurities initially present in the silicon feedstock. In the case of directional solidification of silicon, this assumption does not hold, as the crucible and the coating are important source of impurities contaminating the melt continually during the ingot solidification. In order to account for the flux of impurities $J_c(t)$

originating from the crucible/coating interior walls, an impurity mass balance in the liquid is made at a given time t during solidification

$$\frac{dC_l}{dt} = \frac{1}{1 - f_s(t)} \left[\frac{A(t)}{V} J_c(t) + (1 - k) R(t) C_l \right] \tag{3}$$

With C_l the concentration in the liquid, $f_c(t)$ the solid fraction, $A(t)$ the lateral area of contact between the liquid and the crucible, V the total silicon volume (solid + liquid), and $R(t)$ the normalized growth rate ($R(t) = \frac{df_s}{dt}$). A modification of Eq. (2) can be then analytically derived from Eq. (3), assuming constant normalized growth rate R and impurity flux J_c from the crucible/coating:

$$C_s = k[C_0 + \beta(z)] \times (1 - z/H)^{k-1} \tag{4}$$

with

$$\beta(z) = \frac{4LH\,J_c}{VR(1-k)} \left[1 + \frac{1}{k-2} \right] [1 - (1 - z/H)^{2-k}] \tag{5}$$

where L is the width of the crucible. $\beta(z)$ is the height-dependent correction index of concentration unit accounting for the contamination from the crucible/coating. An application example of Eq. (4) is given here for the case of iron, using different values of J_c. An initial concentration of iron in the melt of 1.5×10^{13} cm^{-3} is considered. The chosen effective partition coefficient of iron is 2×10^{-5}, the growth rate is 3×10^{-3} cm/s, the crucible width is 70 cm, and the silicon is filled up to 40 cm height. The results are plotted in **Figure 5**.

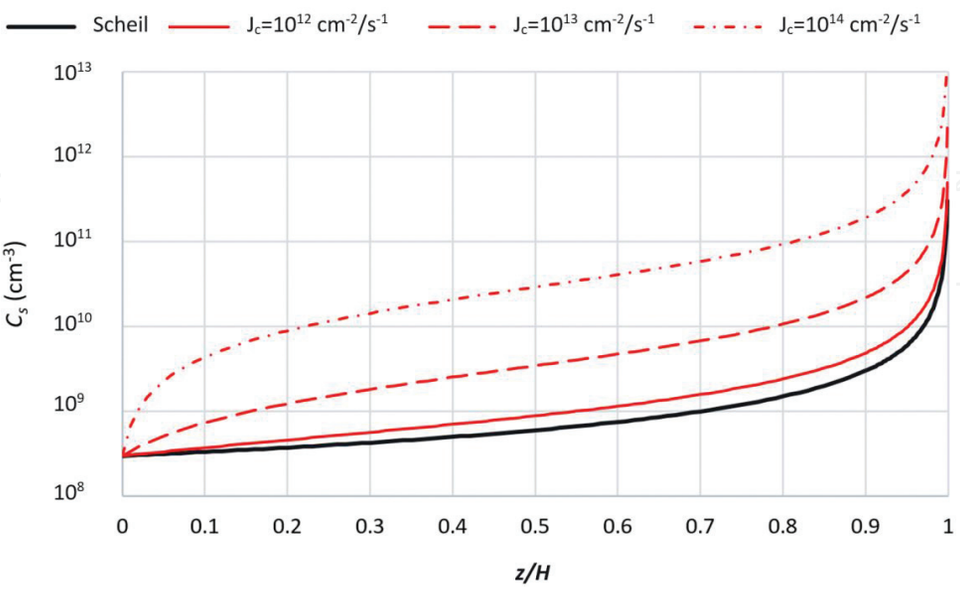

Figure 5. Application example from Eq. (4). Concentration profiles over the height of the ingot are plotted for different values of J_c.

2.2. Czochralski growth

2.2.1. Process details

2.2.1.1. Apparatus

The Cz method apparatus includes several individual components to grown crystals under clean conditions and achieved the solidification of high-quality monocrystalline ingots. The main components are the hot zone, the pulling and rotating systems and the process control system. The hot zone is considered the most important part of the whole apparatus as it determines most of the thermal growth conditions of the crystal. This includes the graphite susceptor, giving mechanical support to the silica crucible, the graphite heater, responsible for providing controlled amounts of heat through the entire process, and the thermal shield, normally used for (1) conditioning the thermal field close to the solid-liquid interface and (2) controlling the gas flow near the melt-gas interface.

The Cz method offers several degrees of freedom. Both crystal and crucible can be rotated and lifted at variable speeds which allow process optimization according to the customer requirements. At the industrial-scale, the process is automated and follows predefined growth conditions. However, the continuous monitoring of process parameters and growth conditions is needed to suppress natural fluctuations of the growth conditions. Among them, the most important is the meniscus inspection by an IR camera. The pulling rate of the seed and the temperature of the heaters are continuously updated according to the feedback received from the monitoring system. The crystal diameter is maintained approximately contestant by this means.

Before the crystal starts to grow, the furnace chambers are evacuated, and inert gas is purged in.

2.2.1.2. Process steps

The growth of a Cz silicon crystal starts with the stacking of high purity polysilicon feedstock in the crucible, where either solar-grade or electronic grade silicon are normally used. The silicon chunks are placed strategically in order to (1) avoid movements during subsequent feedstock melting and (2) minimize the contact between the crucible and the silicon to limit the incorporation of oxygen. The feedstock is then molten by rising the temperature of the heaters above the silicon melting point. The stabilization of the melt is achieved over the next few hours, which is fundamental to obtain a more stable melt temperature and homogeneous solute distribution. A dislocation-free silicon seed of a specific crystallographic orientation (normally <1 0 0>) is finally dipped into the melt, and a meniscus is formed at the seed end. Due to the thermal shock between the melt and the cooler seed, dislocations are generated and need to be eliminated prior full crystal growth. A millimeter-range diameter neck is then grown at high pulling rates, ranging from 2 to 4 mm/min, to promote dislocation diffusion toward the crystal surface and thus stimulate their eradication. It needs to be long enough to ensure dislocation-free growth of the subsequent crystal. The total length of the neck is typically of tens of centimeters. To reach the desired crystal body diameter, two additional steps are needed, that is, crown and shoulder. The crown is grown at constant pull speed, usually lower than the crystal body, while the heater temperature is decreased. It leads to a

constant enlargement of the crystal diameter at a rate depending on both parameters. The shoulder corresponds to a sharp transition at the stage close to the nominal body diameter and is needed to avoid further diameter increase. A sharp increase of the pull speed followed by a decrease of the nominal body pull speed over a short distance will result in a vertical growth of the crystal. The crystal body is finally grown at constant speed, with small adjustment over the entire process in order to adjust for fluctuations of the diameter. The active monitoring system inspecting the meniscus communicates with the controlling system responsible for the regulation of the pulling speed. Nowadays, the crystal body is grown at a nominal pulling rate of approximately 1 mm/min and diameters between 150 and 200 mm for PV applications. The pulling speed and other parameters may vary upon further process optimization. The process ends with the growth of the tail. A gradual decease of the diameter takes place at this stage, and the final part of the ingots presents thus a conical shape. This last step may be optimized in order to have a moderate cooling rate and avoid the formation of high density of oxygen-related defects and thermal stress. Finally, the ingot is brought up to a receiving chamber where it is cooled down to room temperature. A schematic of the different parts of a Cz silicon ingot is shown in **Figure 6**

2.2.2. Incorporation of impurities

In addition to the doping impurities intentionally added to the feedstock, oxygen and carbon are normally found in relatively large amounts in Cz-Si ingots, ranging from 15 to 21 ppma and 0 to 1 ppma, respectively. Nowadays, the control of the oxygen transport in the melt and consequent incorporation into the crystal is one of the main challenges to achieve high-quality crystals. Oxygen originates from the dissolution of the silica crucible, and its incorporation into the melt depends on boundary conditions between crucible and melt, for example, the crucible wall temperature. The dissolved oxygen is transported towards the solid-liquid interface through melt convection. Despite an equilibrium partition ratio close to unity, only a small amount is incorporated into the crystal, that is, less than 1%. Due to the high vapor pressure of oxygen, the majority of the oxygen is indeed evaporated at the melt-free surface, where the evaporation rate depends mostly on the free melt surface area in contact with purging gas. The oxygen transport over large distances and eventually incorporated at Cz crystal depends on an interplay between crucible dissolution rate, melt convection and evaporation at the melt-free surface.

At the industrial scale, Cz ingots are grown in large crucibles, depending on the crystal diameter. To achieve a homogeneous distribution of temperature and impurities in the melt

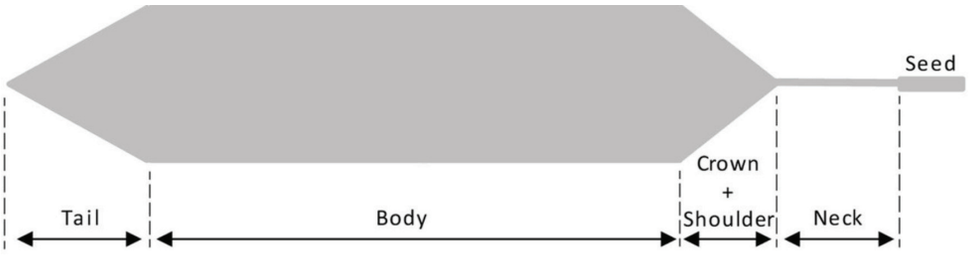

Figure 6. Cross section of a Cz-Si crystal and its different parts after the growth process.

as well as control the solid-liquid interface shape, both crystal and crucible are rotated in opposite directions. It results in forced melt convection which together with other mechanisms such as buoyancy driven flows and Marangoni forces, results in the development of several individual convection cells. Melt convection has also an important role in the solid-liquid interface shape, thermal field in the melt and impurities distribution. Buoyancy driven convection is a result of the temperature gradient between the growing crystal and the heated melt, intentionally created to drive the growth of crystal. Given the nature of the buoyance forces and their strong impact on the melt flow, these can deliver variable amounts of heat and impurities (e.g., oxygen) to the solid-liquid interface. The rotation of the crystal results in liquid areas of variable angular velocities below the solid-liquid interface. The dominant one is the so-called Taylor-Proudman cell and occupies most of the central area below the interface. The centrifugal forces pushing liquid outwards due to crystal rotation compete against the buoyancy flows. The interaction between the two can be controlled by the crystal rotation rate, where higher crystal rotations result on a larger extension of the central force convection cell. The enlargement of this cell may increase the oxygen transport from the crucible walls toward the crystal and govern its axial and radial distribution. Marangoni forces enhance the buoyancy-driven convection. They arise from variations of surface tension along the melt-gas surface, as a result of radial temperature gradients. This leads to the formation of a flow driven from the hot crucible walls to the solid-liquid interface and may influence the crystal growth conditions. Lower oxygen concentration is typically measured at the edge of the crystals in comparison with the center due to the effect of the buoyancy and Marangoni flows.

The evaporated oxygen at the melt surface can react with the graphite parts of the hot-zone and form carbon monoxide (CO) gas. The control of the argon flow in the furnace is then crucial to remove the CO from the furnace and prevent it to dissolve back in the molten silicon, which constitutes the main origin for carbon contamination. Carbon and oxygen contamination are thus closely related. The carbon in the melt is mostly segregated into the crystal after it reaches the solid-liquid interface. Attempts are made to use crucibles made of other material than silica to prevent oxygen incorporation into the melt. In addition to the optimization of the argon flow conditions, alternative materials and coated graphite parts are pathways to minimize carbon contamination of the melt. These new technologies are still facing challenges, and silica and graphite remain the materials of choice for crucibles and crucible holders and heaters, respectively.

2.2.3. Defects in Cz-Si crystals

2.2.3.1. Point defects

During Cz silicon growth, a large amount of native point defects are generated at the interface and are subsequently incorporated in the crystal, the so-called vacancies and self-interstitials. Vacancies correspond to missing atoms in the crystal lattice while self-interstitials to extra ones occupying empty sites in the lattice. Impurity atoms are extrinsic point defects. Substitutional impurities take over silicon atoms, and interstitial ones occupy empty sites in the crystal lattice. Carbon dissolves substantially in the silicon crystal lattice and oxygen interstitially.

The incorporation of native point defects depends on both the growth conditions at the solid-liquid interface and the crystal cooling. The growth rate together with the defects diffusion into the crystal plays a crucial role on the dominant type of point defects and corresponding density near the solid-liquid interface. At lower growth rates, the diffusion of point defects into the crystal dominates, and the crystal becomes interstitial rich due to their higher diffusivity compared to vacancies. Voronkov and his collaborators have successfully described the incorporation of point defects at the solid-liquid interface during Cz silicon growth [8, 9]. Based on the ratio between growth rate (V) and radial thermal gradient (G), it is possible to determine whether vacancies or interstitials are generated in excess. The transition between the two regimes is defined by the critical V/G ratio, and values ranging from 0.12 and 0.2 mm^2/min K are found in literature [10–12]. Given that G increases toward the crystal edge and assuming that the crystal is grown at a steady-state rate, V/G also changes over the crystal radius, as shown in **Figure 7**(left). Therefore, the density of point defects incorporated at the interface also change accordingly. The critical ratio may also be affected by the presence of impurities at the interface. Species such as oxygen can result in a lower critical value and thus promote the incorporation of vacancies. Nowadays, industrial-scale crystals are grown in the vacancy-rich regime due to the relatively high growth rates and large crystals used to increase their productivity.

2.2.3.2. Voids

Voids correspond to agglomerates of vacancies and, due to their nature, belong to the category of volume-type defects. They are formed due to their agglomeration of vacancies during crystal cooling at the temperature range of 1150–1000°C [13]. At temperatures close to 1000°C, vacancies preferentially bond with oxygen which results on dramatic reduction of their the size. Void sizes range from 100 to 300 nm and present a twin or triple structure with facets oriented along the {1 1 1} crystallographic orientation [14]. In addition to TEM, voids can be visualized with several other characterization techniques, namely etching methods, where the etch pits designation differs according to the used method. Secco etching can be used to delineate voids that show up as D-defects at the tip of a wedge-shaped etch pattern. They can further be visualized with optical techniques. Given their small sizes, the formed patterns are the fingerprint of an existing void and make the void density possible to be determined.

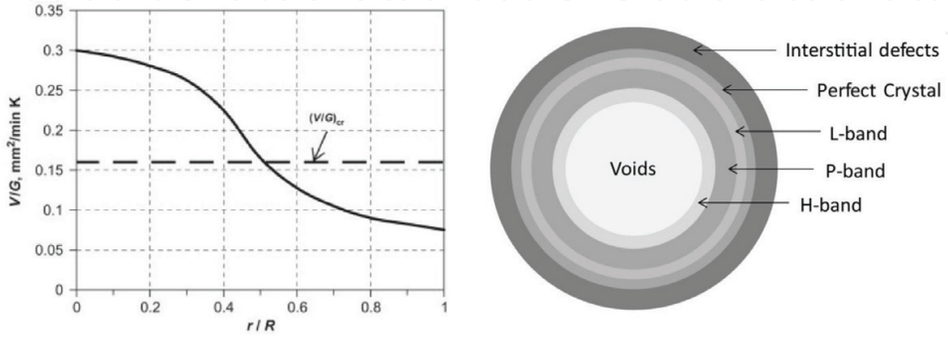

Figure 7. (Left) V/G distribution along the radial direction of a Cz crystal grown under steady-state conditions [8]. (Right) Defect rings distribution for variable V/G along the crystal radial direction, modified from Ref. [16].

Industrial-scale Cz silicon crystals for PV applications tend to be grown at higher growth rates and decreasing oxygen concentrations due to continuous process optimization. Therefore, it is expected to find crystals of higher vacancy concentrations and consequently higher amount of voids in the future.

2.2.3.3. Defect bands

Cz silicon crystals may be grown at different growth rates and dimensions according to the application and pulling conditions. Both the diameter and the growth rate influence the type and amount of defects incorporated, and given that the gradient at the interface changes with the radial position, several types of defects may be found within the same wafer. Defects are distributed as circular bands through the radius according to their nature. This can happen mainly at the top of the ingot, where large variations of the crystal diameter are needed to reach the body width. As such, the *V*/*G* ratio may vary, and all sorts of defects can be generated from interstitials to voids. Due to the lower *G* at the center of the ingot, this ratio is higher at this region, and it is thus more likely to find vacancy-related defects close to the crystal center. Between the two extreme cases and close to the critical *V*/*G* ratio, several bands can be found from interstitial defects to voids regions in the following order: L-band, P-band and H-band. In addition, there is a narrow region between the interstitial region and the L-band, the so-called *perfect crystal*, where interstitial and vacancies are of very low densities, and nucleation of other defects is not promoted. The P-band is found at areas of slightly higher *V*/*G* ratio than the critical one and corresponds to the maximum residual vacancy concentration after the nucleation of voids [15]. Oxide particles are found in densities in the order of 10^8 cm^{-3} and can be visualized as oxygen-induced stacking faults (OiSF) after thermal oxidation and etching. This corresponds to an area of high recombination activity in as-grown crystals and must be avoided. Process optimization is of upmost importance to accommodate this band at the very top of the crystal, for example, in the crown area. A narrow band of smaller particles and higher density compared to the P-band (in the range of 10^{10} cm^{-3}) is formed at the periphery of the last one. It corresponds to the so-called L-band, where only oxide particles can be formed due to the low initial vacancy concentration. On the other hand, particles and voids coexist in the H-band due to the higher initial vacancy concentration compared to the previous two. Due to the higher density of oxide particles, higher recombination activity is found at the L- and H-band compared to P-band after sufficient thermal budget to growth them above a certain size. The different bands that can coexist in a crystal radial cut are schematically shown in **Figure 7**(right)

2.2.3.4. Thermal donors

Interstitial oxygen atoms are not electrically active by themselves, but the same criterion is not applied to their agglomerates. One important class of oxygen related defects is the so-called thermal donors (TD). They are formed during crystal cooling at temperatures close to 450°C [17], and their size and density depend on the cooling rate of the crystal and the interstitial oxygen concentration. Their denomination arises from the fact that they are a source of electrons which results on a direct impact in the electrical properties. Their presence changes the resistivity of the material leading to its reduction in n-type and increases in p-type silicon.

Nevertheless, it leads to an increase of the recombination activity of minority carriers and results on poor material performances. It is possible to completely dissolve TD by applying a rapid thermal annealing for few seconds at 800°C [18]. Other class of TD can be found in Cz silicon that grows at higher temperatures than the previously described. These are formed at temperatures ranging from 650 to 850°C and are mostly developing in silicon with higher concentration of carbon.

2.3. Alternative methods

2.3.1. Liquid phase growth

Ribbon growth processes lead to the fabrication of substrates from the melt directly into a planar one where a crystalline structure suitable for solar cell applications is obtained. The ribbon growth processes can be divided into either vertical or horizontal growth, depending on the crystal pulling direction. The most mature methods of growing ribbons vertically are edge-defined film-fed growth (EFG) and string ribbon (SR), and ribbon growth on a substrate (RGS) for horizontally grown substrates. In the EFG method (see **Figure 8A**), the lower part of the meniscus is formed and shaped by a graphite die, through which an octagonal silicon pipe is directly pulled from the melt at rates approximate to 1.7 cm/min. The pipe is subsequently cut into slices by laser so that it can be processed into solar cells. Due to the use of the graphite die, a high carbon contamination is present in these ribbons [19]. In the SR method, strings are fed through the molten Si to provide edge support for the growing ribbon (**Figure 8B**). It is then used to pull the ribbon from the melt. Si substrates obtained using SR method can be grown at 1–2 cm/min and exhibit low oxygen concentration, but still with high carbon concentrations [20]. The RGS technique (**Figure 8C**) allows the fastest growth rates among these techniques (600 cm/min), and consequently, a high throughput can be achieved [21]. However, it has the main limitation of using a substrate to support the crystal growth. Furthermore, crystals produced with this technique exhibit high carbon concentrations [22], which compromise the solar cells quality.

Another interesting vertical ribbon growth method is the ribbon of a sacrificial template (RST) [23]. This method combines two of the previous concepts; the vertical growth direction is combined with the use of a substrate (**Figure 8D**). It allows faster vertical growth rates, but with the disadvantages of the vertical and horizontal techniques in terms of contamination.

2.3.2. Gaseous phase growth

The substrate material for the solar cell can be grown directly from silane or chlorosilane gases in a low-cost substrate. For such procedure, chemical vapor deposition (CVD) is used for depositing silicon on a substrate at high temperatures. Using a gaseous mixture of H_2 and the precursor SiH_4 or SiH, it is thermally decomposed at the hot surface of the substrate. Si layers of a few microns are deposited on a substrate that is prepared so that the deposited film is releasable onto a carrier substrate [25], as shown in **Figure 9**. Such technique is applied to produce thin films with an amorphous structure, which is a limitation toward the fabrication of high efficiency solar cells.

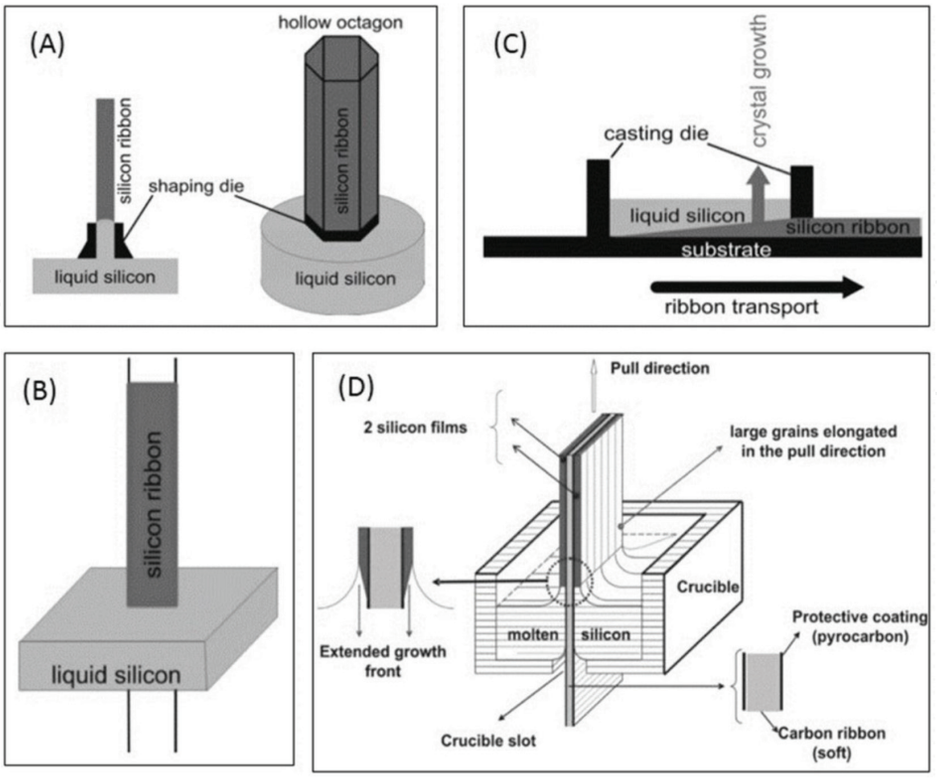

Figure 8. Ribbon growth techniques schematics: (A) edge-defined film fed growth; (B) string ribbon growth; (C) ribbon growth on a substrate; (D) ribbon on a sacrificial template growth schematics. Adapted from Ref. [24].

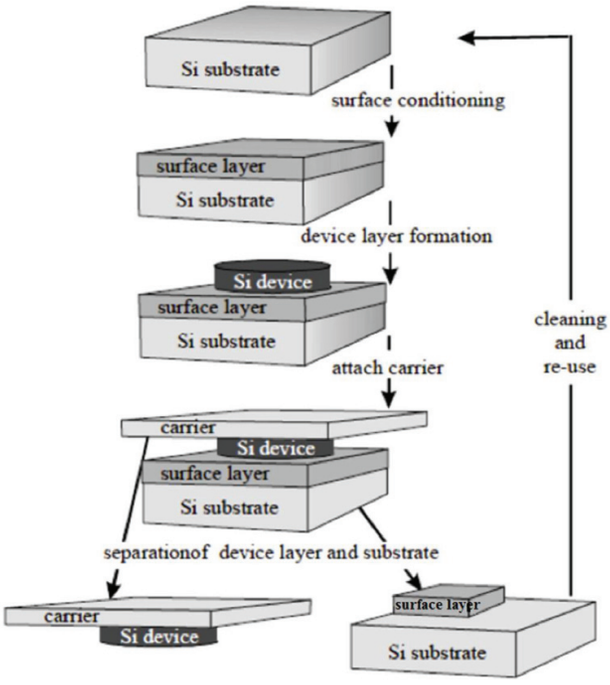

Figure 9. Gas-phase film growth by CVD onto a releasable substrate. Adapted from Ref. [26].

An interesting method to grow silicon ribbons for solar cells directly from a gaseous feedstock is the so-called silicon on dust substrate (SDS) process [27–29]. In this process, a self-supporting silicon sheet is produced directly from a silicon gaseous feedstock by a fast CVD step using gaseous SiH_4. With this method, it is possible to achieve high deposition rate at low temperature (approximately 800°C), and at atmospheric pressure. These characteristics make it a fast deposition process with low energy budget. The SiH_4 is decomposed by the follow pyrolysis reaction,

$$SiH_{4(g)} \rightarrow 2H_{2(g)} + Si_{(s)} \tag{6}$$

The deposition of Si occurs on top of a thin silicon dust layer that is placed on a quartz plate. This deposition process guaranties high homogeneous nucleation rates of silicon nanoparticles of high purity. The resulting film has a nanoporous structure, which after being detached from the dust layer has a thicknesses ranging from 300 to 400 μm. The remaining detached silicon dust acts as a sacrificial layer that can then be reused for a new deposition. The drawback of this method is that the resulting Si sheet is porous Si and of a very low nanocrystalline quality, which makes it unsuitable for solar cell applications. Therefore, the sheet goes through a crystallization process by float zone melting. A localized molten zone is created by a focused radiation in the form of a thin line which goes through the film crystallizing it. After the crystallization step, the resulting sheet has a multicrystalline structure that is suitable to be used as a substrate for solar cells. For this process, a deposition rate of 20 μm/min and constant advance speed of 10 mm/min can be achieved. With low impurity sources, this technique is mainly limited by the high dislocation density, which is produced due to high thermal gradients during crystallization. Recent developments in this technique foresee solar cells of efficiencies of 14%, which is relatively low when compared to standard and more mature processes [30].

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