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Development of Metamaterial EBG Absorbers for Application of Wireless Inter/Intrachip Communication Systems

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Additional information is available at the end of the chapter

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Abstract

First, the chapter presents a novel design of electromagnetic bandgap (EBG) absorber with the characteristics of broad bandwidth, low profile, and polarization-independence to a normal incident electromagnetic wave. The absorber is composed of three consecutive octagon or decagon loops, and highly-resistive frequency selective surface (FSS) layers. Second, based on the feature of the designed absorber unit, a broadband, metamaterial absorber-bounded, wireless inter/intrachip (WIIC) communication channel is constructed at the center frequency of 60 GHz. Third, in order to validate the developed methodology used in WIIC analysis, a wired channel on a conventional PCB has been measured, simulated, and analyzed. Fourth, with the extracted S-parameters of the WIIC system and wired PCB channel, the system impulse responses and transfer functions of the investigated channels have been further extracted, which are used for validation and BER analysis of the WIIC system. Finally, it has been shown that based on the derived BER results, the performance of the designed WIIC channel is close to that of an additive Gaussian white noise (AWGN) channel when the WIIC transceivers are built in with the functionalities of forward error control (FEC), channel estimation, and equalization.

Keywords: metamaterial EBG, wireless inter/intra chip communication, channel design, absorber, bit error rate

1. Introduction

As the dramatic development of high speed integrated circuits and the fast increment of operating frequency of computer systems, the dimensions of complementary metal-oxide

semiconductor (CMOS) transistors have reached at the nanoscale. The very large scale integrated circuits, interconnecting communication channels and devices, and I/O pins have been becoming extremely complex, highly dense, and compact by using multilayer and complicated routing PCB technologies [1]. When the frequency of the computer system operation is greater than 20 GHz or higher, the signal integrity (SI) bottlenecks have been becoming increasingly protuberant, which are particularly resulted in signal reflection, crosstalk, trace loss and delay, parasitic resistance, inductance, and capacitance [2–4].

In order to resolve these serious SI issues, several methods have been recently investigated to improve the interconnection communication systems. For example, using a low-resistivity conductor or a low dielectric constant material, as well as multilayer stacked structures, improves the interconnection communication [5, 6]. Meanwhile, various approaches are used to eliminate traditional trace interconnection issues that have been explored for improving SI systems, including optical interconnects, electromagnetic wave solution, and radio frequency wireless communication technologies [7–11].

This chapter presents an innovative wireless inter/intrachip (WIIC) communication channel, as shown in **Figure 1**, where the major concept of the WIIC communication is illustrated to distinguish the existing high-density trace communication-based PCB and the wireless communication version developed in the chapter.

The rationale and motivation of this research are mainly resulted from the following considerations:

- The WIIC system can greatly reduce the cost of PCB boards as the number of PCB layers is reduced from 10 of layers to less than 5 layers.
- The WIIC system can fully take the advantage of the advanced and well-developed wireless and mobile communication systems.
- The wireless interconnect channel will be more convenient and flexible for layout chip distribution and for computer architecture design without concerning about wiring and routing of complicated vias and traces.

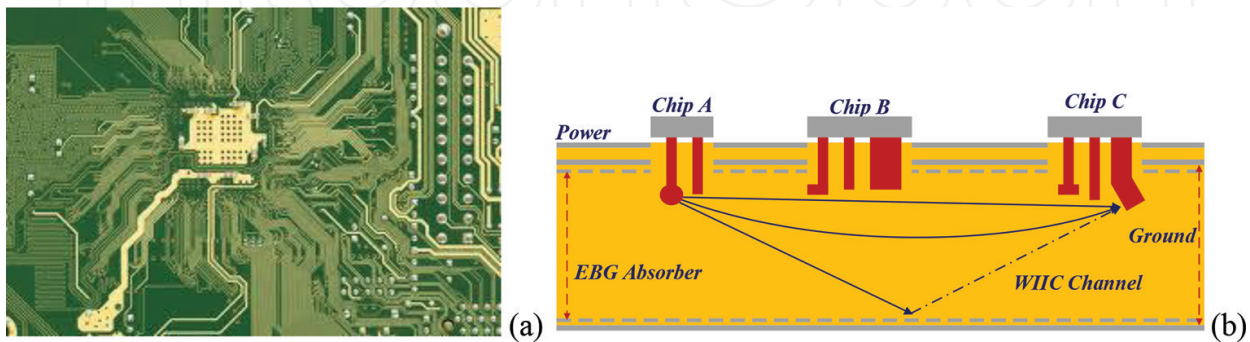


Figure 1. The concept of WIIC communication developed in this research. (a) Traditional high density, trace-based interconnect PCB, and (b) the concept of the proposed WIIC communication channel bounded by EBG absorber layers.

- There is no crosstalk, low distortion, dispersion, and time delay, although interferences between transceivers are unavoidable on this designed WIIC board.
- The long cycle process in designing and testing PCB trace wiring and routing will be completely eliminated.

2. Broadband EBG absorber design

2.1. Configuration of EBG absorber

The unit cell of the firstly proposed metamaterial EBG absorber, which is designed at the center frequency of 25 GHz, is displayed in **Figure 2**. The absorber unit includes a resistive layer, a dielectric substrate layer, and a ground layer. The octagon-shaped resistive layer consists of three consecutive loops of highly resistive frequency selective surface (FSS). The material of the three loops is tantalum nitride with the relative dielectric constant of $\epsilon_r = 1$, the relative permeability of $\mu_r = 1$, and the conductivity of $\sigma = 7400$ S/m. The board substrate is foam-characterized with $\epsilon_{rf} = 1.05$, $\mu_{rf} = 1$, and the loss tangent of $\tan \delta = 0.005$. The ground is made from copper with a conductivity of $\sigma = 5.8 \times 10^7$ S/m.

Similarly, the proposed 60 GHz absorber unit is built with the substrate of foam characterized by the dielectric constant $\epsilon_r = 1.0$. The dimensions of the absorber unit are about $4.2 \times 4.2 \times 1$ mm [13]. The absorber unit consists of three consecutive decagon loops in order to achieve a broadband frequency band centered at 60 GHz. The thickness of the resistive metal layer is 0.02 mm, the width of the loop traces is 0.08 mm, the edge-to-edge spacing is 0.08 mm, and the side lengths of three loops are 0.3245, 0.2503, and 0.2256 mm, respectively.

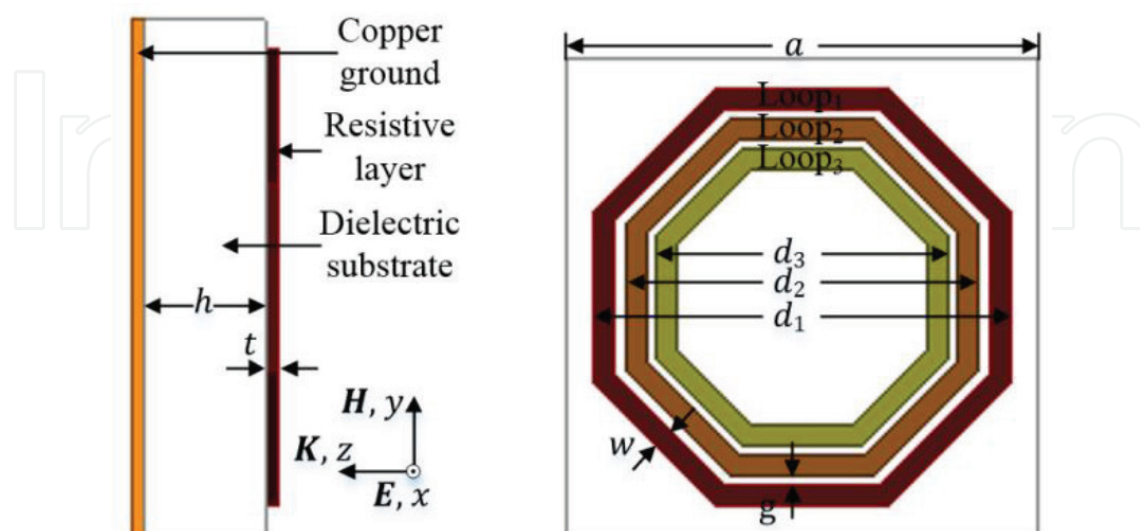


Figure 2. Side and top views of the 25 GHz EBG absorber unit, where $d_1 = 3.69$, $d_2 = 3.13$, $d_3 = 2.57$, $w = 0.18$, $g = 0.1$, $h = 1$, $t = 0.02$, $a = 4.2$, all in mm.

2.2. Broadband absorption performance

The absorber unit has been built into an HFSS (high frequency structure system) environment, as presented in **Figure 3**, where the boundary surfaces of the unit cell are curtailed with the HFSS built-in master and slave boundary conditions (BCs) in addition to two Floquet port excitations placed at the top and bottom as a wave port. In this case, the setting of the absorber unit can be considered as an equivalent, periodic, infinitely large absorbing configuration. Electromagnetic plane waves are placed to be incident onto the top surface of the absorber unit in the normal direction polarized as a transverse electric (TE) or a transverse magnetic (TM) wave.

The absorptance $A(f)$ is a measure of the absorber's EM wave power absorption, which is precisely given as

$$A(f) = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (1)$$

where S_{11} and S_{21} are the reflection and transmission coefficients estimated in the two-port network system, respectively. Because the absorber is essentially shielded by the copper ground, the EM wave cannot penetrate the structure, i.e., $S_{21} = 0$.

As shown in **Figure 4**, it is found that the proposed design of the absorptance $A(f)$ of the 25 GHz EBG absorber unit is about 90% or greater in the frequency band of 19.9–31.2 GHz. The relative bandwidth of the designed absorber unit is approximately 44% centered at the frequency of 25.6 GHz. The predicted $A(f)$ has been verified by an FDTD (finite difference time domain) simulation, which shows a higher agreement between those developed from the FDTD and HFSS methods [12].

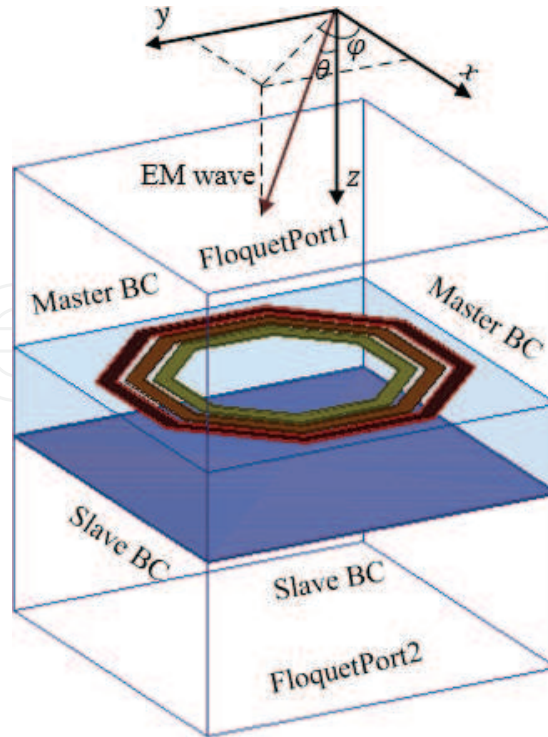


Figure 3. EBG absorber unit assessment system in an HFSS environment.

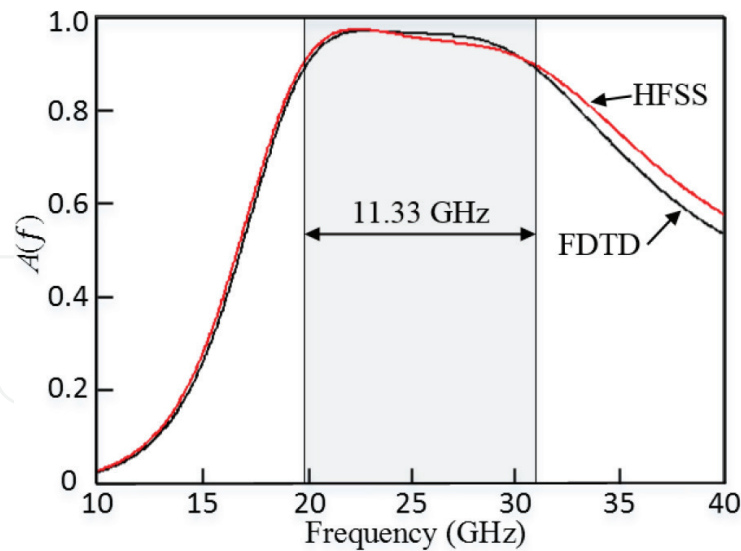


Figure 4. The simulated absorptance of the proposed 25GHz EBG absorber.

2.3. Equivalent circuit analysis

It is very often to develop an equivalent circuit model for evaluating the absorptance $A(f)$ of an EBG absorber speedily and efficiently in electrical engineering research and electronic engineering practice. An equivalent circuit for the EBG absorber unit has been presented using a transmission-line model as displayed in **Figure 5**, where C_i , L_i and R_i ($i=1, 2, 3$) are the capacitance, inductance, and resistance for the i th one of the three resistive loops ($i=1, 2, 3$), and C_{ij} , L_{ij} and R_{ij} ($i, j=1, 2, 3, i \neq j$) are correspondingly the mutual capacitance and inductance as well as resistance between the i th and j th resistive loops.

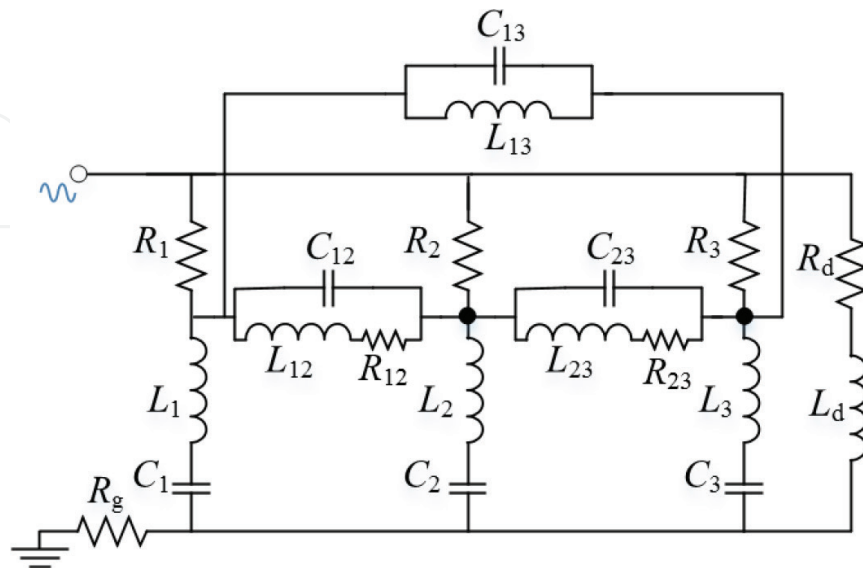


Figure 5. Equivalent circuit model for the absorber unit.

By neglecting the fringing effect, the capacitance of the parallel-plate capacitor is approximated as [14]

$$C = \frac{\epsilon_0 \epsilon_r w l}{h} \quad (2)$$

where l is the perimeter of the resistive loop, w is the width of the trace, and ϵ_r is the relative permittivity of the substrate. C_1 , C_2 , and C_3 are approximately evaluated by this relation.

Subsequently, the self-inductance of a microstrip etched on the substrate can be expressed as [15]

$$L = 2 \times 10^{-13} \times l \times \left(\ln \left(\frac{2l}{w+h} \right) + 0.5 + 0.2235 \times \frac{w+h}{l} \right) \quad (3)$$

where the above relation is used for gauging L_1 , L_2 , and L_3 , respectively, for the equivalent circuit.

The resistance introduced by the transmission-line conductors can be approximated by [16]

$$\begin{cases} R_L = \frac{l}{\sigma w t} & (\delta \geq t) \\ R_H = \frac{l}{w} \sqrt{\frac{\pi \mu_0 \mu_r f}{\sigma}} & (\delta < t) \end{cases} \quad (4)$$

where t is the thickness of the resistive layer, σ is the conductivity of the resistive layer, and δ is the skin depth of the conductor at the specified frequency of f . The skin depth of the resistive layer in the frequency band of 10–40 GHz is within the range of 0.0292–0.0585 mm. Because the skin depth is greater than the resistive layer thickness t , R_L in Eq. (4) should be used to calculate the resistances of the three loops. As shown in **Figure 5**, R_g , the resistance of the ground layer is also evaluated by employing Eq. (4).

The mutual capacitances and inductances among the resistive loops of the EBG absorber unit are approximated by employing the following relations [17]:

$$C_m = \frac{\pi \epsilon_0 \epsilon_r}{\ln(4(w+g)/w)} \times l \quad (5)$$

$$L_m = \frac{\mu_0 \mu_r}{\pi} \times \frac{w}{w+g} \times l \quad (6)$$

where C_{ij} and L_{ij} ($i, j = 1, 2, 3$) are evaluated using the above two relations. In this absorber design, due to the small gaps between any two neighboring loops, the resistances R_{12} and R_{23} are approximately equal to the characteristic impedance of air; while due to that Loop₂ separates Loop₁ and Loop₃, and R_{13} is very small and simply neglected here.

Given the permittivity ϵ_d , permeability μ_d , and conductivity σ_d of the dielectric substrate, by using the relations for the loss tangent, propagation constant and characteristic impedance [16]

$$\epsilon_d = \epsilon'_d - j \epsilon''_d \quad (7a)$$

$$\tan \delta' = \frac{\omega \epsilon'_d + \sigma_d}{\omega \epsilon'_d} \quad (7b)$$

$$\gamma = j\omega \sqrt{\mu_d \epsilon_d - j \sigma_d} \quad (7c)$$

$$\eta_d = \frac{j\omega \mu_d}{\gamma} \quad (7d)$$

The characteristic impedance in the substrate can be written as [18]

$$\eta_d = \frac{\mu_d}{\sqrt{\mu_d \varepsilon_d - j\omega(\varepsilon'_d \tan \delta' - \varepsilon''_d)}} \quad (8)$$

where the permittivity and permeability of substrate $\varepsilon_d = \varepsilon_0 \varepsilon_r$, $\mu_d = \mu_0 \mu_{r2'd}'' = 0$, and $\tan \delta' = 0.005$. The ground-equivalent resistance and inductance shown in **Figure 5** are initially set as $R_d = \text{Re}(\eta_d)$, and $L_d = \text{Im}(\eta_d)/j\omega$, which can be easily evaluated using Eq. (8) for contribution from the substrate.

The equivalent circuit model of the EBG absorber unit has been established in the ADS with the configuration of components, as shown in **Figure 5**. The values of these circuit components are finely tuned and optimized, and the achieved results are listed in **Table 1**. The absorptance $A(f)$ simulated from the equivalent circuit model in ADS is compared to that arrived from the corresponding HFSS full wave field solver as shown in **Figure 6**. In the frequency band of 18–40 GHz, $A(f)$ results obtained from ADS equivalent circuit and HFSS field approach remain a fairly good consistent.

Similarly, for the 60 GHz EBG absorber, an equivalent circuit of the designed absorber unit has also been developed as shown in **Figure 7**.

By using the transmission line model, the self and mutual inductances, capacitances, and resistances are derived and put into a schematic in an ADS window. The values of the components are tuned in ADS as listed in **Table 2**.

The absorptance of the designed decagon absorber obtained in HFSS and the one derived from the equivalent circuit simulated in ADS are displayed in **Figure 8**, where the absorption bandwidths for both cases are approximately 20 GHz. They are fairly consistent, except a frequency shift in the front and back edges of the band. It is apparent that for this designs both the central frequency (60 GHz) and the absolute bandwidth (50–70 GHz) are the highest among the recent metamaterial EBG absorbers [19–24].

R_1 (Ω)	C_1 (pF)	L_1 (nH)	R_2 (Ω)	C_2 (pF)	L_2 (nH)
40.76	0.20	0.45	37.69	0.13	0.26
R_3 (Ω)	C_3 (pF)	L_3 (nH)	R_{12} (Ω)	C_{12} (pF)	L_{12} (nH)
26.45	0.09	0.18	371.89	1.71	23.53
R_{23} (Ω)	C_{23} (pF)	L_{23} (nH)	R_{13} (Ω)	C_{13} (pF)	L_{13} (nH)
334.71	1.66	27.35		1.44	8.82
R_d (Ω)	L_d (nH)	R_g (Ω)			
371.81	0.24	0.0025			

Table 1. Equivalent circuit components for 25 GHz EBG absorber.

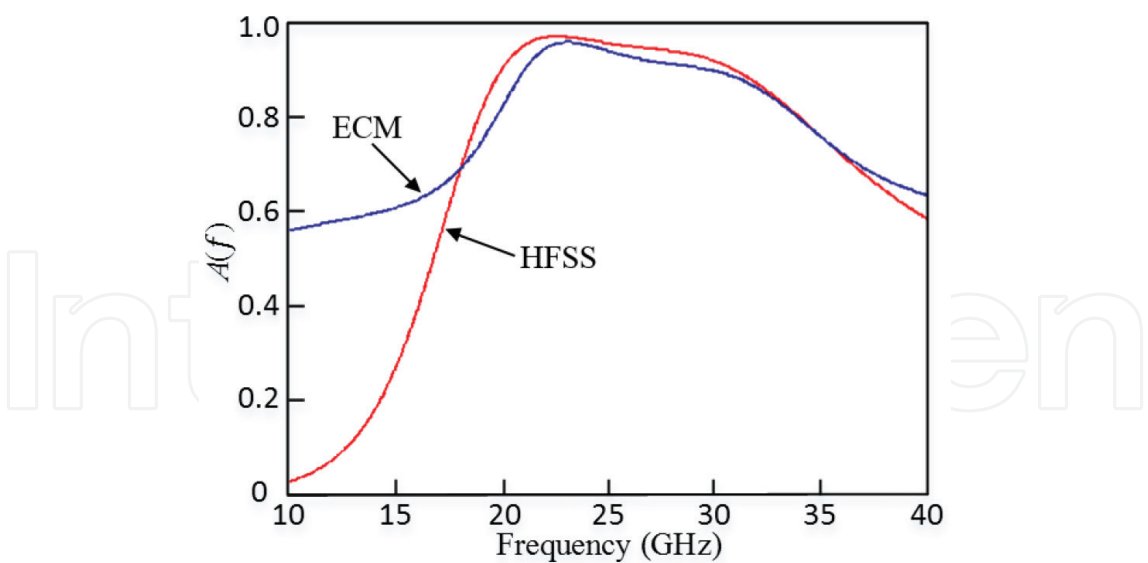


Figure 6. The equivalent circuit-simulated $A(f)$.

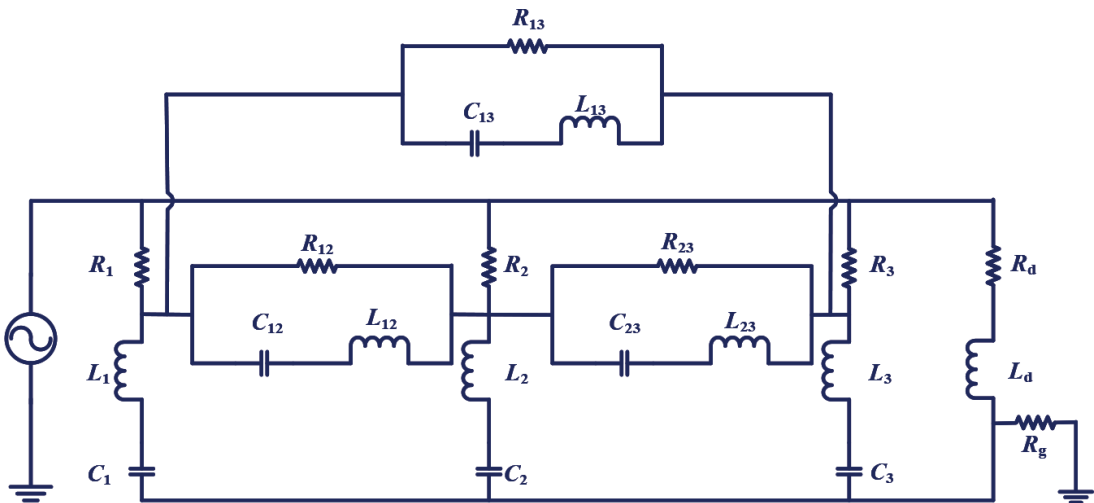


Figure 7. Equivalent circuit of the 60 GHz EBG absorber.

R_1 (Ω)	C_1 (pF)	L_1 (nH)	R_2 (Ω)	C_2 (pF)	L_2 (nH)
55.97	0.0046	0.36	1183.45	0.081	0.061
R_3 (Ω)	C_3 (pF)	L_3 (nH)	R_{12} (Ω)	C_{12} (pF)	L_{12} (nH)
997.31	0.67	0.04	278.80	0.040	
R_{23} (Ω)	C_{23} (pF)	L_{23} (nH)	R_{13} (Ω)	C_{13} (pF)	L_{13} (nH)
0	0.14	0.65	278.80	0.081	0.20
R_d (Ω)	L_d (nH)	R_g (Ω)			
0.0045	0.32	0.72			

Table 2. Equivalent circuit components for 60 GHz absorber.

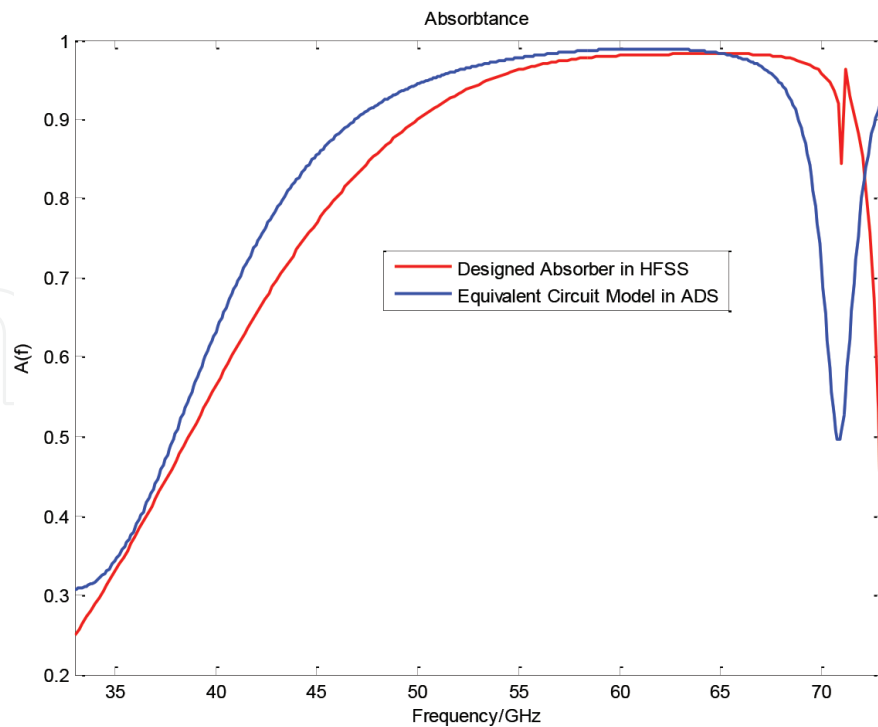


Figure 8. Absorbance of the designed 60 GHz absorber and the equivalent circuit.

3. Wireless WIIC channel design

3.1. Construction of broadband wireless channel

Based on the design of the metamaterial absorber, a metamaterial-absorbing layer bounded WIIC channel has been further designed [13]. In the designed channel, two layers of the metamaterial EBG absorbers are placed on the top and bottom of the PCB board. Also, three antennas are placed on the top layer of the channel to perform the transceivers of chips in the WIIC system. The transceivers are used to transmit and receive signals operating at a 60 GHz frequency band. The WIIC channel is modeled in HFSS as shown in **Figure 9**.

The WIIC channel is designed with the total dimensions of $60 \times 80 \times 5$ mm, which has been equipped with total 249 and 252 (14×18) absorber units on the top and bottom layers, respectively. The substrate dielectric material is filled with Foam in the designed in the WIIC channel. Three microantennas are placed on the top layer, which are fed with the coaxial lines. The antennas are about 30 mm apart from each other.

The HFSS-simulated S-parameters for the wireless PCB channel and a comparable structure, parallel plate system, are shown in **Figure 10**. As seen from the figure, the 10 dB bandwidth with acceptable insertion loss approximately ranges from 50 to 70 GHz. The insertion loss between the two transceivers ranges approximately from 22 to 35 dB in the frequency band from 50 to 70 GHz. The return loss is about -13 dB at the central frequency, with a minimum frequency of -32.06 dB at 49.62 GHz. It is noticed that the S-parameters for the corresponding parallel plates are also fluctuated to meet the bandwidth requirement, and the insertion loss is much lower in the frequency band of interest.

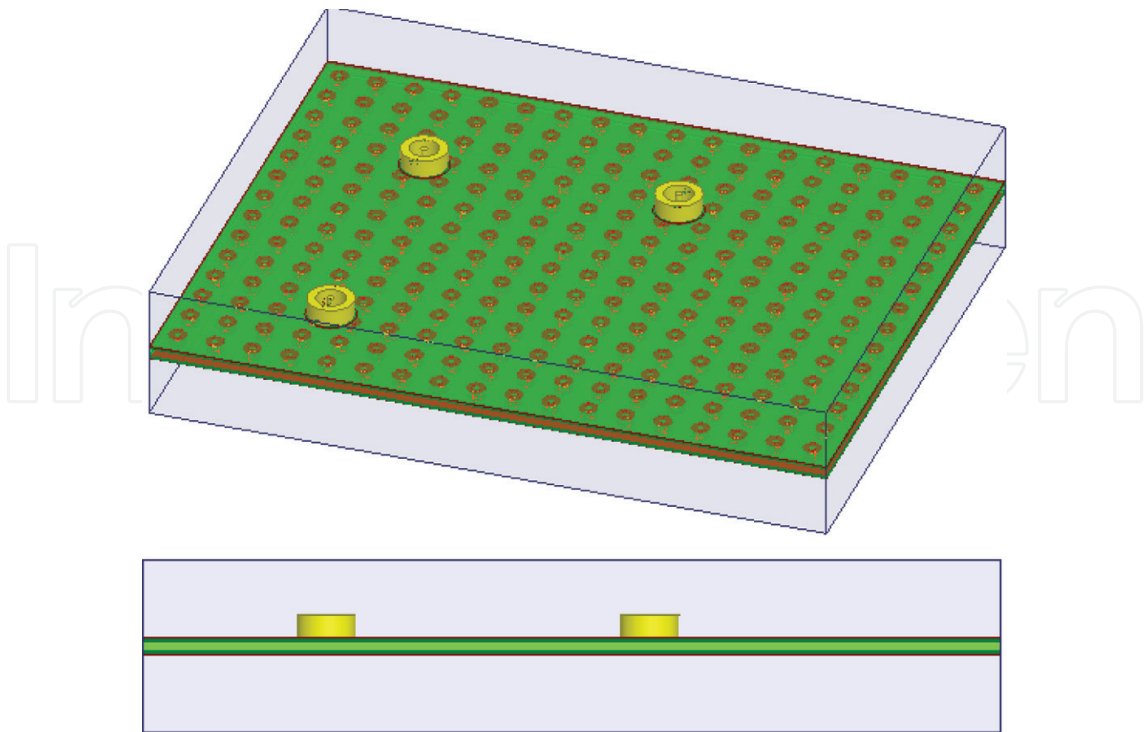


Figure 9. WIIC channel built with the metamaterial EBG absorber units: the geometry of the WIIC channel and its side view.

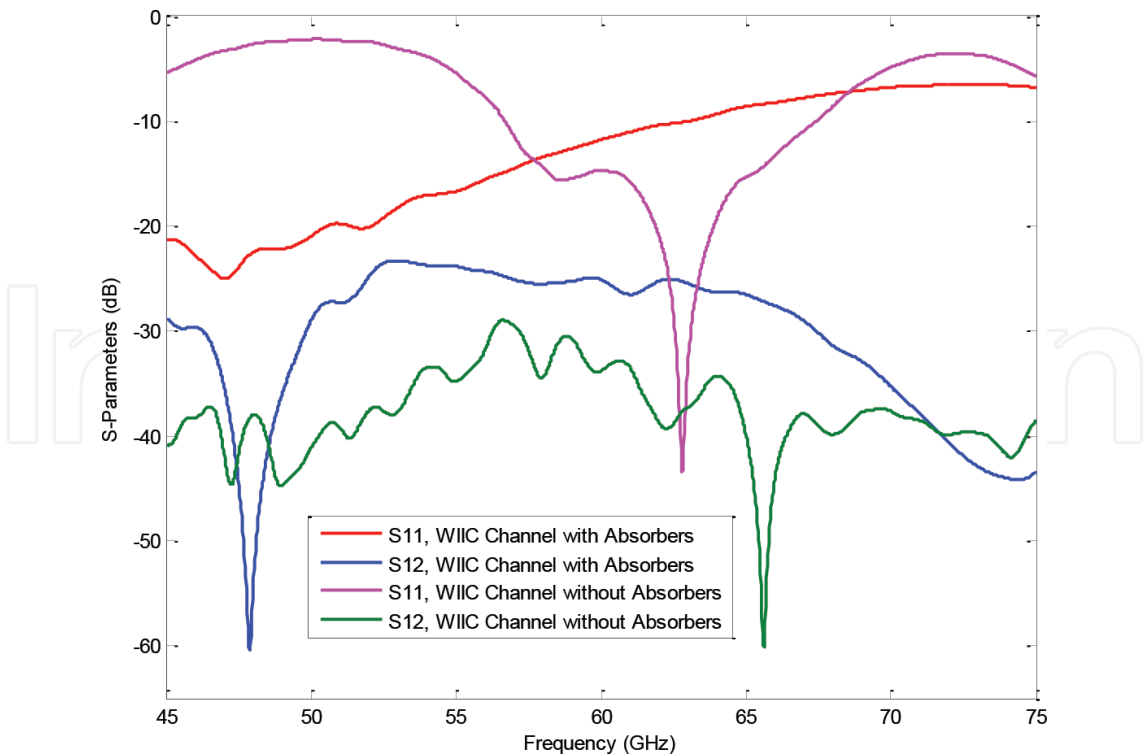
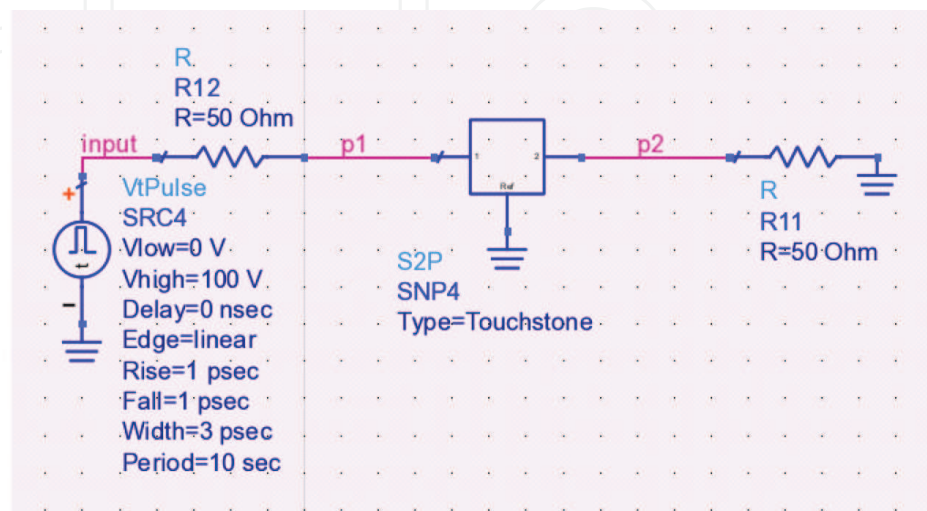


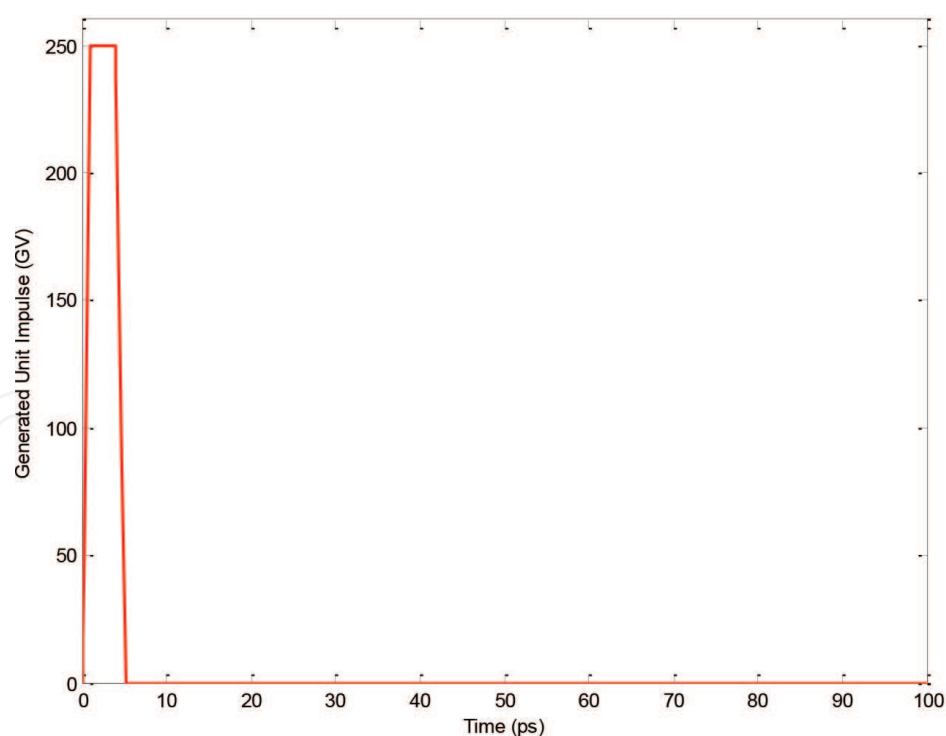
Figure 10. Extracted S-parameters for the designed 60 GHz WIIC channels with the EBG absorber layers and ground plates.

3.2. Numerical extraction of impulse responses and transfer functions

To characterize the WIIC channel and to simplify the channel performance analysis, the impulse response is then extracted in ADS. The schematic for impulse response extraction and the time domain waveform of the input unit impulse are, respectively, shown in **Figure 11**.



(a)



(b)

Figure 11. Impulse response extraction techniques. (a) Schematic for impulse response extraction, and (b) the input unit impulse.

The generated unit impulse is numerically determined to satisfy its definition as follows:

$$\int_{-\infty}^{\infty} \delta_w(t) dt = \frac{1}{2}(\Delta t_1 + \Delta t_2) V_H = 1 \text{ (V} \cdot \text{s)} \quad (9)$$

where V_H is the magnitude of the pulse, Δt_1 and Δt_2 are the total pulse widths at the pulse top and bottom, respectively.

To compare the wireless PCB channel analysis to the existing wired trace approach, a wired PCB channel with a number of vias, striplines, microstrip lines, through whole pins, and connectors has been analyzed and measured. A motherboard, which includes a CPU on the top layer, is shown in **Figure 12**. The dimensions of the motherboard are $508 \times 218 \times 2.54$ mm. There are a total of 22 layers on this PCB board, including eight stripline layers, two microstrip line layers, 10 ground planes, and two power planes. The size of the boards is much larger than the simulated wireless WIIC PCB, because the wired PCB channels consist of hundreds of traces at different layers to reduce the crosstalk among these traces.

The highlighted part of the board to be studied consists of a 300-mil microstrip, two vias, a 5.3-inch stripline, a through whole pin, and a connector. The wired PCB channel is measured using both TDR (time domain reflectometry) and TDT (time domain transmission) signals. The S_{11} and S_{12} can be approximately generated from the measured TDR and TDT signals, respectively. The reason for why not directly measuring the S-Parameters using a Vector Network Analyzer (VNA) to extract the S-Parameters is primarily due to that the cost

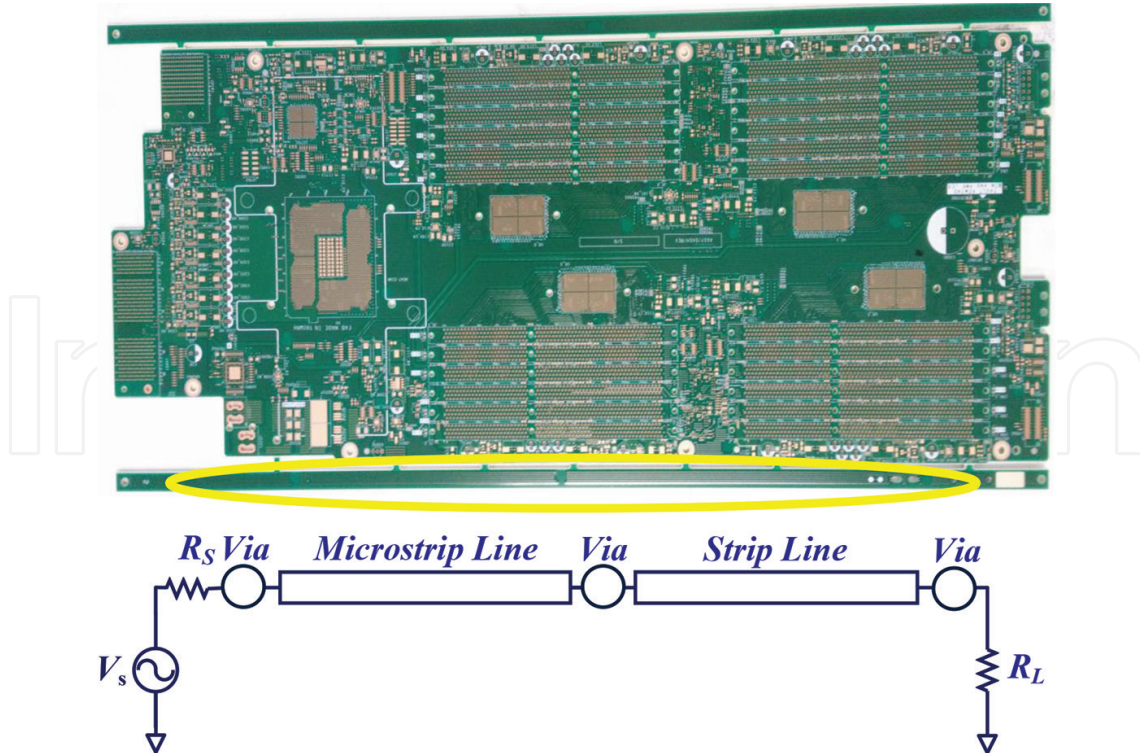


Figure 12. Wired PCB channel consisting of vias, microstrip, and striplines.

of the VNA capable for the desired high frequency band of 50-70 GHz is too expensive. It was unavailable when doing the measurement for the wired PCB channel. The TDR/TDT signals will be used for extraction of the impulse response and transfer function of the channel. The wired PCB channel schematic diagram is displayed in **Figure 12**. The S-parameter models of via, through whole pin, microstrip and stripline simulated in HFSS, and the connector S-parameters model provided by the vendor are cascaded in ADS to generate the overall S-parameters and to obtain the simulated TDT/TDR for the wired PCB channel.

The extracted impulse responses of the WIIC channel, measured and simulated wired PCB channels are shown in **Figure 13**. It is clearly seen that the measured and simulated impulse responses match very well.

As the frequency response of a system can be easily generated in MATLAB by performing an FFT to the impulse response. The discrete frequencies and the sampled time points have to satisfy the following relation [25]:

$$\Delta f = \frac{1}{\Delta t N} \quad (10)$$

where Δt is the sampling time interval of the impulse response, and N is the total samples of the impulse response in the time domain.

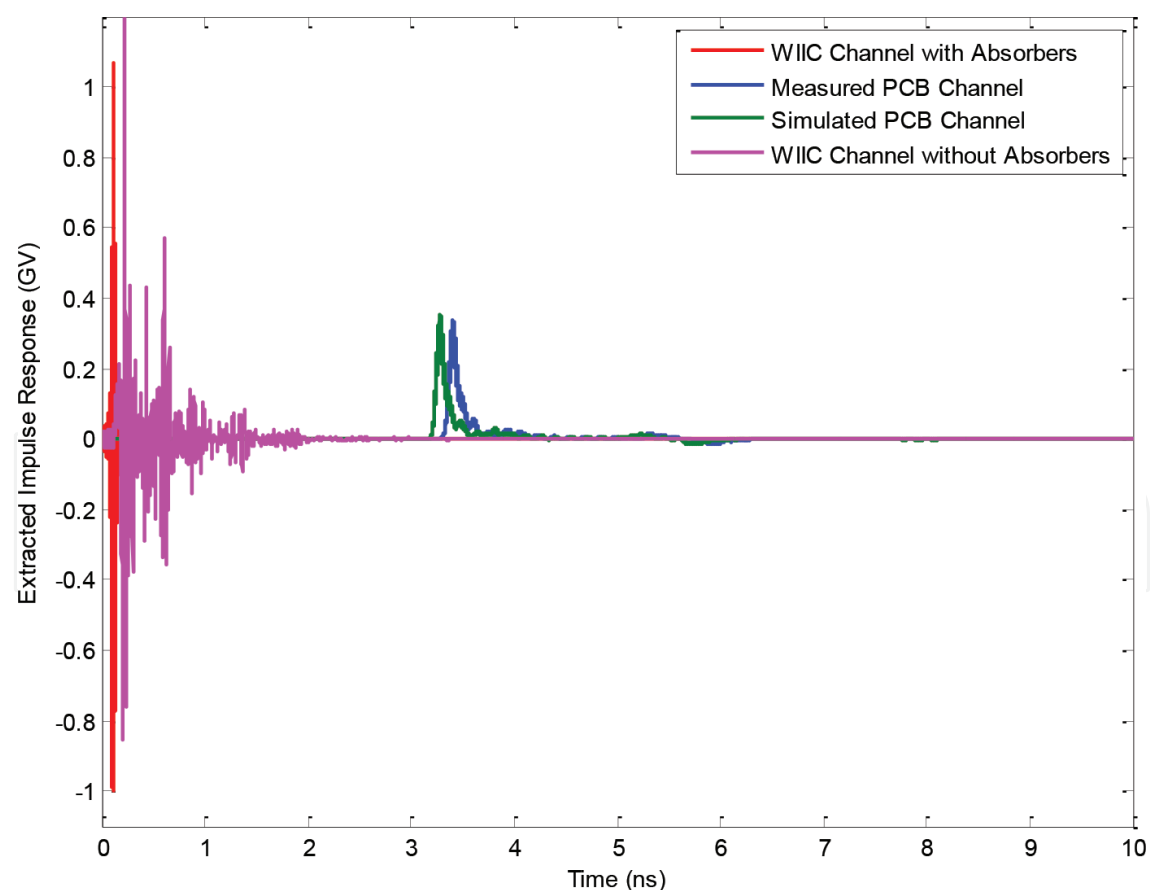


Figure 13. Extracted impulse responses.

The extracted system transfer functions for the measured and simulated wired and wireless PCB channels are shown in **Figure 14**. It is clearly seen that the transfer functions of the simulated and measured PCB channels are very consistent, and they are almost cutoff from 15 GHz. However, the proposed wireless WIIC PCB channel performs very well for the desired frequency band around the neighborhood of 60 GHz. In other words, with an identical input to the channels, the bandwidth of the wireless WIIC PCB channels will be much larger than that of the wired PCB channel. The transfer function for the wireless WIIC PCB channel with the absorbers is relatively flat in the frequency range of 45–65 GHz. It is also noticed that this bandwidth is not completely consistent with that of the insertion loss resulted from HFSS.

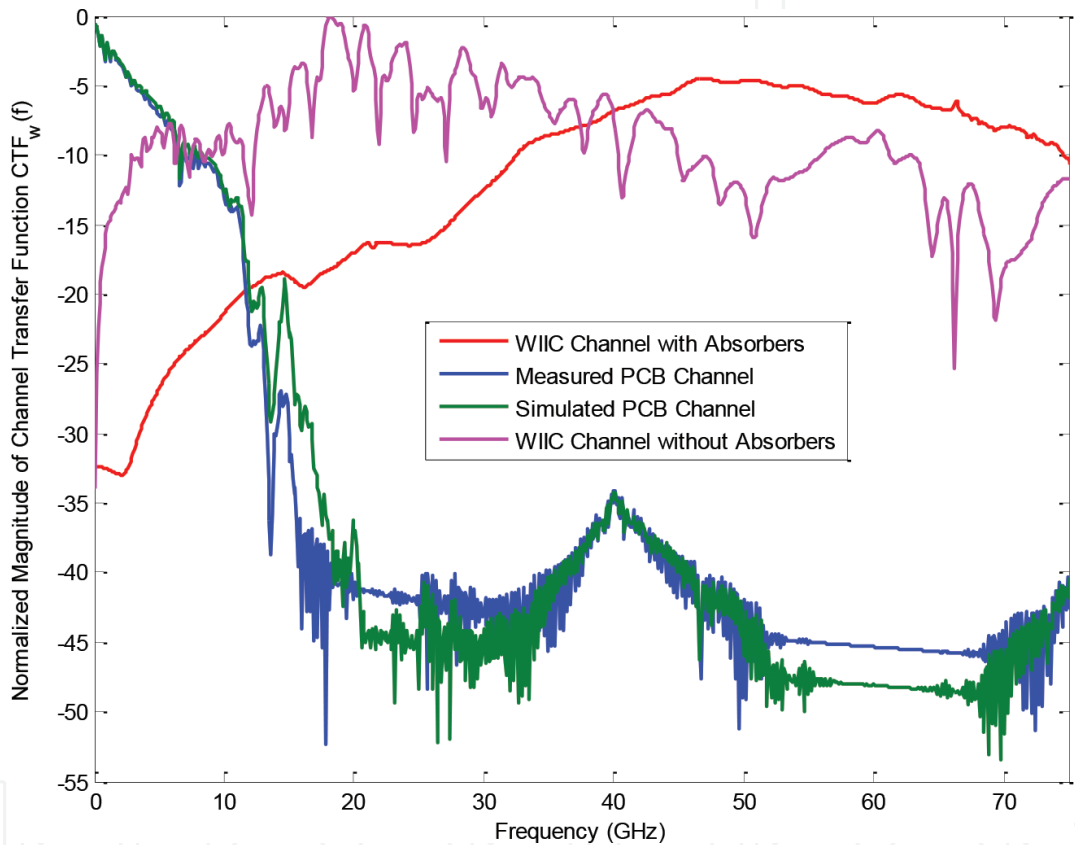


Figure 14. Transfer functions (dB) for the WIIC, measured and simulated wired PCB Channels.

4. System and channel performance analysis

4.1. WIIC transceivers

In this chapter, various advanced wireless and mobile technologies are implemented in the proposed WIIC system, including the orthogonal frequency division multiplexing (OFDM), quadrature phase shift keying (QPSK), quadrature amplitude modulation (QAM), and multiple input multiple output (MIMO). Herein, an ideal 4×4 antenna array with the four identical channels is assumed, which correspondingly will lead to the upper bond data rate of the

system. As the result of employing the technologies of OFDM, MIMO, and QPSK/QAM, the data rate and spectrum utilization of the system are dramatically improved.

The WIIC system in this work also includes forward error control (FEC), and interference mitigation to diminish the error brought by the channel and interferences from the channel and other transmitters. In this system, FEC mainly includes cyclic redundancy check (CRC) and channel coding, and interference mitigation features the techniques of scrambling and interleaving. For the FEC scheme, the system employs 16-bit CRC and 1/3 code rate tail-biting convolution coding. The WIIC system employs cyclic prefix (CP) to deal with the timing problem, and OFDM-UWB (ultra wide-band) to achieve low power consumption. The system block diagram is shown in **Figure 15**.

4.2. OFDM symbol decoding

MIMO demapping, demodulation, descrambling, deinterleaving, and channel decoding are all equipped in the OFDM symbol decoding scheme in this WIIC system [26–28]. Demodulation is able to automatically diminish the mistakes brought by the noise from the channels, and channel decoding can correct some errors in the receiving signals. Correctly MIMO demapping, demodulation, descrambling, deinterleaving, and channel decoding will provide the receiver the correct output bits, which can be used for comparison with the transmitted signals, and can accurately calculate the system BER.

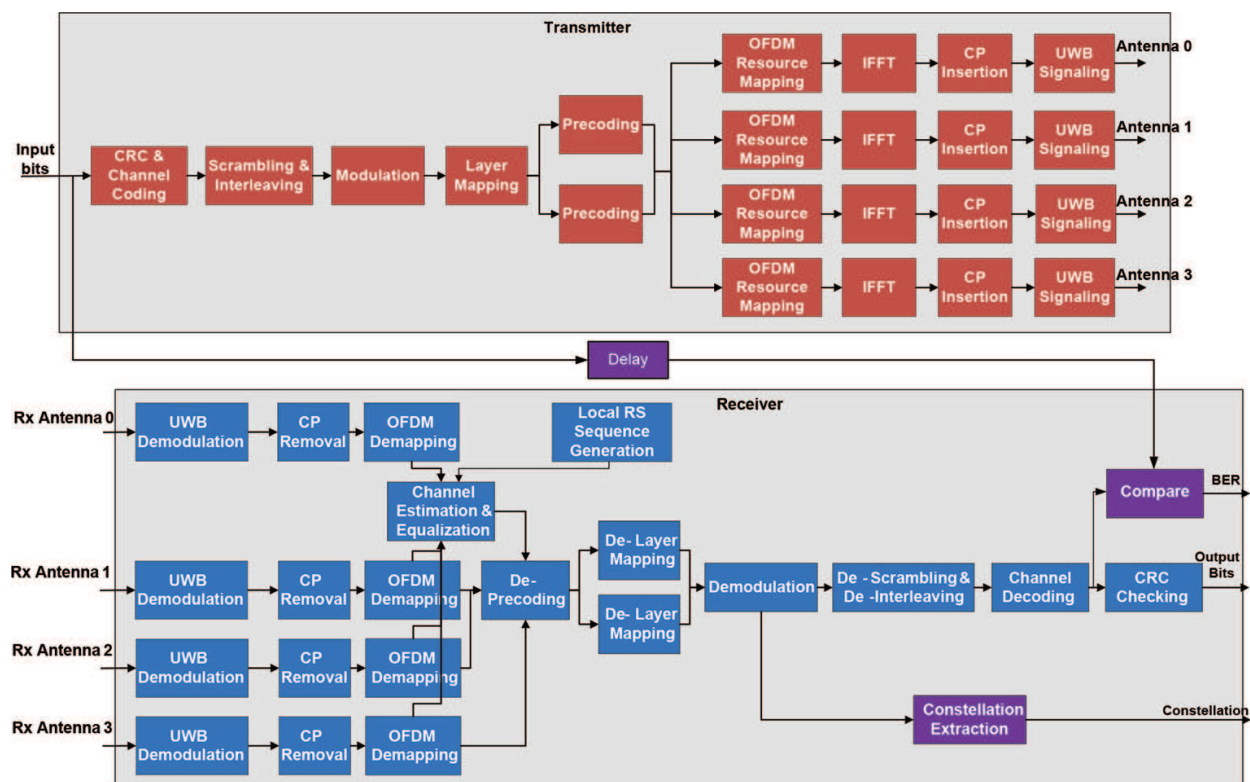


Figure 15. WIIC system block diagrams for transmitter and receiver.

As the precoding matrices employed by MIMO are orthogonal matrices, correspondingly, the inverse matrices, in other words, the deprecoding matrices are simply that are used for transposed precoding matrices. Thus, the deprecoding procedure will be the received signal matrix multiplied by the correct transposed precoding matrix. Besides, after deprecoding, the delay mapping is the inverse procedure of the layer mapping, which is a procedure for collection and rearrangement of deprecoded data.

The constellation improvement of the SDM brought by precoding is simulated in MATLAB. The constellation diagrams collected at the receiver of a system without precoding, and that with precoding are displayed in **Figures 16** and **17**, respectively. The simulation includes 2,048,000 bits, under the AWGN channel, with SNR 5 dB.

4.3. WIIC system performance analysis

In the system and channel performance analysis, four different channels are investigated in MATLAB, which are the additive white Gaussian noise (AWGN), Rayleigh, the designed WIIC, and the measured PCB channels. The relationships of bit error rate (BER) and signal-to-noise rate (SNR) with four different channels are shown in **Figure 18**. In each SNR condition, a random binary of 441,600,000 bit stream is input to these four different channels and the BER is obtained by acquiring the number of bits in which the input and output are different.

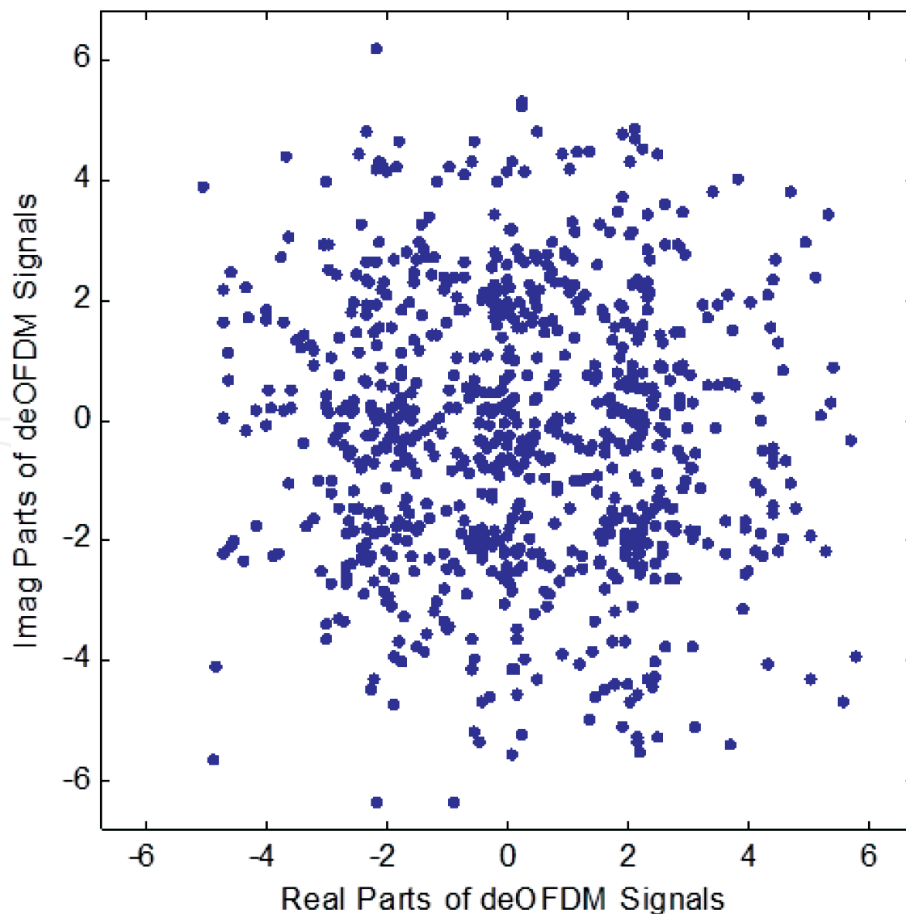


Figure 16. Constellation at receiver without MIMO.

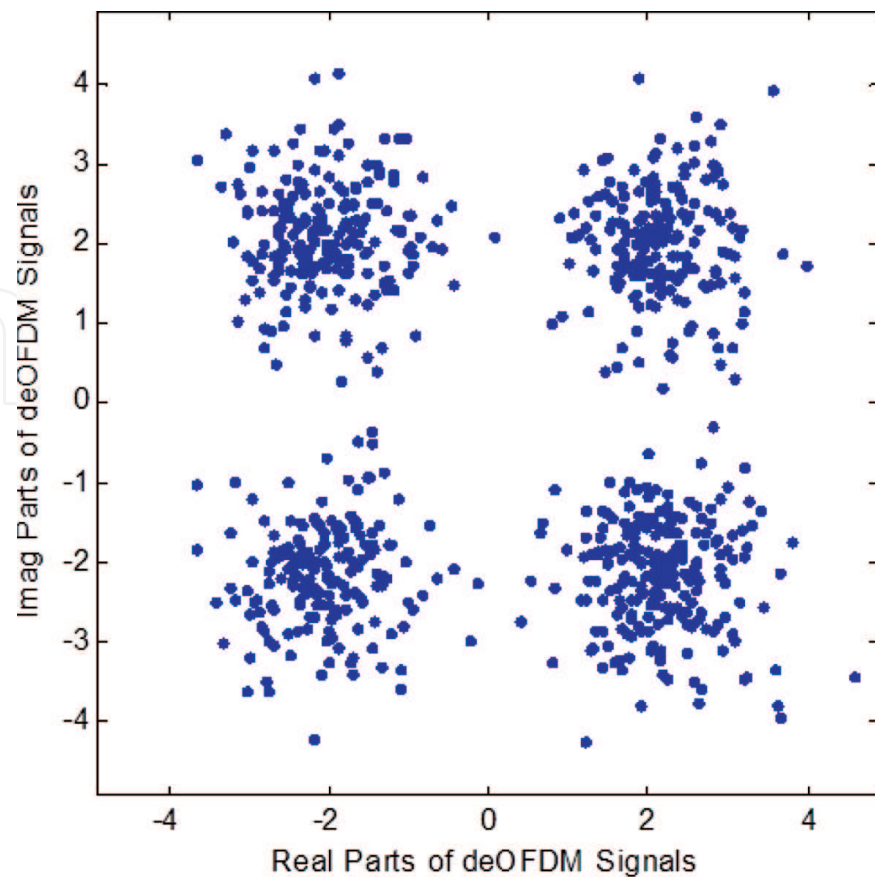


Figure 17. Constellation at receiver with MIMO.

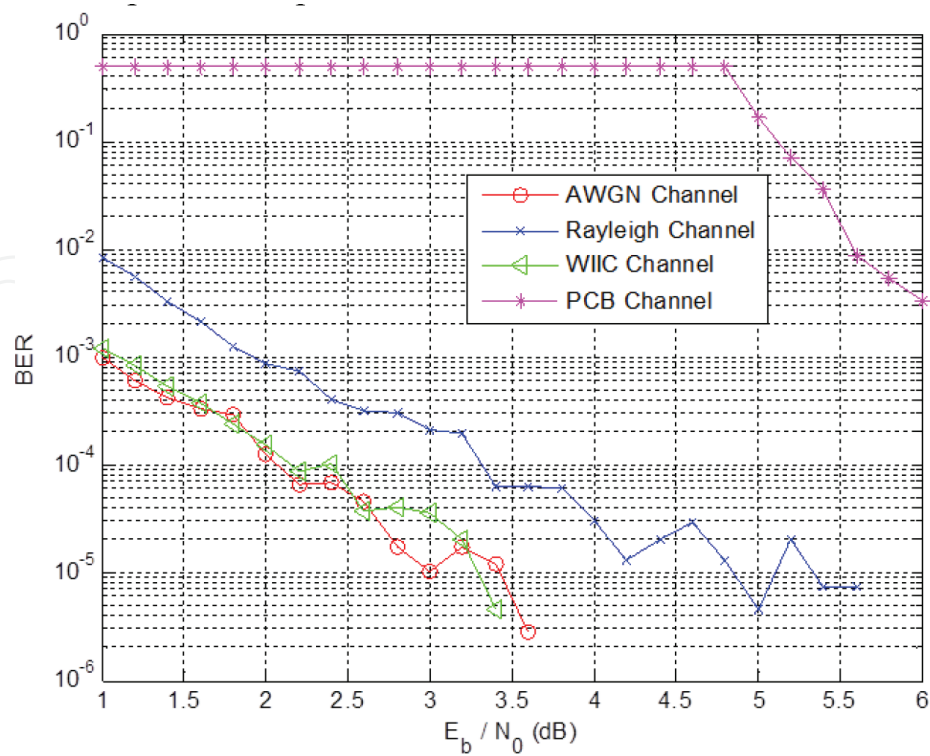


Figure 18. BER versus SNR in different channels.

Herein, BERs are extracted by directly comparing the input and output, so that the results are more reliable than obtaining BER by calculation using CRC-checking results. Besides, in the simulation 0 dB antenna gain is assumed, and without including any low-noise amplifier (LNA), as the worst-case analysis of the simulated channels. Also, AWGN and Rayleigh channels provide the best or worst case for wireless channels, which cannot validate the designed system, but can also be compared to the proposed WIIC and wired PCB channels.

As predicted in the previous analysis, the BER reaches to be less than 10^{-5} at SNR of 3, 3.4, and 5.4 dB for AWGN, WIIC, and Rayleigh channels, respectively. Also, when SNR is greater than 3.6, 3.4, and 5.6 dB, none of the single error bit is found in BER analysis, with AWGN, WIIC, and Rayleigh channels, respectively. In contrast, it is not surprising that the BER for the wired PCB channel is much higher than the other channels due to its cutoff in the frequency band of interest.

5. Conclusion

In this chapter, based on the design of an EBG absorber unit, a WIIC channel has been designed and validated in the WIIC system. Also, as a reference system, a wired PCB channel is measured, simulated, and analyzed for extracting its S-parameters and system transfer functions. It is found that the wired PCB boards are no longer qualified for transmitting signals at a 60 GHz band for the case studied, while the designed WIIC channel works properly in this band. With the extracted WIIC S-parameters, its impulse responses and the normalized transfer functions are obtained in ADS and MATLAB. The BER analysis shows that the performance of the proposed WIIC channel is close to a simple AWGN channel when the WIIC transceivers are characterized with channel coding, channel sounding, channel estimation, and channel equalization.

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