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Semiconductor Nanowire MOSFETs and Applications

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Abstract

Semiconductor nanowires have aroused a lot of scientific interest and have been regarded as one of the most promising candidates that would make possible building blocks in future nanoscale devices and integrated circuits. Employing nanowire as metal-oxide-semiconductor field-effect transistor (MOSFET) channel can enable a gate-surrounding structure allowing an excellent electrostatic gate control over the channel for reducing the short-channel effects. This chapter introduces the basic physics of semiconductor nanowires and addresses the problem of how to synthesize semiconductor nanowires with low-cost, high-efficiency and bottom-up approaches. Effective integration of nanowires in modern complementary metal-oxide-semiconductor (CMOS) technology, specifically in MOSFET devices, and non-volatile memory applications is also reviewed. By extending the nanowire MOSFET structure into a universal device architecture, various novel semiconductor materials can be investigated. Semiconductor nanowire MOSFETs have been proved to be a strong and useful platform to study the physical and electrical properties of the novel material. In this chapter, we will also review the investigations on topological insulator materials by employing the nanowire field-effect transistor (FET) device structure.

Keywords: semiconductor nanowire, gate-surrounding, MOSFET, self-assembly, flash-like non-volatile memory, topological insulator nanowire FETs

1. Introduction

Since the invention of integrated circuit in the 1950s, the scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) continues with the emergence of new technologies to extend complementary metal-oxide-semiconductor (CMOS) down to ever smaller technology node. However, the CMOS scaling has deviated from the trends predicted by Moore and the scaling rules set forth by Dennard et al. due to fundamental physical and technical limitations [1, 2]. Limitations such as heat dissipation, leakage current and channel length

modulation have become a major concern that will inevitably lead to the slowing down in CMOS scaling when approaching atomic dimension. Thus, there is an urgent need to develop new semiconductor technology to solve the issues including cost, speed, density, reliability and power dissipation. A great deal of efforts has been made, and among all the candidates, nanoelectronics involved with replacing existing silicon-based technology has risen to be one of the most promising solutions towards continuous CMOS scaling.

During the past decades, semiconductor nanowires synthesized by bottom-up techniques and derived field-effect transistor (FET) devices have been intensively studied as the fundamental building blocks for nanoelectronic devices and circuit technologies [3–7]. Compared to planar devices based on bulk materials, the nanowires have a smaller channel and large surface-to-volume ratio. In addition, the gate-surrounding or gate-all-around (GAA) structure that can be formed in the nanowire FET allows excellent electrostatic gate control over the nanowire channel. Moreover, the GAA nanowire transistors enable ultimate CMOS device scaling with the best possible short-channel control considering the quantum confinement effects and the scattering at atomic dimensions. The GAA horizontal nanowire FET architecture exhibits high similarities to the FinFET, which is the predominant technology in the current 10 nm or even 7 nm process node. Thus, GAA FETs are very promising candidates in the sub-7 nm nodes to extend the scalability beyond the limits imposed by the FinFET technology with much less complexity compared to the alternative scaling approaches [8].

Till date, nanowire FETs have mainly been fabricated using the “top-down” approaches based on advanced lithography with nanowire prepared by dry/wet etching which usually yields well-oriented nanowire arrays [9, 10]. However, it has been well recognized that nanowires synthesized by “bottom-up” techniques such as chemical vapour deposition (CVD) can have lower cost and higher quality compared to the “top-down” methods [11]. Thus, it would be very attractive to develop an approach to manufacture such nanowire FETs with an excellent performance. Nevertheless, the technique to fabricate FETs from CVD grown silicon nanowires remains a barrier to the development of devices with optimized performance. Current approaches are primarily based on the harvesting and positioning the as-grown nanowires using aligning methods such as fluidic alignment, dielectrophoresis or nanoscale probe methods [12–17]. Such methods will inevitably introduce contaminants to the nanowire surfaces, which will adversely influence the device interface state density and possibly the nanowire surface roughness, and the device performance will be deteriorated as a result.

In this chapter, we first review the fundamentals of semiconductor nanowires and synthetic strategies. Then we introduce a novel self-alignment fabrication process for nanowire FET applications. The high-quality self-aligned nanowire channels possess clean surface and the fabricated FET devices exhibit excellent performance including large on/off ratio, small sub-threshold slope and small leakage current. Such an effective nanowire integration scenario is very attractive for different materials and device investigations. We focus on the flash memory based on the self-aligned Si nanowire FETs and the study of topological insulator nanowire FETs using the self-alignment techniques. The results demonstrate that by employing the one-dimensional nanowire as the active component in the electronic devices, the flash memory performance has been significantly improved such as lower operation voltage and better

reliability, and the basic principles behind the topological insulators have been manifested strongly enabling more delicate characterizations to understand the physics of the specific material. We believe that nanowire MOSFETs will open up a suit of potential applications in future sub-10 nm semiconductor technology as well as solutions towards emerging micro and nanoelectronic device challenges.

2. Review of physics of semiconductor nanowires

The theory of nanowires will be briefly reviewed with a focus on silicon nanowires since the features discussed here can be extended to other types of semiconductor nanowires. The structural and mechanical properties of silicon nanowires will be reviewed first, and then the electronic properties will be discussed in which we will also consider the device-related issues and limitations.

2.1. Structural and mechanical properties

The Si nanowires are intriguing mostly due to the extra high surface-to-volume ratio and the well-defined single crystalline orientation. The nanowire growth direction has been widely studied, and the connection between the diameter and the favoured crystal direction has been established [18]. It has been reported both experimentally and theoretically that the catalyst-assisted Si nanowires with smallest diameter prefer the $\langle 110 \rangle$ direction, while the nanowires with larger diameter favours the $\langle 111 \rangle$ direction [19–21]. The growth direction determines the nanowire cross section to some extent. A pentagonal cross section has been observed from the ground-state structure for Si nanowires up to 5 nm [22, 23]. This cross section due to the joint of five prisms cut of a Si (110) plane has rarely been reported. A more well-known structure in good agreement with experimental work is the hexagonal cross section for $\langle 110 \rangle$ Si nanowires with a bulk core [18, 24].

Mechanical properties of Si become quite different when reaching nanoscale with lower dimension. Due to the compressive surface stress, the Young's modulus of $\langle 100 \rangle$ Si nanowires softens as the surface-to-volume ratio increases and a steep decrease has been detected on shrinking of the nanowire diameter to 2–2.5 nm [25]. It was further discovered that the Young's modulus of Si nanowires is strongly anisotropic [26]. Different from the $\langle 100 \rangle$ nanowires, which exhibit lowest values, the wires grown along $\langle 110 \rangle$ direction give the highest values. These results are also in good agreement with the experimental work [27]. Currently, the mechanical properties of nanowires have become a promising research direction. Static and dynamic nanowire bending with atomistic simulations, which relies on periodic boundary conditions, reveals the influence of surface stress more clearly and provides valuable information for nanowire-based device designs.

2.2. Electronic properties

It is widely recognized that bulk Si has an indirect band gap, with the valence band maximum at the Γ point and the conduction minimum at about 85% along the Γ and X direction.

However, Si nanowires grown along most orientations have a direct band gap, with the maximum of the valence band and the minimum of the conduction band aligned at the same point in k-space. As a result, such nanowire materials have become encouraging candidates in optoelectronics or photonics applications [28].

The electronic properties of nanowires depend on the nanowire growth direction, cross section and diameter. However, it is interesting to find that the band gap of Si nanowire is insensitive to the shape of cross section. The band gap of a 1 nm nanowire was found constant with change less than 0.09 eV by simulating cross sections that are even utterly different, as long as providing the same surface-to-volume ratio [29, 30].

Different types of Si nanowire based electronic devices have been fabricated and studied for a variety of application purposes. An important cause of electrical conductance degradation in such devices is the scattering occurring at the surface with the presence of surface defects or surface roughness [31, 32]. Generally, the surface roughness disorder induces irregularities in the density of states along the nanowire axis, resulting in the carrier reflection and reduction in conductance. A more detailed study shows that the backscattering due to the surface roughness strongly depends on the nanowire orientation, and the anisotropy comes from the difference in band structure [33, 34]. In particular, electrons are less sensitive to surface roughness in $\langle 110 \rangle$ nanowires, and the transfer of holes is more smooth in $\langle 111 \rangle$ nanowires. Other electronic transport parameters such as the mean free path, length and the localization length can be better explained with the above incorporated differences.

Despite the defects or roughness from the nanowire surface, the existence of impurities is another major source of scattering, especially when the nanowire size is scaled down below 10 nm. Unlike the bulk in which the carriers are just slowed down by the impurities, the trajectories of the carriers in an extremely thin one-dimensional medium can be entirely backscattered because the scattering potential often extends throughout most of the cross sections of the thin wire [34]. Impurities can be originated from imperfect growth or intentional doping for targeted electrical properties when referred to semiconductors. For the dopants in Si nanowires, impurities like donor impurities, either segregate to the surface forming electrically inactive components or stay in the wire producing a strong backscattering, both will lead to the decreased conductance.

3. Silicon nanowire synthesis and field-effect transistors

3.1. Silicon nanowire synthesis

There has been a large number of reported works on the nanowire synthesis of a wide spectrum of semiconductor materials during the past decades. Both chemical and physical methods are intensively studied. Understanding the growth mechanism of these synthesis approaches is helpful in developing one-dimensional nanostructures of the desired materials and derivative electrical devices.

Solution phase synthesis of nanowires is a low cost yet high yield method in which selective capping agents are often employed, especially in an anisotropic growth, for the kinetic control of the evolving nanostructure to allow elongation along certain axis by preferentially adsorbing to specific crystal facets [35–37]. The major limitation of such solution phase synthesis lies in the empirical trial-and-error methodology for capping agents. Template-assisted electrochemical synthesis is another popular approach to grow one-dimensional nanostructures. Synthesis of metals, semiconductors and conductive polymers and oxides has been reported by using templates such as anodic aluminium oxide (AAO) and polycarbonate membranes [38, 39]. This method shares the advantages such as low-cost, well-orientation, ambient temperature, pressure operation and feasibility of batch fabrication of nanowire array. However, complete template filling still remains a challenge for the nanowire synthesis through electrodeposition. Template-assisted synthesis has been more utilized in the formation of hollow nanotube and core-shell nanowire structures in combination with atomic layer deposition (ALD) technique [40, 41].

Vapour phase synthesis of one-dimensional nanostructure is probably the most extensively explored approach. Numerous techniques have been developed to grow nanowire from gas precursors. Among all the vapour phase methods, the most widely studied and successful approach in generating high-quality single-crystal nanowires in large quantities is the vapour-liquid-solid (VLS) mechanism [4]. We will be focusing on this method in this section, and the following contents reviewed in this chapter are based on the nanowires synthesized by using the VLS approach.

A typical VLS process starts from the dissolution of vapour reactants into a catalytic alloy phase, followed by the crystal nucleation at the liquid-solid interface. As illustrated in **Figure 1**, gold nanoparticles are commonly used as catalyst for Si nanowire growth by the

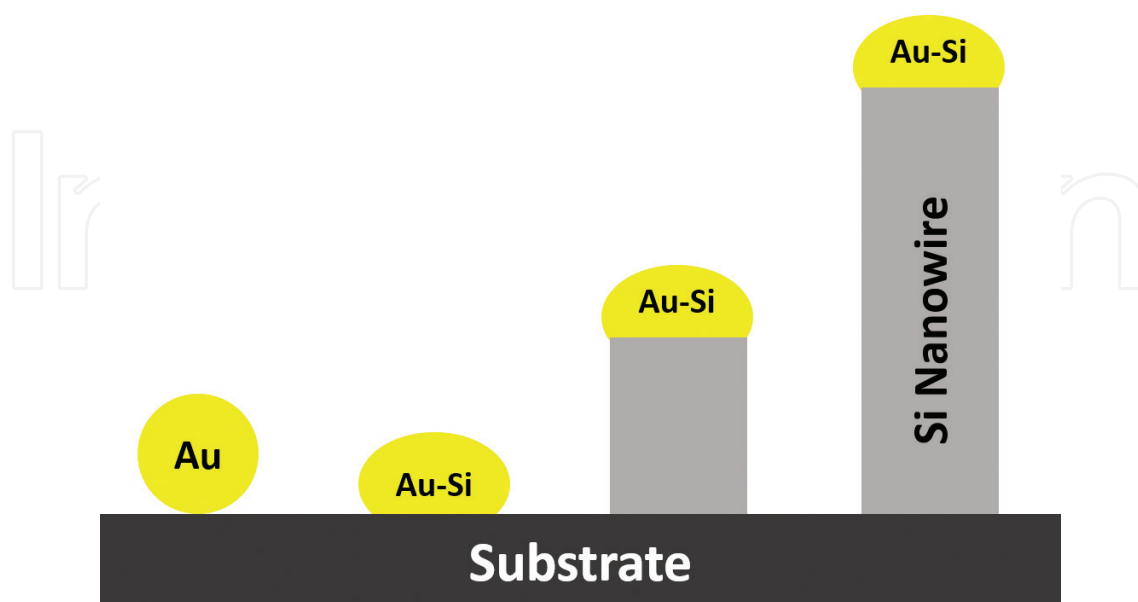


Figure 1. Schematic illustration of the VLS mechanism for Si nanowire synthesis using Au nanoparticle as catalyst.

VLS mechanism. The Au particles catalyze the gas precursor (e.g. SiH_4) and reacts with the Si atoms from the vapour phase, forming Au-Si eutectic droplets. Si was introduced from the vapour and adsorbed onto the liquid surface, then diffused into the droplet leading to a supersaturated state where the Si atoms precipitate and the nanowire starts nucleating. In the growth, the droplet serves as the “seeds” limiting the lateral growth of individual nanowires, and the droplet size remains unchanged during the growth which determines the diameter of the subsequent nanowires.

The VLS process has become a widely used growth method for one-dimensional nanostructures of a broad variety of materials. In addition to elemental semiconductors such as Si and Ge, binary compounds including III-V semiconductors (e.g. GaN, GaAs and InAs), oxides (e.g. ZnO, SiO_2 and ITO) and chalcogenides (e.g. Bi_2Se_3 , In_2Se_3 and CdS) have also been fabricated and studied in nanowire morphology following the VLS mechanism.

3.2. Silicon nanowire field-effect transistors

In this section, we review the fabrication and characterization of Si nanowire FETs prepared by using a self-alignment method based on VLS synthesis mechanism [42]. Unlike the traditional nanowire harvesting and alignment methods, the self-alignment approach not only enables simultaneous batch fabrication of reproducible and homogeneous nanowire devices of high quality, but also limits the contaminations of the nanowire during the fabrication process. The fabricated self-aligned Si nanowire FETs exhibit excellent current-voltage (I-V) characteristics, high on/off current ratio and small subthreshold slope providing an excellent platform for other devices and material investigations and applications.

3.2.1. FET fabrication

The Si nanowire FETs are fabricated using the directed self-alignment process as shown in **Figure 2**. The main concept of this fabrication approach is that Si nanowires are synthesized from Au catalysts on predefined locations as on wafers and well aligned with the source/drain and gate electrodes by photolithographic processes without harvesting the nanowires. At the first step of the fabrication process, a thin layer of Au catalyst (~ 1 nm) was deposited on the SiO_2/Si substrate and patterned by photolithography and lift-off processes. The Si nanowires were grown from the catalyst at the defined locations in a low-pressure chemical vapour deposition (LPCVD) furnace at 440°C for 2 hours with an ambient SiH_4 stream under a pressure of 500 mTorr. The nanowires are typically 20 μm in length and 20 nm in diameter. Immediately after the VLS growth, the Si nanowires were loaded in a dry oxidation furnace and oxidized at 750°C for 30 minutes in O_2 to form a ≈ 3 nm thick SiO_2 which was expected to provide a good interface between the nanowire and the subsequent top gate dielectric stack [42]. Photolithographic and lift-off processes were then performed to form the source and drain contacts. To facilitate proper contact formation, a 2% HF wet etch was applied to remove the oxides from the Si nanowires at the source/drain region before electrode metal (Al in this case) deposition. The next step is to deposit top gate dielectric (25 nm HfO_2) by ALD at 250°C , followed by a deposition of 5 nm of Al_2O_3 to improve the interface with the

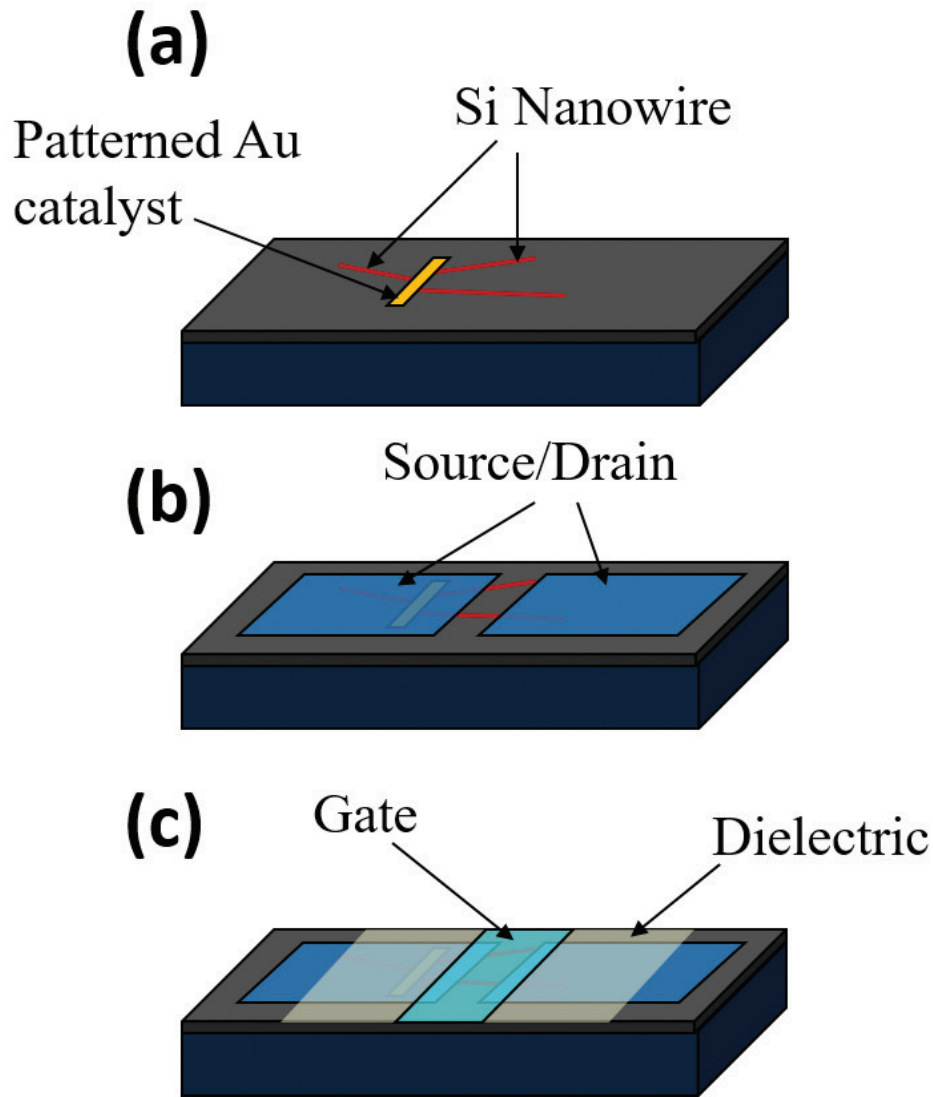


Figure 2. Self-alignment fabrication process: (a) patterned Au catalyst on SiO₂; (b) synthesis of Si nanowire from the Au catalyst, nanowire oxidation and alignment of source/drain contacts; (c) deposition of gate dielectric and pattern of top gate electrode [42].

Al top gate which was formed by the same lift-off process as of the source/drain electrodes. The final devices were annealed in forming gas (5% H₂ in N₂) at 325°C for 5 minutes to reduce the interface trap density between the nanowire and dielectric layer, as well as to improve the contact between the Al metal to the Si nanowire and HfO₂. **Figure 3** shows the top-view scanning electron microscopy (SEM) image of a finished self-aligned Si nanowire FET with gate length of 2 μm.

3.2.2. Electrical characterizations

Si nanowire FET with single or multiple nanowire channels is expected to exhibit better performance than planar bulk Si. The Gate-surrounding structure can be enabled allowing excellent electrostatic gate control over the channel for reduced short-channel effects.

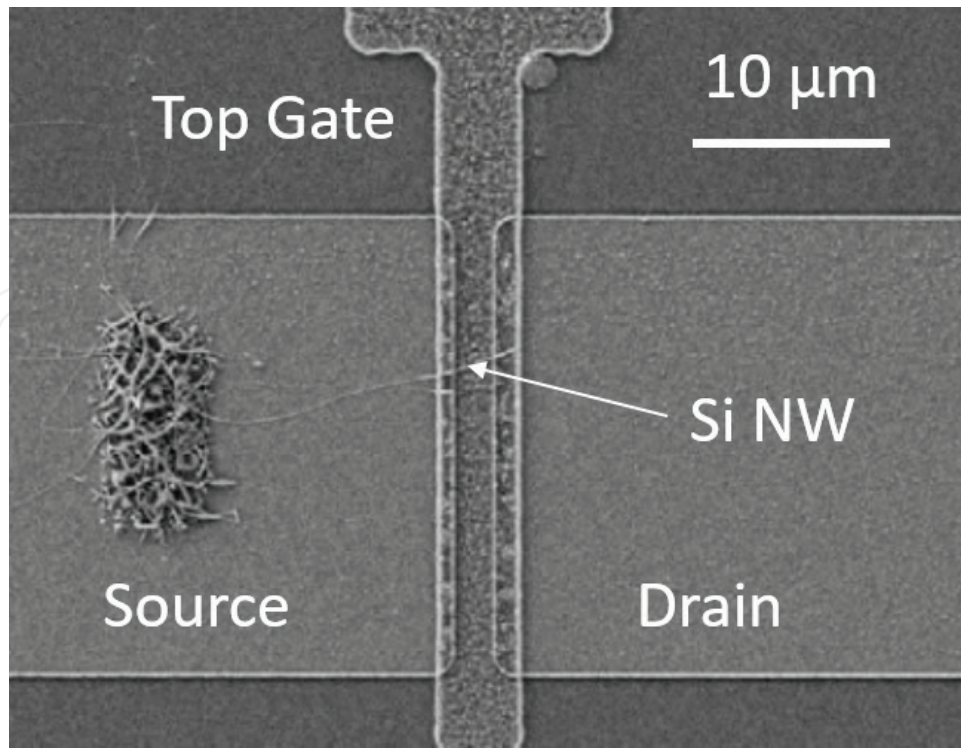


Figure 3. Top-view SEM image of a typical self-aligned Si nanowire FET with gate length of 2 μm [42].

The following equations define the minimum gate length to avoid short-channel effects for single-gate, double-gate and surrounding-gate structures:

$$\lambda_{\text{single-gate}} = \sqrt{\frac{\epsilon_{\text{Si}} t_{\text{ox}} t_{\text{Si}}}{\epsilon_{\text{ox}}}} \quad (1)$$

$$\lambda_{\text{double-gate}} = \sqrt{\frac{\epsilon_{\text{Si}} t_{\text{ox}} t_{\text{Si}}}{2 \epsilon_{\text{ox}}}} \quad (2)$$

$$\lambda_{\text{surrounding-gate}} = \sqrt{\frac{2 \epsilon_{\text{Si}} t_{\text{Si}}^2 \ln\left(1 + \frac{2 t_{\text{ox}}}{t_{\text{Si}}}\right) + \epsilon_{\text{ox}} t_{\text{Si}}^2}{16 \epsilon_{\text{ox}}}} \quad (3)$$

where t_{Si} , ϵ_{Si} , t_{ox} and ϵ_{ox} are the thickness and permittivity of Si and gate oxide, respectively [43]. The above equations demonstrate that the surrounding gate structure offers the best characteristics for controlling the short-channel effects.

Figure 4a and **b** shows the output characteristics of a self-aligned Si nanowire FET in both linear and logarithmic scale. From the drain current (I_{DS}) versus drain voltage (V_{DS}) curves, the leakage-affected region, weak, moderate and strong inversion operation regions of the FET are clearly shown in **Figure 4b**. In the weak inversion region, I_{DS} increases exponentially with gate voltage (V_{GS}) due to the diffusion of carriers (holes) and is saturated at $3 \phi_t$ ($\sim 78 \text{ mV}$ at room temperature, $\phi_t = kT/q$ is the thermal voltage). In moderate inversion region, I_{DS} varies by a couple of orders of magnitude, changing gradually from one form of functional dependence to the other. In strong inversion region, I_{DS} approximately follows the quadratic law

and is proportional to $(V_{GS} - V_{TH})^2$ with saturation at $V_{DS} = V_{GS} - V_{TH}$. These curves demonstrate that the self-aligned Si nanowire FET has similar electrical behaviours to those of conventional MOSFETs, even though it has much simpler device structure and no source/drain junction doping. It should be noted that the I_{DS} - V_{DS} curves increase sharply in the linear region, indicating a small source and drain contact resistance.

Due to the Schottky contacts between the Al contacts and the intrinsic Si nanowire, Schottky-barrier pMOSFET characteristics are expected for these FETs. **Figure 5** shows typical transfer characteristics of self-aligned Si nanowire FET with V_{DS} of -50, -100 and -150 mV, respectively.

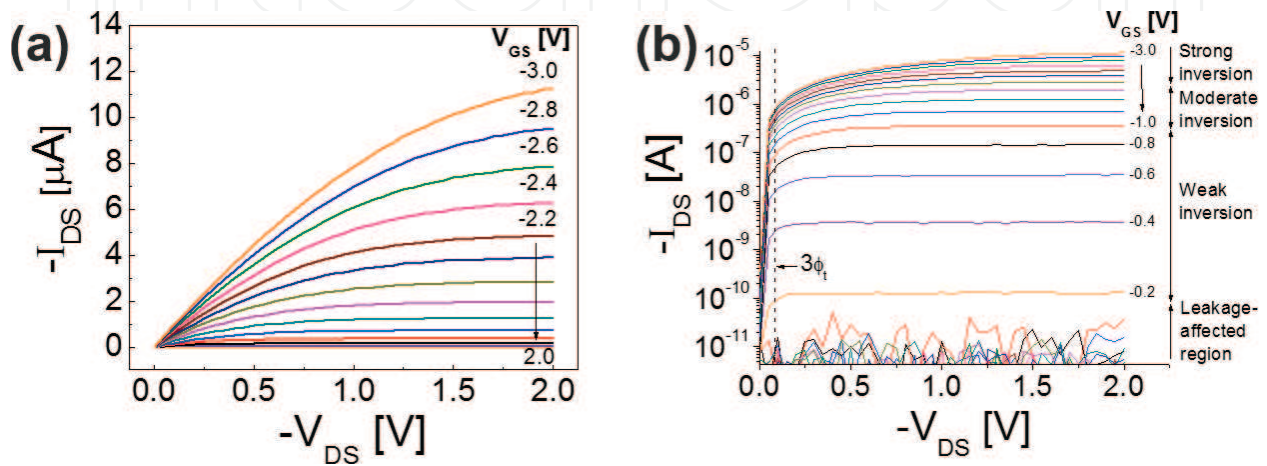


Figure 4. Output characteristics of the self-aligned Si nanowire FET in (a) linear and (b) logarithmic scale [42].

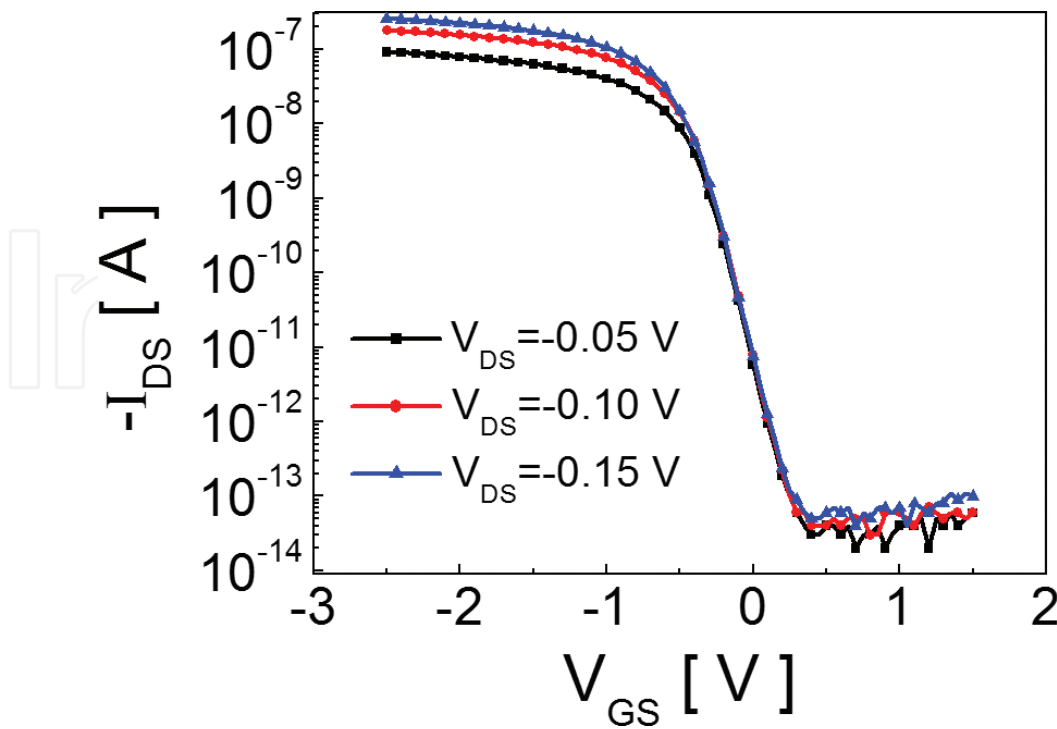


Figure 5. Transfer characteristics of the Si nanowire FET, with V_{DS} value of -50, -100 and -150 mV, respectively [42].

The on/off current ratio is $\sim 10^8$ within a 1.2 V V_{GS} window and no ambipolar behaviour is observed. The carrier mobility can be calculated from the linear region of the transconductance when $V_{DS} = -50$ mV with a presumed diameter of 20 nm for the nanowire channel. The calculated results show that the fabricated Si nanowire FETs have a relatively consistent hole mobility around 100 cm²/Vs. The subthreshold swing (SS) can be extracted from the subthreshold region of I_{DS} in the log-scale I_{DS} - V_{GS} curves. The SS values of the Si nanowire FETs are as low as 75 mV/dec, which is quite small as compared to most reported results on nanowire FETs and poly-Si thin-film transistors [42].

The Si nanowire FETs fabricated through the self-alignment approach exhibit excellent performance as indicated by a high on/off current ratio ($\sim 10^8$), small leakage current ($< 10^{-14}$ A), good carrier mobility (~ 100 cm²/Vs) and small subthreshold slope (75 mV/dec). These excellent characteristics are due to the clean interfaces formed in the self-alignment fabrication process, and such Si nanowire FETs are very attractive for future nanoelectronic device applications.

4. Silicon nanowire-based flash-like non-volatile memory

4.1. Introduction of flash-like non-volatile memory

Today, computing architectures and electronic systems built on CMOS components are still pursuing without any sign of slowing down of requirements for low power, fast speed and high density alternatives. Up to now, electronic systems whose main function is to focus on date computing and storage take up more than half of the semiconductor market, and the demand is still growing explosively in areas such as portable electronic devices and systems. Solid-state mass storage occupies a large portion of this market, due to their compatibility with CMOS scaling technology, suitability for harsh environment without mechanical parts and the fact that most types of memory are non-volatile.

Non-volatile memory is typically employed for the task of secondary storage or long-term storage, which usually does not require fast operation speed or integration density. The current primary storage or on-chip memory still relies upon volatile forms of random-access memory. During the past decades, the size of cache memory in the central processing unit (CPU), which is also known as the static random-access memory (SRAM) has been doubled several times as a feasible strategy to increase the CPU capability. However, increasing SRAM will decrease CPU net information throughput because it is volatile and occupies a large chip floor space. Thus, it will be a revolutionary breakthrough in microelectronics if a truly non-volatile memory can be implemented as the on-chip memory in CPUs replacing SRAM.

4.1.1. Basic memory concepts and scaling challenges

Among all the non-volatile memory candidates for primary storage applications, flash memory is the most widely studied and electrically accessible form and is the most promising non-volatile memory in the electronics market. Flash memory has fast read access times, good retention and reliability and CMOS compatible fabrication process [44–46].

Also known as the floating-gate memory (shown in **Figure 6**), a flash memory device stores the trapped electrons in the floating gate until they are removed by another application of electrical field. Because the floating gate is insulated from the control gate and the MOSFET channel by a relatively thick blocking oxide and a thin tunnelling oxide, respectively, the trapped electrons can be retained for many years, and logical “0” and “1” states can be defined according to the presence or absence of electrons trapped in the floating gate. In the past years, the flash capacity, integrated density and performance have been continued to increase with lower manufacturing cost. Due to its compatibility with conventional CMOS process, it is easier and more reliable to integrate flash memory than other forms of non-volatile memory in logic and analog devices with increasing embedded and stand-alone memory to achieve higher chip performance.

However, current flash memory also exhibit disadvantages such as relatively slow write/erase speed and medium endurance, which make it far below the standards of on-chip memory applications. In a conventional floating-gate memory, the tunnelling oxide can hardly be scaled below 7 nm due to the requirement of data retention. Moreover, ultra-thin tunnelling oxide will lead to severe stress-induced leakage current (SILC) issue. On the other hand, the conventional floating-gate materials, poly Si and oxynitride operate at large programming voltages and endure only 10^5 operation cycles. Even though some new flash technologies are promising for low-voltage operations, the voltage supply is in excess of the working voltage standard of the advanced processes, and the gap between the operation voltage of memory device and CMOS logic continues to be broadened.

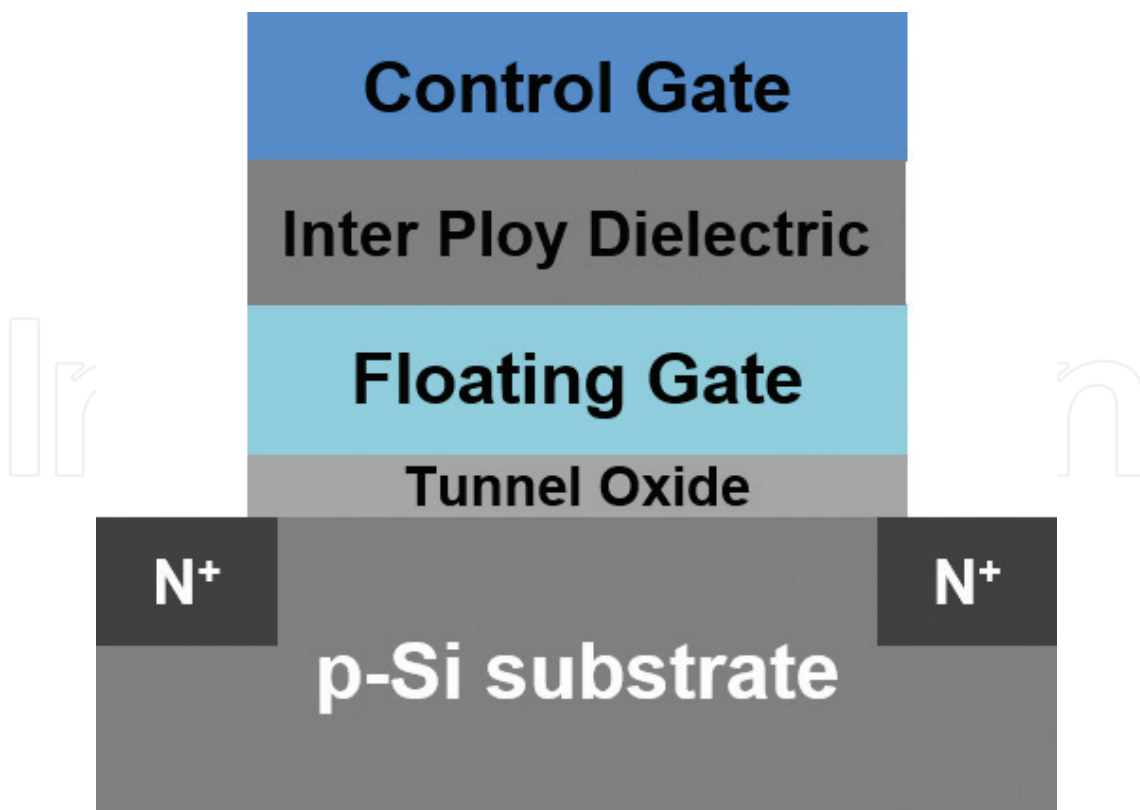


Figure 6. Schematic diagram of a floating-gate flash memory.

4.1.2. SONOS type charge-trapping memory

In recent decades, polysilicon-oxide-nitride-oxide-silicon (SONOS) type charge-trapping non-volatile memory has attracted intensive attention to replace the conventional floating-gate memory due to their advantages such as lower consumption, better reliability and scalability, and simpler structure and fabrication process [47–49]. **Figure 7** demonstrates the schematic structure of a SONOS charge-trapping memory, in which the electrons tunnel through the tunnelling layer and stored in the nitride layer. However, the conventional charge-trapping materials in SONOS memory are not compatible with the dimensional scaling and lead to poor performance in speed, retention and endurance. Furthermore, to achieve faster speed, the tunnelling oxide must be shrinking to enhance the electric field across it while the blocking oxide should be thicker to suppress the leakage current. But thinner tunnelling layer may in turn cause poor stability and reliability, and thicker blocking layer requires larger working voltages. Great efforts have been made for good memory characteristics via various approaches to gain a trade-off between speed and data retention. An effective strategy is to use non-planar channel such as nanotubes and nanowires, to enhance the gate control over the channel. Compared to planar devices based on bulk materials, the nanowires have larger surface-to-volume ratio, therefore, it requires less stored charges to induce the same memory window for nanowire-based flash memory.

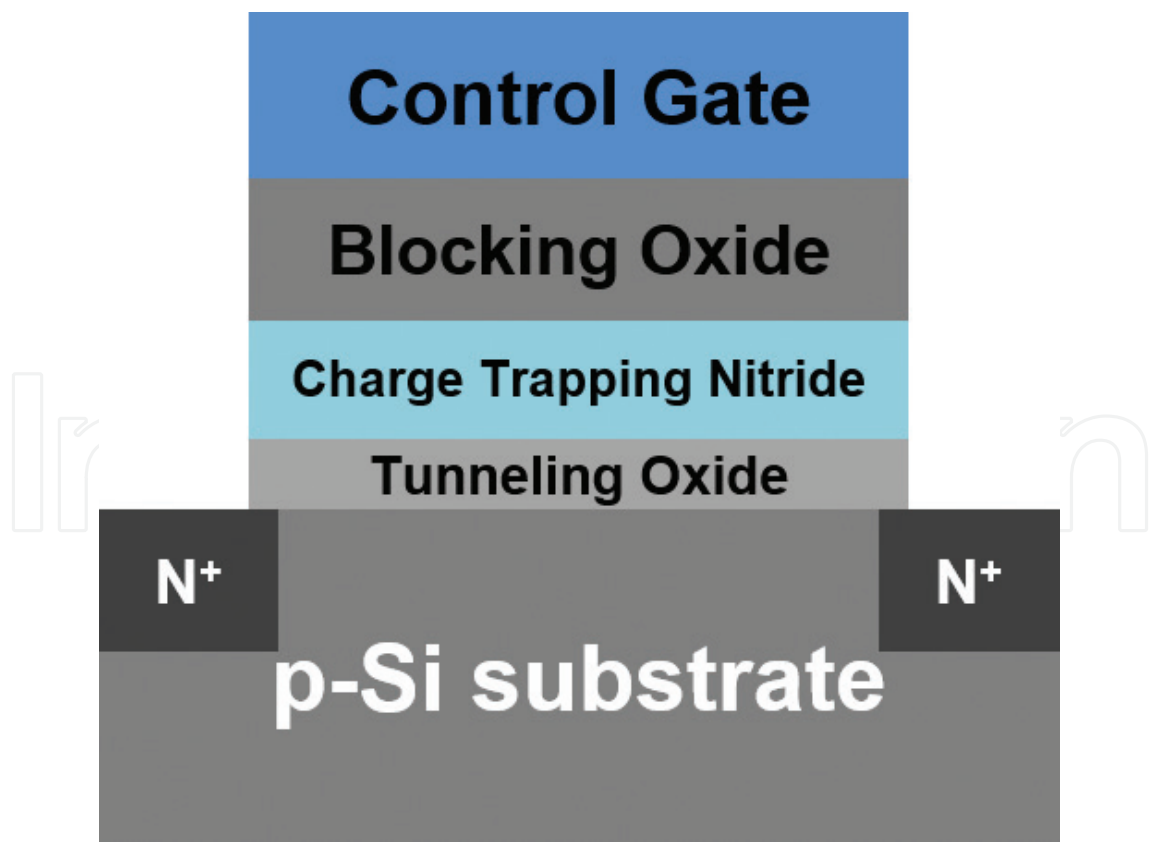


Figure 7. Schematic diagram of a SONOS-type charge-trapping flash memory.

The following in this section reviews the work on the device engineering of flash memory with novel dielectric materials and redox molecules as charge trapping medium based on the Si nanowire FETs. As compared with planar structure memory device, much better performances have been achieved by utilizing the one-dimensional nanowire channel in the memory devices.

4.2. Silicon nanowire-based dielectric charge-trapping memory

4.2.1. History of one-dimensional nanostructure based charge-trapping memory

The first non-volatile memory cell was demonstrated in 2002 by Fuhrer et al. with one-dimensional nanostructure as the active channel component based on carbon nanotube [50]. Sufficient memory window was witnessed, and Fuhrer et al. predicted that the charge detection of such narrow and high mobility nanotube FETs will outperform planar FET cells [50]. In 2003, Choi et al. reported a carbon nanotube based non-volatile memory with oxide-nitride-oxide (ONO) dielectric stack [51]. A high electric field was generated by 5 V top gate voltage surrounding the surface of 3 nm nanotube, which was sufficiently high to produce Fowler-Nordheim tunnelling.

In 2006, Cha et al. reported a non-volatile flash memory having GaN nanowires with SiO₂ as a charge trapping material, and the operation mechanism was also investigated [52]. It was reported that the electric field distribution in the gate dielectric was different at the centre and the edge beneath the gate. The field is uniform under the centre of the gate across the oxide, and the field distribution at the edge changes along the distance. Non-volatile memory cells based on Si nanowire with CMOS compatible gate dielectric were reported by Zhu et al. in 2011 [53]. HfO₂ was used for charge storage, the thickness of which does not affect the electric field across the tunnelling oxide. The programming speed and retention time have been significantly improved through the surrounding gate structure.

Various high-k materials such as Y₂O₃, Gd₂O₃ and ZrO₂ have been proposed and studied as charge-trapping layer for better reliability and speed [54–56]. Using thicker high-k dielectric with relatively larger band gap as the blocking oxide can be expected to lower the electric field across the blocking layer. Integration of novel dielectric materials as the gate stack in the nanowire FET architecture is therefore very promising to realize practical applications of flash memory with faster speed, higher density, smaller size and better reliability.

4.2.2. Device fabrication

The Si nanowire FET based dielectric charge-trapping flash memory is prepared by following the self-alignment method [57]. Typically, a 300 nm SiO₂ was first grown on Si substrate by dry oxidation. Then a thin film of Au catalyst (1–3 nm) was deposited on patterned area pre-defined by photolithography. Then the Si nanowires were grown from the catalyst following the VLS mechanism and were oxidized at 750°C for 30 minutes to form a \approx 3 nm SiO₂ which will function as the tunnelling layer. The 3/100 (unit: nm) Ti/Pt source and drain electrodes were then patterned with photolithography and deposited by e-beam evaporation. The channel length

between the source/drain electrodes was controlled to be 5 μm . The following process is the deposition of charge-trapping layer and blocking oxide dielectric. Different charge-trapping layer and stacks were fabricated— Ta_2O_5 , $\text{Ta}_2\text{O}_5/\text{Al}_2\text{O}_3/\text{Ta}_2\text{O}_5$ (TAT) and a reference HfO_2 , with thickness of 20, 6/8/6, 20 nm, respectively [57]. The blocking oxide for all memory devices was selected to be 25 nm for Al_2O_3 . Ta_2O_5 was deposited by sputtering, whereas Al_2O_3 and HfO_2 layers were deposited by ALD with TMA and TEMA as precursors, respectively. Finally, a 100 nm Pd top gate was formed by the same photolithographic and lift-off processes as the source/drain electrodes.

4.2.3. Characterization and performance discussion

Three SONOS-like charge-trapping flash memory devices with structures of metal/ Al_2O_3 / Ta_2O_5 / Al_2O_3 / Ta_2O_5 / SiO_2 /Si (MATATOS), metal/ Al_2O_3 / Ta_2O_5 / SiO_2 /Si (MATOS) and metal/ Al_2O_3 / HfO_2 / SiO_2 /Si (MAHOS) have been fabricated and electrically characterized [57]. **Figure 8** shows the schematic top view and a cross-sectional transmission electron microscope (TEM) image of a MATATOS device.

Typical output characteristics ($I_{\text{DS}}-V_{\text{DS}}$) of the self-aligned Si nanowire FET based flash memory are shown in **Figure 9a** (MATATOS) with smooth and well-saturated drain current curves and a small source and drain contact resistance. **Figure 9b–d** shows the transfer characteristics of the three memory devices with counterclockwise hysteresis loops suggesting the charging and discharging behaviour. By comparing the memory window, the MATATOS and MATOS devices show larger values than the MAHOS device [57].

The programming and erasing (P/E) operations on the MATATOS memory were measured by studying the threshold voltage shift (ΔV_{th}) under different P/E operations and were

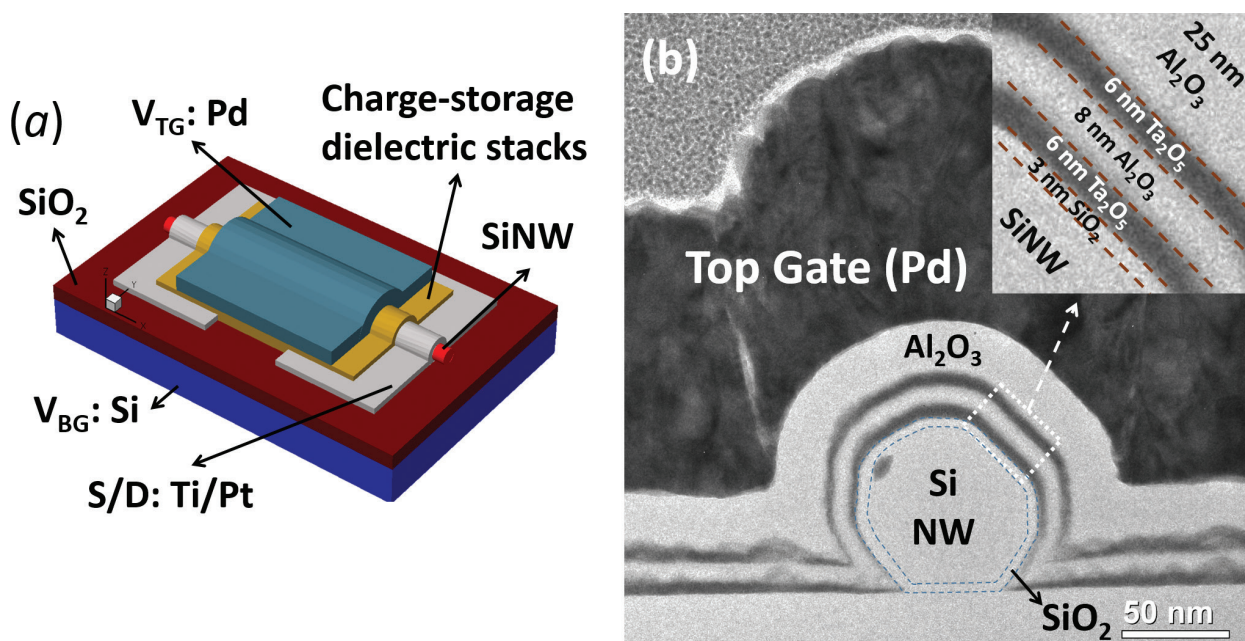


Figure 8. (a) Schematic of top-view of the dielectric charge-trapping flash memory based on Si nanowire FET; (b) cross-sectional TEM image of the dielectric flash memory with TAT charge-trapping layer [57].

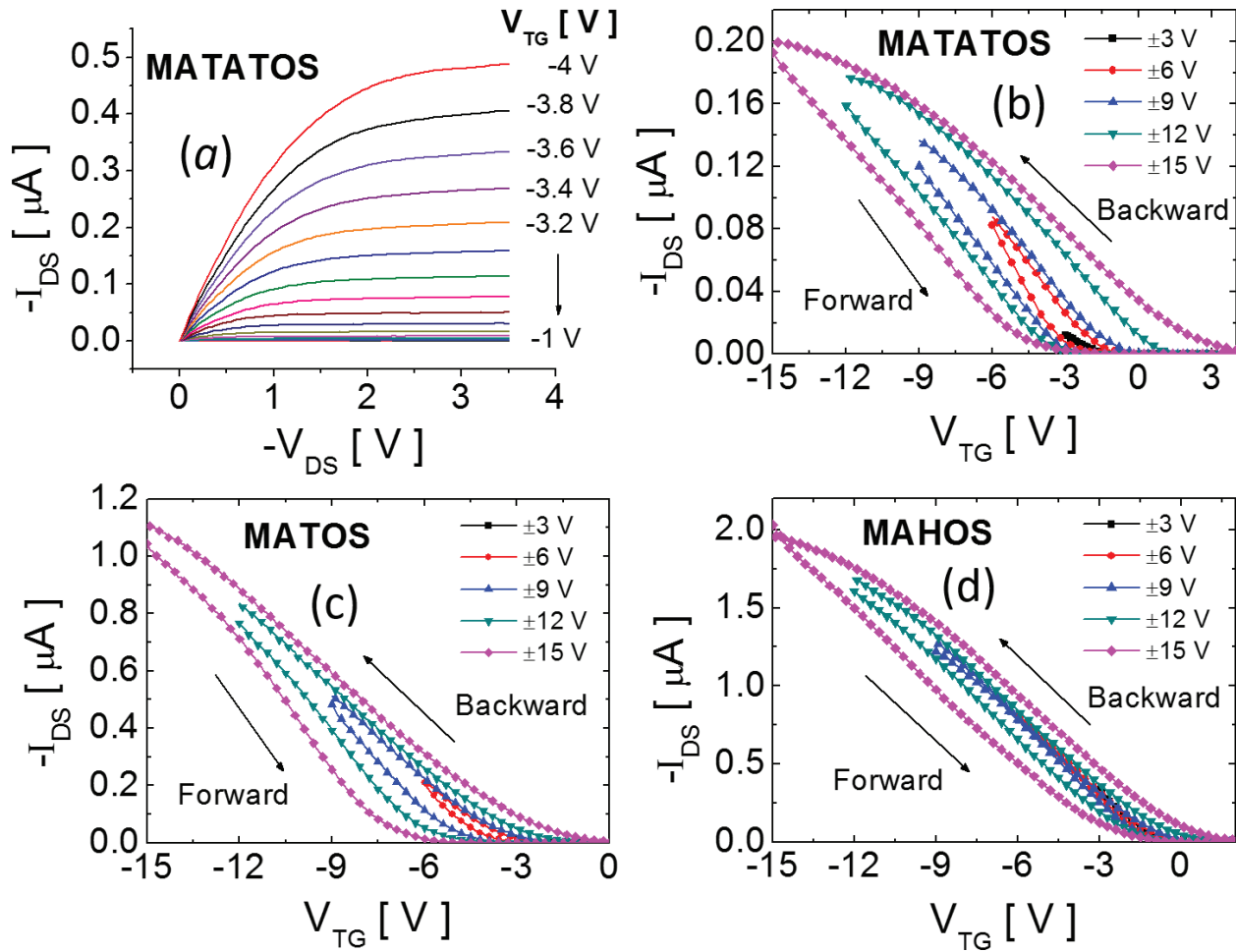


Figure 9. (a) Output characteristics of MATATOS device for V_{GS} from -4 to -1 V with 0.2 V step; transfer characteristics of (b) MATATOS, (c) MATOS, and (d) MAHOS devices, showing counterclockwise hysteresis loops under different V_{GS} sweep ranges [57].

illustrated in **Figure 10**. The $I_{DS}-V_{GS}$ curves show clear ΔV_{Th} under accumulative rectangular gate voltage pulses but exhibiting same subthreshold slope (~ 300 mV/dec) before and after the programming or erasing operations. This indicates that the ΔV_{Th} is due to the fixed charges in the charge-trapping layers instead of the interface states. By stressing a positive gate voltage, the electrons will tunnel through the tunnelling oxide from the Si nanowire and get trapped in the charge-trapping layers. This corresponds to the programming operations, which will result into a V_{Th} shift towards the positive direction. Negative gate voltage will reversely shift the V_{Th} in the opposite direction by removing the pre-trapped electrons from the charge-trapping layer to the Si nanowire. This is defined as the erasing operations. By comparing the ΔV_{Th} under different P/E gate voltages, it was found that both MATATOS and MATOS devices showed faster speed than the MAHOS device, and MATOS device showed a larger ΔV_{Th} for a long P/E time due to the thicker charge-trapping layer.

Figure 11a shows the charge retention properties of the devices. Less than 25% charge loss was observed for both MATATOS and MATOS devices. **Figure 11b** demonstrated the

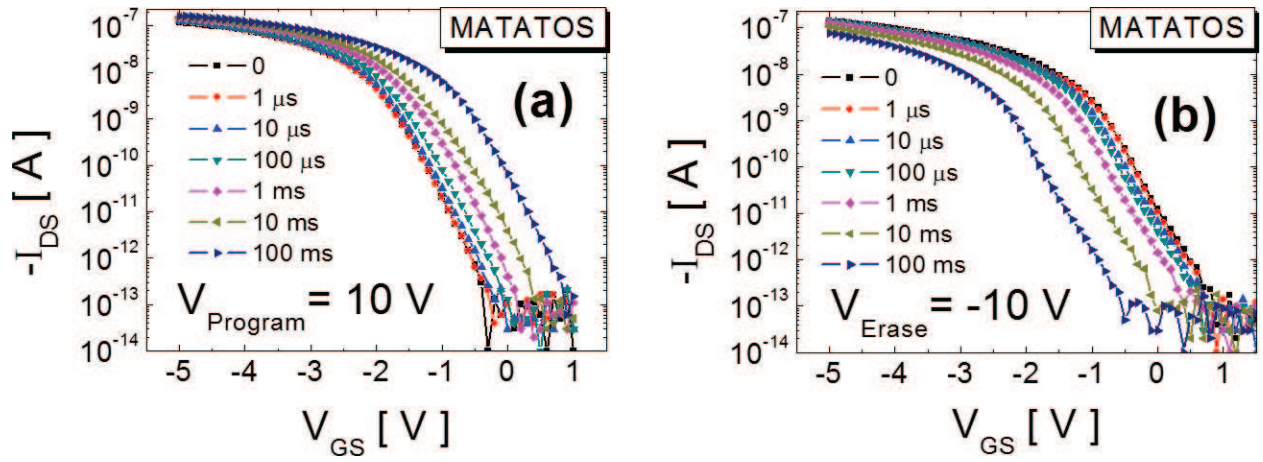


Figure 10. (a) Programming and (b) erasing operations with accumulated P/E time at ± 10 V gate voltage pulses on the MATATOS flash memory device [57].

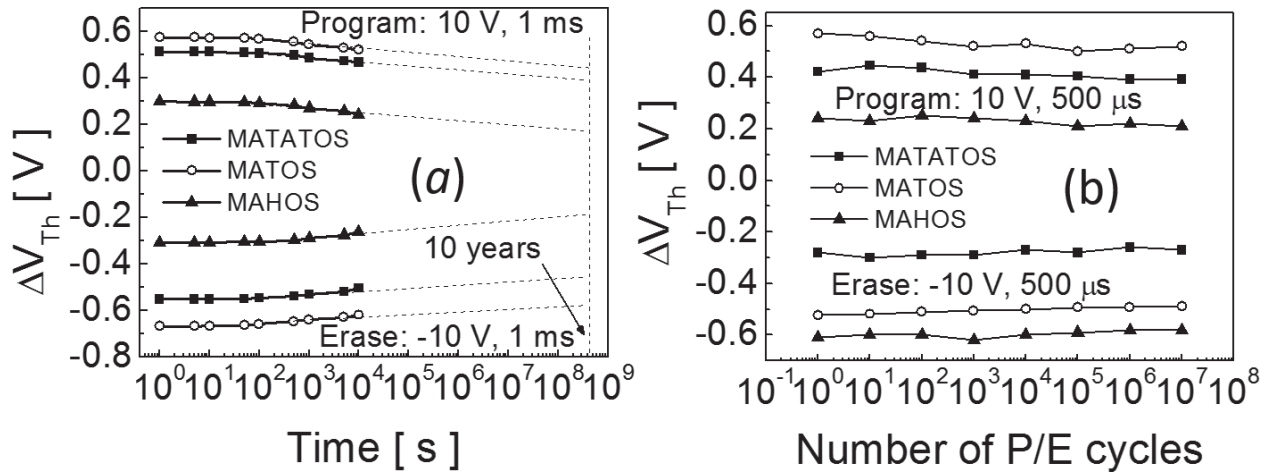


Figure 11. (a) Retention and (b) endurance characteristics of three flash memory devices [57].

endurance properties of the three devices. Very small memory window degradations were observed for all the devices after 10^7 P/E cycles. Such good endurance behaviour arises from the good interface between the Si nanowire and the high-k stacks formed in the self-alignment fabrication process.

The design of the TAT charging-trapping stack with an Al_2O_3 layer sandwiched between two Ta_2O_5 layers is for the multiple charge storage, in which the Al_2O_3 layer functions as the blocking oxide for the first Ta_2O_5 layer and tunnelling oxide for the second Ta_2O_5 layer. As shown in **Figure 12**, clear two-step charging behaviour is successfully observed in the MATATOS device. The first step around 10 V gate voltage is due to the charge storage in the first Ta_2O_5 layer, and the second step at around 20 V is observed indicating the charge-trapping centres in both Ta_2O_5 layers have been filled with electrons. The charge density of the two Ta_2O_5 layers are calculated to be 1.75×10^{19} and $4.98 \times 10^{19} \text{ cm}^{-3}$, respectively.

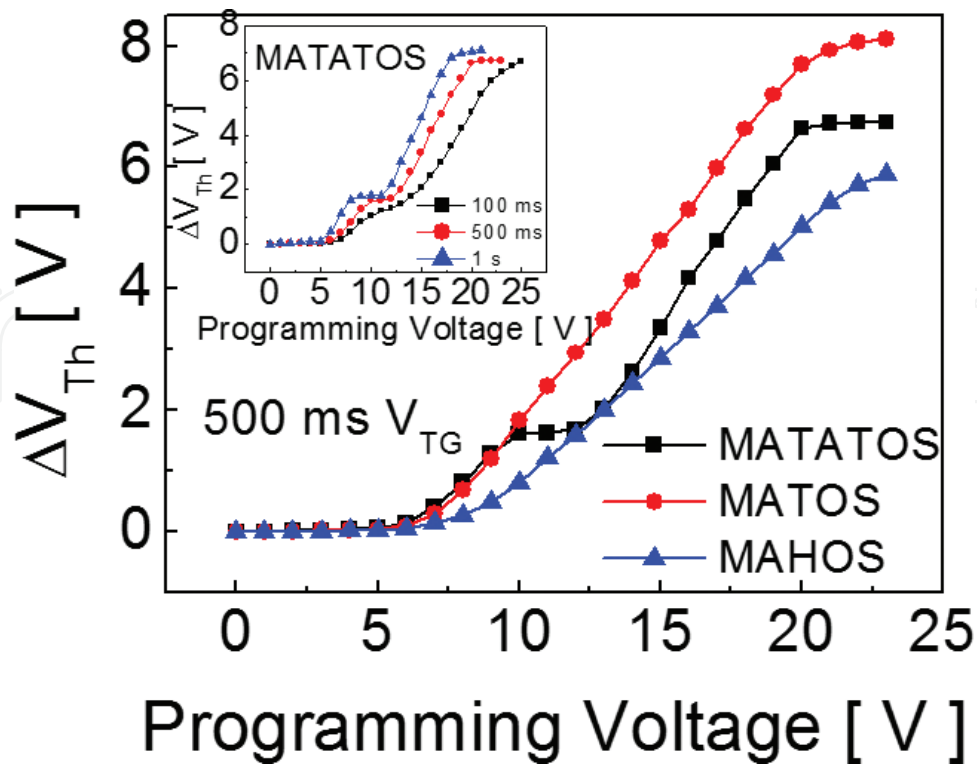


Figure 12. ΔV_{Th} as a function of programming voltage of the three devices. MATATOS device shows a two-step charging storage behaviour. Inset: ΔV_{Th} versus programming voltage of the MATATOS device under gate voltage pulse with different width [57].

By comparing the above results from the flash memory based on Si nanowire FET to the electrical performance of planar capacitor structure with same gate dielectric stack, the nanowire FET-based flash memory exhibits faster speed, better endurance and more remarkable discrete multi-bit memory storage at lower operation voltages [58]. The scaling from planar Si to nanoscale Si nanowire channel effectively enhance the gate electric field introduced by the gate-surrounding structure, enabling faster speed and lower operation voltage. The device reliability is improved with the clean nanowire surface and dielectric interfaces formed by using the self-alignment technique. Such a high-performance and CMOS compatible flash memory is very attractive for future multi-bit non-volatile memory applications.

4.3. Silicon nanowire-based molecular charge-trapping memory

4.3.1. Introduction of redox-active molecules

CMOS and semiconductor non-volatile memory scaling have generated various approaches towards building memory devices with higher scalability and better performance. The hybrid silicon/molecular approach is very attractive as a technology that leverages advantages afforded by a molecule-based active medium with the vast infrastructure of traditional MOS technology.

In reduction-oxidation, redox-active molecules can be attached on various surfaces such as Si and SiO₂ by forming a self-assembled monolayer (SAM) or multiple layers with simple and low-cost processes. Due to the inherent reduction and oxidation of the redox centres, such molecules can exhibit distinct charged and discharged states which can represent the logic on and off states. It has been demonstrated that the redox-active molecules attached on Si structures are stable and can endure more than 10¹² P/E cycles [59]. Such an excellent reliability is derived from the intrinsic properties of redox molecules. Thus, incorporating redox-active molecules as charge-storage medium in a Si-based flash memory is quite interesting. By taking advantage of the high-quality thin oxide surrounding the Si nanowire, which is readily feasible in various chemical functionalizations, a molecular flash memory with redox molecules attached on the Si nanowire surface serving as the charge storage medium can have even better memory performance including lower operation voltage, faster speed, better device scalability and better reliability.

4.3.2. Redox-active molecules attachment and memory device fabrication

Two redox-active molecules were integrated and studied in the molecular flash memory: α -ferrocenylethanol (referred as ferrocene) and Ru₂(ap)₄(C₂C₆H₄P(O)(OH)₂) (referred as Ru₂), in which ap = 2-anilinopyridinate, with the molecular structures shown in **Figure 13** [60].

The molecular flash memory device fabrication follows the self-alignment Si nanowire FET process as well. After the catalyst patterning, nanowire growth and oxidation and source/drain electrode formation, the molecules SAM attachment on the nanowire was performed by placing droplets of a solution of dichloromethane with 3-mM ferrocene and 2 mM Ru₂ on the active areas separately [60]. Each drop was in place for 3–4 minutes and the samples were held at 100°C in an N₂ environment during the attachment. Saturated SAM will be formed after ~30 minutes. After the self-assembly process, dichloromethane was used to rinse the substrates to remove any residual molecules that are not bonded to the SiO₂ surface. Then, the samples were immediately loaded into the ALD chamber for a deposition of 25 nm Al₂O₃ with TMA and H₂O as precursors at 100°C. Finally, a 100 nm Pd top gate was formed with photolithographic and lift-off processes. A reference sample without molecules was fabricated for comparative study.

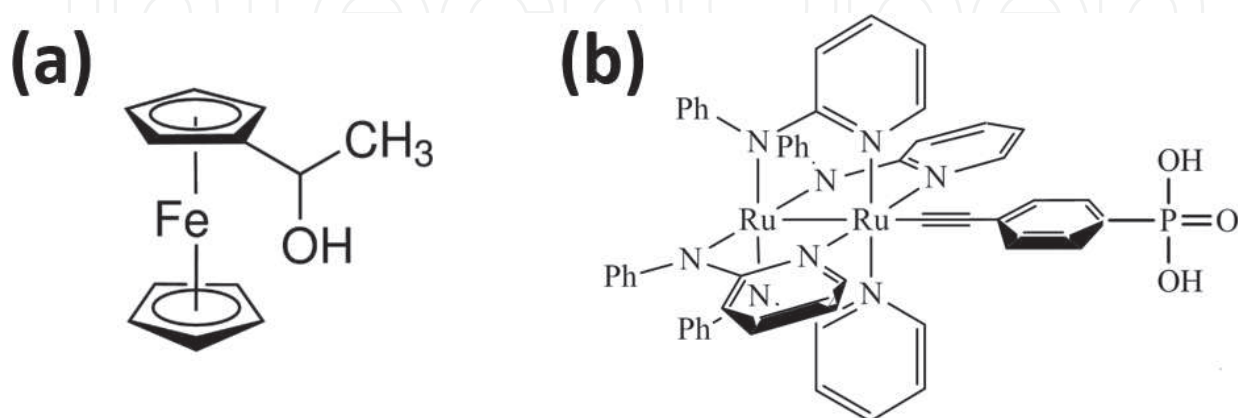


Figure 13. Molecular structure of (a) α -ferrocenylethanol and (b) Ru₂(ap)₄(C₂C₆H₄P(O)(OH)₂) [60].

4.3.3. Electrical characterization and memory performance

Schematic structure of a completed molecular flash memory device was shown in **Figure 14a**. **Figure 14b** shows the TEM image of the cross-section of a ferrocene-attached molecular flash memory. A clear gate surrounding structure has been obtained, with an “intermixed” region observed (indicated by the red dash line). Schottky-barrier p-type MOSFET characteristics have been observed for the Si nanowire based molecular flash memory cells as the source/drain was engineered as Schottky junction. **Figure 15a** and **b** shows the output characteristics of a typical ferrocene molecular flash memory. Smooth and well saturated $I_{DS}-V_{DS}$ curves have been observed with clear leakage-affected region and the weak, moderate and strong inversion operation regions. From the $I_{DS}-V_{GS}$ curves shown in **Figure 15c** and **d**, counterclockwise hysteresis loops were obtained for both devices, suggesting the charge trapping mechanism. The log-scale transfer characteristics shown in the insets demonstrated an on/off ratio as high as $\sim 10^7$. The inset (ii) in **Figure 15c** shows the $I_{DS}-V_{GS}$ curves of the reference sample (without molecules), and a negligible memory window was observed, ruling out the possibility of charge storage in the Al_2O_3 dielectric traps.

The P/E speed characterizations of the ferrocene flash memory were shown in **Figure 16a** and **b**. Threshold voltage shift towards the positive (negative) direction was observed during the programming (erasing) operations, indicating the electrons (holes) were injected from the Si nanowire through the SiO_2 and stored in the centres of the molecules. From **Figure 16c** and **d**, both molecular memory devices showed fast P/E speed, which arises from the intrinsic fast speed of the charging behaviour of the molecules and the strong electric field induced through the top gate control over the channel in the gate-surrounding structure.

Similar to the multiple charging behaviour demonstrated in the previous dielectric flash memory, the Ru_2 molecular flash memory is also designed and expected for the application

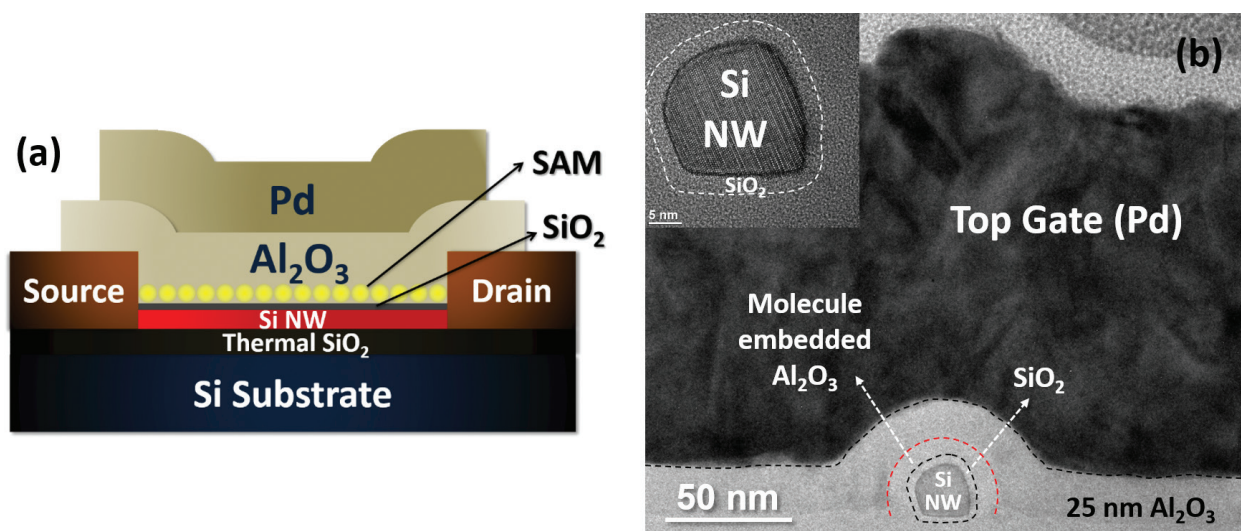


Figure 14. (a) Schematic structure of a completed molecular flash memory device based on Si nanowire FET; (b) TEM image of the cross section of a ferrocene-attached molecular flash memory. The red dashed line indicates the ferrocene-embedded Al_2O_3 region. Inset: Cross section of the nanowire channel, with SiO_2 layer indicated by the dashed line [60].

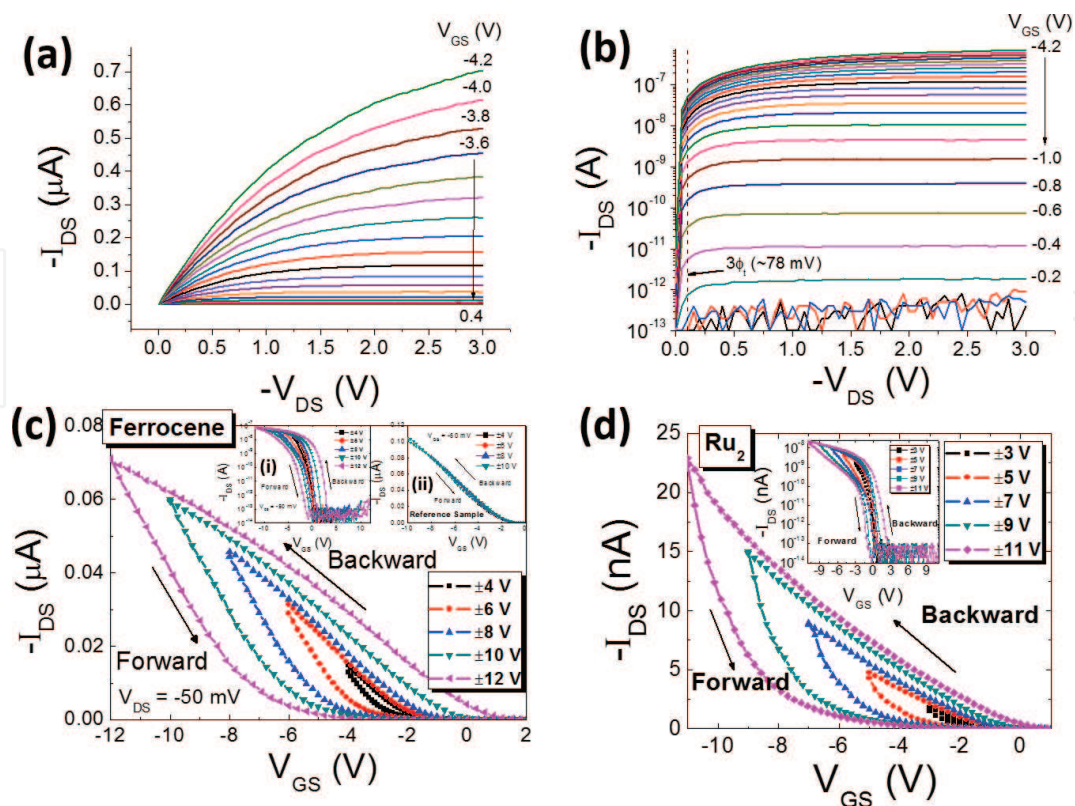


Figure 15. (a) Linear and (b) log-scale output characteristics of ferrocene molecular flash memory; I_{DS} - V_{GS} of the (c) ferrocene and (d) Ru_2 molecular flash memory with the insets showing the log-scale transfer curves. Inset (ii) in (c) shows the I_{DS} - V_{GS} curves of the reference sample with negligible hysteresis observed [60].

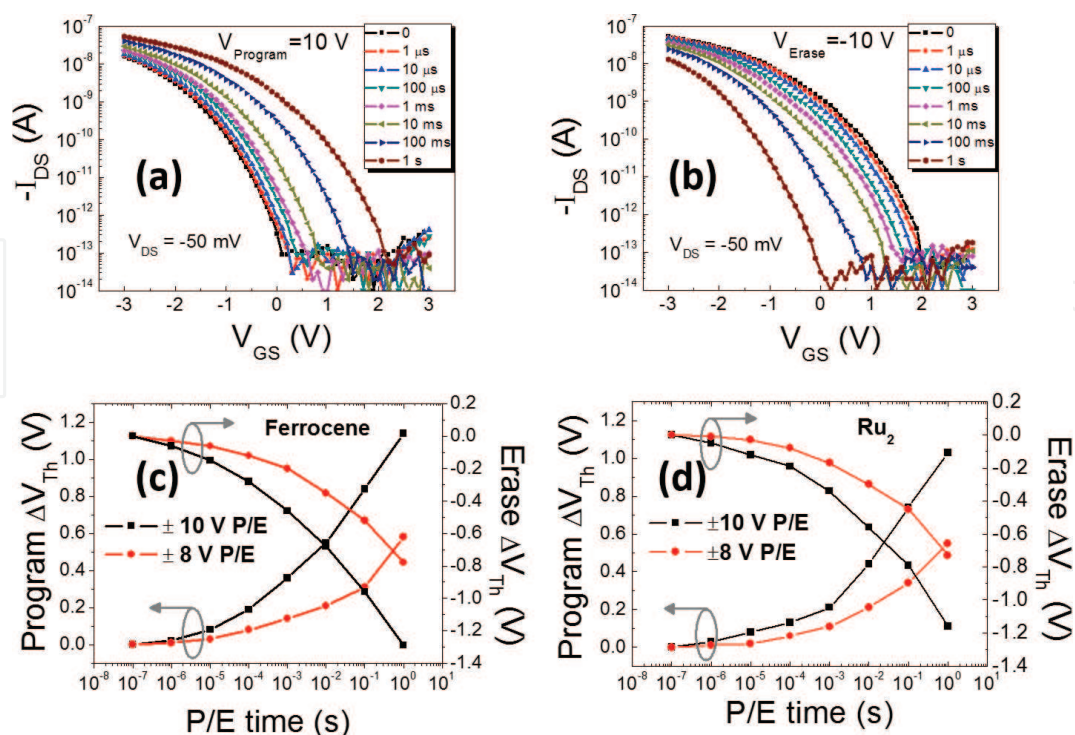


Figure 16. (a) Programming and (b) erasing operations of the ferrocene molecular memory under accumulative rectangular P/E gate voltage pulses. Speed characterizations of the (c) ferrocene and (d) Ru_2 molecular flash memory [60].

of multi-bit memory storage due to the two redox centres, which can exhibit stable and distinct charged states at different voltage levels [57, 60]. As shown in **Figure 17b**, two charged steps were observed at around 10 and 14 V, respectively. The overall charging density of the Ru₂ SAM was calculated to be $1.12 \times 10^{13} \text{ cm}^{-2}$, which is sufficiently high for discrete multi-bit memory applications. One of the most intriguing features of a molecular flash memory is the reliability. **Figure 17c–f** shows the data retention and the endurance properties of the

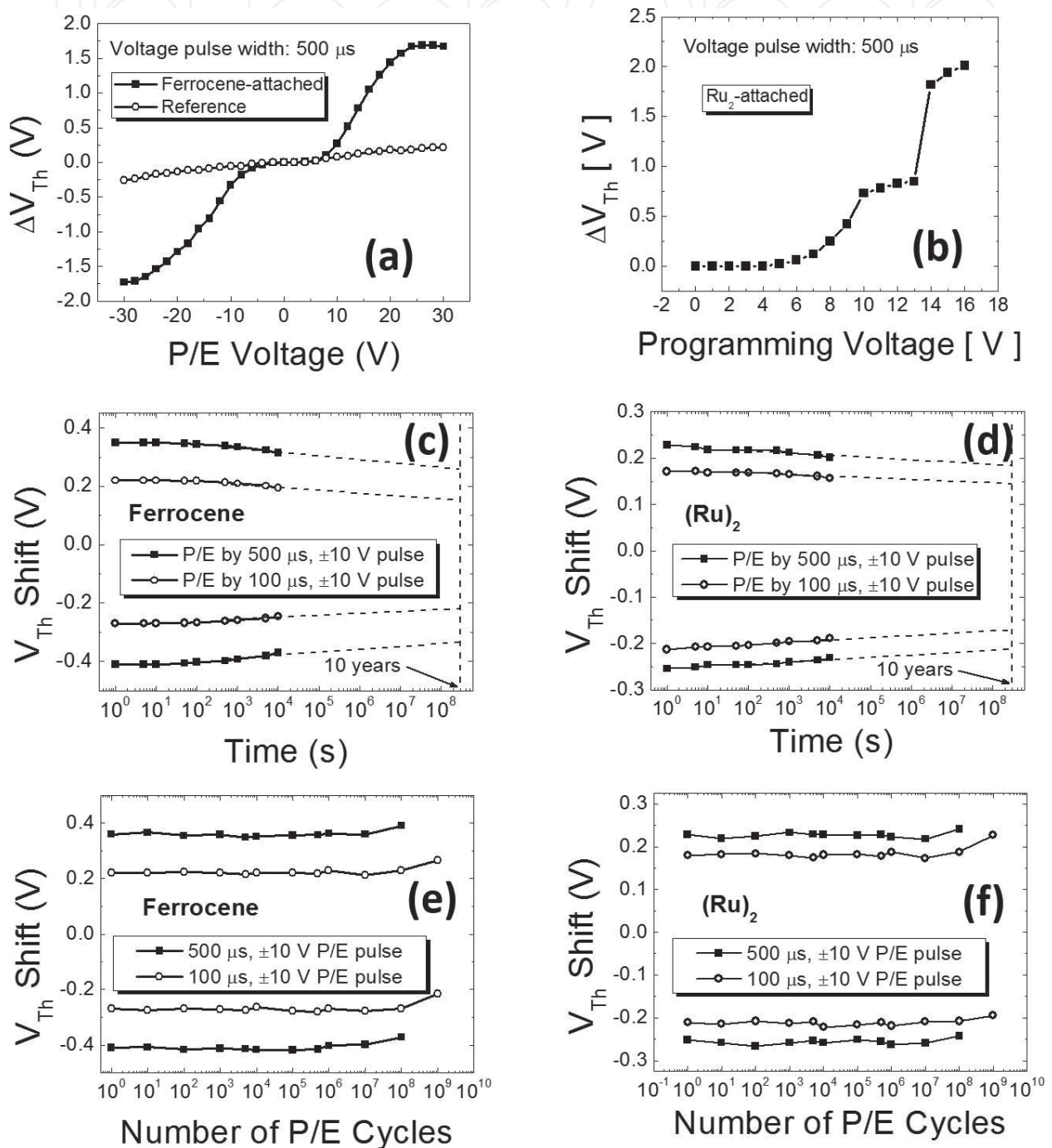


Figure 17. ΔV_{Th} of (a) ferrocene and reference sample and (b) Ru₂ flash memory as a function of P/E voltage. Room temperature retention characteristics of (c) ferrocene and (d) Ru₂ flash memory. Endurance properties of (e) ferrocene and (f) Ru₂ flash memory [60].

ferrocene and Ru₂ flash memory devices, respectively. The projected 10 year memory window showed a charge loss of only 20%, and the excellent endurance characteristics were demonstrated by the negligible memory window degradation after 10⁹ P/E cycles, which is about 10,000 times better than that of the conventional floating gate memory [60]. Such a good reliability is due to the intrinsic stable redox behaviour of the molecules and the high-quality tunnelling oxide with clean solid/molecule and dielectric interfaces by using the self-aligned nanowire FET fabrication process. The nanowire FET based molecular flash memory is thus very attractive for future fast speed, high-endurance and high-density on-chip non-volatile memory applications.

5. Nanowire field-effect transistor as a platform for novel materials research

Semiconductor nanowires have shown unique properties in the manner of both physics and technology. The significance of nanowires over planar materials has been more and more discovered and focussed through various interesting and fundamental phenomena, when nanowires have nanoscale diameter at or even below the characteristic length scale of such basic parameters as phonon mean free path, exciton Bohr radius, magnetic domain size, exciton diffusion length and so forth [61]. Many physical properties of semiconductor nanowire are utterly different from the planar bulk materials due to the confines of nanowire surface. Moreover, the large surface-to-volume ratio of nanowires allows for distinct structural, electrical and transport behaviours, as well as advanced technological applications.

This section focuses on the applications of nanowire MOSFETs as a platform for novel materials research. Topological insulator materials and devices are discussed here as an example illustrating the significance of semiconductor with nanowire morphology in the understanding and implementation of fundamental physics and properties behind the materials.

5.1. Introduction to topological insulators

Topological insulators are characterized as a new class of materials having insulating band gaps in the bulk but gapless surface states topologically protected by time-reversal symmetry [62, 63]. Recently discovered three-dimensional topological insulators such as Bi₂Se₃, Bi₂Te₃ and Sb₂Te₃ have been intensively investigated both theoretically and experimentally [64, 65]. Most current experimental research focuses on the surface states of thin films grown by a molecular beam epitaxy (MBE) or mechanically exfoliated from bulk materials. For example, the gapless surface states featuring helical Dirac electrons have been observed by angle-resolved photoemission spectroscopy (ARPES) and scanning tunnelling microscopy (STEM) techniques. A few groups have reported the modification of surface conduction of such materials by doping, electrical gating or polarized light [66–68]. But there has rarely been reported of high-performance nanoelectronic devices based on topological insulators such as the analog of MOSFET. For conventional CMOS devices, the Si surface conduction is protected by thermal SiO₂ to optimize the inversion properties for good transistor performance. For topological insulators, the gapless surface state is derived from the inherent material properties

and maintains a robust surface conduction. Therefore, it will be very attractive to integrate the topological insulators as the active conducting channel in MOSFETs.

However, despite the significant efforts made in engineering of materials and devices based on bulk topological insulators, it is always a challenge to modulate the surface conduction due to the dominant contribution from bulk conduction. Topological insulator nanowires can be expected to greatly enhance the surface conduction due to their extra-high surface-to-volume ratio. Here, we will review the work on MOSFET devices based on topological insulator nanowires and the effective separation of surface conduction from the bulk conduction by an external electrical means [69].

5.2. VLS nanowire synthesis of topological insulator Bi_2Se_3 nanowires

The Bi_2Se_3 topological insulator nanowire FETs were fabricated by following the self-alignment process, similar to that of previous Si nanowire FETs [69]. The essential steps are as follows: the SiO_2/Si substrates with patterned Au catalyst were loaded in the downstream end in a horizontal tube furnace while Bi_2Se_3 source powder was located at the heating centre. The furnace was heated to a temperature in a range of 500–550°C and kept for 2 hours with a 50 sccm flow of Ar gas as a carrier gas. The Bi_2Se_3 nanowires were grown following the VLS route at pre-defined locations with typical length of 20 μm and 50 nm in diameter. Ti (3 nm)/Pt (100 nm) source/drain electrodes were formed by photolithography. A layer of 30 nm HfO_2 was then deposited at 250°C by ALD covering the nanowire channel and also a part of source/drain electrodes. The final step is the formation of 100 nm Pd top gate electrode.

Figure 18a shows the SEM image of the as-synthesized Bi_2Se_3 nanowires. Au nanoparticles were found at the top end of each wire, indicating the VLS mechanism. The high-resolution TEM (HRTEM) image shown in **Figure 18** demonstrates that the Bi_2Se_3 nanowires are in a well-defined single-crystal rhombohedral phase with growth direction close to $[11\bar{2}0]$. From the cross-sectional TEM image (**Figure 18d**); it is clear that the hexagonal nanowire core is surrounded by the insulating HfO_2 and the Omega-shaped top gate [69].

5.3. Characterizations of Bi_2Se_3 nanowire FET

The Bi_2Se_3 nanowire FET shows excellent transfer characteristics, as shown in **Figure 19**, such as close-to-zero cutoff current, strong-inversion-like on state current and over 10^8 on/off ratio within 1.0 V gate voltage. The nanowire FET has unipolar current dominated by electron conduction, which is similar to a conventional long-channel Schottky-barrier MOSFET with either electron or hole conduction determined by the unipolar Schottky junctions at the source and drain. **Figure 19b** and **c** shows well-saturated and smooth $I_{\text{DS}}-V_{\text{DS}}$ curves. I_{DS} saturates roughly at $V_{\text{DS}} = V_{\text{GS}} - V_{\text{Th}}$ in the highly conductive region but does not saturate at $V_{\text{DS}} \approx 3\phi_t$ in the weak/moderate conductive region. Instead, I_{DS} keeps increasing significantly after $3\phi_t$, suggesting the fact that the Bi_2Se_3 nanowire FET does not follow the diffusion current model as described for the conventional MOSFETs. It is believed that I_{DS} in the weak/moderate conductive regions is also dominated by drift current [69].

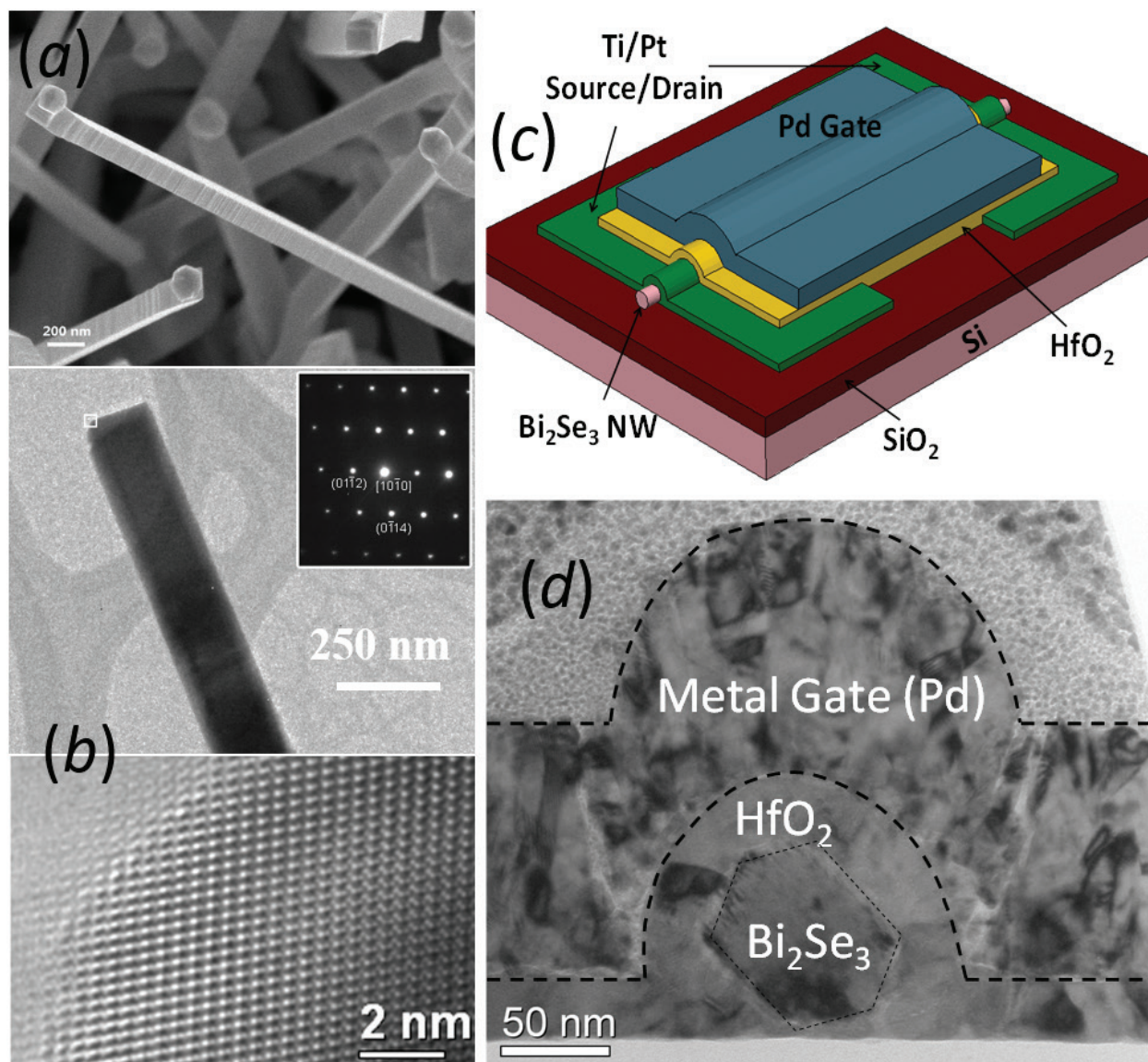


Figure 18. (a) SEM image of Bi_2Se_3 nanowires synthesized by following the VLS mechanism; (b) HRTEM image of Bi_2Se_3 nanowire showing the $[11\bar{2}0]$ growth direction. Inset: Magnified region of the nanowire; (c) schematic structure of a Bi_2Se_3 nanowire FET; (d) cross-sectional TEM image of a Bi_2Se_3 nanowire FET [69].

Further characterizations at different temperatures confirm that the saturation of I_{DS} is due to the electron velocity saturation at the source end instead of the pinch-off at the drain end of the nanowire channel, because a linear relationship was observed between the saturation drain current and the over-threshold voltage ($V_{\text{GS}} - V_{\text{Th}}$) as shown in **Figure 19**. By comparing the transfer characteristics at different temperatures (**Figure 20a**), it was found that $I_{\text{DS}} - V_{\text{GS}}$ curves obtained at temperatures lower than 240 K show a clear cutoff region with higher on/off ratio. The off state current for temperatures greater than 240 K flattens and saturates at negative voltages much below V_{Th} . Such temperature dependence indicates metallic conduction in the on state and insulating behaviour in the off state. By fitting the strongly activated temperature-dependent current to $I_{\text{DS,Off}} = I_0 e^{-E_a/kT}$ where E_a is the activation energy, k is

Boltzmann's constant and I_0 is a constant prefactor. E_a value of about 0.33 eV was obtained which is very close to the reported band gap value of bulk Bi_2Se_3 [69].

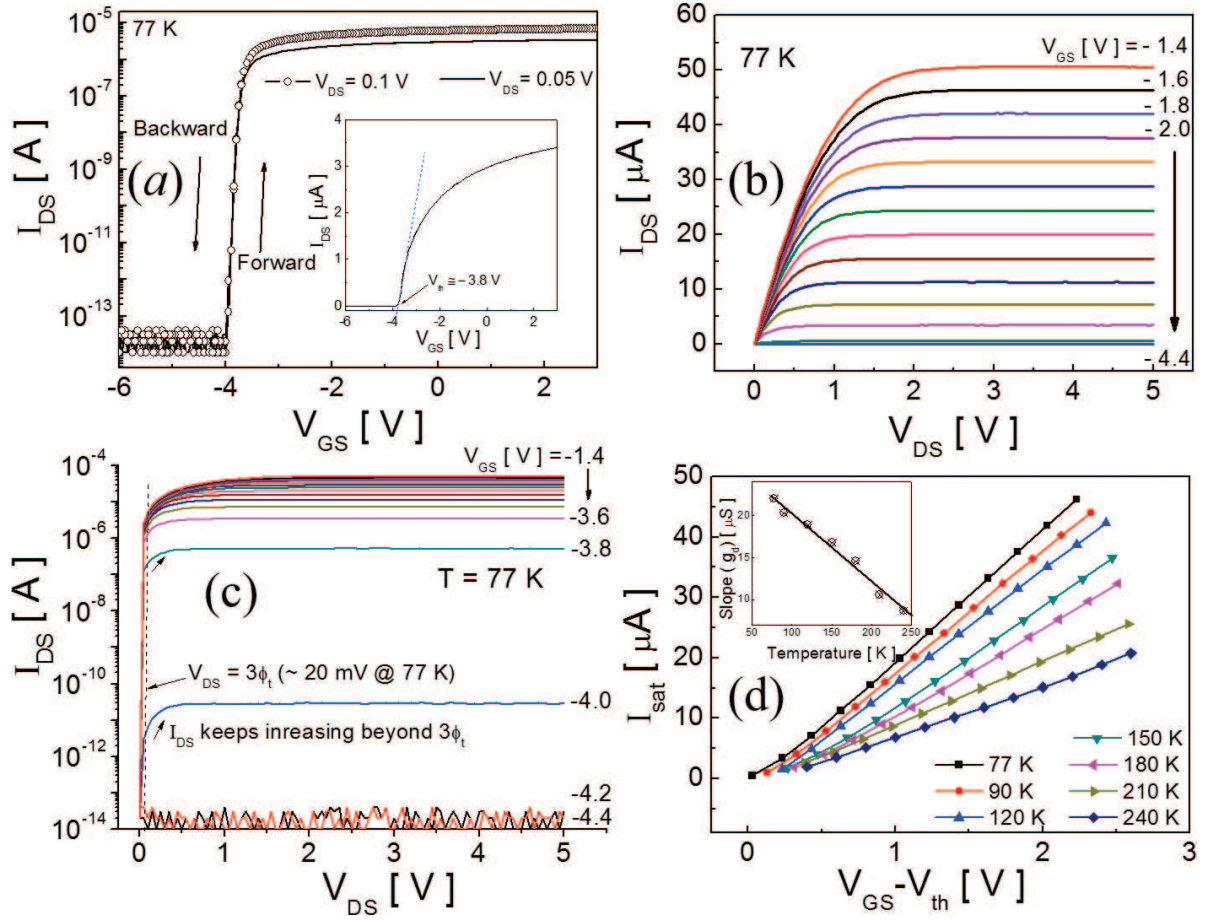


Figure 19. (a) Transfer characteristics and (b and c) output characteristics of the Bi_2Se_3 nanowire FET at 77 K. (d) I_{DS} as a function of over-threshold voltage. Inset: Linear fit slope versus temperature [69].

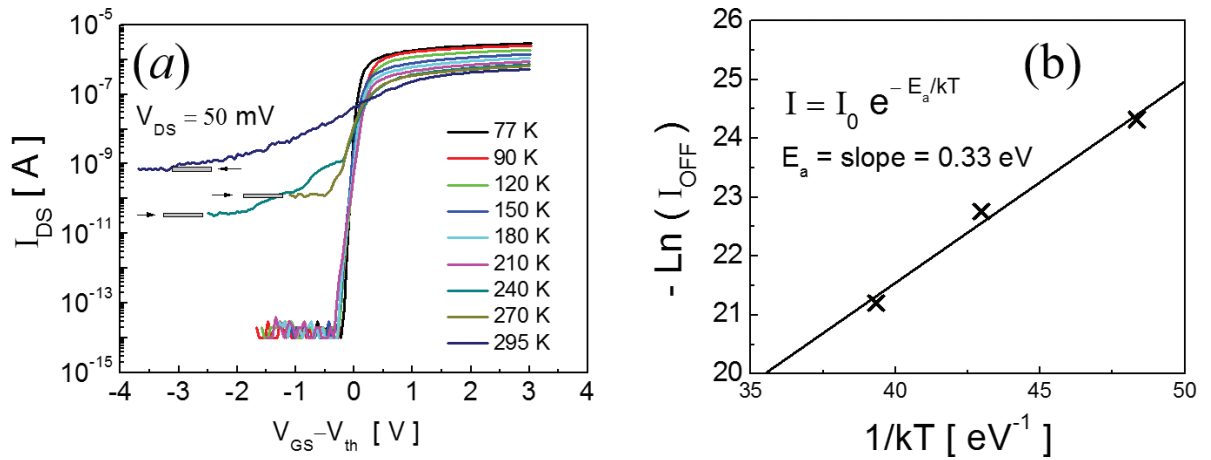


Figure 20. (a) $I_{DS} - V_{GS}$ curves at different temperature; (b) $\ln(I_{DS})$ at off state versus $1/kT$ above 240 K and its fit to $I_{DS, \text{Off}} = I_0 e^{-E_a/kT}$. [69].

5.4. Performance discussion

In the off state, the gate voltage is large enough to fully deplete the electrons from the nanowire, and the small temperature-dependent off-state current is due to the thermal excitations across the energy band gap of the bulk of Bi_2Se_3 nanowire. This further indicates the fact that the electric field generated surround the gate by the gate voltage below the threshold is strong enough to modify the spectrum of the nanowire and destroy the surface conduction channels [69]. Different with the conventional semiconductor nanowires, the saturated current of the Bi_2Se_3 nanowire FET in the on state is linear in gate voltage, indicating metallic conduction and is most likely flowing at the nanowire surface. Such interpretation also agrees with the temperature dependence shown in **Figure 20a**. The most significant achievement is that the surface metallic conduction and the insulating switch-off can be controlled by a surprisingly small gate voltage, resulting from the excellent gate control by the surrounding gate nanowire FET structure.

The above electrical performance obtained from the Bi_2Se_3 topological insulator nanowire FET is very impressive by taking advantages of the nanowire surrounding gate structure, leading to an enhanced gate control over the nanowire channel to realize electrical behaviour that have not been observed on planar counterparts. For example, the sharp switching from cutoff to surface conduction and saturation current by a gate voltage of a few volts is neither expected nor has been previously reported. Since the spin and momentum are locked in the surface states of topological insulators, possibilities of electric manipulation of spin current using gate voltage as well as novel circuit applications may be opened up using such one-dimensional topological insulator materials.

6. Conclusions

The physics and operation principles of nanowire materials and device have been systematically studied. Semiconductor nanowires enable the surrounding-gate structures, which significantly enhance the gate control over the channel in the electrical devices, leading to quite distinct and interesting device behaviours compared with the planar or bulk materials. The “self-alignment” approach enables simultaneous batch fabrication of large numbers of nanowire devices, while effectively reducing the processing steps in which nanowire surfaces might be contaminated. Si nanowire FETs with excellent electrical performances have been used as the platform to fabricate novel flash non-volatile memory devices. Both high-k dielectric and molecular charge-trapping memory demonstrate excellent memory behaviour and are very interesting for future on-chip non-volatile memory applications. The “self-alignment” method and the nanowire FET device architecture have been proved to be an effective platform and approach to be implemented and study other novel materials. High-performance topological insulator Bi_2Se_3 nanowire FET has been fabricated and investigated. The surface states are successfully separated from the bulk conduction within a small range of gate voltage due to the strong electric field induced through the surrounding-gate structure formed in the self-alignment fabrication

process. Such a high-performance nanoelectronic device and the analysis on surface conduction have never been previously reported. Therefore, the nanowire MOSFETs not only exhibit their potential in future CMOS scaling at advanced technology nodes but also provide an excellent approach for novel materials research towards next-generation micro and nanoelectronic devices.

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