Chapter 13

LTCC-Based System-in-Package (SiP) Technology for Microwave System Applications

Young Chul Lee

Additional information is available at the end of the chapter

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Abstract

Monolithic low-temperature co-fired ceramic (LTCC) SiP modules have been presented for microwave applications. In order to integrate almost passive circuits of a radio system into the LTCC substrate, key technologies such as suppressing parasitic resonant modes, low-loss transitions and compact passive devices have been investigated. Well analyzed mechanisms on the parasitic resonant modes and their suppressing methods have been applied to high-isolation SiP structures. A strip line (SL) to CPW vertical transition using a stepped via structure embedding air cavities has been devised and has been used to design a SL BPF. A surface mount technology (SMT) pad transition has been developed by utilizing a modified coaxial line. A LPF composed of vertical plate capacitors and helical inductors and a 2 × 2 array antenna have been developed. A 61 GHz heterodyne transmitter LTCC SiP module has been implemented by monolithically embedding all passive circuits such as a SL BPF, 2 × 2 array antenna, SMT pads and feeding lines into it. A 60 GHz amplitude shift-keying (ASK) transceiver LTCC SiP module has been implemented as small as 17.8 × 17.9 × 0.6 mm^3 by integrating a high-isolation via fence and a LPF. They have been characterized in terms of an output power, spectrum and link test.

Keywords: LTCC, SiP, transition, BPF, antenna

1. Introduction

In general, the final stage for implementation of microwave systems is system integration. It could be either integrated circuit (IC) die-level integration or package level one. And also, how to integrate microwave systems should be considered at the first stage of its development. Roughly, there are two categories for an integration technology of microwave systems: on-chip

technology and in-package one. The progress in these integration technologies has been formidable over the past decade for microwave applications. In these technologies, the main key issue is antenna integration on the chip or in the package, because its integration can provide several advantages such as low cost, compact size, high reliability and high reproducibility.

In the case of on-chip integration technologies based on complementary metal-oxide-semiconductor (CMOS), bipolar CMOS (BiCMOS) and silicon germanium (SiGe) BiCMOS, various researches have been explored up to recently. However, due to high permittivity (~11.7) and low resistivity (~10 Ω cm) [1, 2] of the Si-based substrate, integrated antennas have been suffered from low radiation efficiency and matching bandwidth. In order to modify properties of the substrate, although several novel techniques such as air cavity [3], artificial magnetic conductor [4], suspended membrane [5], ion implantation [6] and meta-surface [7] have been investigated; high-gain and broadband requirements are still below expectations, compared to those of package-based integration technologies [1, 8, 9].

In the package-based integration technologies, aside from highly integrated radio dies, almost passive components such as antenna, BPF and others are monolithically realized in the package substrate, thanks to three-dimensional (3D) stacking capability using via, multilayer and cavity. Very compact and high-performance microwave modules have been recently presented by using multilayer ceramic or printed circuit board (PCB) [10] technologies. Low-temperature co-fired ceramic (LTCC) [11–13] is a representative multilayer ceramic technology. For the past two decades, several LTCC modules involving antennas and other passive circuits with microwave radio chips have been developed and also it is possible to integrate high-gain antennas because of its properties of low-loss substrate and metallization (Ag).

In this chapter, highly integrated monolithic SiP modules have been presented for microwave system applications. In order to integrate radio systems in the single LTCC package module, key technologies such as suppressing parasitic resonant modes, low-loss transitions and compact and high-performance passive devices have been investigated after definition of monolithic SiP module. Finally, a 61 GHz transmitter (Tx) LTCC SiP module and a 60 GHz ASK transceiver one have been implemented in a size of 36 × 12 × 0.9 and 17.8 × 17.9 × 0.6 mm^3, respectively and they have been characterized in terms of an output power, spectrum and link test.

2. Monolithic SiP module

Figure 1 shows a three-dimensional (3D) schematic concept of the monolithic LTCC SiP module integrating a whole radio system consisting of active ICs and passive components in the single LTCC substrate. The filter and antenna are monolithically integrated in the LTCC dielectric and on its top layer, respectively. Active ICs are also mounted on the top of the LTCC multilayers. For miniaturization of the SiP module, passive circuits such as filters, antenna, surface mounted technology (SMT) pads, DC bias feedings and transmission lines are vertically or horizontally deployed by using vertical via interconnections, internal ground

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plane (I-GND) and signal line transitions in the substrate. Several transmission lines such as a strip line (SL), conductor-backed coplanar waveguide (CB-CPW), or microstrip line (MSL) are utilized within the LTCC block or on its top layer. By considering device and interconnection structures to be integrated in the SiP module, suitable transmission line is designed.

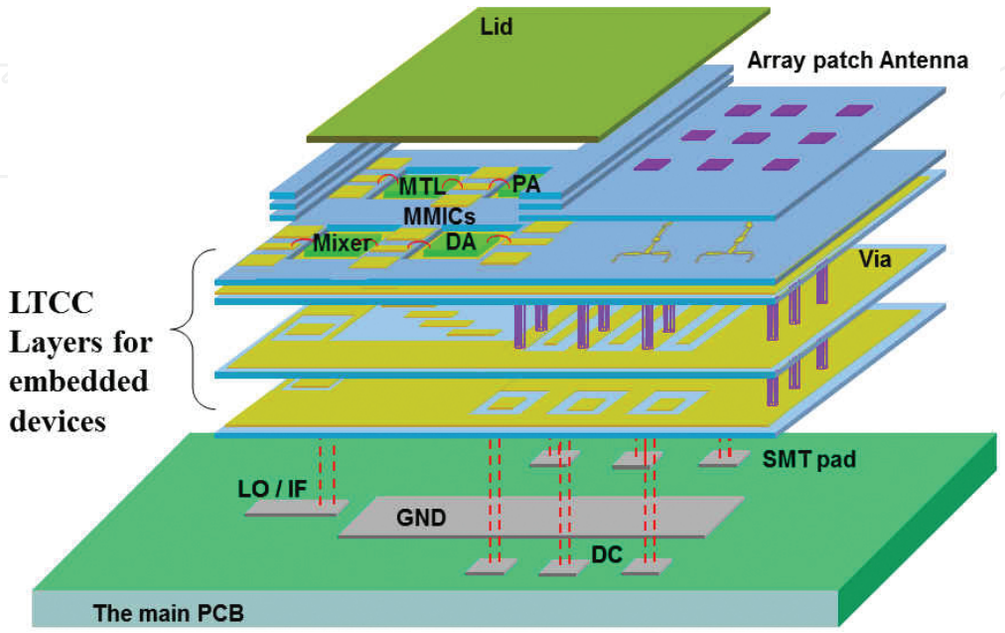

Figure 1. Three-dimensional (3D) schematic concept of a monolithic SiP module.

However, because various integrated transmission lines, passive devices and transitions are compactly integrated in the small area of the monolithic LTCC SiP module, they can make parasitic propagating structures and lead to unwanted cross talk issue. So, suppression of the parasitic resonant modes is one of the key issues in the design of SiP module. In addition, attenuation in interconnections between different signal lines or inter layers should be minimized for power efficiency and noise performance of the SiP module. And also, high-performance and compact passive devices should be designed.

3. Suppression of parasitic resonant modes

A CB-CPW and SL are in general used as signal lines of a SiP module because of their low dispersion and radiation. The CB-CPW consists of a lower and upper ground plane, embedded vias and a signal line (W) and the SL as shown in **Figure 2A**. However, these ground planes and vias can make parasitic resonant circuits such as rectangular waveguide (R-W/G), a parallel-plate waveguide and a patch antenna [14, 15] and they cause undesired resonant modes. An input signal is coupled by the gap of the CB-CPW, propagates through the parallel plate and finally radiates due to a parasitic patch resonator. In the case of the SL as shown in **Figure 2B**, it is basically a buried device and its structure is also composed of a lower and upper

ground plane, vias and a strip. The ground planes and vias generate the parasitic R-W/G, which is analogous to that of the CB-CPW.

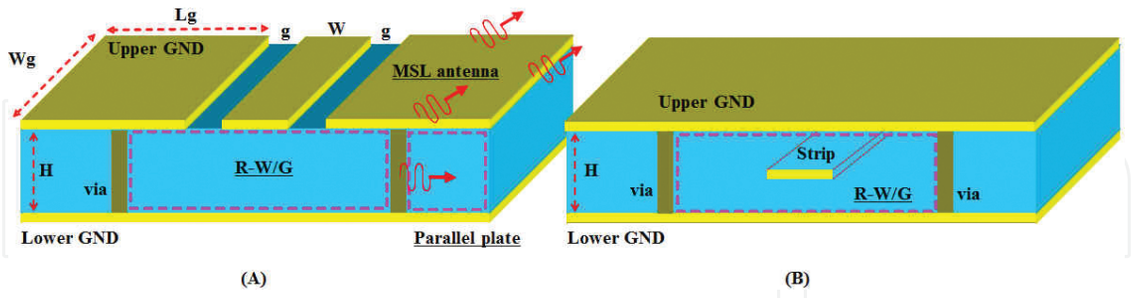

Figure 2. Structure of a CB-CPW (A) and SL (B) involving parasitic resonant circuits.

The resonant frequency (f_{WG}) due to the R-W/G is given by Pozar [16],

$$c_{p\ sample} = \frac{Q_{sample}}{Q_{ref}} \frac{m_{ref}}{m_{sample}} C_{p\ ref} \tag{1}$$

where D is the spacing between vias and it is the same as a horizontal dimension of a rectangular waveguide, ε_o is the permittivity of free space, μ_o is the permeability of free space and ε_r is the relative dielectric constant of the substrate.

The resonant frequency (f_{pr}) due to the surface ground planes is similar to that of the simple patch antenna [14, 15],

$$f_{pr} = \frac{c}{2W_g}\left(\frac{\epsilon\_r + 1}{2}\right)^{-1/2}\left[\text{GHz}\right] \tag{2}$$

where W_g is a width of a rectangular patch and c is the speed of light.

Figure 3 shows measured insertion loss characteristics of a 50 Ω CB-CPW line (A) and a SL BPF (B) fabricated in the LTCC substrate. Unwanted resonant modes are distinctly observed in the CB-CPW and SL BPF. In the case of the CB-CPW as shown in **Figure 3A**, its width, gap and length are 300, 150 and 3260 μm, respectively and its substrate height is 400 μm. Vias in order to short the lower and upper ground planes are placed at the both sides with a distance (D) of 1620 μm. The parasitic R-W/G is generated in the CB-CPW due to the ground planes and vias. In these dimensions of the CB-CPW, a propagation mode of the parasitic R-W/G is generated at 34 GHz. Resonances at 19.5 and 39 GHz are due to a parasitic patch antenna mode and its harmonic, respectively. Some input signal in the CB-CPW propagates to the parasitic R-W/G by coupling through its gap, passes through a parallel-plate W/G and finally radiates from the parasitic patch antenna. **Figure 3B** presents tested insertion losses of the 40 GHz SL BPF. The BPF was realized with six-stacked LTCC layers. Among the six-stacked layers, the SL filter was placed on the third layer and the CPW pads are on the top layer for on-wafer probing.

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Both top and bottom ground planes were connected to each other through ground vias to equalize the electric potential. The inset of **Figure 3B** shows the critical two dimensions (D_{CPW} and D_{SL}), which cause resonant phenomena. D_{CPW} of 1.15 mm is the distance between embedded vias. The lower and upper ground planes of the SL are shorted by using via blocks. The distance of D_{SL} is 2.32 mm. Two parasitic R-W/Gs with the lengths of D_{CPW} and D_{SL} are created in this SL BPF. Therefore, its performances are degraded due to spurious responses at 36 and 47.6 GHz, which are the parasitic R-W/G modes of TE20 generated by D_{SL} of 2.32 mm and D_{CPW} of 1.15 mm, respectively.

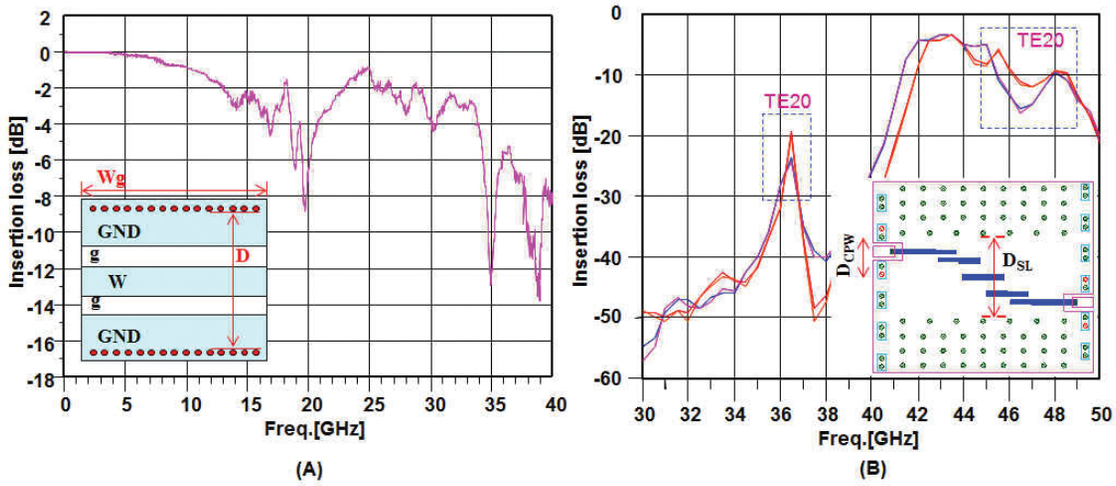

Figure 3. Unwanted resonance modes due to parasitic structures in the fabricated CB-CPW (A) [an inset: the top view of the CB-CPW] and the fabricated SL BPF (B) [the inset: the layout of the BPF].

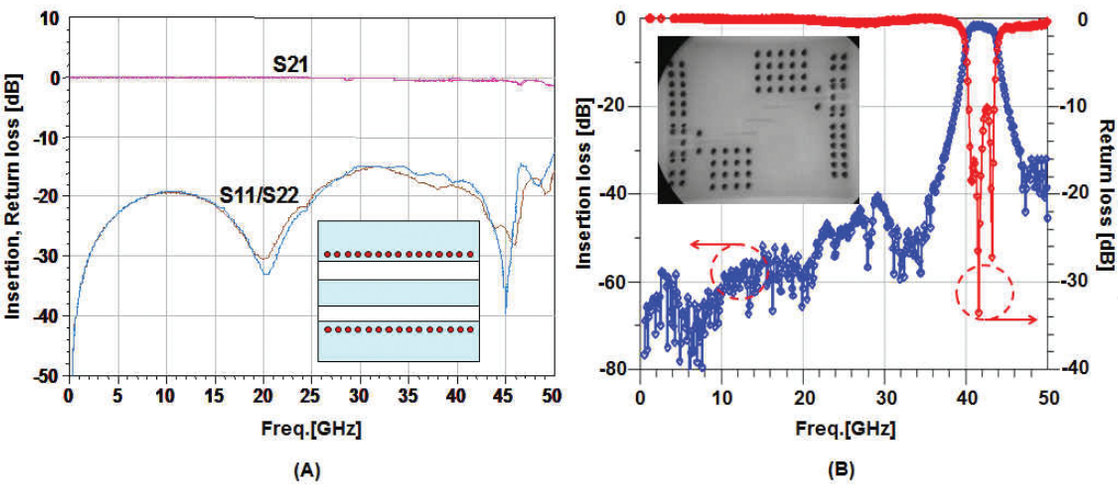

Figure 4. Resonance-free CB-CPW (the inset: the top view of the CB-CPW) (A) and SL BPF (the inset: X-ray photo of the fabricated SL BPF) (B).

The parasitic R-W/G modes (f_{WG}) in operating frequency band can be successfully suppressed by placing the vias within shorter distance than the calculated value from Eq. (1), because

parasitic propagating modes are generated in the higher frequency than that of an interesting band. By using this method, the CB-CPW and SL BPF were modified and fabricated. Their measured characteristics are indicated in **Figure 4**. The modified via placement for the CB-CPW and the SL BPF is presented in each inset of **Figure 4A** and **B**, respectively. The parasitic resonant modes are clearly suppressed in the operation frequency region [17]. In the CB-CPW, the distance (D) of 1620 μm is shortened to 700 μm and its layout and measured results are shown in **Figure 4A**. For the SL BPF, D_{CPW} of 1.15 mm is modified to 760 μm, which corresponds to the parasitic rectangular WG mode of TE10 at 76 GHz. One of the two GND-via blocks facing each other is deleted in order not to make the parasitic R-W/G in the SL structure. The X-ray photo of the fabricated SL BPF and the measured loss characteristics are presented in **Figure 4B**.

4. Low-loss transitions for 3D integration

For the 3D integration of microwave radio systems, several vertical transitions such as CPW-to-SL transition [18, 19], MSL-to-SL transition [20, 21], CPW-to-CPW transition [18, 22] and coaxial-like surface mount technology (SMT) pad transition [23] have been developed. These transitions allow the integration of passive and active circuits to be placed in inner layers or mounted on the top layer. The main issue for **3D** interconnection using transitions is to reduce attenuation and discontinuity. In particular, radiation due to structural discontinuity causes cross talk issue. Therefore, several attempts have been tried in order to remedy problems due to discontinuities. In order to improve impedance matching or compensate parasitics, the coaxial-like transition and intermediate ground planes have been utilized [18–23].

4.1. Strip line (SL)-to-CPW vertical via transition

In the vertical via transitions, the total physical height of the directly stacked vias has a decisive effect on their RF performance besides capacitive or inductive effects in the transition region. In the case of its height over one tenth of the wavelength (>0.1 λ) in the mm-wave frequencies, input signals can be significantly radiated or reflected.

Figure 5 shows proposed SL-to-CPW transition and its simulated performances [24]. A cross-sectional structure of the proposed SL-to-CPW via transition is shown in **Figure 5A**. Each LTCC layer is 100 μm high. The CPW on the top layer is connected with the embedded SL on the 4th layer (L4) by using vertical vias, which are subdivided into three-stepped one. Because of the proposed three-stepped via structure, the critical dimension, which mainly causes the physical discontinuity, is decreased from 300 to 100 μm. The wavelength (λ) on the LTCC CPW with relative dielectric constant of 7.0 is 2.56 mm at 60 GH. Its rate of the critical dimension to λ is decreased from 11 to 3.9%, respectively. However, it leads to the increase in the shunt capacitance between the vias and SL ground planes. For reduction in the increased shunt capacitance, the embedded air cavities are inserted below the stepped vias. In order to evaluate the proposed vertical via transition, the SL-to-CPW vertical transition is designed in back-to-back type as shown in **Figure 5B**. The ground planes of the CPWs and SL are connected by shielding vias. In order to design the 50 Ω CPW and SL, the CPW with the width of 250 μm and gap of

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99 μm is designed and the width of the SL is 135 μm. For comparison purposes, the conventional transition using the directly stacked vias is also designed. For the conventional transition, two 526 μm-long CPW lines are connected with the 2650 μm-long SL. In the proposed one, two 526 μm-long CPW lines and 2050 μm-long SL are used. The air cavities are embedded through the 2nd to 5th layer below the 7th layer via and through the 2nd to 3rd layer below the 5th layer via. By using a 3-D finite integration technique (FIT) simulator [25], all transitions have been designed and analyzed. Calculated results of the proposed transition in comparison with the conventional one are presented in **Figure 5C** and **D**. The proposed transition shows better performance in terms of return and insertion loss than that of the conventional one because of reduced via discontinuities. For quantitative analysis of improved performance, radiation losses ($1-|S_{11}|^2-|S_{21}|^2$) of the SL-to-CPW vertical transitions are calculated by using the simulated insertion and return loss and are illustrated in **Figure 5D**. At 60 GHz, radiation of the proposed transition is reduced by 23 and 62% by using the three-stepped via structure and embedded air cavities, respectively, compared to the conventional one.

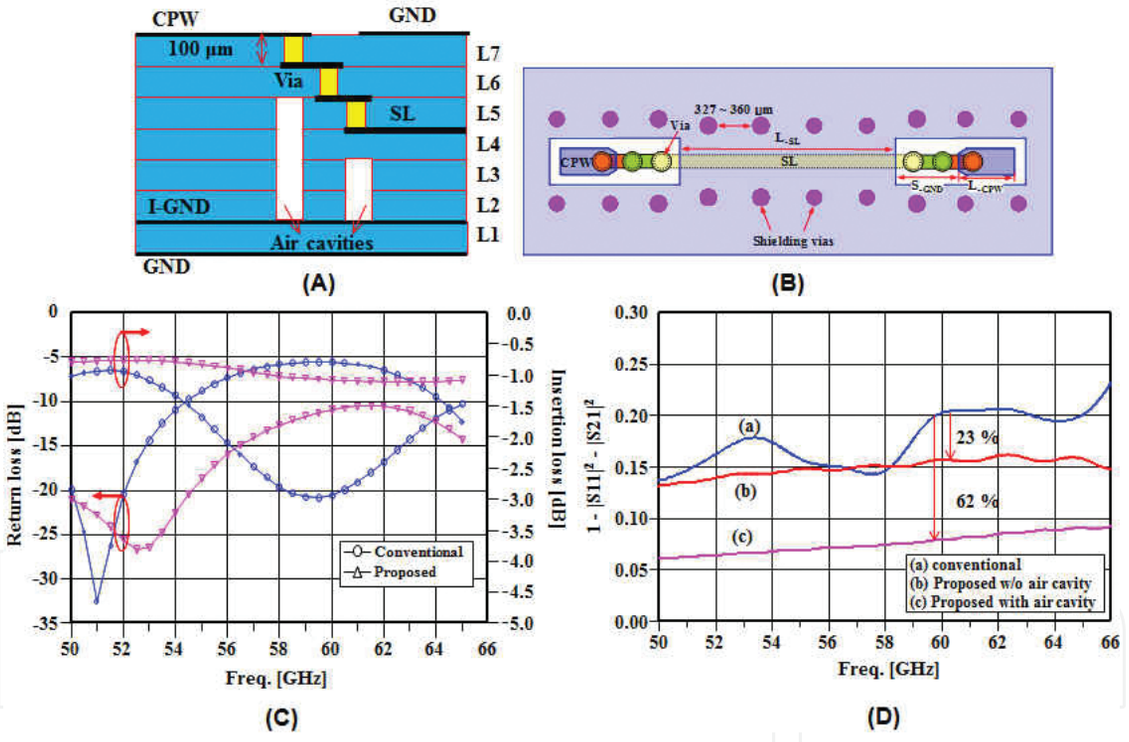

Figure 5. Proposed SL-to-CPW via transition and its simulated performances [(A): its cross-sectional view (Lx: the number of LTCC layers), (B): its layout in a back-to-back structure, (C): return and insertion loss characteristics and (D): radiation loss ones].

The designed transitions in the back-to-back structure were fabricated using seven-layered LTCC substrate and the fabricated ones were characterized by using a probing method as shown in **Figure 6**. For the proposed transition, embedded air cavities are clearly formed below the 5th and 7th layer via as shown in an inset of **Figure 6B** and also its S_{11} and S_{21} characteristics are improved compared to the conventional one. The measured S_{11} and S_{21} of the CPW-SL-

CPW are less than −10 dB and −2.0 dB, respectively, from 50 to 65 GHz. In particular, its low S_{21} of −1.6 dB is achieved at 60 GHz. These values represent all losses along the three-segment transmission lines and the two vertical via transitions. Considering the total loss of transmission lines with −0.19 dB, which is calculated by using a conventional line calculator, the transition loss per a ST transition is 0.7 dB at 60 GHz.

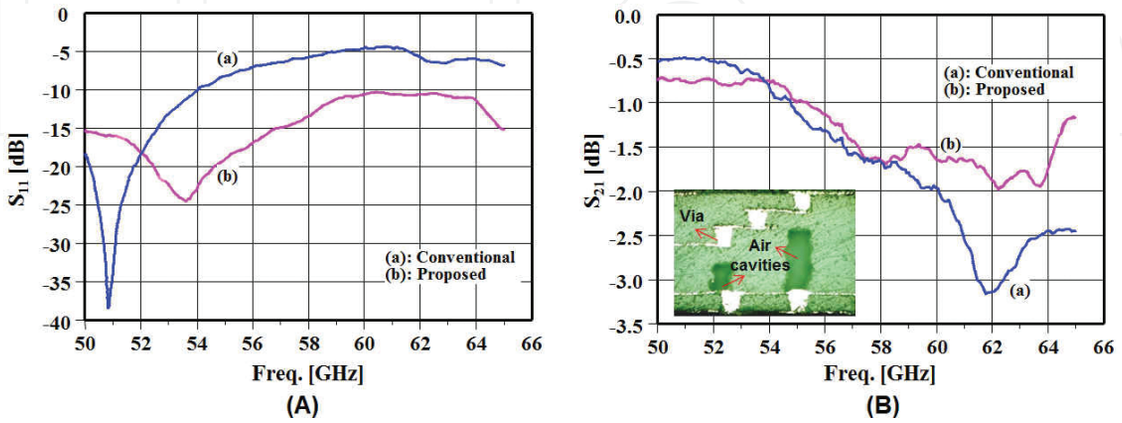

Figure 6. Measured return losses (A) and insertion ones (B) of the fabricated vertical via transitions in the back-to-back type using the proposed transition and the conventional one (an inset: cross-sectional views of the fabricated proposed one).

4.2. SMT pad using a coaxial-line transition

In general, LTCC SiP modules have been developed in type of SMT package because of low cost and easy assembly. In order to mount LTCC SiP modules on the main board, the low-loss transition between the signal port and SMT pad is required. In addition, the excitation of package modes [26] should be investigated for millimeter-wave applications. Typical transitions from I/O (input and output) port to the SMT pad in the SiP module have been designed by using vertical via structures [18–24]. In the case of long transition with several stacked vias over seven layers (>0.7 mm), it is difficult to control discontinuities and radiation. Therefore, by using a coaxial-line structure, the SMT pad has been implemented for the SMT LTCC SiP applications.

In order to suppress radiation in the long transition with several stacked vias, a SMT pad transition using a coaxial-line structure is proposed. By using a commercial tool [25], a CPW-to-coaxial line-to-SMT pad transition in a nine-layer LTCC substrate has been designed and its structure and designed results are presented in **Figure 7A**, **B** and **C**, respectively. The relative dielectric constant of the LTCC substrate is 7.8 at 20 GHz. Each layer is 100 μm thick. The total height of the vertical vias in the transition region is 700 μm. Because of a bulky structure of a 50 Ω coaxial line, an inner and outer diameter is optimized in terms of its transition loss and size. Considering losses in the transition, the impedance of the coaxial line of 37 Ω is determined. The diameter of the inner conductor (via) is fixed in 135 μm. The diameter and width of the outer conductor are 695 and 235 μm, respectively. The CPW line is designed in the cavity on L7 for interconnection with other devices or measurement. An embedded CPW (ECPW)

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between the coaxial line and CPW is designed on the same layer for their interconnection. The CPW line is with a 144 μm wide strip and a gap of 83 μm. The width and gap of the ECPW are 90 and 95 μm, respectively. Because of the overlapped part between the outer conductors of the coaxial line and the CPW line on the PCB board, E-fields are concentrated and consequently, a significant amount of reflection can be generated. The overlapped part, which is coaxial-line outer conductor to the left of the SMT pad, is cut off. In addition, in order to suppress the radiation at the bending part of interconnection between the coaxial line and CPW, a semicircular cap on the 9th layer (L9) of the LTCC substrate is designed. It radius is 928 μm. The modified SMT pad transition is shown in **Figure 7A**. Its E-field distribution at its cross section and its designed characteristics, comparing the effect of the cap are illustrated in **Figure 7B** and **C**, respectively. E-fields of the pad transition with a cap (WC) are confined between the cap and coaxial cable in the LTCC substrate in **Figure 7B**. From 8 to 20 GHz, the return losses (S_{11} and S_{22}) and insertion losses (S_{21} and S_{12}) of the pad transition with the cap (WC) are clearly improved compared with the pad transition without the cap (WOC).

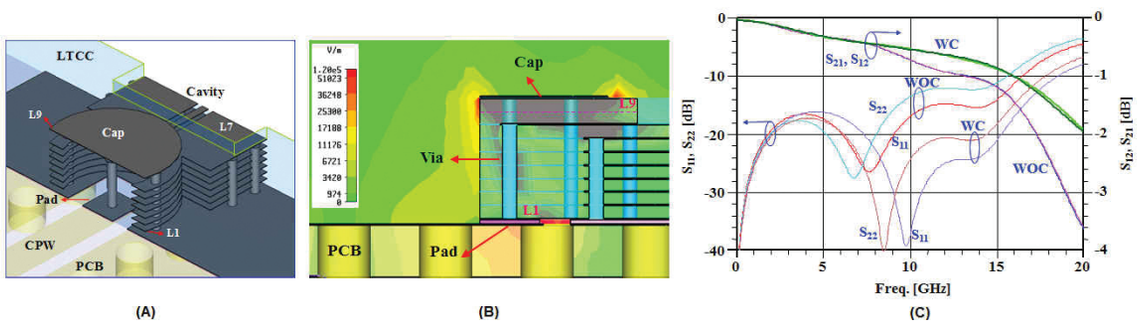

Figure 7. Perspective view (A) of the SMT pad transition using a modified coaxial-line structure, E-field distribution at its cross section (B) and its designed characteristics, comparing the effect of the cap on the top layer (C).

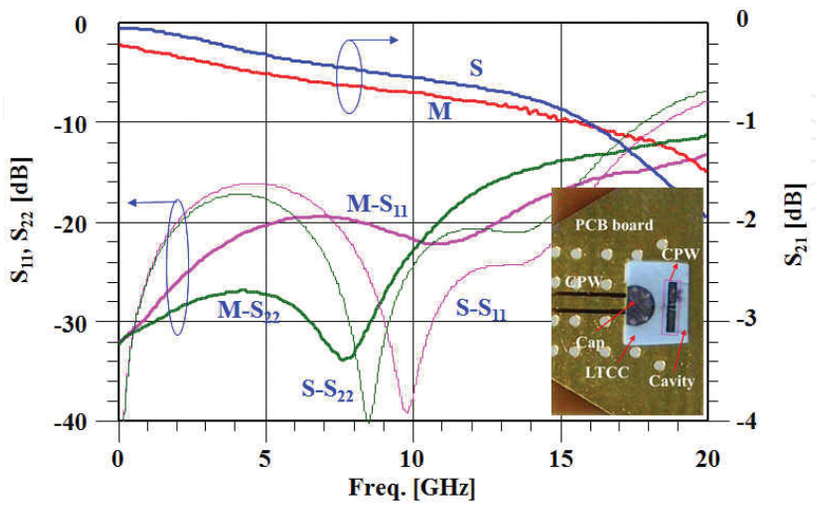

Figure 8. Measured results of the fabricated SMT pad transition, compared to the simulated ones (the inset: the fabricated SMT pad transition on the PCB board, M: measurement and S: simulation).

The modified SMT pad transition was fabricated by using LTCC standard fabrication process. Its measured characteristics are presented in **Figure 8**, compared with simulated ones. Poles of both return (S_{11} and S_{22}) and insertion loss (S_{21}) make a difference between the simulated and measured results. This difference comes from parasitic components due to soldering works. The measured insertion loss of 0.9 dB is achieved at 15 GHz. The return losses of S_{11} and S_{22} are below −14 dB at the same frequency. This SMT pad can be used for X- or Ku-band applications or LO-frequency ports for millimeter-wave SiP applications.

5. Compact LTCC passive devices—SL BPF, LPF and 2 × 2 array antenna

For compact radio system SiP module applications, the key components are the band-pass filter (BPF) and antenna, because they cover significant space and are difficult to be integrated in the RF ICs by using semiconductor technology. In general, they have been implemented in types of planar structures. However, planar structured circuits are usually bulky and are prone to unwanted radiation. Therefore, compact size, shielded electromagnetic cross talk and low-loss **3D** interconnection have been considered as the most important issues for passive device integration in the RF system SiP module.

5.1. A dual-mode four-pole 60 GHz LTCC SL BPF

A SL structured BPF using a dual-mode patch resonator can satisfy key issues for filter integration such as miniaturization and suppressed cross talk, because the dual-mode patch resonator offers a very compact structure [27] and radiation of the SL structure buried between upper and lower ground planes is negligible. However, in order to interconnect it with other circuits on the surface, the low-loss vertical via transition is required.

Figure 9A, **B** and **C** shows a fully embedded SL dual-mode BPF, its perspective view and a layout of two CPW-to-CPW planar transitions, respectively. The BPF is designed on seven-layer LTCC substrate with a relative dielectric constant of 7.0. The dual mode can be generated by adding a perturbation (cut) at a point that is 45° from the axes of coupling to the patch resonator (P-R). Two resonators are used on the 3rd and 5th layer for wide bandwidth characteristics and two P-R blocks are 684 μm away. The feed lines, external coupling between the resonators on the 3rd and 5th layers and internal coupling between their two blocks are on the 4th layer. Its center frequency (fc) and bandwidth (BW) are 61 GHz and 4.5%, respectively. The side length of the resonator is about half a wavelength (613 μm). The widths of the feed lines are 135 μm. By changing the depth of the cut, the coupling coefficients can be controlled and the calculated optimum cut length is 150 μm. The external coupling distances on the 4th layer are 140 μm and the internal coupling is realized by an overlap of 40 μm between two resonators on the 3rd and 5th layer. By using the low-loss CPW-to-SL transitions described in Section 4.1, the 600 μm-thick SL BPF is interconnected with 100 μm-thick RFICs mounted in the SiP module. However, the steep height difference between their GND planes can cause radiation problems. Therefore, by using CPW planar transition, GND planes are gradually transited from the 1st layer to the 3rd and 5th layers as shown in **Figure 9B**. This CPW planar

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transition consists of three CPW lines and two transitions (TR1 and TR2). Their width and the gap for 50 Ω impedance CPW lines are designed. The width of a CPW1 (=CPW2) and CPW3 is 244 and 100 μm, respectively. Its corresponding gap is 90, 140 and 90 μm, respectively. The transition length of TR1 and TR2 is 40 and 144 μm, respectively. LCPW1, LCPW2 and LCPW3 for each CPW length are 500, 430 and 500 μm, respectively.

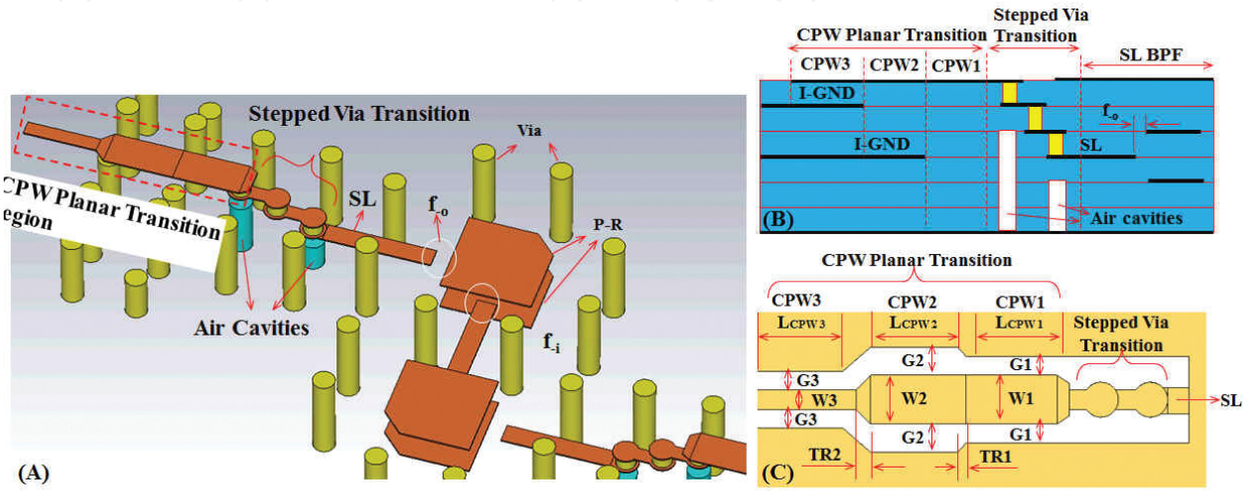

Figure 9. Perspective view (A) of a 60 GHz SL LTCC BPF involving CPW-to-SL stepped via transitions embedding air cavities, its cross-sectional view (B) and CPW-to-CPW planar transitions (C) [P-R: a patch resonator, f_o: an input and output feed line, f_i: an inter coupling feed line, I-GND: an internal ground plane].

The SL 60 GHz BPF fabricated in seven LTCC dielectric layers and its measured results are presented in **Figure 10**. Its total size including the entire transitions is 3.2 × 6.5 × 0.7 mm^3. By using the on-wafer probing method, the implemented BPF was tested. The comparison of the simulated and measured results is presented. While the measurement shows a lower center frequency and narrower BW than the simulation results, two results coincide rather well in the pass band from 60.075 to 61.925 GHz. The misalignment among feed lines and resonators results in different coupling coefficients, compared to the designed ones. Therefore, its frequency characteristics are a little different from the simulated results. The measured fc and fractional BW are 60.8 GHz and 4.1%, respectively. The return loss is less than −10.0 dB at the pass band. Its insertion loss including two vertical and four planar transitions is 4.98 dB. Considering the insertion loss of the transitions, its insertion loss is 3.74 dB.

5.2. A 5th order low-pass filter (LPF)

In order to eliminate harmonics or analog components among output signals, in general, a LPF has been used. The LPF based on the Chebyshev LPF prototype [16] as shown in **Figure 11** is designed in order to fully embed in this LTCC SiP module [28]. It has a cutoff frequency of 1.5 GHz, ripple of 0.05 dB and order of 5. In order to improve its return loss characteristics, values of capacitance (C1–C3) and inductance (L1, L2) in the designed basic LPF circuit are optimized.

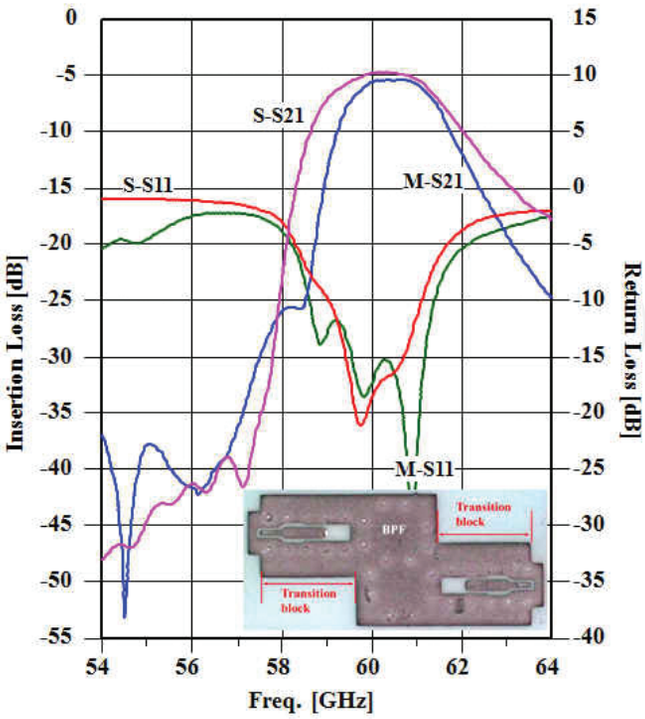

Figure 10. Measured performance of the fabricated SL BPF, compared to the simulated one (the inset: the photo of the fabricated BPF, S: simulation and M: measurement).

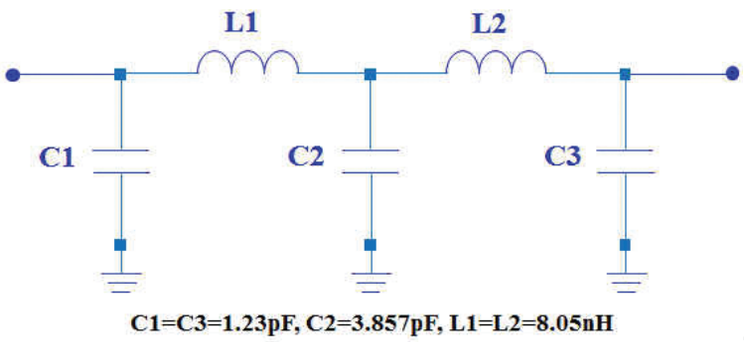

Figure 11. A prototype circuit of the 5th order Chebyshev LPF.

These capacitors and inductors are vertically designed within the six-layered LTCC dielectric whose permittivity is 7.2 at 2 GHz. In the case of the capacitor, three parallel-plate capacitors are interconnected in parallel by using vertical vias. Its capacitance value (C1 and C2) is controlled by an overlapped area among plates. The overlapped area of the C1 (=C3) and C2 is 400 × 500 and 600 × 1100 μm^2, respectively. In the case of the inductor, a 10,175 um-long line is coiled in the six-layer LTCC dielectric. The number of turn is 4.5. Its width of a metal strip is 170 μm. The number of turn and inner opening area of the helical inductor is 4.5 and 600 × 330 μm^2, respectively. The 5th order LPF is designed by integrating these elements in the size of 4.0 × 3.2 × 0.68 mm^3. It was fabricated using a LTCC commercial foundry. In **Figure 12A**, **B** and **C**, **3D** structures of the LPF elements (C1, C2 and L1), the designed LPF and measured

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results of the fabricated LPF are presented. The measured insertion loss (S_{21}) and return losses (S_{11}, S_{22}) are less than −0.46 and −11 dB, respectively. They are similar to simulated results.

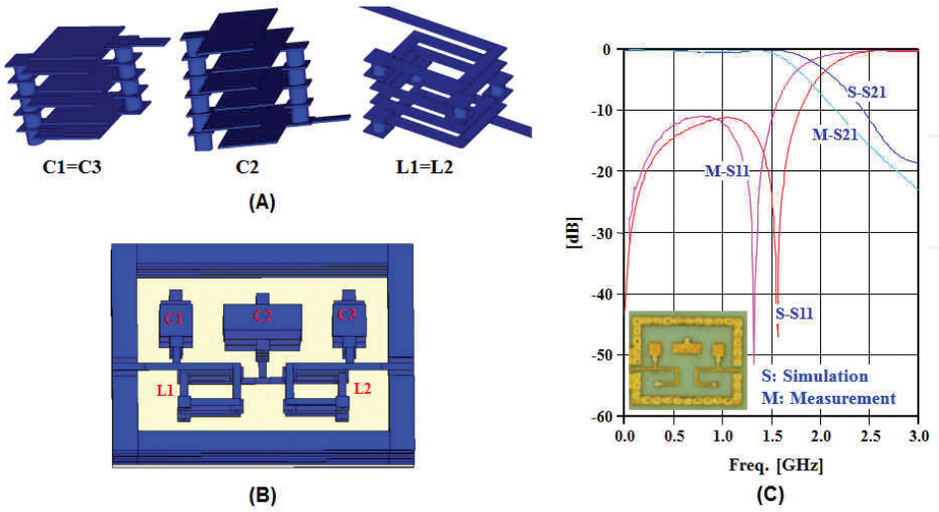

Figure 12. Perspective views of the elements (A) and LPF integrating them (B) and measured results compared to the simulated ones (C) [the inset: the fabricated LPF].

5.3. A compact 2 × 2 array patch antenna

The 2 × 2 patch array antenna is designed with a LTCC MSL structure. **Figure 13A** and **B** shows the **3-D** structure of the LTCC antenna and an embedded MSL (EMSL) power divider, respectively. Three layers from L6 to L8 are for the antenna and additional layers from L1 to L5 are used for internal and outer ground planes. The radiating patches are placed on the 8th layer (L8) and their size is the same as 645 × 1299 μm^2. The EMSL structured feeding network is designed on the 7th layer (L7) using a T-divider (power divider). In this structure, 70.7 Ω-quarter-wavelength ($\lambda_g/4$) transformers are required. However, it is impossible to implement them because limitation of the line width is 90 μm in the LTCC design rule. Therefore, the additional $\lambda_g/4$ transformers with low impedance (Z) are designed at the common port as shown in **Figure 16B**. The width of high-Z lines is 90 μm and their impedance is 47 Ω. For the low-Z lines, their width and length are optimized considering overall characteristics. The optimized width and its impedance are 130 μm and 40 Ω, respectively. The GND plane is on the 5th layer. The antenna size is as small as 10 × 10 × 0.3 mm^3.

Figure 14A and **B** shows the measured return loss characteristic and beam patterns of the fabricated antenna, respectively. Its X-ray photo is in the left inset of **Figure 14A**. In order to test a return loss and beam patterns, a WR15 waveguide (WG)-to-MSL transition was used as shown in the right insets of (A). A −10 dB bandwidth is 6.3 GHz from 56.5 to 62.8 GHz. At 61 GHz, the measured E- and H-plane radiation patterns are presented in **Figure 14B**. A gain of 7 dBi and a 3-dB beam width of 36° in H-plane pattern are obtained. The E-plane pattern is wider because of spurious generated in the E-plane direction of the feeding network.

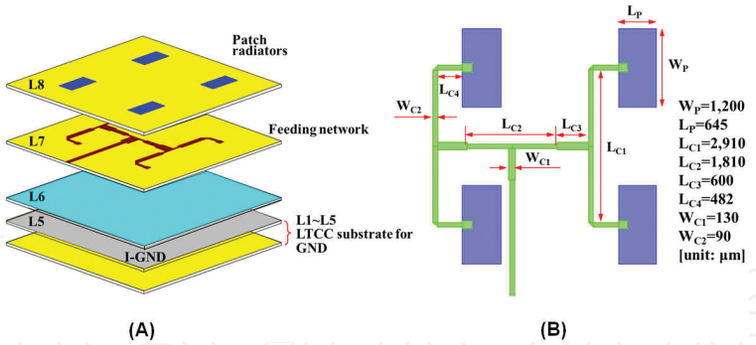

Figure 13. Layer structure of the 2 × 2 array LTCC antenna (A) and its feeding network and radiating patches (B).

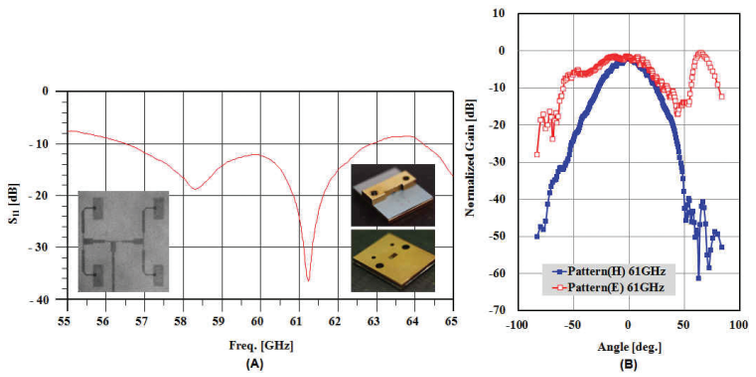

Figure 14. Measured return loss characteristic of the fabricated 2 × 2 array LTCC antenna (the left and right inset: its X-ray photo and the antenna assembled with a WR15 WG-to-MSL transition, respectively) (A) and its measured beam patterns (B).

6. Compact LTCC SiP modules for V-band applications

In this chapter, a typical heterodyne 61 GHz transmitter (Tx) and a highly integrated 60 GHz amplitude shift-keying (ASK) transceiver (TRx) SiP module are presented in detail [29–31]. They have been designed and implemented by using the key technologies such as suppression unwanted resonant modes, low-loss vertical transitions and compact passive devices presented in the previous chapters.

6.1. Monolithic 61 GHz transmitter LTCC SiP module

A block diagram of a typical heterodyne 61 GHz transmitter (Tx) is shown in **Figure 15**. This Tx is comprised of a BPF, a antenna, a up-converting mixer, two frequency multipliers (MTLs), a drive amplifier (DA) and a power amplifier (PA). The local oscillation (LO) signal (59.15 GHz) of the mixer is supplied by multiplying the external LO source of 14.79 GHz by 4.

The 61 GHz Tx is monolithically integrated into the single SiP module as shown in **Figure 16**. This SiP module consists of a nine-layer LTCC dielectric. The BPF, which is implemented in

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the previous subchapter 5.1, is fully embedded through L2 to L7 by using the CPW-to-SL vertical transition and the CPW-to-CPW planar transition. The BPF is connected with a driver amplifier and mixer IC. The 2 × 2 array MSL patch antenna is integrated in L6 through L8. In order to mount the 61 GHz Tx LTCC SiP module on a printed circuit board (PCB), a SMT package is adopted. Therefore, using SMT pads, all the ports of the module are designed on its bottom side. In particular, the SMT pad for a LO port is integrated by using the transition implemented in Section 4.2. Pad dimensions for DC ports, IF ports of 1.85 GHz and LO ports of 14.79 GHz are 700 × 700, 320 × 550, 560 × 560 μm^2, respectively. Five active chips mounted in the cavity of the L7 are isolated from each other using isolation cavities structure, which consists of L8 and L9. The DC bias lines and long IF feed lines are shielded using isolating ground planes and vias.

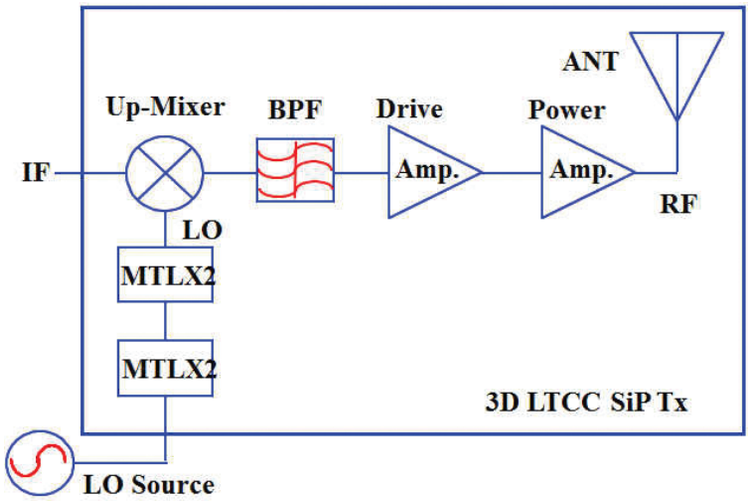

Figure 15. Block diagram of the 61 GHz heterodyne transmitter.

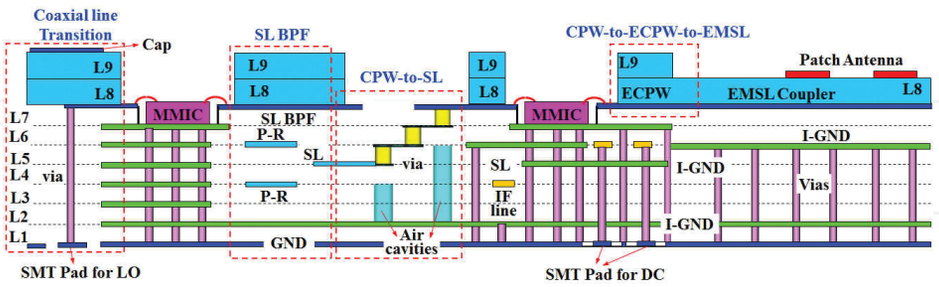

Figure 16. A cross-sectional view of the monolithic 61 GHz Tx LTCC SiP module integrating a BPF, an antenna, MMICs and DC bias circuits (ECPW: the embedded CPW, EMSL: the embedded MSL, P_R: the patch resonator and Lx: the layer number of the LTCC multilayer).

Designed SiP module was implemented in nine-LTCC multilayers using the standard LTCC process. **Figure 17A** shows the fabricated monolithic LTCC SiP module of the 61 GHz Tx. The whole size of the transmitter is as small as 36 × 12 × 0.9 mm^3. **Figure 17B** shows its bottom side with SMT pads.

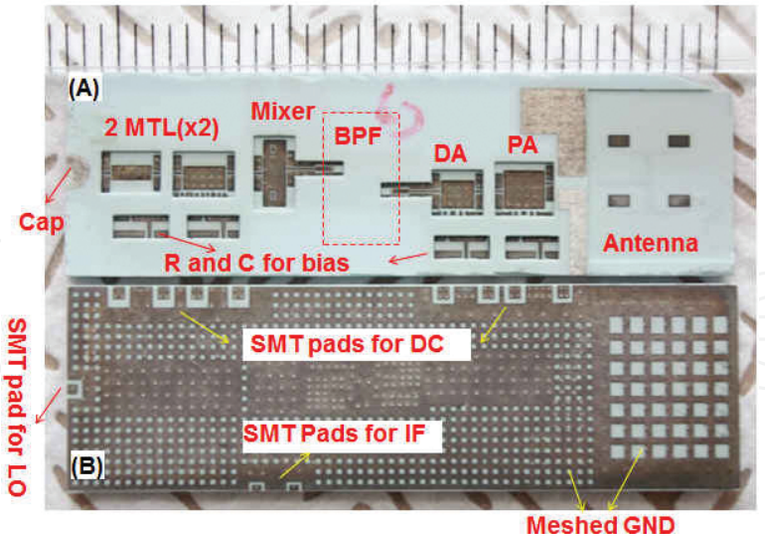

Figure 17. Implemented monolithic 61 GHz Tx LTCC SiP module [36 × 12 × 0.9 mm^3, (A) and (B): top and bottom side].

The fabricated LTCC Tx module was mounted on the PCB. At the output port of the power amplifier of the module, the output power and frequency spectrum were measured using on-wafer probing. **Figure 18A** plots the RF output power and the power gain as a function of the IF input power of 1.85 GHz. A measured output power at a 1-dB gain compression point (P1dB) and up-conversion gain is 10.2 dBm and 7.3 dB, respectively, at 61 GHz. Output spectrums such as a LO, RF and spurious signals are shown in **Figure 18B**. The isolation level between the LO and RF and the spurious one are less than 26.4 and 22.4 dBc, respectively. The measured output performance demonstrates that the integrated BPF suppresses effectively the LO and spurious signal.

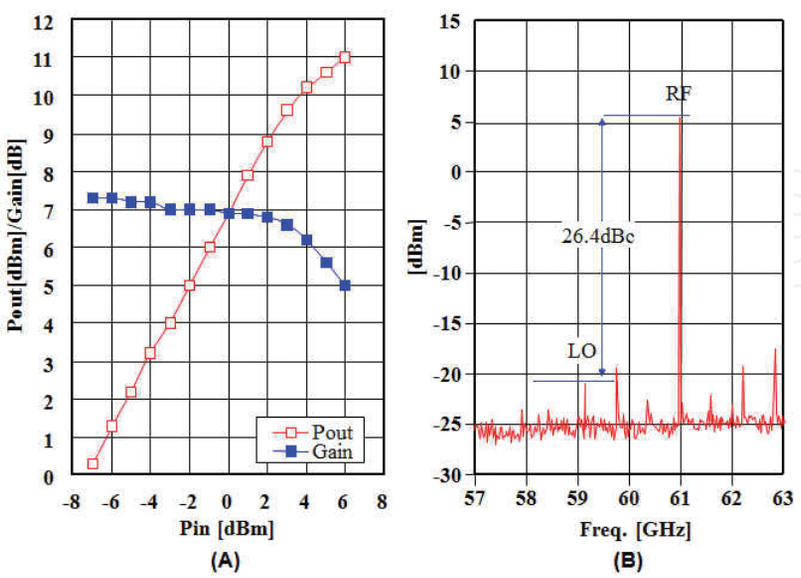

Figure 18. Measured output performance of the fabricated module (A) output power and conversion gain and (B) output frequency spectrum.

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6.2. Compact 60 GHz ASK transceiver LTCC SiP module

The amplitude shift-keying (ASK) modulation has been utilized in various microwave systems [32]. In particular, several millimeter-wave systems have adopted it for high-speed applications, because of circuit simplicity and high power efficiency. In addition, an analog-digital converter (ADC) is hard to be implemented and it is easy to demodulate ASK noncoherently by using an envelope detector.

In this work, the 60-GHz ASK transceiver (TRx) is designed and implemented. **Figure 19A**, **B** and **C** shows its block diagram, its layout for a LTCC SiP module and its cross-sectional structure, respectively. The Rx part consists of a high-gain and low-noise amplifier (LNA) block, detector, low-pass filter (LPF) and attenuator (ATT), which is inserted for the impedance buffering in the high-gain budget. The Tx part is composed of an up-converting mixer, two frequency multipliers (MTLs) and a power amplifier. The LO signal of the Tx is supplied to the mixer by multiplying the external LO source of 7.78 GHz by eight times. The carrier frequencies of the Tx and Rx link are 62.24 and 58.75 GHz, respectively. The whole 60-GHz ASK TRx is integrated into the six-layered LTCC SiP module in the size of 17.8 × 17.9 × 0.6 mm^3 as shown **Figure 19B**. In the conceptual vertical structure in **Figure 19C**, a LPF, isolation via fence and DC bias components are embedded. RFICs are mounted on cavities in L6. Each LTCC layer is 84 μm high. A via diameter is 120 μm before co-firing process. The main signal line is a 50 Ω CPW line, whose width and gap are 123 and 100 μm, respectively. The five-order Chebyshev LPF with a cutoff frequency of 1.5 GHz inserted in the ASK de-modulator (Rx part) in order to eliminate harmonics and analog components at its output. The previously implemented LPF in Section 5.2 was utilized. The ground plane in the bottom side of the Tx and Rx part is also separated for eliminating return path.

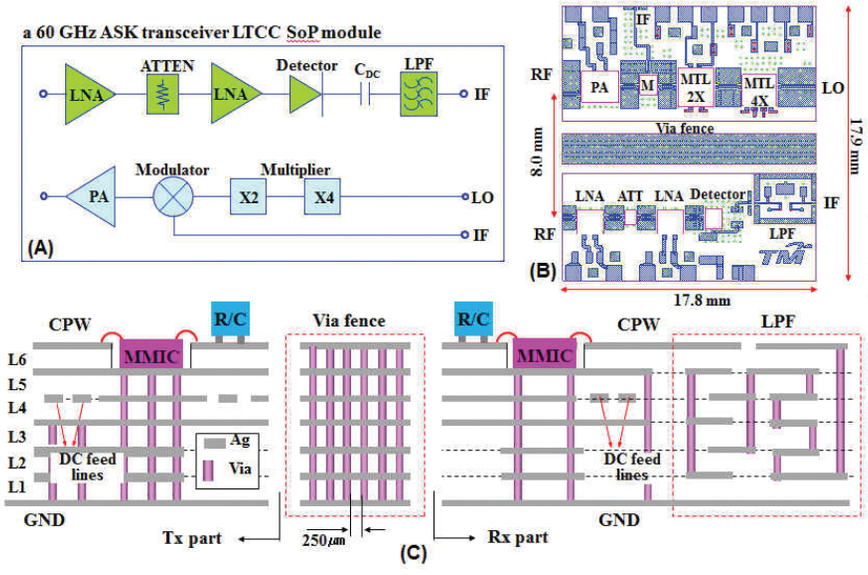

Figure 19. A block diagram of a 60 GHz ASK transceiver (TRx) (A), the layout of the ASK TRx LTCC SiP module (B) and its conceptual vertical structure (C) embedding a LPF, via fence, RFICs and DC bias components in the 6-layer LTCC dielectrics [Lx: the number of the LTCC dielectric layer].

The high-isolation via fence between Tx and Rx part is investigated by using a 3-D electromagnetic (EM) tool [25] as shown in **Figure 20A**. In general, the isolation of over 80 dBc is required between the ASK modulator and demodulator. In order to confine the EM-fields within each Tx or Rx area, the via fence is designed between 50 Ω CPW lines, which can be assumed as the signal path of the Tx (P1–P2) and Rx (P3–P4) part. The spacing between them is 8 mm, which is the same that between the Tx and Rx port in the diplexer of the main system. The diameter of vias and spacing between their edges are 120 and 250 μm, respectively. The E-field distribution of the designed model at 60 GHz is presented in **Figure 20A**. This result shows that E-fields inputted from a port 1 (P1) can be effectively confined within one path (Tx) due to the via fence. Simulated isolation characteristics between two lines from DC to 100 GHz are presented in **Figure 20B**. It clearly shows that the isolation better than 80 dBc is obtained.

The designed ASK TRx LTCC SiP module was fabricated using a six-layer LTCC substrate in the commercial Foundry [33]. The implemented ASK TRx LTCC SiP module is as small as 17.8 × 17.9 × 0.6 mm^3 as shown in the inset of **Figure 21A** and it was assembled into a metal housing with DC bias boards. **Figure 21B** and C shows the measured RF and IF spectrum in the Tx and Rx part, respectively, of the ASK TRx LTCC SiP module. In **Figure 21B**, the measured output power (Pout) is 12.8 dBm at the LO of 62.24 GHz and IF frequency swept from 10 MHz to 1.5 GHz. By inserting a 20 dB attenuator between the Tx and Rx parts considering the free space path loss, the IF spectrum of the Rx part was tested. By changing the IF signal from 10 MHz to 1.5 GHz at the Tx part with the LO signal of 58.752 GHz, the flat IF output signal less than −2 dBm is obtained up to 1.25 GHz as shown in **Figure 21C**. The conversion gain is 38 dB at the IF output of 1.25 GHz.

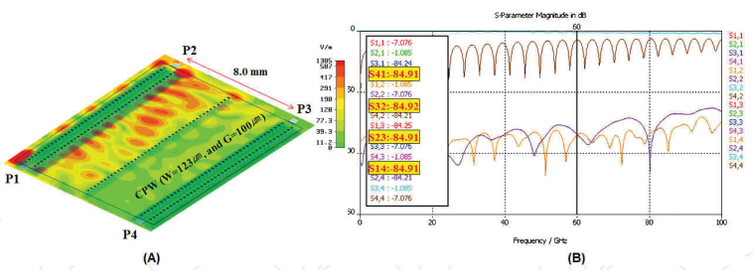

Figure 20. An assumed model for evaluation of isolation between the Tx and Rx and its E-field distribution (A) and simulated results (B).

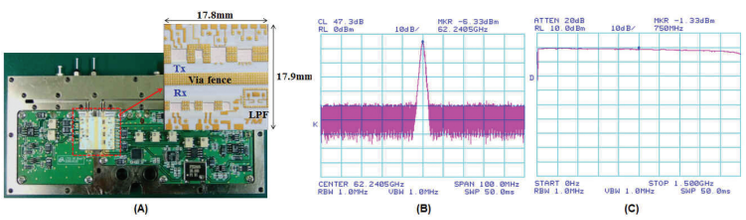

Figure 21. Fabricated ASK TRx LTCC SiP module (A), its measured spectrum at the output port of the Tx part (B) and the IF port of the Rx one (C).

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7. Conclusion

In this chapter, highly integrated monolithic LTCC SiP modules have been presented for microwave applications. Almost passive circuits of the whole radio system have been monolithically embedded in the LTCC multilayer dielectric substrate. The main key technologies for the monolithic SiP module are suppressing parasitic resonant modes, low-loss transitions and compact and high-performance passive devices. In general, the parasitic rectangular waveguide consisting of via, upper ground plane and lower one is easily and frequently formed in the SiP module and also effectively suppressed by reducing its horizontal dimension, spacing between vias. The low-loss SL-to-CPW vertical via transition using the stepped via structure and embedded air cavity achieves −0.7 dB transition loss at 60 GHz. By using the modified coaxial line, the SMT pad transition is developed and demonstrates 0.9 dB loss at 15 GHz. By using the developed SL-to-CPW transition, the dual-mode four-pole 60 GHz SL BF is fully embedded in the LTCC substrate in the size of 3.2 × 6.5 × 0.7 mm^3 and the insertion loss of 3.74 dB and the BW of 4.1% are obtained. The fully embedded 5th order LPF composed of vertical plate capacitors and helical inductors is implemented as small as 4.0 × 3.2 × 0.6 mm^3. Its measured insertion and return losses are −0.46 dB and less than −11 dB, respectively. The 2 × 2 array patch antenna with the gain of 7 dBi and beam width of 36° has been developed. By utilizing the well analyzed and developed key technologies, 61 GHz transmitter and 60 GHz ASK transceiver LTCC SiP modules have been implemented. The 61 GHz Tx LTCC SiP module achieves an output power of 10.2 dBm at 61 GHz and the conversion gain of 7.3 dB. Because of the integrated SL BPF, the LO and spurious signals are suppressed below 26.4 dBc and 22.4 dBc, respectively. Using the off-shelf receiver, the wireless link is verified. In the case of the 60 GHz ASK LTCC SiP module, in order to achieve 80 dBc isolation between the Tx and Rx part, the high isolated substrate using the via fence is proposed and used in the SiP design. The 60 GHz ASK TRx LTCC SiP module is fabricated as small as 17.8 × 17.9 × 0.6 mm^3 and it achieves the output power of 12.8 dBm at LO of 62.24 GHz and the flat IF output signal less than −2 dBm up to 1.25 GHz.

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Author details

Young Chul Lee

Address all correspondence to: leeyc@mmu.ac.kr

Department of electronic engineering, Mokpo National Maritime University (MMU), Mokpo, South Korea

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