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FPGA-SRAM Soft Error Radiation Hardening

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Abstract

Due to integrated circuit technology scaling, a type of radiation effects called single event upsets (SEUs) has become a major concern for static random access memories (SRAMs) and thus for SRAM-based field programmable gate arrays (FPGAs). These radiation effects are characterized by altering data stored in SRAM cells without permanently damaging them. However, SEUs can lead to unpredictable behavior in SRAM-based FPGAs. A new hardening technique compatible with the current FPGA design workflows is presented. The technique works at the cell design level, and it is based on the modulation of cell transistor channel width. Experimental results show that to properly harden an SRAM cell, only some transistors have to be increased in size, while others need to be minimum sized. So, with this technique, area can be used in the most efficient way to harden SRAMs against radiation. Experimental results on a 65-nm complementary metal-oxide-semiconductor (CMOS) SRAM demonstrate that the number of SEU events can be roughly reduced to 50% with adequate transitory sizing, while area is kept constant or slightly increased.

Keywords: SRAM, FPGA, Radiation, single event upset, hardening

1. Introduction

The dimensions of integrated circuit devices decreased in each successive technology generation. The goal of this scaling is, on the one hand, to improve the performance of integrated circuits and, on the other hand, to integrate a greater number of devices per unit area. Static random access memories (SRAMs) are not an exception to this evolution, the dimensions of the transistors forming memory cells decreased roughly following Moore's Law. Consequently,

the area occupied by each cell decreased from generation to generation [1]. Current technological processes used to manufacture complementary metal-oxide-semiconductor (CMOS) SRAM memories are in the nanometer region, since the nominal characteristic dimensions of the transistors forming each cell are of the order of tens of nanometers.

The supply voltage of SRAMs has also been reduced. However, this decrease did not follow the predictions of the International Technology Roadmap for Semiconductors (ITRS), in fact, it was more moderate. This is mainly due to the limitation imposed on the transistors threshold voltage scaling to avoid an excessive increase of leakage current [2]. To meet performance demands of current electronic systems, large capacity integrated SRAMs are usually needed, and in fact, FPGA-SRAMs are not an exception. This requirement results in a large proportion of area dedicated to SRAM memory. Forecasts indicate that in the coming years this figure may reach 90% [3]. Of course, integrating large memories has an adverse impact on circuit area, which in turn results into higher costs. For this reason, designers try to integrate the largest possible number of SRAM cells per unit area. This leads to cells designs with small sizes to squeeze the full potential of technology. SRAMs are usually designed with transistors close to the minimum possible size, and arranged with the highest possible density. In addition, to reduce power consumption, voltages are kept as low as possible. Although, as mentioned before, the expected voltage reduction have not been fully implemented in real technology.

As a result of the decrease in device dimensions and of the reduction of supply voltage in successive technology generation, designing SRAM faces two major challenges: the first one is related to the stability of the cells and second one has to do with their susceptibility to radiation-induced transient events. This chapter focuses on the second challenge, the CMOS SRAM radiation problem. However, SRAM stability issues are also discussed.

SRAMs are one of the most sensitive to radiation parts of a circuit. They are especially sensitive to those effects caused by a single energetic particle. These effects are the so-called single event upsets (SEUs). They are considered soft errors (SE) because they trigger an error without permanently damaging the circuit. This chapter focuses on six-transistor (6T) CMOS SRAM SEUs and on a technique to mitigate its effects, which is easily implementable in current FPGA design workflows. The architecture of 6T RAMS cell is described in Section 2.

Regarding the process that generate SEUs, the interaction of an energetic particle creates electron-hole pairs, so that part of this deposited electric charge can be collected by a sensitive node affecting its voltage. If this node is the node of an SRAM and the perturbation is high enough, it can flip the cell state altering data stored in it, and thus generating an error. These errors are not necessarily destructive. In particular, in an SRAM, a particle is capable of modifying data stored in one or more memory cells without damaging them. This means that cells can be rewritten and operate normally. Nevertheless, cell data has been corrupted, and if the cell is read before a new write occurs, a read error will be produced.

The problem of radiation effects in integrated circuits is not new. It has been studied and taken into account for decades by designers in areas such as the aerospace industry and, since the mid-1990s, also by the aeronautics manufacturers [4]. This is due to the high flow of energetic particles that devices operating in these high-altitude environments are exposed to. The

atmosphere shields part of the energetic particles that come from outside the Earth, so that, the higher the altitude, the higher the particle flux. To mitigate these effects, radiation shields, redundant components, techniques of error detection and correction and radiation tolerant elements are used. The implementation of these measures ranges from technological aspects of architecture to system level. Many of these measures increase costs and negatively impact circuit performance. There exist many well-known techniques to mitigate SEU effects, such as triple modular redundancy (TMR), which can be suitable for certain applications. However, most of them involve high penalties in terms of cost, power, or performance, which can be affordable for the space industry but could be non-acceptable for other FPGA fields of application.

In addition, due to technology scaling, SEUs are becoming a major reliability concern for electronic devices in general and SRAMs in particular, not only in harsh radiation environments but also at ground level, where radiation fluxes are low. In the case of SRAMs, this is due to the fact that the number of errors per time unit in SRAM memories due to radiation-induced transient events has increased with technology scaling [3, 5]. This fact has two main causes. The first cause has to do with both reducing the dimensions of the transistors forming the cells and with decreasing the supply voltage. Both factors contribute to reduce the amount of electrical charge used by a cell to store one bit of information. Thus, it is easier that the charge induced by the interaction of a particle upsets the cell content. The second cause includes three related factors: the increase in the number of cells integrating SRAMs, the higher density of cells, and the amount of chip area occupied by SRAM cells. All of them contribute to increase the probability that an energetic particle interacts with a sensitive area of a memory causing a transient event that leads to cell data corruption. In a FPGA, this can be a serious problem, since SRAM-based FPGAs rely on SRAMs to store configuration bits. An SEU affecting one of those bits can produce an unpredictable behavior or even a complete system failure.

To conclude, SEU effects are not a new problem and the space industry has developed specialized techniques to deal with them for decades. However, FPGAs are used in a broad range of applications, and in many of them circuits are not subject to high radiation fluxes. Nevertheless, due to technology scaling, they are becoming sensitive to radiation either from the environment or from the circuit materials. For this reason, it is necessary to implement some radiation hardening techniques, especially if the circuit is operated in critical systems. Traditional aerospace techniques are not suitable for most SRAM-based FPGA applications, since they involve high costs or significant performance degradation, which cannot be assumed. One of the most paradigmatic examples is commercial electronics or any other FPGA application field where FPGAs are attractive due to its fast time to market, flexibility, and reprogrammability, which reduce costs while keeping good performance. Thus, the aim of this chapter is to present a technique that fills this gap and can be used as a suitable technique to improve radiation reliability in a broad range of FPGA-SRAMs applications. More specifically, the technique works at the cell design level, and its goal is to enable the design of intrinsically more robust cells. In addition, the technique is also attractive because it is compatible with current memory compilers, since it does not change SRAMs cell architecture.

2. Radiation impact on SRAMs

The analysis of radiation impact on integrated circuits is difficult and is typically performed by experimental tests or using device-level simulations. However, the critical charge (Q_{crit}) is a parameter usually used as a standardized methodology to analyze the circuit-level impact of radiation on SRAMs [6, 7]. One of the main advantages of this parameter is that it can be obtained by electrical simulations, which are cheaper than experimentation and less time consuming than device-level simulations. In addition, it helps to understand how SEUs are produced.

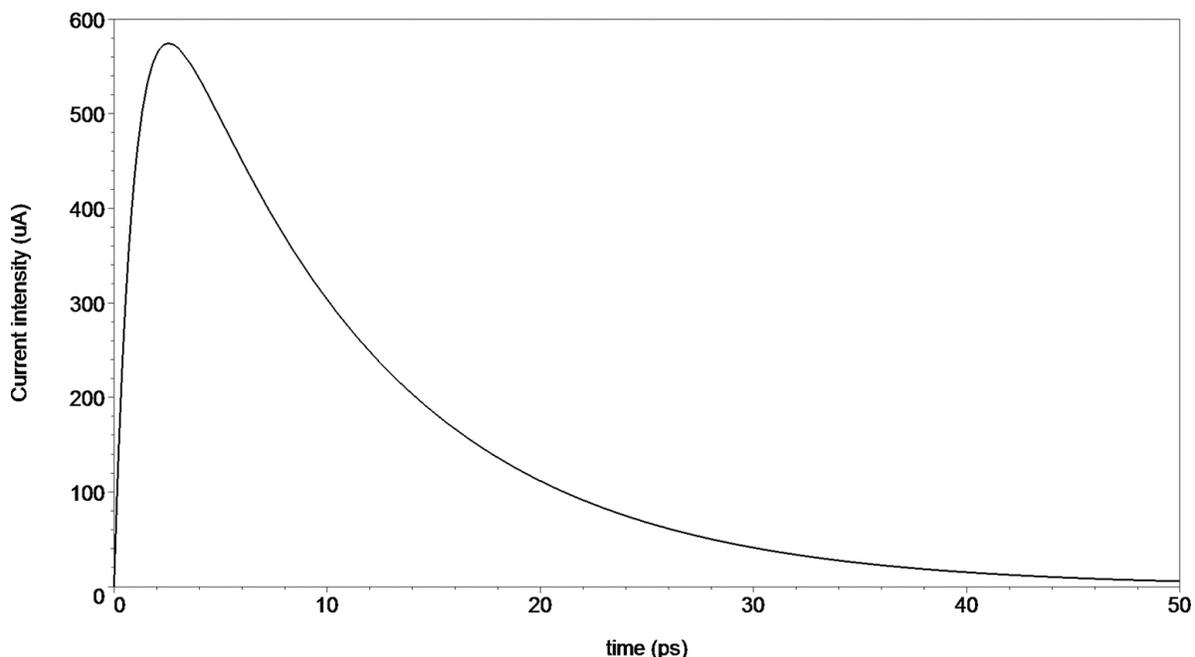


Figure 1. Example of a double exponential current pulse.

When an energetic particle impacts a CMOS circuit substrate, it induces a charge track due to electron-hole pair generation. This deposited charge can be collected by a sensitive node—typically the drain of an off transistor—which is near to the ionization track [4]. This results in a transient current pulse at the node. A sufficiently strong current pulse will modify data stored in the cell (cell flip). If this occurs, an SEU is produced. The word “Single” means that the cell upset is caused by a single energetic particle. The parameter used to quantify the minimum amount of charge collected by a memory element node that changes its state is the critical charge. Typically, Q_{crit} is determined by electrical simulation analyzing how a given memory cell flips under current pulses having different shapes and intensities. It has been reported that energetic particle strikes lead to current transients with varying pulse durations (pulse width), and that the Q_{crit} value of a node is a function of the waveform shape [8, 9]. For this reason, a proper choice of current waveforms to estimate the critical charge is important. In this chapter, we will use the well-known double-exponential current source model given by

$$i(t) = i_0 \left(e^{-\frac{t-t_0}{\tau_1}} - e^{-\frac{t-t_0}{\tau_2}} \right) \quad (1)$$

where $i(t)$ is the current intensity at time t , i_0 is a parameter that scales the current intensity, τ_1 determines the current fall-time, τ_2 its rise time, and t_0 is the time at which the current peak is initiated. The total charge injected in the node is the area under the $i(t)$ curve. The shape of one of these curves is represented in **Figure 1**.

Figure 2 depicts a 6-transistor SRAM (6T-SRAM) cell configuration. It has two cross-coupled inverters which form the two internal cell nodes (LN and RN). In addition, it has two access transistors, which are used to reach the internal nodes from outside the cell in the read and write operations.

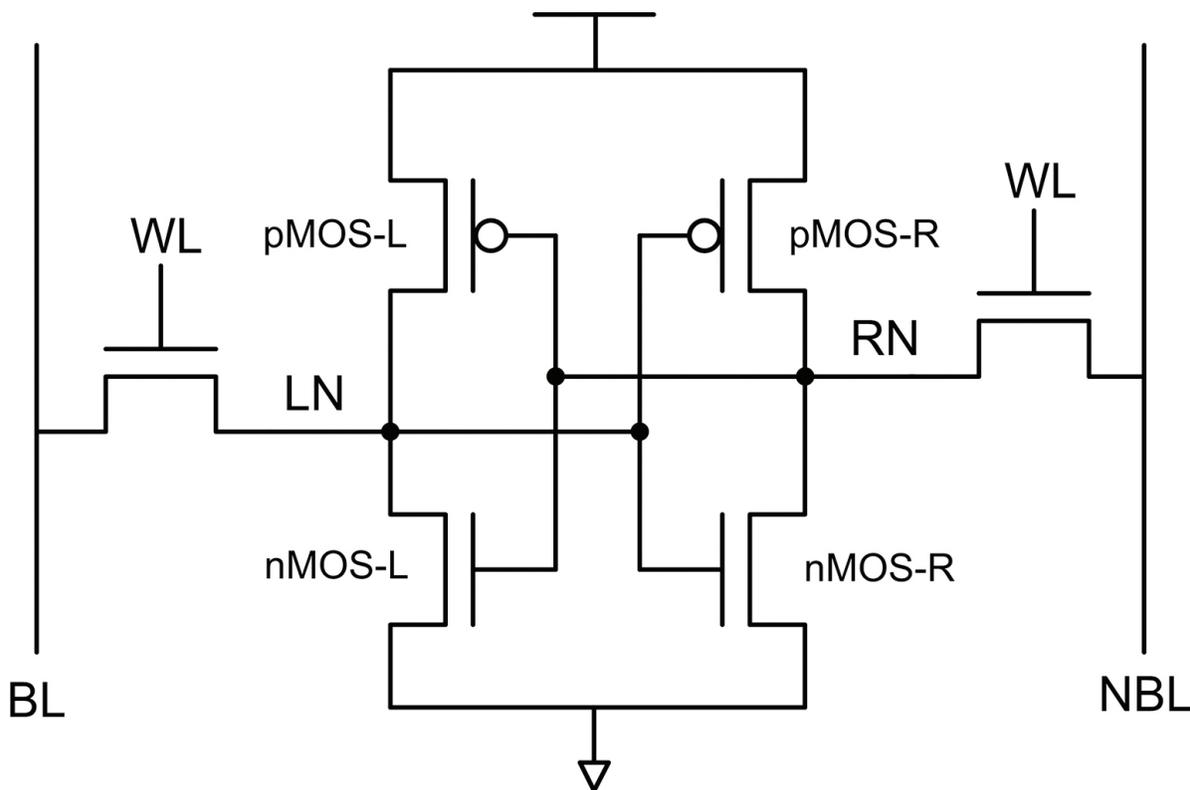


Figure 2. 6T-SRAM cell schematic.

Figure 3 shows the current sources scheme used to simulate SEUs. In particular, it is necessary to investigate two types of SEUs: a 0-to-1 SEU, where the impacted node is at 0 level, and a 1-to-0 SEU, where the impacted node is at 1 level. Due to cell symmetry, only two configurations cover all possibilities of memory cell perturbation. **Figure 3** also shows that a charge injection on a node which is at 0 requires the nMOS transistor to drain the collected charge due to the particle hit. Conversely, when a particle hits a node which is at 1, the pMOS transistor maintains the stored value by providing the current needed to hold the node electrical value.

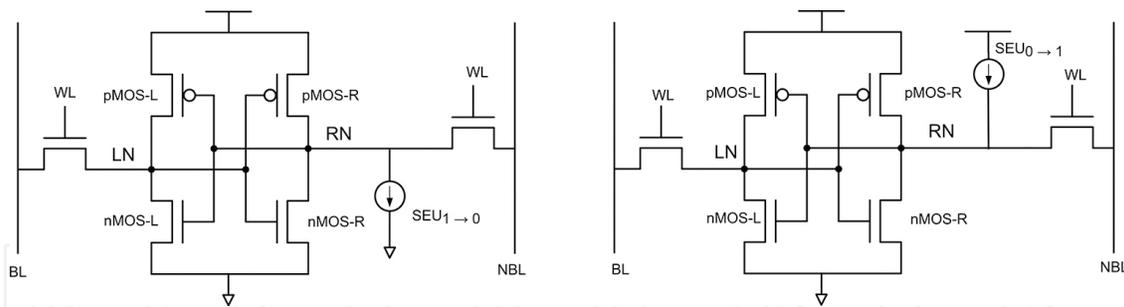


Figure 3. 6T-SRAM cell schematics for simulating a 1 to 0 SEU (left) and a 0 to 1 SEU (right).

This chapter deals only with 6T SRAM cells, although there are other SRAM which are specially designed to deal with radiation issues. In general, they are hardened SRAM cells that maintain their stored data even if the electrical state of some of their nodes is flipped by a particle strike, some of them are described in [10, 11]. The main drawbacks of them are the increase in cell transistor count with the consequent area increase. In addition, in these cells, it is difficult to implement regular cell layouts, which, as it will be described in Section 3, is a useful method for parameter variation minimization. Furthermore, nonstandard cells complicate the possibility to include them in current SRAM and FPGA design flows. Conversely, the technique that will be described in Section 3 is fully compatible with SRAM memory compilers and easily adaptable to current FPGA designs. Other mitigation techniques, such as supply voltage increase [9], are not suitable to be implemented in many applications due to their impact on power consumption and long-term reliability.

3. SRAM cell transistors channel width modulation technique

Memories are usually structures in which the maximum density of integration is requested. Therefore, the transistors forming memory cells are usually close to the minimum dimensions enabled by technology. Nevertheless, this section describes how it is possible to achieve more robust SRAM cells by varying the channel width of some of the cell transistors. This technique has a clear impact on the area occupied by each cell and, therefore, in the total memory area. For this reason, we will study how to use the area increase in the most efficient way, that is, how to get some gain in critical charge with minimum additional area. Moreover, the impact of this technique in terms of power consumption, stability, and access time is characterized in Section. 4.4.

Designing SRAMs is a challenge as technology scales down mainly due to parameter variations. There are two main causes of mismatch between the cell cross-coupled inverters: polysilicon and diffusion critical dimensions, as well as implant variations [12]. The use of subwavelength lithography and reactive ion etching are two of the main causes that converts the drawn polygon corners on the layout mask into rounded shapes on the manufactured circuits. Although proper optical proximity corrections can minimize those distortions, these techniques alone cannot compensate all the distortions, especially as the lithography gap is

increasing with each successive technology node [12]. As a result, traditional cell designs are very sensitive to misalignment because they include transistor diffusion width changes. These changes in width produce bends and steps in the diffusion regions, which in turn, cause small variations of the poly placement that lead to significant poly-diffusion overlay misalignment. This variability impacts directly on transistor matching, which can compromise cell stability and functionality.

The so-called regular cell layouts (**Figure 4**) have shown to be more tolerant to parameter variations due to several factors: all poly lines are drawn in the same direction, poly lines are aligned facilitating better polysilicon critical dimension control, and helping phase shift masking techniques [13]. In addition, when a cell is inside the SRAM array, all transistors see the same polysilicon patterns, thus minimizing poly proximity issues [12]. Finally, regular cells have straight diffusions and, therefore, are much less sensitive to misalignments [14, 15].

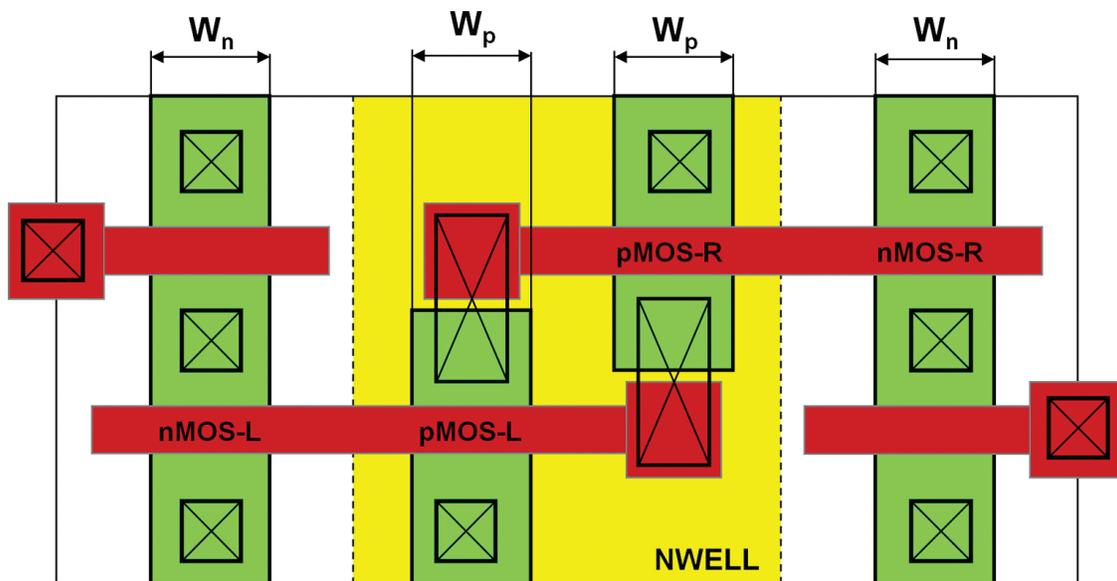


Figure 4. 6-T SRAM regular layout.

Parameter variation has become a key factor in SRAM memory design. For this reason, the regular layout is the one that is considered in this chapter. Using regular layouts imposes geometrical restrictions, for example, as previously mentioned, it is necessary to orientate all polysilicon lines in the same direction and keep them aligned. However, the determining factor that mainly affects the transistor channel width modulation technique is the impossibility to introduce steps and bends in the diffusion areas. This means that the designer will be unable to freely change SRAM transistors channel widths.

The formation of bends in the diffusion regions of a cell, like the one considered in **Figure 4**, can be avoided if all nMOS transistors channel width (W_n) is the same, as well as all pMOS transistors channel width (W_p) is also the same. In **Figure 4**, it can be seen that this way the diffusion areas (colored in green) remain straight. If we consider as a reference a cell where channel width of all transistors is the minimum (W_{min}), the restriction is expressed as

$$\begin{aligned} W_n &= r_n \cdot W_{\min} \\ W_p &= r_p \cdot W_{\min} \end{aligned} \quad (2)$$

With these two restrictions, the nMOS channel width can vary independently from the pMOS channel width. This implies that the designer has two degrees of freedom.

3.1. Critical charge results

As it was mentioned before, the behavior of the cell undergoing a current injection due to an energetic particle impact depends on the duration of the pulse (pulse width); for this reason, it is interesting to use it as a parameter to explore.

Pulse widths of current transients are highly variable and depend on multiple parameters, but several studies show that they are between a few picoseconds and hundreds of picoseconds [6]. 3D simulations also show that short pulses correspond to ionization events whose track crosses the drain of a cut-off transistor, while long ones are the result of events whose track does not pass through the drain [9]. It is necessary to consider both cases, since the location of the trace ionization with respect to drain is a random parameter. For this reason, to characterize the behavior of the cell, simulations with pulse widths ranging between 20 and 200 ps have been performed.

In addition, there are two different critical charges depending on which node (the one at 0 or the one at 1) receives the collected charge modeled by the current injection. The collection of electrons by the drain junction of an nMOS in OFF state results in a current pulse that upsets the affected node from 1 to 0, so this critical charge is named $Q_{\text{crit,e}}$. Similarly, the collection of holes by a pMOS drain junction upsets the affected node from 0 to 1, so this critical charge is called $Q_{\text{crit,h}}$. If both critical charges are represented as a function of pulse width, **Figure 5** is obtained.

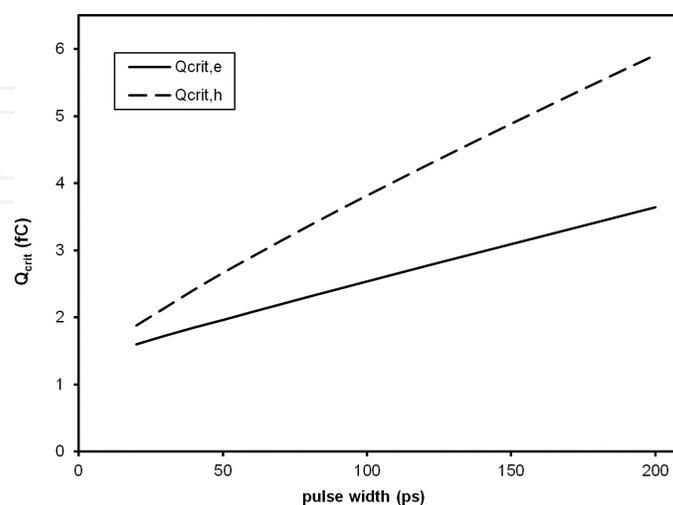


Figure 5. Critical charge for electrons and holes of a minimum-sized 6T-SRAM ($r_n = r_p = 1$) as a function of pulse width.

It can be observed that $Q_{crit,e}$ is lower than $Q_{crit,h}$. Therefore, it is normally considered that the cell-flip process is dominated by $Q_{crit,e}$ and sometimes $Q_{crit,h}$ is neglected. However, accurate models need to include both critical charges, as it will be shown in Section 4.4.

In addition, critical charges for a 6T cell for various combinations of W_p , W_n were calculated. **Figure 6** shows the results in a graph where the independent variables are r_p , r_n . Results are shown for two different pulse widths and only for $Q_{crit,e}$ since $Q_{crit,h}$ show similar results.

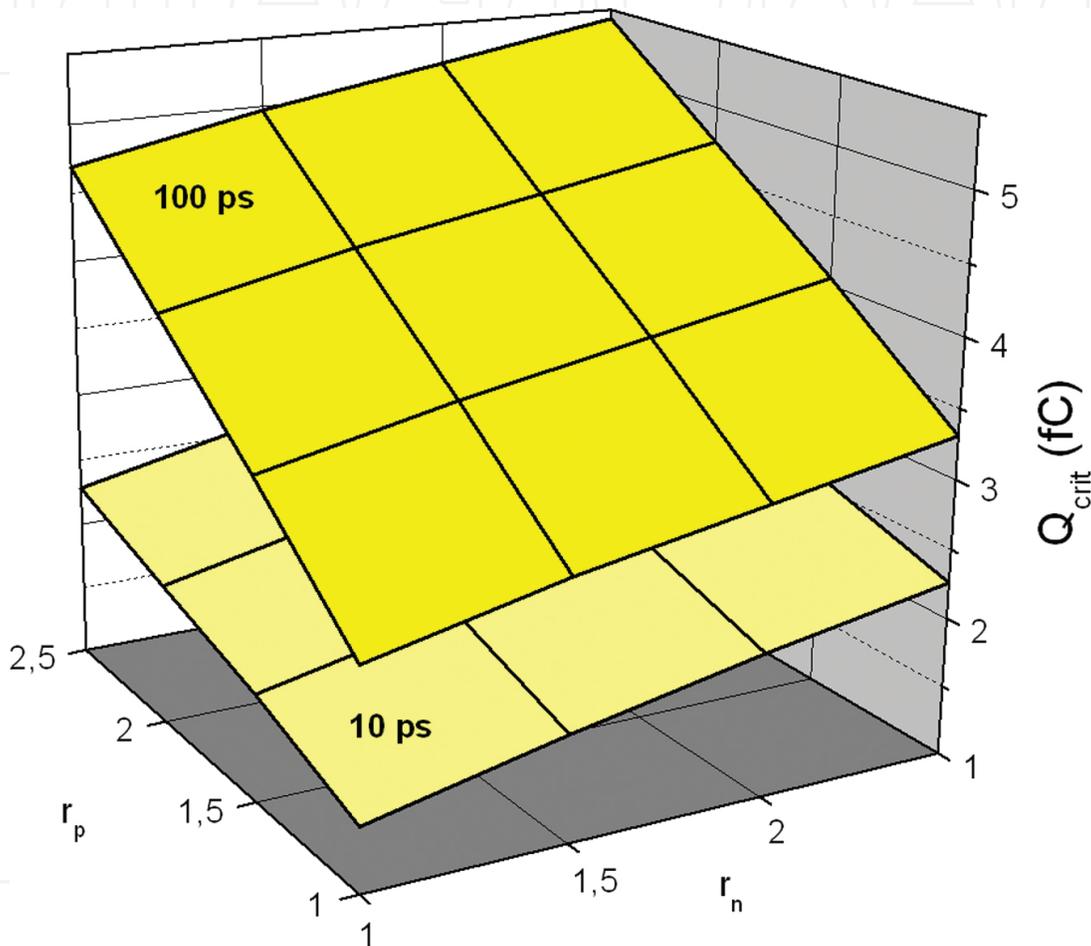


Figure 6. Critical charge ($Q_{crit,e}$) as a function of r_n and r_p and for two different pulse widths.

Figure 6 shows how the cell is more robust as the transistors channel width is increased. However, increasing the channel width of transistors produces a clear and undesired impact on the area of each cell and, therefore, on the total memory area. For this reason, it is necessary to establish a trade-off between the increased radiation robustness and the additional area used. Moreover, it is convenient to use the additional area in the most efficient possible way. This is discussed in the following subsection.

It has also been studied how the supply voltage affects cell robustness. **Figure 7** shows the results of critical charge for a typical alpha-particle pulse width of 30 ps [6] as a function of r_p , r_n for two different supply voltages.

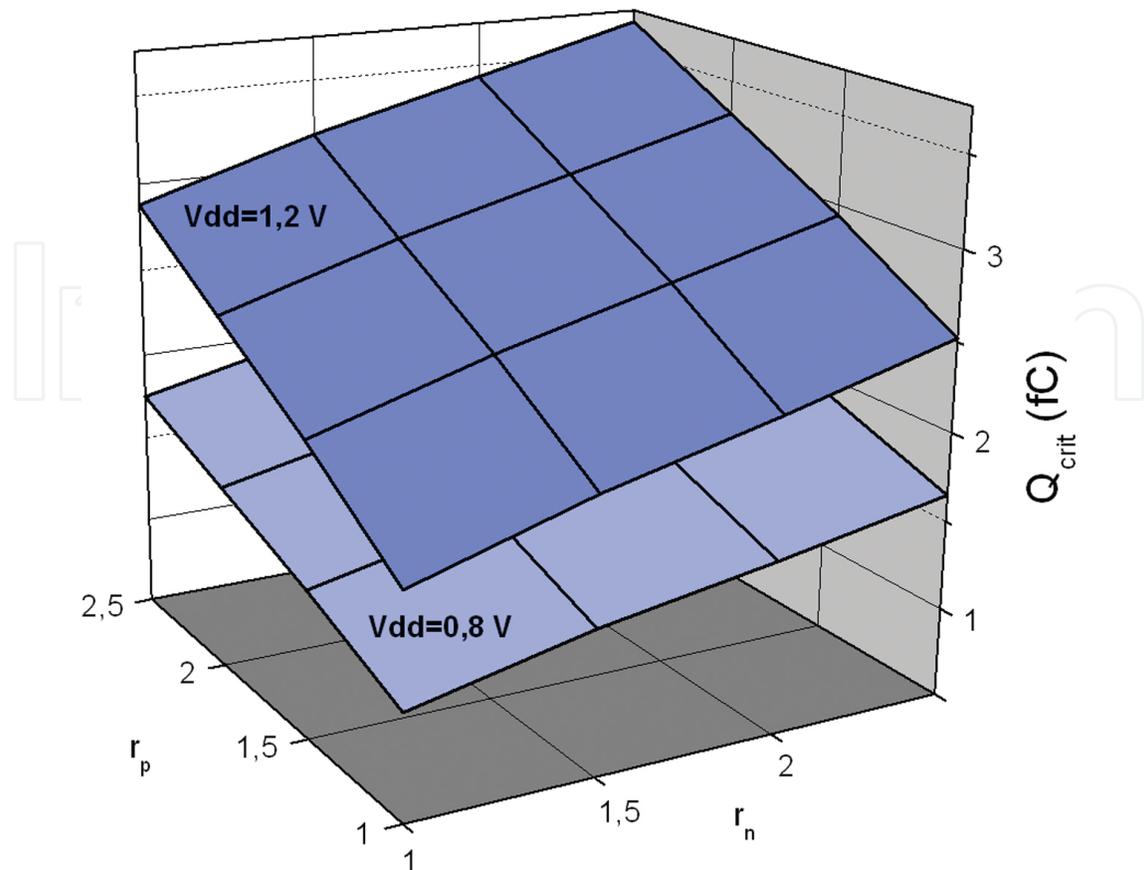


Figure 7. Critical charge ($Q_{crit,e}$) as a function of r_n and r_p and for two different supply voltages and for a 30 ps pulse width.

As it can be observed, a decrease in the supply voltage causes a reduction in the critical charge for all combinations of transistors channel widths. This result is in line with the previously mentioned fact that a cell with reduced voltage supply uses less charge to store data and, therefore, it is easier to change its stored value.

3.2. Additional area optimization to harden the SRAM cell

Due to the almost linear behavior of the graph in **Figure 6**, the following coefficients can be defined and are virtually independent of W_p and W_n :

$$\chi_p = \frac{\partial Q_{crit}}{\partial W_p} \quad \chi_n = \frac{\partial Q_{crit}}{\partial W_n} \quad (3)$$

These two coefficients represent the efficiency, in terms of critical charge, of a certain increase in the transistors channel width (pMOS in the case of χ_p , and nMOS in the case of χ_n). Geometrically, these coefficients represent the slopes in the two horizontal directions of the planes of **Figure 6**. These slopes vary as a function of the different pulse widths; therefore, coefficients are a function of the considered pulse width. If this dependence is plotted, **Figure 8** is obtained.

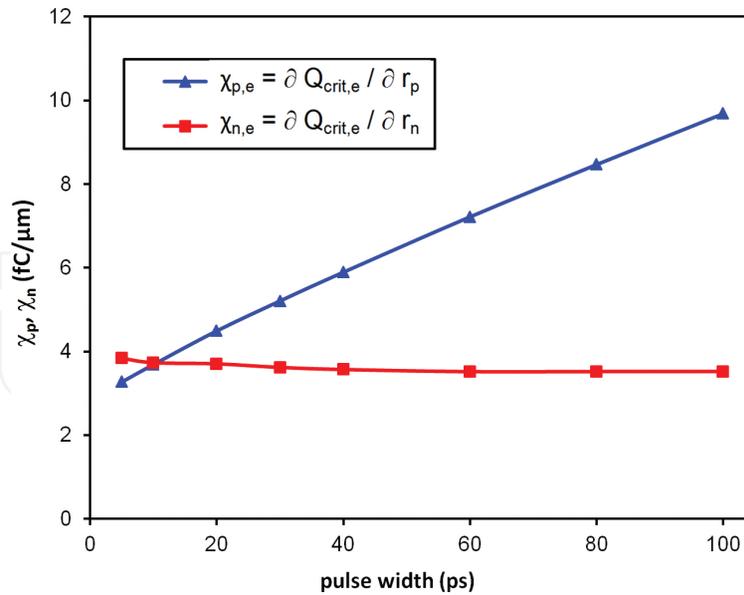


Figure 8. Dependence of $\chi_{p,e}$ and $\chi_{n,e}$ with pulse width for nominal supply voltage (1.2 V).

Figure 8 shows that, in general, χ_p is larger than χ_n only for very short pulses χ_n tends to equal or even exceed the value of χ_p . This means that for pulses longer than about 10 ps, increasing only pMOS transistors width (W_p) is more efficient than increasing nMOS transistors (W_n). As it has been mentioned before, the widths of the current pulses generated by SEU vary. However, for alpha particles, a typical pulse width is about 30 ps [6]. For this typical pulse width, increasing W_p is more efficient than increasing W_n .

Same simulations were repeated for 0.8 V supply voltage, the results are shown in **Figure 9**.

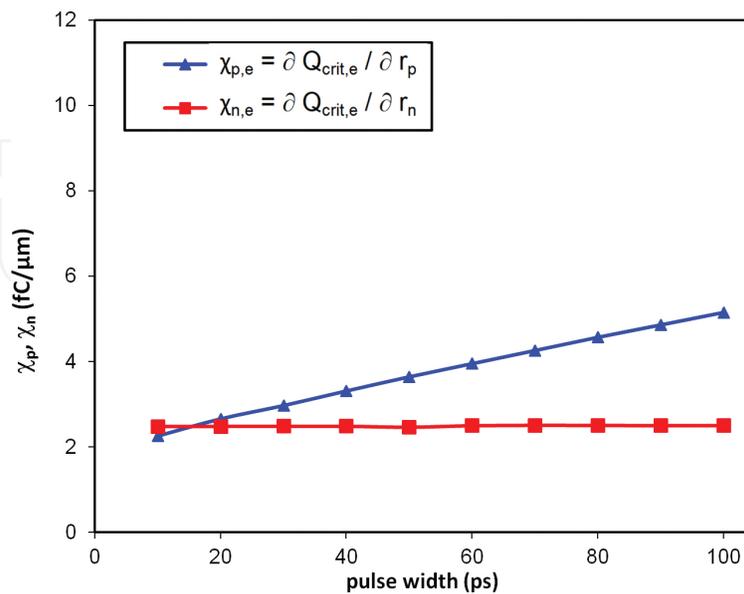


Figure 9. Dependence of $\chi_{p,e}$ and $\chi_{n,e}$ with pulse width for 0.8 V supply voltage.

The results obtained are analogous to those of **Figure 8**. However, the values of χ_p and χ_n at 0.8 V are lower than at 1.2 V (note that the graphs in **Figures 8** and **9** are represented at the same scale). This means that reducing the supply voltage not only reduces the critical charge but also reduces the efficiency in terms of critical charge to make wider pMOS transistors.

Finally, **Figure 10** plots χ_p as a function of the pulse width and supply voltage in a surface plot and as a family of curves generated by the supply voltage parameter.

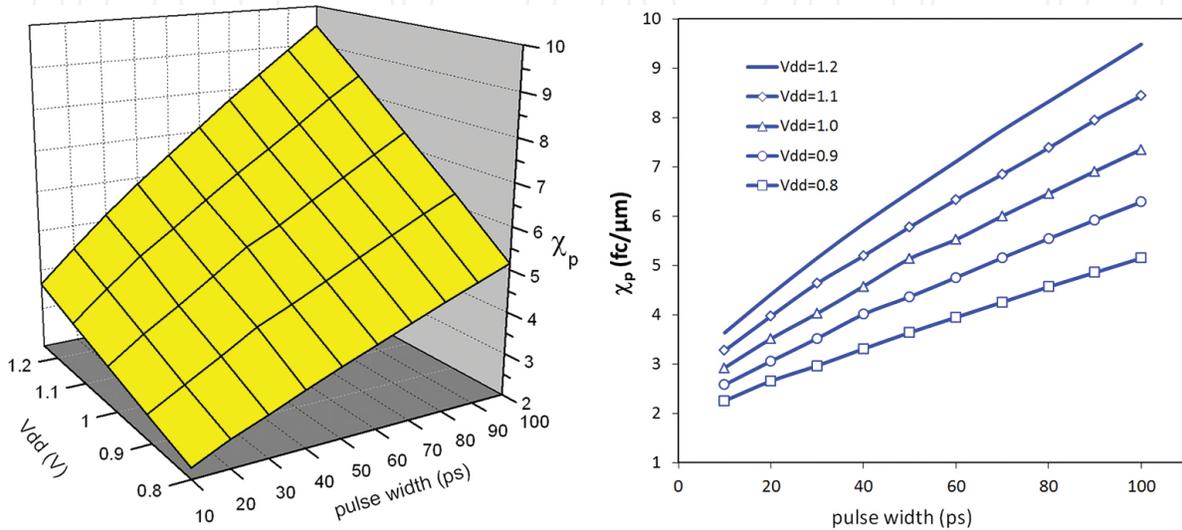


Figure 10. Dependence of $\chi_{p,e}$ with pulse width and supply voltage.

The graph in **Figure 10** shows that reducing both the supply voltage and the pulse width decreases the efficiency, in terms of critical charge, of modulating the pMOS transistors channel width.

From all the results presented in this section, it can be deduced that if the SEU robustness of an SRAM cell is to be increased in a certain percentage, increasing the widths of only the pMOS and leaving the nMOS unmodified is more efficient than any other combination of transistor width modulation. Or, for a given percentage area budget, increasing only pMOS widths maximizes critical charge.

r_p	W_p (μm)	$Q_{\text{crit},e}$ (fC)	$Q_{\text{crit},e}$ increment with respect to minimum cell (%)	Area increment with respect to minimum cell (%)
1.0	0.15	1.72	0	0
1.5	0.23	2.14	24	9
2.0	0.30	2.51	46	17

Table 1. Critical charge and cell area increment for three different values of r_p , and $r_n = 1$ ($W_{\text{min}} = 0.15 \mu\text{m}$). The supply voltage is nominal.

Table 1 shows the critical charges for a pulse of 30 ps for three values r_p (and $r_n = 1$) at nominal voltage. In addition, it shows the increased area with respect to the minimum sized cell ($r_p = 1, r_n = 1$). Areas are obtained by designing cells with the regular layout features and restrictions described earlier.

Table 1 shows that, for example, for an area increase of 17%, an increment 46% in critical charge is achieved.

To sum up, the transistors channel width modulation technique has shown by simulation to be effective in terms of improving critical charge. For this reason, it was decided to implement and test this technique in a real memory prototype (test chip) described in Section 4.1.

4. Experimental results of the modulation technique

4.1. Test chip description

The transistor width modulation technique was implemented in a custom fabricated SRAM test chip in a 65-nm CMOS commercial technology. Memory cells are six-transistor (6T) cells and were implemented following regular layout design specifications to minimize parameter variations. The regular layout characteristics were described in Section 3, and include the use of straight diffusion regions and regular alignment of word line polysilicon lines.

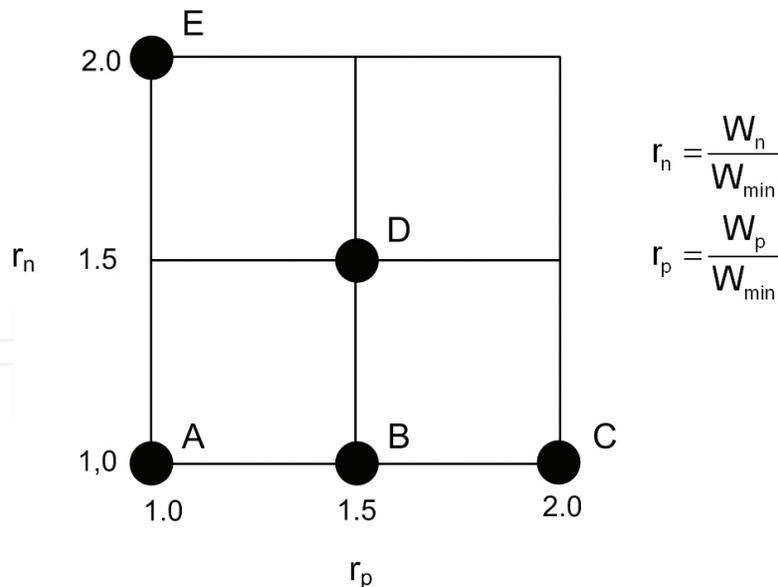


Figure 11. Schematic representation of the five cell types implemented in the test chip.

From all the previously simulated cells, five of them were implemented in the test chip (five different combinations of transistors channel widths). All these combinations satisfy the restrictions imposed for a regular layout. The selected combinations (cell types) of r_n and r_p are schematized in **Figure 11** and detailed in **Table 2**. For each one of the five cell types, a total of

4096 cells were implemented. Finally, the test chip was irradiated following the procedure detailed in Section 4.2 to experimentally test the modulation technique.

Cell type	pMOS width, W_p (μm)	nMOS width, W_n (μm)	Cell height (μm)	Cell width (μm)	Cell area (μm^2)	Cell area increment with respect to A (%)
A	0.15	0.15	0.58	1.75	1.01	0
B	0.23	0.15	0.58	1.91	1.10	9
C	0.30	0.15	0.58	2.05	1.18	17
D	0.23	0.23	0.58	2.07	1.19	18
E	0.15	0.30	0.58	2.05	1.18	17

Table 2. Main geometric features of the five cell types implemented in the test chip.

4.2. Experimental irradiation procedure

The objective of the experiment is to obtain the soft error rate (SER) of each one of the five cell types, that is, the number of soft errors (SEUs) for time unit.

The 65-nm CMOS test chip was mounted on a specifically designed PCB and controlled by an FPGA to drive and capture data.

As a radiation source, it was used an Am-241 alpha source with a 5 kBq activity providing alpha particles of 5.5 MeV. The source active area was 7 mm in diameter and was placed atop the unencapsulated chip, and all five cell types were irradiated at the same time. The control FPGA was not irradiated because the objective of the experiment was only to study the behavior of the test chip SRAM cells under radiation conditions.

The test procedure was performed following the subsequent steps:

1. Write all memory cells to a known value.
2. Read all memory cells, and compare to the written values.
3. Initiate the memory radiation.
4. Wait for a sampling time T_s .
5. Read the whole memory and determine the number of cells whose state changed. Go to Step 4.

Steps 4–5 were cycled until the experiment was finished. The overall number of SEUs, N_{TOT} , is given by the addition of the number of SEUs recorded at each sampling period (N_i), i.e.

$$N_{\text{TOT}} = \sum_{i=1}^n N_i \quad (4)$$

with n being the number of times that the memory is read. The overall time experiment (t_{exp}) is given by $t_{\text{exp}} = nT_s$. The SER at each sampling time period (SER_i) is given by $\text{SER}_i = N_i/T_s$, while the mean SER of the overall experiment is given by

$$\text{SER} = \frac{\sum_{i=1}^n \text{SER}_i}{n} = \frac{\sum_{i=1}^n N_i}{n \cdot T_s} = \frac{N_{\text{TOT}}}{t_{\text{exp}}} \quad (5)$$

The determination of the sampling period T_s is important, since it must guarantee that the probability of a given cell to experience two or more flips within the same sampling period is negligible, while keeping the overall read time small with respect to the overall hold time (we are interested in computing the memory SER when the memory is not being accessed) [16]. We ran an initial experiment using a small one-minute T_s value and determined an SER order of magnitude of 1 SEU/minute. Based on this, we set a T_s value of 30 min to not increase the memory read rate. The mean estimated SEU error using this T_s value is 1‰.

4.3. Experimental results

The experiment was conducted under the conditions and procedure described in Section 4.2 for a total time of 72 h to accumulate enough SEUs as to obtain a reliable SER result.

The SEU count evolution is shown in **Figure 12**. As expected, results show that the accumulated SEU count with time is linear. An alternative way to calculate SER is by obtaining the slope of the plot of accumulated number of SEU as a function of time.

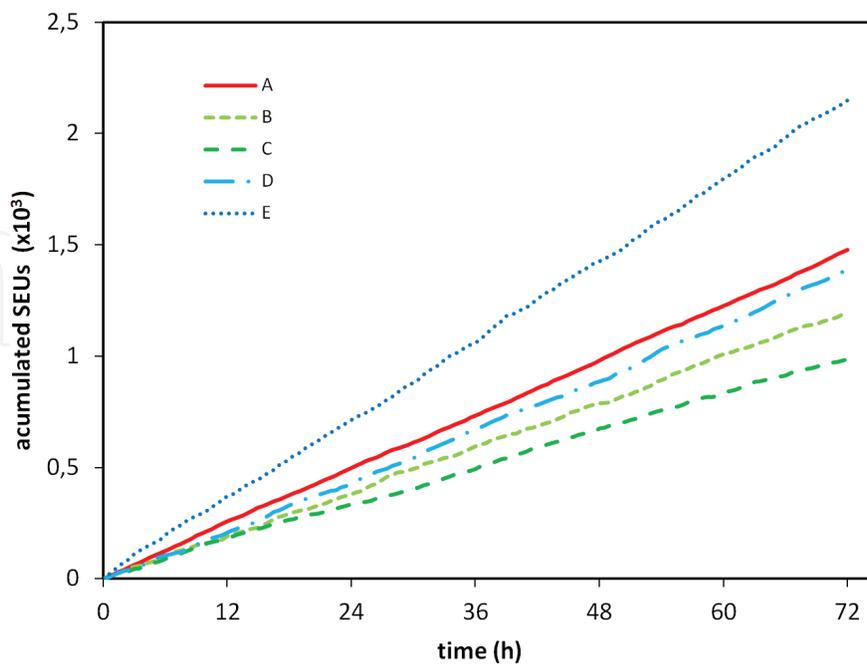


Figure 12. Accumulated SEUs in a 72 h period irradiation for the five cell types.

The first important result from **Figure 12** is that different memory cell types have different SER values (i.e., different slopes). If each SER is computed and represented in a bar plot, **Figure 13** is obtained.

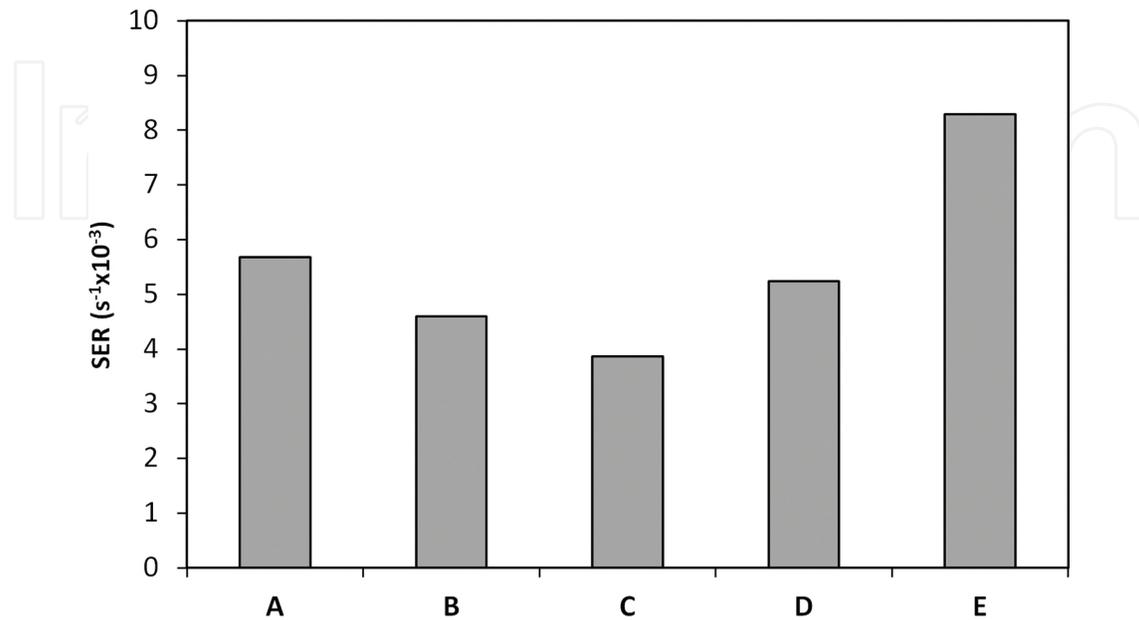


Figure 13. SER of 4096 cells for each one of the five cell types.

In addition, SER values are tabulated in **Table 3** along with critical charge results. Keep in mind that a more robust cell means more critical charge but less SER.

Cell type	SER ($s^{-1} \times 10^{-3}$)	$Q_{crit,e}$ (fC)
C	3.87	2.51
B	4.60	2.14
D	5.24	2.44
A	5.68	1.72
E	8.30	2.26

Table 3. SER and critical charge values for the five different cell types (sorted by SER value).

From **Figure 13** and **Table 3**, it is observed that the stronger cell—from a SER point of view—is the C, followed by B, and that the less robust is E. In addition, if critical charge is also taken into account, the following can be observed:

- The best cell is C; note that this occurs from both critical charge and SER points of view.
- Increasing the pMOS transistors channel widths (cells A, B, and C) causes an increase in critical charge, which directly results into a decrease in SER. That is, cell C is more robust than B, and B more robust than A, from both from critical charge and SER point of view.

- There is no the same direct correlation when cells in which nMOS transistors have been modified are involved. Cells D and E are among the most robust ones in terms of critical charge, and yet are among the ones that show worst SER.
- In Section 3.2, it was justified that increasing pMOS transistor widths was, from a critical charge point of view, the most efficient way to use the additional area. Cells B and C are the ones in which only pMOS transistor width is increased. From these results, it can be concluded that, in terms of SER, increasing only the pMOS transistors width is also the best way to improve SRAM cells robustness.

In short, increasing the pMOS transistors channel width improves critical charge and SER. However, increasing the nMOS transistors channel width improves critical charge, but worsens SER. The reason for this nonsymmetrical behavior must be sought in the fact that increasing critical charge by widening the channel of the transistors has a dual effect on SER:

- It increments cell robustness, because more charge is needed to flip the cell (higher critical charge).
- It lowers cell robustness because a wider transistors channel involves a sensitive area increase, which may also involve an increase in the ability of the cell nodes to collect the charge that has been deposited by an impacting energetic particle.

The key point is that the relative contribution of these two factors (critical charge and area increase) is not the same in the case of widening nMOS and pMOS transistors. Increasing the channel size of pMOS implies an area increase inside the well, while increasing the channel size of nMOS increases the area directly on the substrate. The different ability to collect charge of pMOS (in the well) or nMOS (on the substrate) is the qualitative explanation of the observed relation between SER and critical charge for nMOS and pMOS width modulation. This behavior is quantitatively explained in the following section.

4.4. Analysis of the results

Experimental data show that maintaining minimum nMOS transistors width ($r_n = 1$) while increasing pMOS transistor channel widths improves both critical charge and SER for a 6T memory cell. However, increasing nMOS transistor channel width improves memory cell critical charge, but worsens SER. As it has been mentioned before, this can be qualitatively explained as follows: Increasing transistor width has two competing effects on SER. On the one hand, SEUs are more difficult to occur, because Q_{crit} is raised due to the increase of both the drain capacity and the transistor width, which enhances transistor strength. On the other hand, widening a transistor increases its sensitive area, raising the probability of the cell to collect charge and thus be flipped by the effect of an energetic particle. The relative contribution of these two opposite effects on SER depends on the transistor type (nMOS or pMOS), especially for CMOS bulk technologies with well areas for pMOS transistors [17].

To model these two effects, it is necessary to use an expression that relates SER and critical charge. The following expression [18] will be used:

$$\text{SER} = \kappa \left(A_{\text{diff},n} \cdot e^{-\frac{Q_{\text{crit},e}}{\eta_e}} + A_{\text{diff},p} \cdot e^{-\frac{Q_{\text{crit},h}}{\eta_h}} \right) \quad (6)$$

where $A_{\text{diff},n}$ and $A_{\text{diff},p}$ are the nMOS and pMOS sensitive drain area. $Q_{\text{crit},e}$ and $Q_{\text{crit},h}$ are respectively the critical charges due to the collection of electrons and holes, and κ is a parameter that depends on the radiation flux. Parameters η_e and η_h represent electron and hole charge collection efficiency. To compute SER, parameters κ , η_e and η_h need to be experimentally obtained, as they depend on the environment and on the device precise characteristics. Note that the model includes both critical charges ($Q_{\text{crit},e}$ and $Q_{\text{crit},h}$) introduced in Section 3.1.

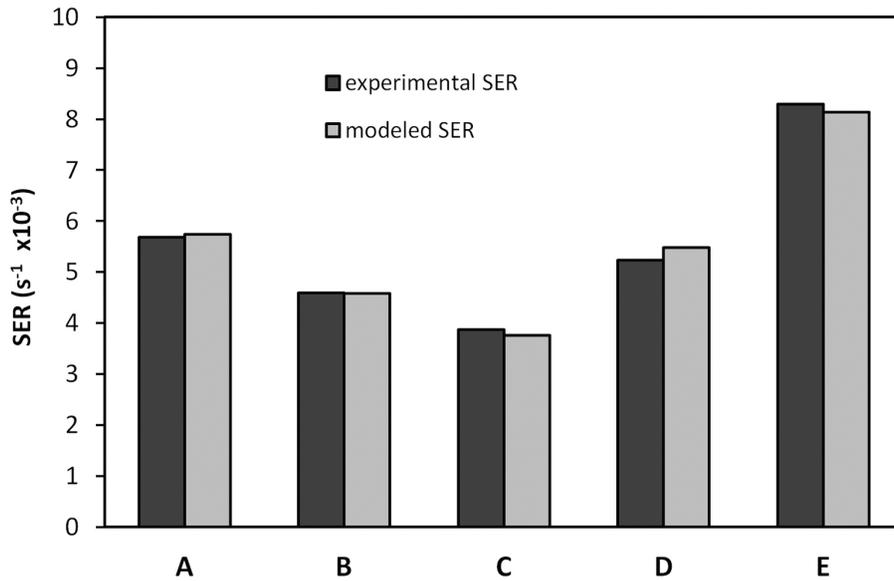


Figure 14. SER (experimental and modeled) of 4096 cells for each one of the five cell types.

In our case, since we obtained SER and critical charge for different cell types, we can fit SER experimental data to the calculated critical charge values and obtain the unknown parameters κ , η_e and η_h . Diffusion areas can be expressed as $A_{\text{diff},n} = W_n \cdot H_n$, and $A_{\text{diff},p} = W_p \cdot H_p$, being H_n and H_p the diffusion lengths of the drains of the nMOS and pMOS transistors. The design rules restrictions for symmetrical and regular cell layout impose H_n to be slightly longer than H_p (in fact we used the minimum possible diffusion length in the pMOS transistor, $H_p = H_{\text{min}}$, while $H_n = K_{\text{diff}} \cdot H_{\text{min}}$ with $K_{\text{diff}} = 1.1$ for the five different cells). Introducing again r_n and r_p coefficients defined in Eq. (2) we obtain:

$$\begin{aligned} A_{\text{diff},n} &= r_n \cdot W_{\text{min}} \cdot K_{\text{diff}} \cdot H_{\text{min}} = r_n \cdot K_{\text{diff}} \cdot A_{\text{min,diff}} \\ A_{\text{diff},p} &= r_p \cdot W_{\text{min}} \cdot H_{\text{min}} = r_p \cdot A_{\text{min,diff}} \end{aligned} \quad (7)$$

where $A_{\text{min,diff}} = W_{\text{min}} \cdot H_{\text{min}}$. Therefore, Eq. (7) becomes:

$$SER = \frac{K_A}{\kappa \cdot A_{min,diff}} \left(K_{diff} \cdot r_n \cdot e^{-\frac{Q_{crit,e}}{\eta_e}} + r_p \cdot e^{-\frac{Q_{crit,h}}{\eta_h}} \right) \quad (8)$$

The values of SER , $Q_{crit,e}$, $Q_{crit,h}$, r_n , r_p , and K_{diff} in Eq. (8) are known and, therefore, K_A , η_e and η_h remain as fitting parameters, being K_A the product of κ and $A_{min,diff}$. The obtained values after the fitting for these parameters are: $K_A = 3.13 \times 10^{-6} \text{ s}^{-1}$, $\eta_e = 2.02 \text{ fC}$, and $\eta_h = 0.79 \text{ fC}$.

Figure 14 compares the experimental and fitted SER . As it can be seen, Eq. (8) accurately describes the experimental SER as a function of critical charge and geometrical parameters. In addition, the model properly describes quantitatively the asymmetrical influence of nMOS and pMOS transistor width in terms of SER , which was previously interpreted qualitatively.

The experimentally fitted parameters and the resulting critical charge values from Eq. (8) allow to plot SER as a function of r_n and r_p . The resulting surface is shown in **Figure 15**.

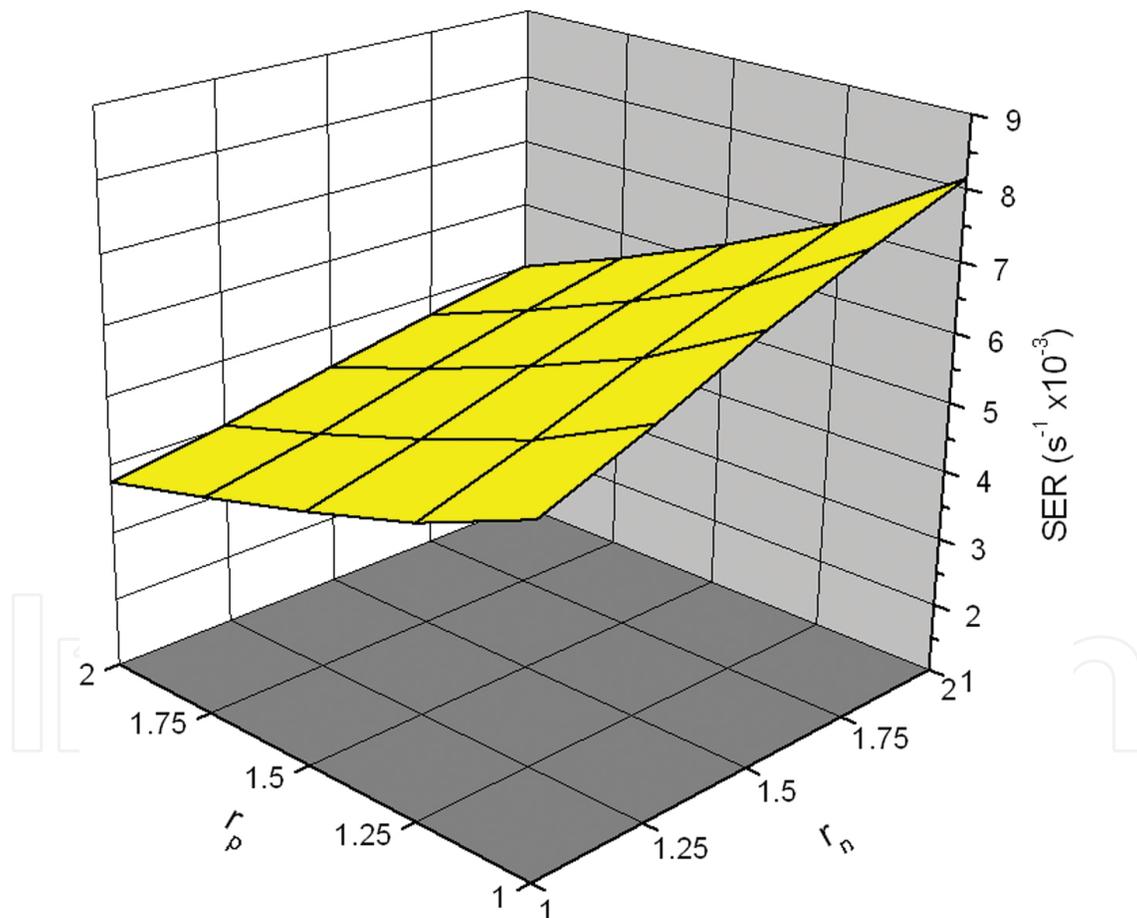


Figure 15. SER as a function of r_n and r_p .

Results of **Figure 15** confirm that increasing r_p leads to a SER reduction, whereas increasing r_n produces an undesired SER increment. This SER surface can be compared to the critical charge surface of **Figure 6**, where critical charge was improved as both r_n and r_p were increased.

If the charge collection efficiency values obtained as fitting parameters are analyzed, it is confirmed that charge collection efficiency for electrons (η_e) is higher than for holes (η_h) [19]. In addition, critical charge for electrons ($Q_{crit,e}$) is smaller than for holes ($Q_{crit,h}$). This electron and hole asymmetry in terms of charge collection efficiency and in terms of critical charge is the root cause of the observed differences of SER dependency with r_n and r_p .

Usual 6T-cells are designed with minimum sized access transistors ($W_{acc} = W_{min}$), minimum sized pMOS ($W_p = W_{min}$), and non-minimum-sized nMOS ($W_n = CR \cdot W_{min}$). The CR parameter is called cell ratio and is usually greater than 1, being the most frequent values between 1.5 and 2.5 as a trade-off to assure cell stability during write and read operations [3]. Note that this cell with this transistor dimensions does not have straight diffusions. In addition, also note that this cell has the internal latch (cross coupled inverters) equal to the ones in E cell.

From the irradiation experiments, it has been obtained that the C cell shows an SER that is a 46% of the E cell SER, that is, C cell receives less than half the number of SEUs per time unit than E cell. Note that this improvement is achieved only by adequate transistor sizing, because both cells (C and E) have the same area. If instead of considering this two cells, we compare the C cell with respect to a usual cell with $CR = 2$, then the SER of the C cell is a 57% the SER of the $CR = 2$ cell.

The effects of the transistor width modulation technique on power consumption and access time are summarized in **Table 4**. For example, it can be observed that C and E cells show similar access times and power consumption levels (although there is an increase of the energy needed to change the logic state of the C cell, it presents lower leakage current than the E cell).

Cell type	Leakage (pW/cell)	Write energy (fJ/cell)	Write time (ns)	Read time (ns)	RSNM (mV)	WSNM (mV)
A	125.5	4.65	0.32	0.28	168	468
B	134.2	5.93	0.33	0.28	178	429
C	144.1	7.10	0.35	0.28	184	346
D	163.8	6.45	0.36	0.27	165	468
E	180.6	5.59	0.36	0.26	149	517

Table 4. Summary of different power, speed and stability figures of the five different cell types.

Finally, it was also analyzed how the modulation technique affects read and write stability, by computing two well-known parameters: read static noise margin (RSNM) and write static noise margin (WSNM). As it can be seen in **Table 4**, RSNM is not very affected. Despite that, in [20], a technique to recover the RSNM of a 6T cell is analyzed. In addition, WSNM is degraded in some cell types (the ones in which pMOS transistors are increased in size). To overcome that, if needed, there are write assist techniques that could be suitable to improve WSNM [21, 22]. However, all tested cells types are experimentally writable with no write assist technique applied.

5. Conclusions

Due to technology scaling, radiation effects have become a major concern for modern integrated circuits even at ground level. FPGA SRAMS are not an exception, and radiation effects are even maximized, because these circuits are usually designed with transistors sizes close to the minimum allowed by technology. The so-called SEUs are the main radiation issue for SRAMs. SEUs are capable of altering the memory content of SRAM cells without permanently damaging the circuit.

A technique based on transistor width modulation was developed and tested. The technique consists in modifying the cell transistors channel width in a way that is compatible with the so-called regular layouts (i.e. avoiding the formation of bends in the diffusion regions). The main advantage of this layout scheme is that it reduces parameter variation. Nevertheless, it imposes some geometrical restrictions over transistor sizes, so that the modulation technique has to be designed to meet those constraints.

The technique was implemented and tested using two approaches: critical charge and experimental SER. Critical charge is a parameter cheap and easy to obtain, because it can be calculated using electrical simulations. However, as it was shown, it does not give a directly accurate measurement of the robustness of an SRAM cell if transistor areas are modified. Conversely, SER is a better parameter to assess cell robustness. The main drawback of SER is that it can only be directly obtained with experimental measurements, which are expensive and time consuming. After a preliminary analysis, the most interesting transistor size combinations were selected and implemented in a custom-fabricated test chip. The test chip has 4096 cells of each one of the five selected cells types, and all of them were irradiated with alpha particles to experimentally obtain SER.

Results show that some of the cell types are much more robust to radiation than others. In addition, results also reveal that, while a larger critical charge can lead to a better SER, some memory cells with higher critical charge also exhibit worst SER. This behavior was found when increasing nMOS channel widths. This suggests that special care must be taken when comparing SRAM cells with different transistor areas using critical charge as a figure of merit. Despite that, results indicate that SER can be estimated from critical charge with a model if some cell intrinsic cell parameters are known.

Results also show that SER is improved by increasing the pMOS transistors channel width (W_p), and worsened when the nMOS transistors channel width is increased (W_n). For this reason, the best way to design a hardened 6T SRAM cell is by minimizing the nMOS transistors channel width and dedicating all additional area to increase pMOS transistor channel width. In addition, for a 65-nm CMOS commercial technology, SER was reduced to a 57% of the value that conventional nonstructured layout cells exhibit. Due to careful transistor sizing, this radiation robustness improvement was achieved with minor area penalty. However, this hardened cells with wider pMOS transistors, also show a reduction in cell writability. To overcome this issue, write assist techniques can be implemented. Nevertheless, if a trade-off between writability, area, and radiation robustness is achieved by proper transistor sizing,

hardened cells remain writable without any further action. Finally, with the modulation technique presented in this chapter, the achieved cell radiation robustness gain is fundamentally an area trade-off, provided that the cell remains writable. For this reason, at design level, radiation robustness can be set as an adjustable parameter in memory compilers.

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