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Screen-Printed Front Junction *n*-Type Silicon Solar Cells

Yuguo Tao

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Abstract

This chapter aims to provide students/engineers/scientists in the field of photovoltaics with the basic information needed to understand the operating principles of screen-printed front junction *n*-type silicon solar cells. The relevant device fabrication processing is described, from texturing, diffusion, passivation and antireflection coating, to screen-printed and fired-through metallization as well as the technologies that are currently used for most industrially produced solar cells. A brief description of the characterisation approaches is given and discussed for an understanding and analysis of the loss mechanisms in a finished cell, including resistance loss, recombination loss, and optical loss. The application of advanced cell concepts and the improved technologies for further increasing cell efficiency, such as selectively doping structure and tunnel oxide passivated contact, are addressed for screen-printed front junction *n*-type silicon solar cells.

Keywords: screen printed, front emitter, *n*-type silicon solar cell, recombination, surface passivation

1. Introduction

Photovoltaics is the process of converting sunlight directly into electricity using solar cells. For the past few decades, the main research tendency in solar cells has been to develop cells which are both highly efficient and also cost-effective. Because of the abundance and nontoxicity of silicon, the fabrication simplicity, and the vast amount of accumulated knowledge in processing developed in the integrated circuit industry, silicon wafer-based solar cells dominate the very dynamic photovoltaic market. Silicon solar cells generate electricity via absorbing photons and generating electron–hole pairs, which are separated by a *pn*-junction and flow to electrical contacts and then into an external circuit. Due to its relative insensitivity to the degradation caused by exposure to cosmic rays, *p*-type (typically boron doped) silicon solar cells have

dominated all industrial development for decades. Until the 1980s, the main application of photovoltaics was to power space satellites [1]. For today's industrial mass production for terrestrial electricity generation, a typical state-of-the-art p-type silicon solar cell with an homogeneous emitter and full aluminium back surface field (Al-BSF) has an efficiency of ~19% with the standard silicon nitride passivation and screen-printed silver paste metallization on the front. However, a lot of research has been being conducted in the field of n-type (typically phosphorus doped) silicon-based solar cells, because n-type silicon provides several advantages over p-type, including better tolerance to common impurities (e.g., iron) [2], high bulk lifetime, and no light-induced degradation due to the boron–oxygen complex formation [3]. Accordingly, n-type silicon solar cells with high efficiency can be potentially more cost-effective than p-type silicon-based cells. In addition, for either n-type or p-type silicon solar cells, electrical contacts are needed to extract carriers to an external circuit. In order to form electrical contacts, the silver paste screen-printing/firing-through technology is a very reliable and relatively simple process in today's silicon solar cell mass production. Hence, in this chapter, the focus will be on front junction n-type silicon solar cells with screen-printed and fired-through contacts on both sides, including their operating principles, fabrication processes, and more advanced cell concepts.
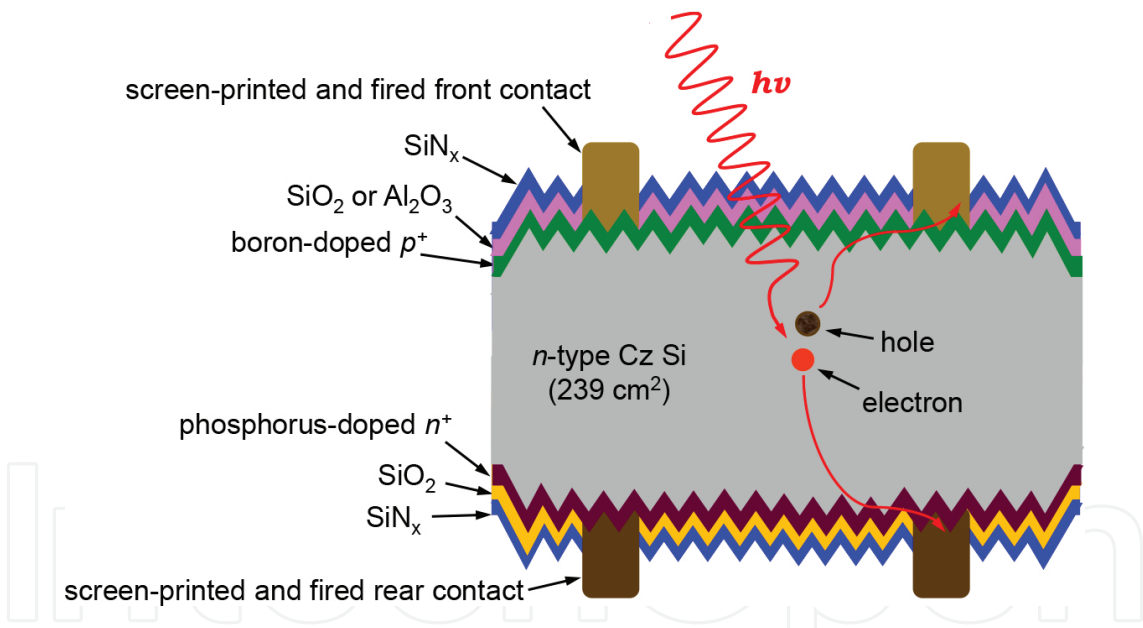
Figure 1. Schematic structure of a screen-printed front junction n-type silicon solar cell in cross-section (not to scale), featuring bifacial architecture.

Figure 1 shows a schematic of the basic structure for a typical screen-printed front junction n-type silicon solar cell, which represents the passivated emitter and rear totally diffused (PERT) cell structure [4]. The bulk material is n-type silicon wafer with a resistivity of around 5 Ω cm (phosphorus doping level about $9.2 \text{E} 10^{14}$ cm^{-3}) and a thickness of ~180 μm. The wafer surface is randomly textured to form small size of pyramids to reduce surface reflection. Hence, more photons can be absorbed in the cell. The front emitter is boron-doped with a surface dopant concentration in the range of $8 \text{E} 10^{18}$ to $8 \text{E} 10^{19}$ cm^{-3}, and passivated by silicon dioxide (SiO_2) or

aluminium oxide (Al_2O_3). The back surface field is phosphorus-doped with a surface concentration of typically over $1E10^{20}$ cm^{-3} and passivated by SiO_2. A hydrogen-rich silicon nitride (SiN_x) on both the front and rear surfaces acts as a passivation layer and as an antireflective coating (ARC) layer. The electrical contacts on both sides are formed by screen-printing different silver pastes and then co-firing through SiN_x the layer at a high temperature (over 700°C). Note that this basic cell structure features a bifacial architecture, which can also collect radiation from the rear side of solar cell, and hence has the potential to achieve an increased energy yield in certain module configurations. To understand the operating principles of a silicon solar cell with this basic structure, the next section will describe the basic physics in detail.

2. Operating principles of a front junction *n*-type silicon solar cell

2.1. Energy-band diagram

Figure 2 shows the schematic energy-band diagram for the fundamental operating principles of a screen-printed front junction *n*-type silicon solar cell. The p^+ emitter region is formed by 'doping' the front side of an *n*-type silicon wafer with boron dopants in high concentration, and joining the p^+ region and the *n* region forms the *pn*-junction. Due to the doping concentration gradient across the *pn*-junction, electrons flow by diffusion from the *n* region to the p^+ region, and holes flow by diffusion from the p^+ region to *n* region. This leaves behind exposed charges on ionized doping atoms at lattice sites, which form the space charge region (SCR). These exposed charges build up an electric field that hinders the natural flow of electrons and holes until an equilibrium situation is reached. The built-up electric field causes a bending of the energy bands (E_V and E_C).
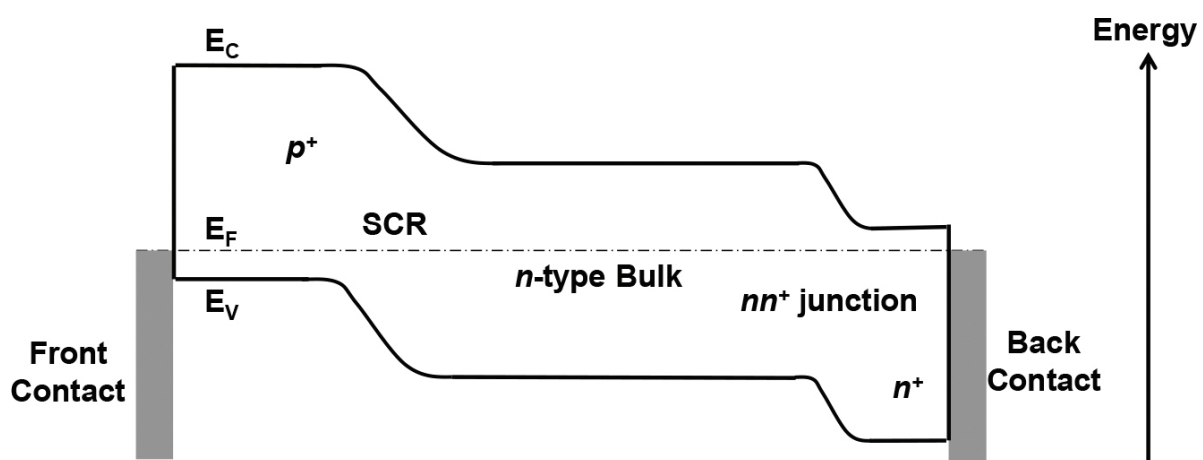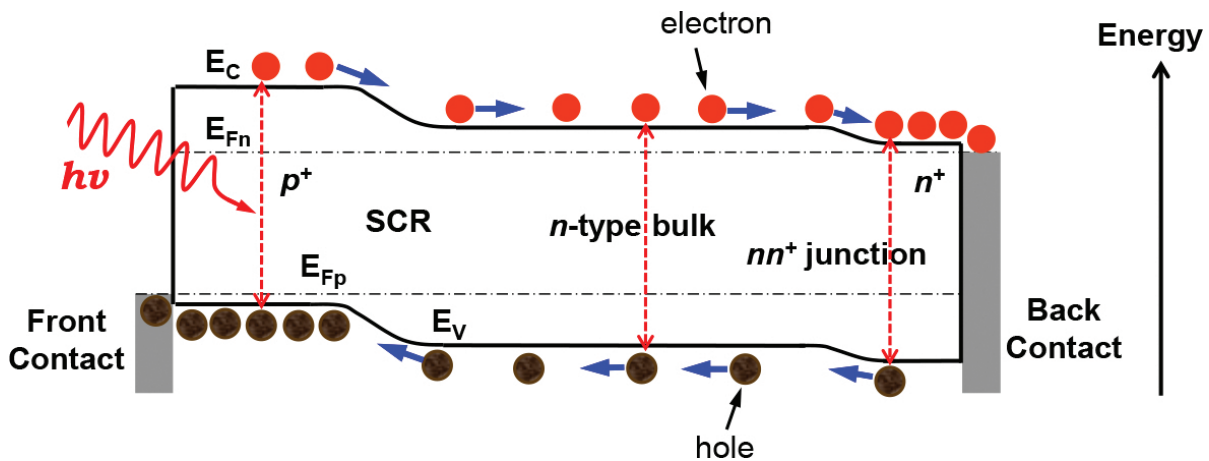

Figure 2. Schematic energy-band diagram of a screen-printed front junction *n*-type silicon solar cell in thermal equilibrium (without illumination or applied voltage), including p^+ emitter, *pn*-junction, space charge region (SCR), nn^+ high–low junction and n^+ back surface field (BSF).

The n^+ back surface field region is produced by 'doping' the rear side of n-type silicon wafer with phosphorus dopants in much higher doping concentration (typically over 1E10^{20} cm^{-3}) than in the n bulk region (typically about 1E10^{15} cm^{-3}). The formed nn^+ high–low junction induces a slight bending of the energy bands. In the case without illumination or applied voltage, the cell is in thermal equilibrium with a single, constant-valued Fermi level (E_F), as shown in **Figure 2**.

When the cell is illuminated, photons with energy greater than the silicon band gap energy are absorbed to excite electrons from the valence band to the conduction band, which generates an electron–hole pair (a hole refers to the missing electron in the valence band), as shown in **Figure 3**. The generated electrons and holes can diffuse within the solar cell until they reach the SCR, if they do not recombine. Then, the electric field at the pn-junction separate these carriers by sweeping electrons to the n region and holes to the p^+ region. The induced nn^+ high–low junction also can sweep holes away the back surface field and the back contact, and hence reduce the back surface recombination. In the case of illumination, quasi-Fermi levels (E_{Fn} for electrons and E_{Fp} for holes) are used to analyse the solar cell in non-equilibrium. To allow electrical contacts to extract carriers from both front and back sides, E_{Fp} is essentially continuous with the Fermi level of the front contact metal, while E_{Fn} is at the same energetic position with the back contact metal. In the bulk quasi-neutral regions, both E_{Fp} and E_{Fn} are approximately constant. In the p^+ emitter region, the electrical contact is described as an ohmic contact. In the n^+ back surface field region, the contact is of a Schottky-type that the contact metal induces a barrier to majority carriers (electrons), which gives rise to an undesirable contact resistance. Therefore, to obtain a decent cell performance, a proper doping profile in both the p^+ and the n^+ regions is needed.

Figure 3. Schematic energy-band diagram of a screen-printed front junction n-type silicon solar cell in a non-equilibrium (with illumination); including photon absorption, carrier generation and separation.

2.2. Solar cell output parameters

The *Ideal Diode Law* (one-diode model) is often used to describe an ideal silicon solar cell, which is expressed as

$$J = J_0 \left[\exp\left(\frac{qV}{kT} \right) - 1 \right] \qquad (1)$$

where J is the current density, J_0 is the saturation current density (the solar cell leakage current density in the dark), V is the voltage, q is the electronic charge, k is the Boltzmann's constant, and T is the absolute temperature. J_0 is defined as [5]

$$J_0 = \frac{qD_e n_i^2}{L_e N_A} + \frac{qD_h n_i^2}{L_p N_D} \qquad (2)$$

where D_e (D_h) is the diffusion constant of electrons (holes), n_i is the intrinsic carrier concentration, L_e (L_p) is the diffusion length of electrons (holes), and N_A (N_D) is the total density of acceptors (donors).

When the cell is illuminated, it is ideally modelled as

$$J = J_0 \left[\exp\left(\frac{qV}{kT} \right) - 1 \right] - J_I \qquad (3)$$

where J_I is the light-generated current density. At the short-circuit condition ($V = 0$), the maximum light-generated current density is the short circuit current density J_{sc}, hence $|J_{sc}| = J_I$.
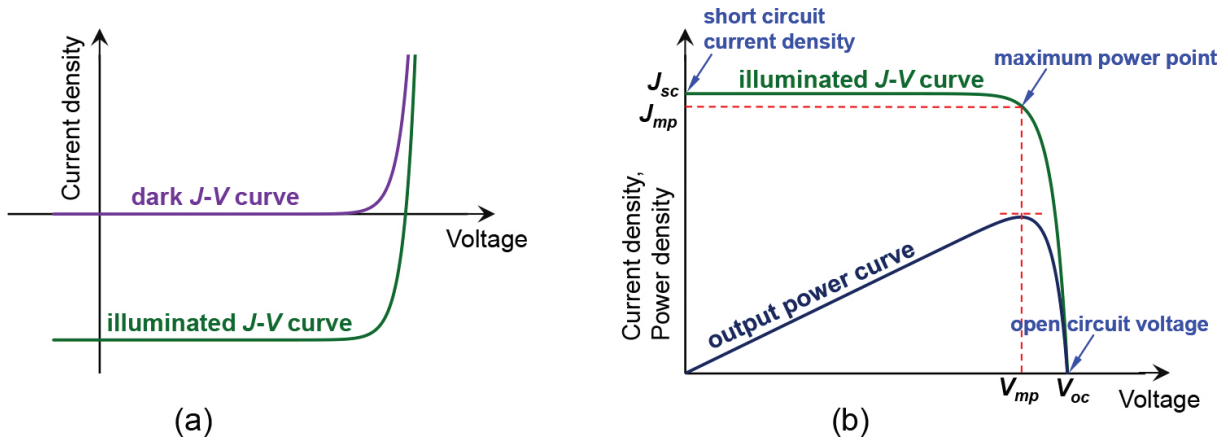
For an actual solar cell, Eq. (3) becomes

$$J = J_0 \left[\exp\left(\frac{qV}{nkT} \right) - 1 \right] - J_I \qquad (4)$$

where n is the ideality factor, and typically in the range of between 1 and 2.

The resulting dark and illuminated J–V curves by the diode law are shown in **Figure 4a**. The illuminated J–V curve is most often plotted with the output power in the first quadrant, as shown in **Figure 4b**, and represented by

$$J = J_I - J_0 \left[\exp\left(\frac{qV}{nkT} \right) - 1 \right] \qquad (5)$$

Figure 4. Dark and illuminated *J–V* curves of a silicon solar cell (a); a typical representation of an illuminated *J–V* curve as well as output power density curve as a function of voltage (b), including indication of the short-circuit point (0, J_{sc}), the open-circuit point (V_{oc}, 0), as well as the maximum power point (V_{mp}, J_{mp}).

In **Figure 4b**, the maximum power point (V_{mp}, J_{mp}) is indicated. The fill factor (*FF*) is a metric of the *pn*-junction quality and the parasitic resistance of a finished silicon solar cell, and defined as

$$FF = \frac{J_{mp}V_{mp}}{J_{sc}V_{oc}} \tag{6}$$

where V_{oc} is the open circuit voltage. At the open-circuit condition (J =0), the cell voltage is the V_{oc}.

Finally, the cell energy-conversion efficiency is defined as

$$\eta = \frac{J_{sc}V_{oc}FF}{P_{in}} \tag{7}$$

where P_{in} is the total power density of the light incident on the solar cell. For an ideal single junction crystalline silicon solar cell (energy band gap E_g =1.12 *eV* at 25°C), its theoretical efficiency limit is about 30%, based on a detailed balancing of incident and generated power density [6]. The major fundamental loss mechanisms in an ideal silicon solar cell include: (1) photons with energy less than 1.12 eV ($E\_photon < E\_g$) cannot be absorbed (directly transmit through the cell); (2) the excessive energy in the photons with high energy ($E\_photon > E\_g$) is wasted as the generated electron–hole pair relax back to the edges of respective carrier band (electrons back to conduction band, and holes to valence band) through thermalization; and (3) the split between the two quasi-Fermi levels must stay within two energy gap ($| E\_Fn - E\_Fp | < E\_g$).

2.3. Resistance loss

Actual silicon solar cells generally have a parasitic series resistance (R_s) and a shunt resistance (R_{sh}). Both R_s and R_{sh} have a negative impact on *FF* and cause ohmic losses. For a screen-printed front junction *n*-type silicon solar cell, **Figure 5** shows the schematic components of total R_s in a finished cell, including: (1) sheet resistance of the p^+ emitter layer ($R_{emitter}$) and the n^+ back surface field layer (R_{BSF}); (2) bulk resistance of *n*-type wafer ($R_{substrate}$); (3) metallic resistance of the front gridline (R_{finger}) and the rear gridline (R'_{finger}); (4) contact resistance between screen-printed metal contacts and silicon on the front side ($R_{contact}$) and the rear side ($R'_{contact}$); and (6) metallic resistance of the front bus-bar (R_{busbar}) and the rear bus-bar (R'_{busbar}). The specific values of these components can be approximately estimated by the approach developed in [7].
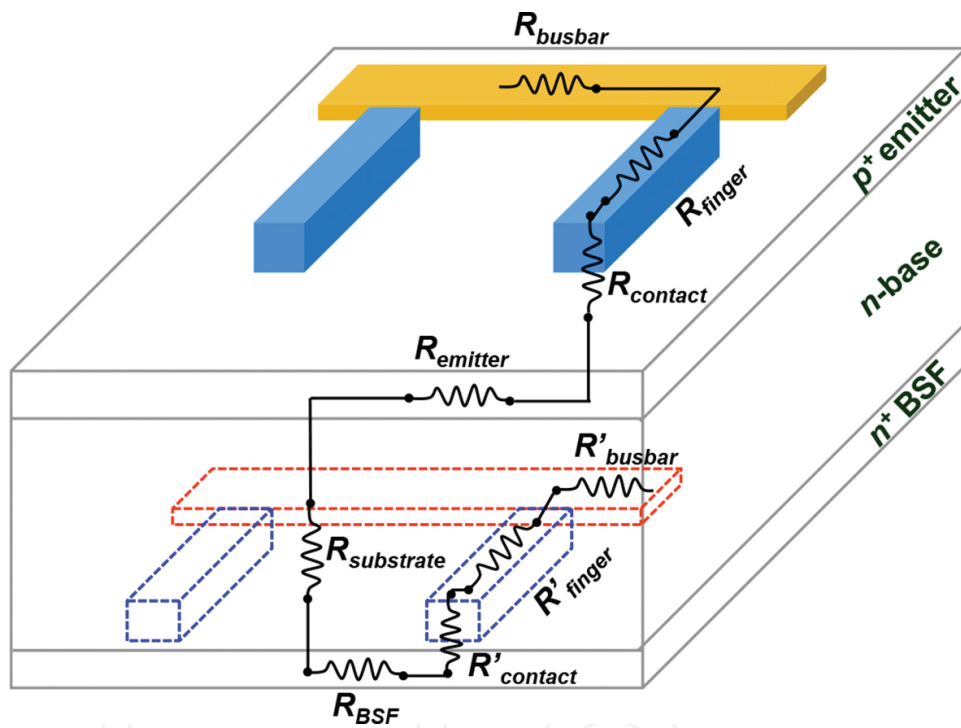
Figure 5. Schematic structure of major components of series resistance (R_s) in a screen-printed front junction *n*-type silicon solar cell.

The R_{sh} is particularly due to the non-ideality of the *pn*-junction and some defects near the junction, especially around cell edges. Consequently, in reality, the illuminated *J–V* curve of a screen-printed silicon solar cell with R_s and R_{sh} is given by

$$J = J_I - J_0 \left\{ \exp\left[\frac{V + AJR_s}{\left(\frac{nkT}{q} \right)} \right] - 1 \right\} - \frac{V + AJR_s}{AR_{sh}} \tag{8}$$

where A is the total area of a solar cell, and typically about 239 cm² for the industrial pseudo-square n-type silicon solar cells. So, in order to design and fabricate a silicon solar cell with high-efficiency performance, minimizing the ohmic losses is necessary. In addition, carrier recombination after generation can also degrade the cell performance as described in the following section, so it should be minimized as well.

2.4. Recombination loss and saturation current density

The generated electron–hole pair can recombine if they are not efficiently separated and collected. There are typically three recombination mechanisms that can occur in parallel in silicon solar cells. First, radiative recombination is the process that electron makes a band-to-band transition while emitting a photon as light. Hence, it is the reverse of the light absorption. But it is often neglected for silicon solar cell, because silicon is an indirect-band-gap material and a phonon is required for this type of recombination. Second, Auger recombination refers to electrons and holes that recombine and use the excess energy to excite a free carrier. Then, this excited free carrier relaxes back to its original energy status by emitting phonons. This type of recombination is particularly effective in the heavily doped regions with doping concentration over 10^{17} cm⁻³, for instance, the p^+ emitter and the n^+ back surface field regions in screen-printed n-type silicon solar cells. Third, recombination through traps, the so-called SRH recombination named from Schockley, Read and Hall [8, 9], is a very effective process whereby electrons relax from the conduction band to the defect levels (within the forbidden gap) that are created by impurities or defects, then relax to the valence band and recombine with holes. For industrial n-type silicon Czochralski wafers, this type of recombination is also very usual as the impurities induced during the entire device fabrication process introduce energy levels near the middle of the forbidden gap and become very effective recombination centres.

The carrier lifetime is typically used to define the time for recombination to occur after the electron–hole generation. Because the three recombination mechanisms occur in parallel, the silicon material bulk lifetime (τ_{bulk}) is given by

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{radiative}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{9}$$

where $\tau\_radiative$ is the radiative lifetime, τ_Auger is the Auger lifetime, τ_SRH is the SRH lifetime.

In addition, for crystalline silicon wafers, dangling bonds are present on the front and back surfaces, and introduce defect levels throughout the energy-band gap. Surface recombination velocity (s) is typically used to estimate the surface passivation quality and can be approximately calculated for a decently passivated surface ($s < 1000$ cm/s) by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2s}{d} \tag{10}$$

where d is the silicon wafer thickness, τ_eff is the effective lifetime. Both τ_eff and τ_bulk can be directly measured by the quasi-steady-state photoconductance (QSSPC) technique [10], hence s can be extracted.

For silicon solar cells, recombination after carrier generation not only reduces J_{sc} but also degrades V_{oc}. According to Eq. (4), the total saturation current density ($J_{0,total}$) has a strong impact on V_{oc}. At open-circuit condition, Eq. (4) becomes

$$V_{oc} = \frac{nkT}{q} ln\left(\frac{J_{sc}}{J_{0,\,total}} + 1\right) \tag{11}$$

In order to conduct a detailed analysis about the recombination contribution from each part of a finished screen-printed *n*-type silicon solar cell, $J_{0,total}$ can be estimated by

$$J_{0,\,total} = J_{0e} + J_{0b,\,bulk} + J_{0b} \tag{12}$$

where J_{0e} is the total saturation current density of front emitter side, including the passivated emitter regions and the metal contact regions, and is expressed by

$$J_{0e} = \left(1 - f_{front}\right) \cdot J_{0e,pass} + f_{front} \cdot J_{0e,contact} \tag{13}$$

where f_{front} is the fraction of screen-printed metal contact coverage on the front emitter. $J_{0e,pass}$ is the emitter saturation current density of passivated regions and can be directly obtained from the lifetime measurement on symmetrical structures (passivation/p^+/n/p^+/passivation) by the QSSPC technique. $J_{0e,contact}$ is the metal-induced emitter saturation current density on the contacted regions and can be extracted by numerical modelling, i.e, two-dimensional simulations [11]. It also can be experimentally estimated on a specifically designed test sample structure, as shown in **Figure 6a**, by the following equation

$$2 \cdot J_{0e,\,measured} = \left(J_{0e,contact} - J_{0e,pass}\right) \cdot f_{front} + 2 \cdot J_{oe,\,pass} \tag{14}$$
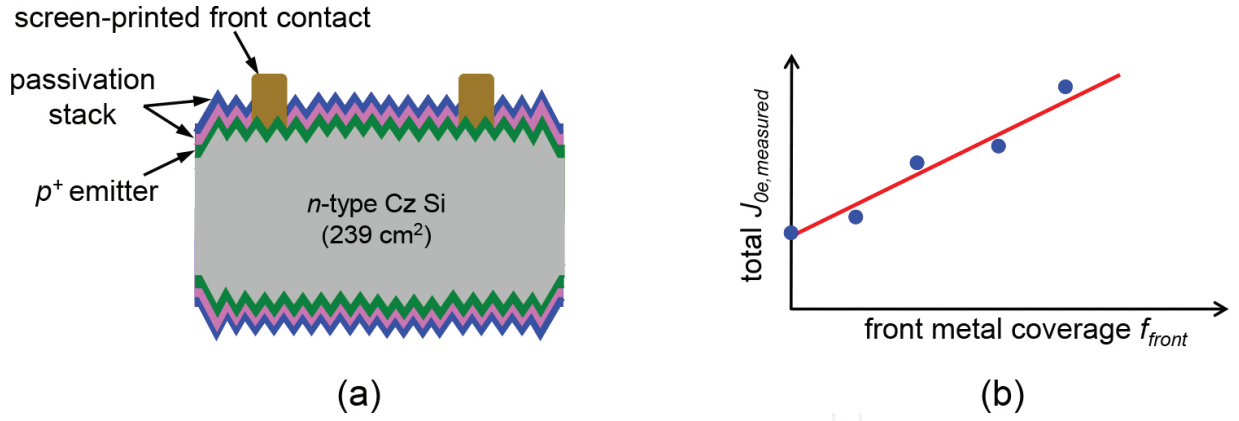
Figure 6. Schematic of a test sample symmetrical structure with screen-printed contact on one side for extracting $J_{0e,contact}$ (a); a typical representation of $J_{0e,contact}$ line fitting as a function of the front metal contact coverage f_{front} on the test samples (b).

where $J_{0e,measured}$ is the directly measured saturation current density value from the lifetime measurement on the test sample structure. So, $J_{0e,contact}$ can be extracted from the resulting slope of the line fitting, as shown in **Figure 6b**.

In Eq. (12), $J_{0b,bulk}$ is the saturation current density of substrate bulk region and is determined by bulk lifetime and the bulk resistivity. Although it is a limited validation, $J_{0b,bulk}$ can be approximately given by [12]

$$J_{0b,bulk} = qn_i^2 \frac{W}{N_D \tau_p} \tag{15}$$

where the intrinsic carrier concentration $n\_i = 8.3 \times 10^9 \ cm^{-3}$ [13]. N_D is the doping density of n-type silicon bulk region, i.e., $N\_D = 9.2 \times 10^{14} \ cm^{-3}$ for a bulk resistivity of 5 Ω cm. W is the silicon wafer thickness, typically about 180 μm. τ_p is the Auger lifetime with the specific value referred to [14].

Similar to J_{0e}, J_{0b} in Eq. (12) is the saturation current density of rear side on a finished cell, including the passivated back surface field regions and the metal contacted regions, and is given by

$$J_{0b} = \left(1 - f_{rear}\right) \cdot J_{0b,pass} + f_{rear} \cdot J_{0b,contact} \tag{16}$$

where f_{rear} is the fraction of metal contact coverage on the back surface field. $J_{0b,pass}$ is the saturation current density of passivated back surface field regions and also can be directly obtained from the lifetime measurement on symmetrical structure (passivation/n^+/n/n^+/passivation) by the QSSPC technique. $J_{0b,contact}$ is the metal-induced saturation current density of contacted regions on the back surface field and can be extracted by using the same method

as estimating $J_{0e,contact}$. Its test sample structure is shown in **Figure 7a**, with the following calculation equation

$$2 \cdot J_{0b, measured} = \left(J_{0b,contact} - J_{0b,pass}\right) \cdot f_{rear} + 2 \cdot J_{ob, pass} \tag{17}$$
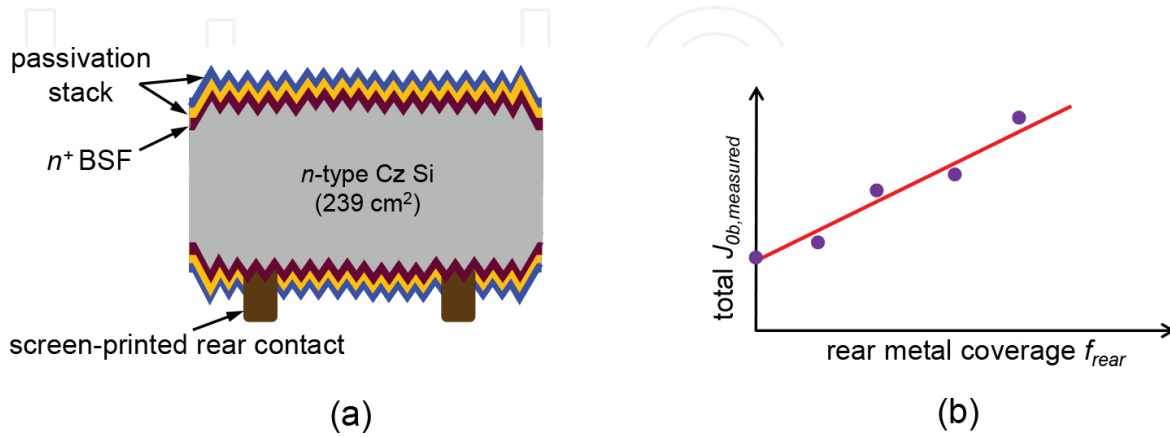

Figure 7. Schematic of a test sample symmetrical structure screen-printed contact on one side for extracting $J_{0b,contact}$ (a); a typical representation of $J_{0b,contact}$ line fitting as a function of the rear metal contact coverage f_{rear} on the test samples (b).

where $J_{0b,measured}$ is the directly obtained value from the lifetime measurement on the test sample structure. So, $J_{0b,contact}$ can be extracted from the resulting slope of the line fitting, as shown in **Figure 7b**.

So, in order to obtain a low $J_{0,total}$ (hence high cell V_{oc}), considering a trade-off among these saturation current densities in Eqs. (12)–(17) is necessary. A detailed example about the recombination contribution from each part of a finished cell will be specifically given in Section 3.

2.5. Optical loss

Apart from the recombination that contributes to the J_{sc} loss because the total number of generated electrons decreases after recombination, optical loss is another contributor for the J_{sc} loss since the total number of photons that can be absorbed to create electron–hole pair becomes less. **Figure 8** shows the typical mechanisms of optical losses in a screen-printed *n*-type silicon solar cell, including (1) reflection/shading at the screen-printed front metal contact, (2) reflection at the cell front surface, (3) reflection from the rear side out of cell, (4) absorption in the front passivation and antireflection coating layers, (5) absorption via free carrier absorption in the p^+ emitter layer, (6) absorption via free carrier absorption in the n^+ back surface field layer, (7) absorption in the rear passivation layers, (8) absorption in the screen-printed rear metal contact, (9) transmission without being absorbed in the cell. Therefore, to fabricate high-efficiency screen-printed front junction *n*-type silicon solar cells, these optical losses need to be reduced.
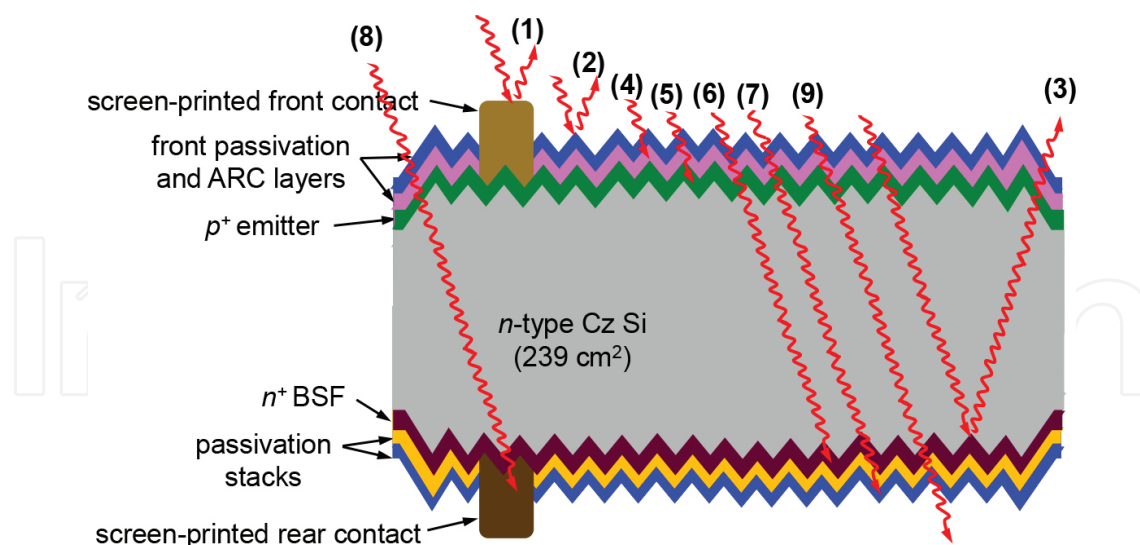
Figure 8. Schematic structure of optical loss mechanisms in a screen-printed front junction n-type silicon solar cell.

So, to reduce the optical loss in a finished cell, front gridline should be as narrow as possible to reduce metal shading while not sacrificing conductivity. Currently, the screen-printed gridline in mass production typically demonstrates ∼60 μm width. The size of pyramids also needs to be as small as possible to reduce reflection at the front surface, and currently, typical size is in the range of 3–6 μm. Low doping levels in the diffused regions (p^+ emitter and n^+ back surface field) can reduce the free carrier absorption, but the metal contact resistance and the lateral transport resistance of these layers should not be sacrificed.

3. Cell fabrication process with screen-printed metallization

In this section, the typical processes of fabricating screen-printed front junction n-type silicon solar cells are presented, starting from as-cut wafers to finished cells. All these cell fabrication processes are industrially relevant, and some of them have already been implemented on production lines.

3.1. Saw damage removal and texturing

After the silicon ingot is grown, wire sawing is typically used to slice silicon ingots into wafers with a resulting thickness of around 200 μm, and often in pseudo-square shape (∼156 × 156 mm^2) with total area of about 239–242 cm^2 depending on the diameter of the original ingot. During this process, the sawing damages the entire surface of both sides of the silicon wafers, with the damage depth of approximately 10 μm. This saw-induced damage has a very bad effect on the electronic quality of the wafer as they dramatically increase the surface recombination velocity, and hence have to be removed together with other contaminants prior to the next high-temperature diffusion step. This etching of the saw damage normally occurs in heated potassium hydroxide (KOH) solution at ∼80°C for few minutes. This etching reaction

takes place in three steps, including oxidation of silicon, formation of a solvable salt and dissolving of the salt in water, which is summarized in [15, 16]

$$Si + 2H_2O + OH^- \rightarrow HSiO_3^- + H_2 \qquad (18)$$

In addition, this is a selective etching process as different crystallographic orientations have different etch rates, with the lowest etch rate for the <111> plane. In order to effectively reduce the reflection at the front surface, isopropyl alcohol (IPA) is normally added into KOH solution to form small pyramids with a square base randomly distributed over the <100> oriented silicon surface, as shown in **Figure 9**.
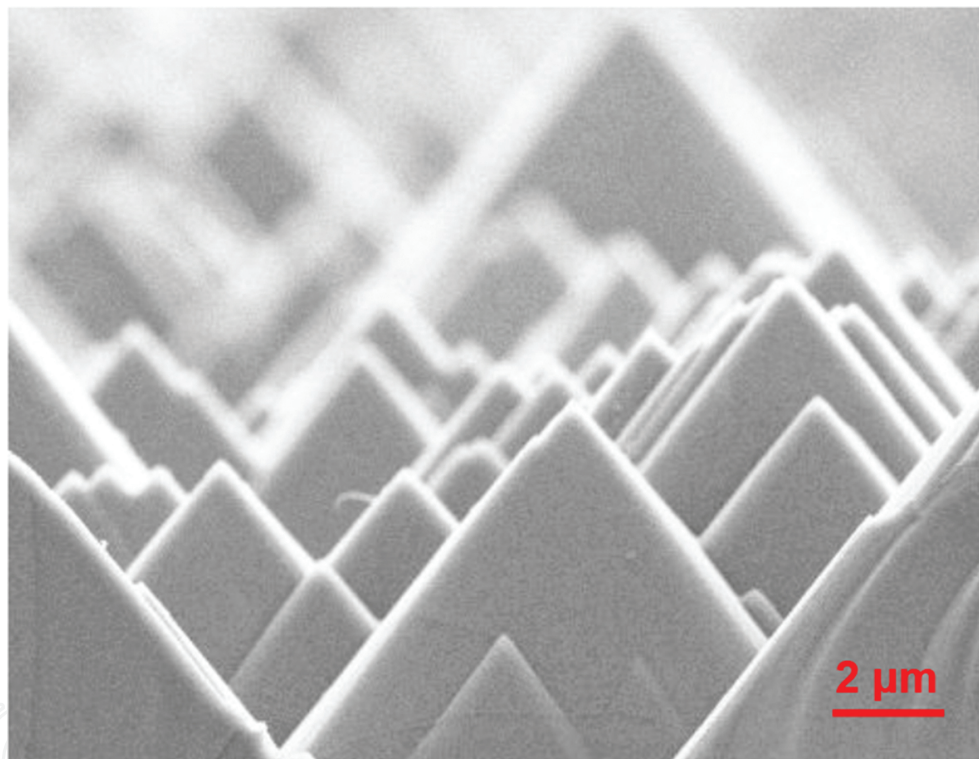
Figure 9. Appearance of a textured silicon surface for *n*-type mono-crystalline silicon wafer under a scanning electron microscope using alkaline texturing.

After texturing, the wafers are processed by a thorough cleaning to remove impurities present on the wafer surface that could diffuse into the wafer and cause carrier recombination. This cleaning typically consists of a rinsing in deionized (DI) wafer, a thorough etching in hydrochloric acid (HCl) to remove metal impurities from wafer surfaces, then another DI water rinsing, a short etching in hydrofluoric acid (HF) to etch off the native silicon dioxide (SiO_2) and to form a hydrophobic surface feature, and a final DI water rinsing and then air drying [17]. The more aggressive and more expensive 'RCA' clean ('SC-1' and 'SC-2') is another standard set of wafer cleaning steps typically used in R&D labs [18].

3.2. Boron emitter formation

To form the *pn*-junction of *n*-type silicon solar cells, a typical approach is to diffuse boron atoms into the silicon wafers. This can be implemented by depositing boron-doped silicon oxide via plasma-enhanced chemical vapour deposition (PECVD) or atmospheric pressure chemical vapour deposition (APCVD), and then annealing at high temperature. Another promising technology is direct thermal diffusion of boron from a boron tribromide (BBr_3) source, the so-called 'BBr$_3$ diffusion' process. In this process, pure nitrogen (N_2) carrier gas flows into a bubbler-containing liquid BBr_3, which forms gaseous BBr_3 and transports it into the quartz tube where the wafers are loaded in quartz boat. In the oxygen (O_2) ambient, a boron trioxide (B_2O_3) layer is formed on the silicon wafer surface through the reaction

$$4BBr_3 + 3O_2 \rightarrow 2B_2O_3 + 6Br_2 \tag{19}$$

This reaction is often referred to as the deposition stage, as a very high concentration of boron forms in the very thin layer on the silicon surface. Next, the formed B_2O_3 reacts with the silicon atoms which can diffuse boron atoms into the silicon bulk to form the p^+ emitter layer at high temperatures (over 900°C) through the reaction

$$2B_2O_3 + 3Si \rightarrow 4B + 3SiO_2 \tag{20}$$

which is often referred to as the diffusion stage. The formed SiO_2/B_2O_3 stack on the silicon surface is the so-called borosilicate glass (BSG) that needs to be removed to improve surface passivation quality. The resulting boron-doped p^+ emitter properties (surface doping concentration, depth and the shape of the doping profile) depend on the diffusion process temperature, diffusion duration, and gas flow rates [19, 20]. It is noteworthy that the boron emitter profiles typically show a concentration decline towards the silicon wafer surface due to the higher solubility of boron in the grown SiO_2 than in silicon [21].

Due to BBr_3 diffusion being a double-sided coating process, a mask on the rear side is needed to protect the rear surface where the n^+ back surface field is formed in the next process for the *n*-type front junction silicon solar cells. To eliminate these extra processes (masking, then removing mask after diffusion), ion implantation is another promising alternative technology due to its other advantages [22]: (1) formation of very uniform single-sided junction, (2) elimination of edge isolation and (3) elimination of dopant glass removal. Because boron is light element, crystal point defects (self-interstitials and vacancies) without amorphization are created during implantation [23], and a very high temperature (over 1000°C) is needed to anneal out this lattice damage [24]. To achieve high-efficiency screen-printed *n*-type silicon solar cells, an optimal boron emitter is needed to balance emitter sheet resistance, contact resistance and emitter saturation current density J_{oe} shown in Eq. (13). This can be achieved by flexibly controlling implant energy, boron ion dose and post-implantation annealing conditions.

3.3. Formation of phosphorus-doped back surface field

The most commonly used technique to form phosphorus-doped n^+ layer in the photovoltaic industry is a tube furnace diffusion process, the so-called 'POCl$_3$ diffusion' (phosphorus oxychloride) process. In this process, pure nitrogen carrier gas flows into a bubbler filled with liquid POCl$_3$, which forms gaseous POCl$_3$ and transports it into the quartz tube where the wafers are loaded in quartz boat. Phosphorus oxide (P$_2$O$_5$) is formed on the wafer surface in the oxygen ambient with the chemical reaction by

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \tag{21}$$

where the formed P$_2$O$_5$ acts as a phosphorus dopant source. This is often referred to a deposition stage, as a very high concentration of phosphorus forms in the very thin layer (only tens of nanometres) on the silicon surface. Then, in the same process, the furnace temperature is often slightly increased for the next drive-in stage: in which the phosphorus atoms diffuse deeper into the silicon. Phosphorus atoms diffuse into the silicon substrate to create an n^+ layer at a relatively higher temperature, typically in the range of 800–900°C through the reaction at the wafer surface

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \tag{22}$$

where the formed SiO$_2$/P$_2$O$_5$ stack is the so-called phospho-silicate glass (PSG). The resulting doping profile depends on diffusion temperature, diffusion time and gas flow rates [25, 26].

Because the POCl$_3$ diffusion is also a double-sided coating process, a mask on the front side is needed to protect the p^+ emitter layer for the n-type front junction silicon solar cells. Both silicon dioxide (SiO$_2$) and silicon nitride (SiN$_x$) deposited by PECVD can act as a mask layer. Similar to the p^+ emitter formation, in order to eliminate the complicated masking process, ion implantation is a promising technology to form the n^+ back surface field. Unlike the light elements (i.e., boron), phosphorus is a heavy enough ion, that nuclear collisions dominate and result in amorphized surface during implantation. Hence, a relatively lower annealing temperature (around 850°C) can recover implantation-induced defects on the silicon wafer surface. A proper combination of implant energy, phosphorus ion dose and post-implantation annealing conditions is needed to obtain high-efficiency screen-printed n-type silicon solar cells [27, 28].

3.4. Surface passivation and antireflection coating

To obtain high cell performance, surface passivation plays an important role in reducing recombination in the finished cell. There are two fundamental mechanisms for surface passivation: (1) chemical passivation that the surface defect states are removed or reduced; (2) field-effect passivation that a fixed-charge dielectric is deposited on the surface to create an internal electrical field that repels or screens minority carriers inside the wafer from the

defective surfaces. For field-effect passivation, the positive-fixed-charge dielectrics (i.e., SiN_x and SiO_2) repel the positively charged holes inside the silicon wafer from the surfaces and are ideally suitable to passivate n^+ surfaces. The negative-fixed-charge dielectrics repel the negatively charged electrons from surfaces and typically are used to passivate p^+ surfaces. Aluminium oxide (Al_2O_3) is the most studied of these dielectrics [29, 30]. So, in screen-printed n-type silicon solar cells, the p^+ emitter is more often passivated by Al_2O_3 which can be formed by atomic layer deposition (ALD), APCVD or PECVD. A minimum Al_2O_3 thickness is required to achieve excellent surface passivation quality without adding significant optical loss due to its insufficient antireflection properties. The n^+ back surface field is typically passivated by thermally grown SiO_2. To simplify the cell fabrication process, in some cases, the thermally grown SiO_2 is also used to passivate the p^+ emitter, but the resulting surface passivation quality is inferior to p^+ emitters passivated by Al_2O_3 [29].

In order to further reduce reflection losses at the textured front side, a layer of hydrogen-rich silicon nitride (SiN_x:H) is normally deposited by PECVD on top of the passivation layer (Al_2O_3 or SiO_2) as an ARC. Since there is significant amount of H in this ARC layer, it can be released during the metal contact firing step at high temperature ($\sim$800°C) and diffuse into the silicon wafer bulk region to passivate bulk defects, which reduces bulk recombination. The thickness of this ARC can be calculated by the quarter wavelength law [31]

$$d = \frac{\lambda}{4 \times n_{SiN}} \tag{23}$$

where λ is the wavelength, n_{SiN} is the refractive index of ARC layer. Reflection can be further minimized when n_{SiN} equals the geometric mean of the materials on both its sides, for instance,

$$n_{SiN} = \sqrt{n_{air} \cdot n_{Si}} \tag{24}$$

where n_{air} is the air refractive index (=1) n_{Si} is the silicon refractive index (=4). Therefore, for n_SiN =2, a typical ARC thickness is about 75 nm to obtain minimum reflectivity at wavelength of 600 nm. Because cells are eventually encapsulated to make modules under ethylene vinyl acetate (EVA) and glass which have refractive index of $\sim$1.5, a slightly higher n_{SiN} ($\sim$2.3) is typically implemented in module application. The precursor silane and ammonia ratio (SiH_4/NH_3) during PECVD deposition are typically adjusted to obtain the proper n_{SiN} and absorption coefficient of the resulting ARC layer. Note that in the screen-printed n-type silicon solar cells, the ARC layer is deposited on top of a passivation layer, so its thickness d needs to be modified according to the thickness of the passivation layer to achieve the antireflection quality without sacrificing any surface passivation quality.

3.5. Screen-printed metallization

Screen-printed metallization is very robust, simple and widely used for PV applications since its introduction about four decades ago [32]. **Figure 10** shows the schematic of a screen-printing process. The squeegee is moved with a proper pressure over the screen that consists of emulsion and mesh wires, which presses down the screen locally against the wafer surface and pushes the paste on the wafer surface through the well-defined opened region (typically 40–60 μm wide openings). During the printing, wafer stays on the stage under vacuum condition. The printer settings, i.e., snap-off distance, print pressure and print speed, are very critical parameters to obtain a good aspect ratio (height to width ratio) of screen-printed gridlines.
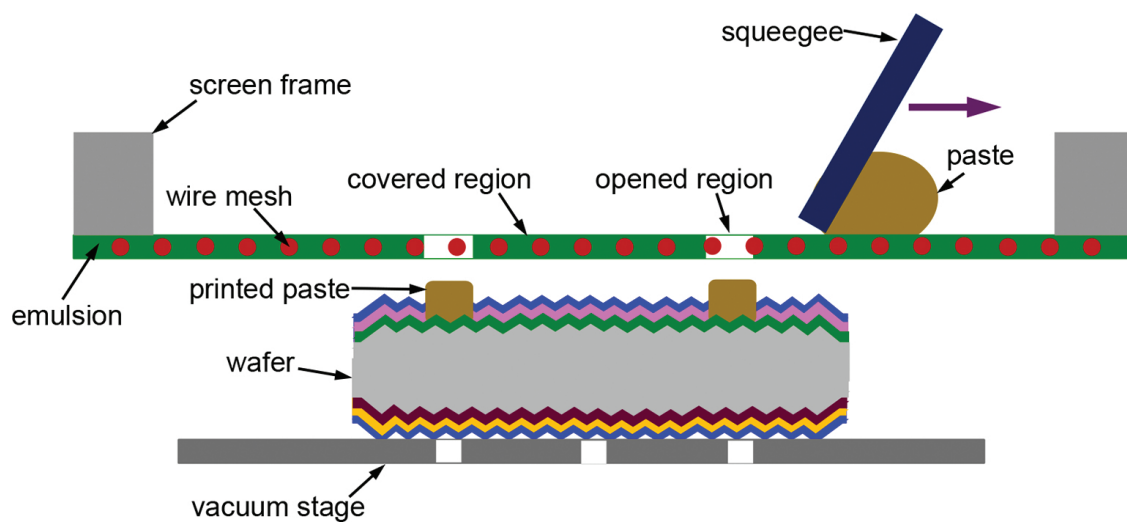
Figure 10. Schematic of a screen-printing contact process for front junction *n*-type silicon solar cells.

The paste ingredients are also crucial to obtain a high aspect ratio, good conductivity and low contact resistance. For front junction *n*-type silicon solar cells, the paste for front contact gridlines (typically named Al/Ag paste) is different from the one for rear contact gridlines (typically named Ag paste), because a proper fraction of Al in the paste can dramatically reduce the contact resistance on the p^+ emitter [33]. Glass frits containing lead oxide (PbO) are essential for both pastes to etch through the ARC and passivation stacks to promote the adhesion of Ag contact to silicon. Organic binders are also important to ensure the continuity of and the high aspect ratio of screen-printed gridlines [34].

Figure 11 shows an example of firing-temperature profile, including the firing-temperature ramp up and ramp down. During this firing step in a conveyor belt furnace at a peak temperature of over 700°C, the metal contact is formed on both sides (p^+ emitter, and n^+ back surface field), which is the so-called co-firing process. Due to the different paste ingredients and the different doping profiles on the front and back, the firing parameter settings have to be optimized to achieve an optimum cell performance, including the conveyor speed and temperature ramp up/down.
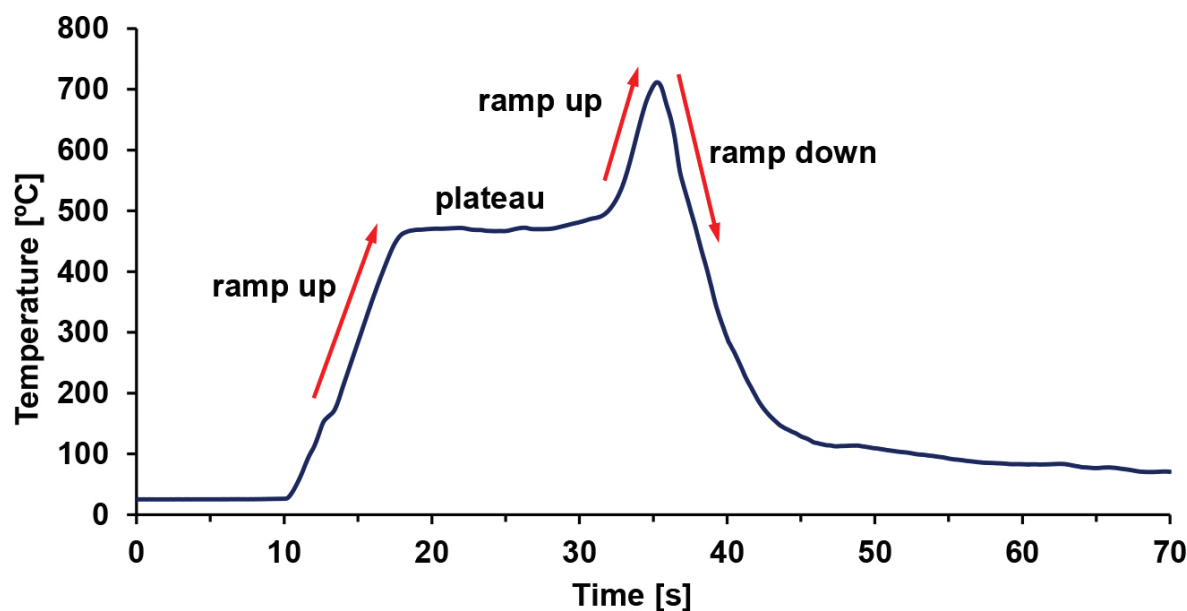
Figure 11. A typical firing-temperature profile for front junction *n*-type silicon solar cells.
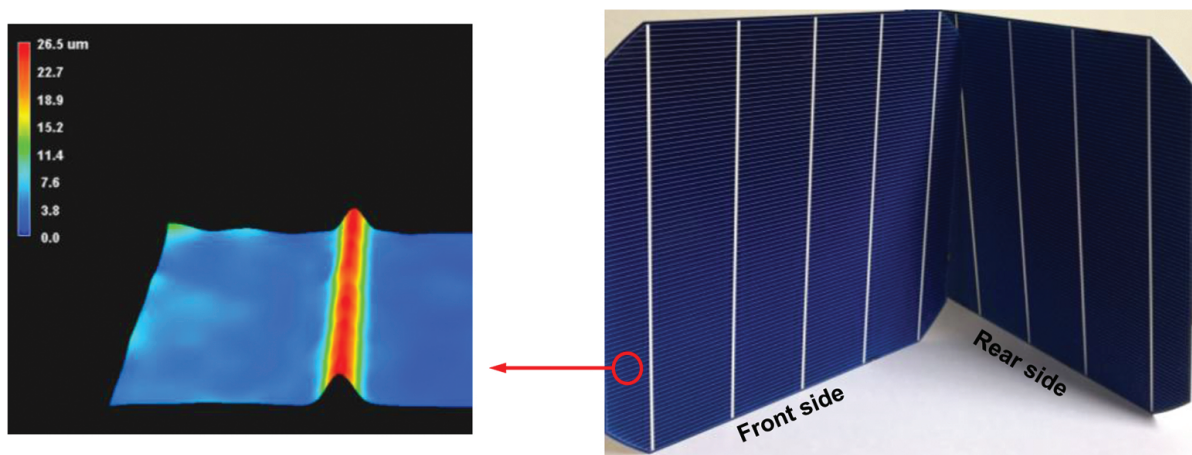

Figure 12. Optical microscope false colour height image of a screen-printed gridline (a); a large-area (~239 cm²) front junction *n*-type silicon solar cell with screen-printed contact on both sides, featuring 5 bus-bars (b).

During the firing process, organic binders are burned out below 600°C, which typically occurs during the plateau stage as shown in **Figure 11**. In the higher-temperature zones of the furnace, including the peak firing temperature, both the front and rear contacts are simultaneously formed by etching through the ARC and passivation layers, Ag particle sintering, and forming the ohmic contact [35]. In the meantime, the hydrogen of the SiN_x:H ARC layer is released into the wafer to passivate electrical defects at interfaces and in the wafer bulk regions. The duration of the peak temperature often only lasts for a few seconds. **Figure 12b** shows the physical appearance of a finished cell with screen-printed contacts, featuring 5 bus-bars on both front

and rear sides. The final gridline on the cell is typically ~60 μm wide, and ~20 μm high, as shown in optical microscope image of **Figure 12a**.

3.6. Characterization

After cell fabrication, the illuminated current density–voltage (*J–V*) characteristic is measured by using an IV tester with a solar simulator with a light intensity of 1000 W/m², AM1.5 spectrum, and temperature of 25°C. This light *J–V* measurement determines important solar cell parameters, such as, V_{oc}, J_{sc}, *FF*, *n*-factor, R_s, R_{sh}, and cell efficiency *η*. Excellent results on large-area screen-printed front junction *n*-type silicon solar cells have been reported to date, with cell V_{oc} of ~665 mV, J_{sc} of 39.8 mA/cm², *FF* of 79.3%, and an efficiency of 21% [36]. For module application purposes, the cell's reverse breakdown characteristics are also determined to avoid hot-spot heating.

To obtain a better understanding of the loss mechanisms in a finished cell, detailed analysis is typically needed. For instance, a cell's internal and external quantum efficiency (*IQE* and *EQE*) and reflection are measured, as shown in **Figure 13**, including the illustration of optical and recombination losses. In addition, saturation current densities from each part of the
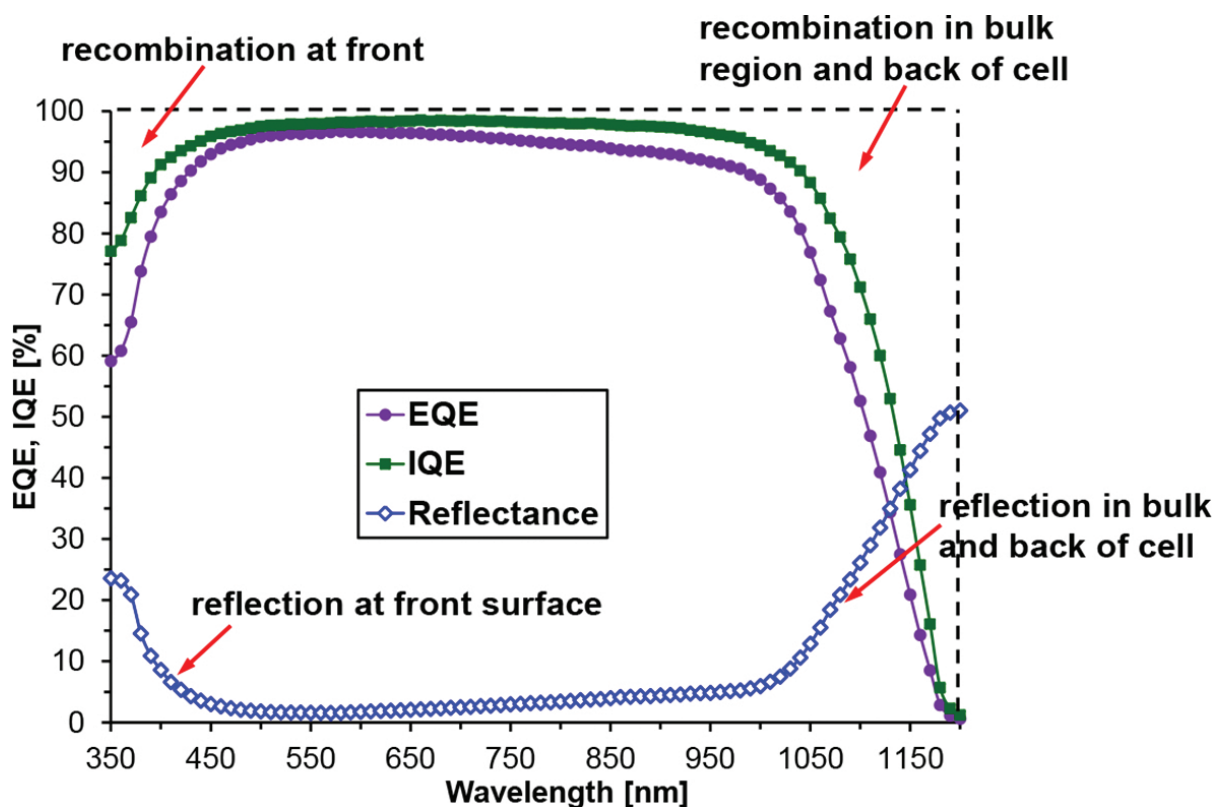

Figure 13. Typical internal and external quantum efficiency (*IQE* and *EQE*) and reflection in actual screen-printed front junction *n*-type silicon solar cells.

finished cell, as described by Eqs. (12)–(17), are also often extracted to quantitatively analyse these recombination losses.

4. Advanced cell concepts and fabrication

4.1. Selective doping

Due to the recent improvements in material quality and surface passivation, current high-efficiency silicon solar cells are often limited by the recombination at the metal/semiconductor contacts. A feasible solution to minimize contact recombination is a selectively doped structure, which allows decoupling of the metallized and non-metallized areas of the doped regions. **Figure 14** shows an example of a selective doping structure on the front emitter (p^+/p^{++}) and the back surface field (n^+/n^{++}). The higher surface doping concentration and the deeper doping profile underneath the screen-printed contact regions can result in lower contact resistance and lower metal-induced saturation current density ($J_{0e,contact}$ and $J_{0b,contact}$). In addition, the lower surface doping concentration on the non-metallized (passivated) regions can lead to lower saturation current density on the passivated regions ($J_{0e,pass}$ and $J_{0b,pass}$) due to less Auger recombination and better surface passivation quality. Consequently, the selective doping structure results in higher J_{sc} and V_{oc}.
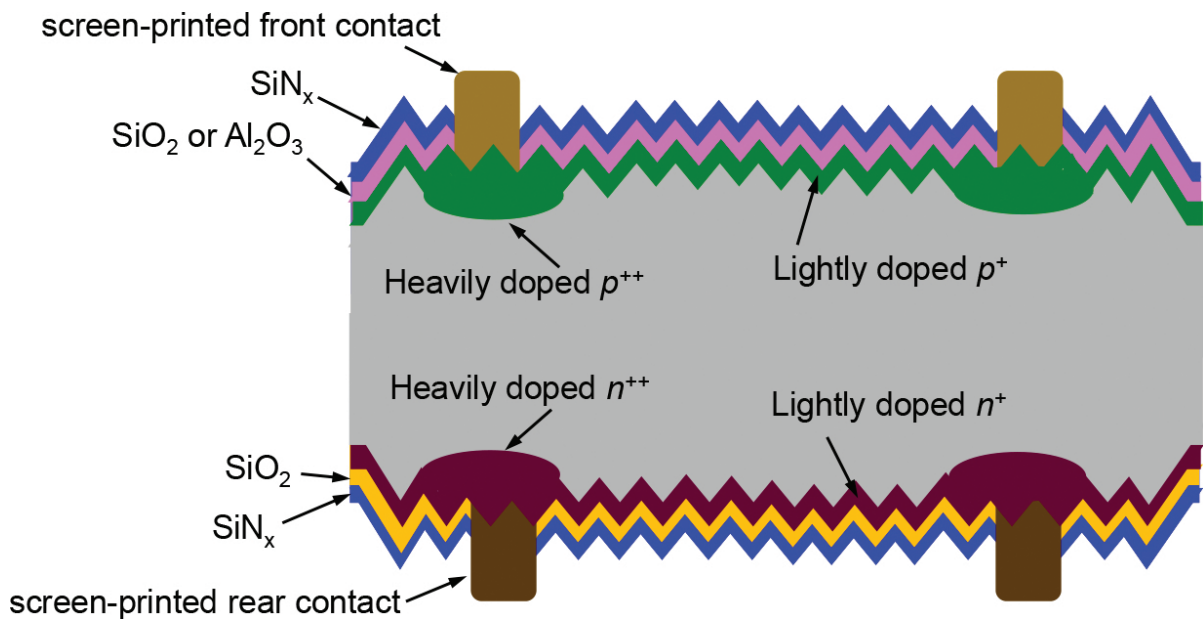
Figure 14. Schematic of selective doping for a screen-printed front junction *n*-type silicon solar cell.

There are several selective doping technologies that have been developed over years in the field of photovoltaics. One of these promising technologies is based on ion implantation through a mask which only increases the dopant dose on the regions underneath the screen-printed contacts. The advantages of this technology are eliminating the formation of PSG and/

or BSG, and fewer process steps. Other selective doping technologies, such as the etch-back process, laser-doping, oxide mask process, etc., have been addressed by Hahn, et al. [37]. As a rule of thumb, in order to implement these selective doping technologies to an industrial production line, every extra process step should provide the enhancement in cell efficiency of 0.2–0.3% absolute considering the related extra manufacturing costs.

4.2. Tunnel oxide passivated contact

Another feasible solution to minimize contact recombination is to put a passivating material with offset bands between the metal and silicon, also known as a passivated contact. Introduction of a thin passivating interlayer between the high recombination regions and the silicon absorber mitigates their negative impact because they are not in direct contact with the absorber. This reduces total recombination or saturation current density ($J_{0,total}$), resulting in much higher V_{oc}. However, the interlayer must passivate the silicon surface without interfering with the majority carrier transport to ensure good fill factor *FF* and efficiency. The best example of a passivated contact is the heterojunction silicon solar cell with an intrinsic thin amorphous layer (HIT), which has demonstrated cell V_{oc} of 750 mV [38] and cell efficiency of over 25% [39]. However, this passivation scheme cannot withstand temperature above 250°C for the back-end metallization process; hence, it is not compatible with the widely used industry standard simple and reliable screen-printed and fired-through metallization, which requires a temperature over 700°C for contact formation.

A promising approach to achieving a carrier selective passivated contact involves an ultra-thin (~15 Å, see the TEM image in **Figure 15b**) tunnel oxide capped with phosphorus doped n^+ polycrystalline silicon (*poly*-Si) and metal on the entire back side of *n*-type silicon cell (see **Figure 15a**), which is the so-called tunnel oxide passivated contact (TOPCON) [40]. This passivation scheme is thermally stable and so compatible with screen-printed and fired-through metallization. In this passivated contact structure as shown in its band diagram of **Figure 15b**, three parallel mechanisms contribute to carrier selectivity. First, heavily doped n^+ *poly*-Si creates an accumulation layer at the absorber surface due to the work function difference between the n^+ *poly*-Si and the n^- silicon absorber. This accumulation layer or band bending provides a barrier for holes to flow to the tunnel oxide, while electrons can migrate easily to the oxide/silicon interface. Second, the tunnel oxide itself provides the second level of carrier selectivity, because it presents a 4.5 eV barrier for holes to tunnel through relative to 3.1 eV for electrons [41], which is also the most important carrier selectivity feature [42]. Third, there are very few or no states on the other side of the dielectric (n^+ region) for holes to tunnel through because of the forbidden gap. Furthermore, due to the full area metal contact on the back, there is only one-dimensional current flow, which eliminates the lateral transport resistance (two-dimensional current flow) in a finished solar cell, and so results in much higher *FF*. By optimizing the depositions conditions of the *poly*-Si and the tunnel oxide growth temperature in nitric acid (HNO_3), excellent interface passivation quality and carrier selectivity can be achieved. For instance, a back saturation current density $J_{0b,pass}$ of less than 5 fA/cm² [43], and a cell efficiency of ~21.4% for large-area front junction *n*-type silicon solar cells with screen-

printed contact on an homogeneous emitter have been demonstrated (as shown in **Figure 15a**) [44].
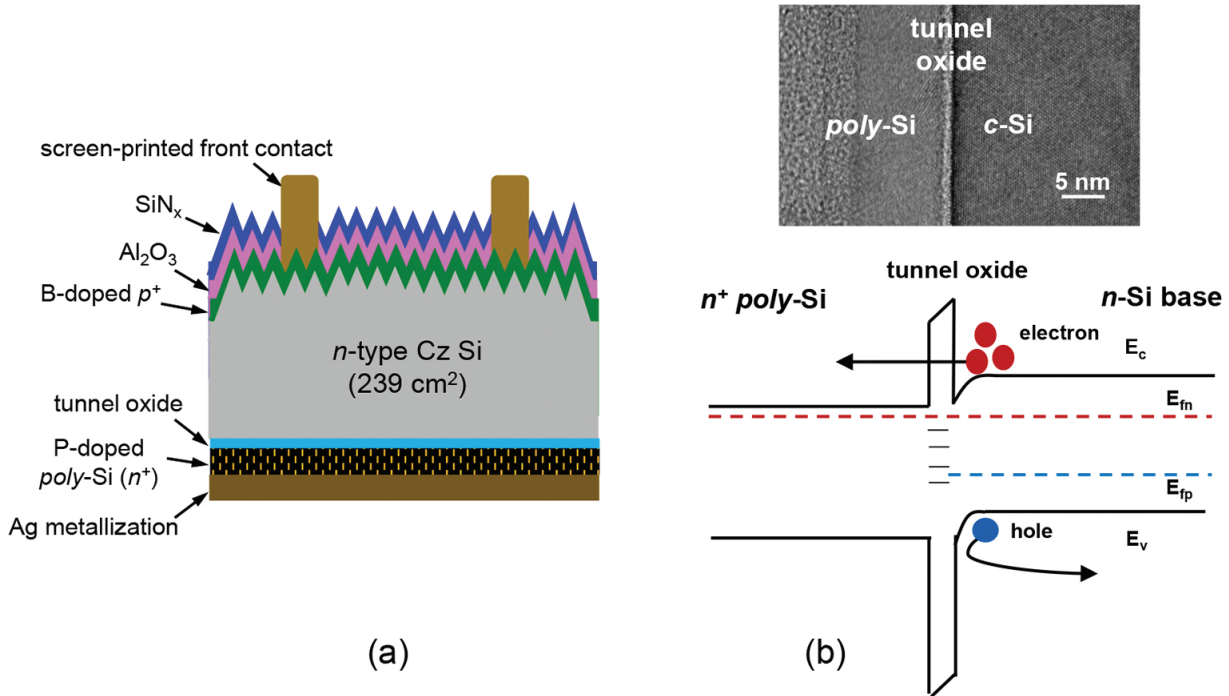
Figure 15. Schematic structure of a front junction n-type silicon solar cell with tunnel oxide passivated rear contact (a); a transmission electron microscopy (TEM) image of tunnel oxide passivated contact structure and its schematic band diagram (b) [42, 44].

5. Summary and outlook

The annual shipment and installation of PV cells and modules up to date are still dominated by the standard industrial solar cell fabrication process on p-type silicon wafers (full Al-BSF). However, screen-printed front junction n-type silicon solar cells featuring bifacial structure are attracting more and more interest, due to their potential for higher efficiency, higher-energy yield, and hence lower LCOE (levelized cost of electricity). The next few years promise to be an exciting timeframe for research and development of screen-printed front junction n-type silicon solar cells, which are also predicted in the latest Internal Technology Roadmap for Photovoltaic (ITRPV) [45].

Although it is hard to exactly predict which process approach and cell architecture will be the most cost-effective in the future, selective doping and tunnel oxide passivated contacts have become active areas of investigation for silicon solar cells, because they can produce higher cell efficiency due to reduced minority carrier recombination. Combining these two promising technologies into a screen-printed front junction n-type silicon solar cell may attract even more research investigation in the future. For instance, by applying atomic hydrogenation process,

boron-diffused selective front emitter and photolithographically defined front metal contacts (Ti/Pd/Ag), the TOPCON cell has successfully demonstrated over 25% efficiency on a small-area *n*-type float zone (FZ) silicon substrate [46, 47]. So, this cell structure explores research areas for future industrial application with screen-printed front contacts (as shown in **Figure 16**), due to its potential for high cell efficiency and its compatibility with high-temperature firing contact formation process.
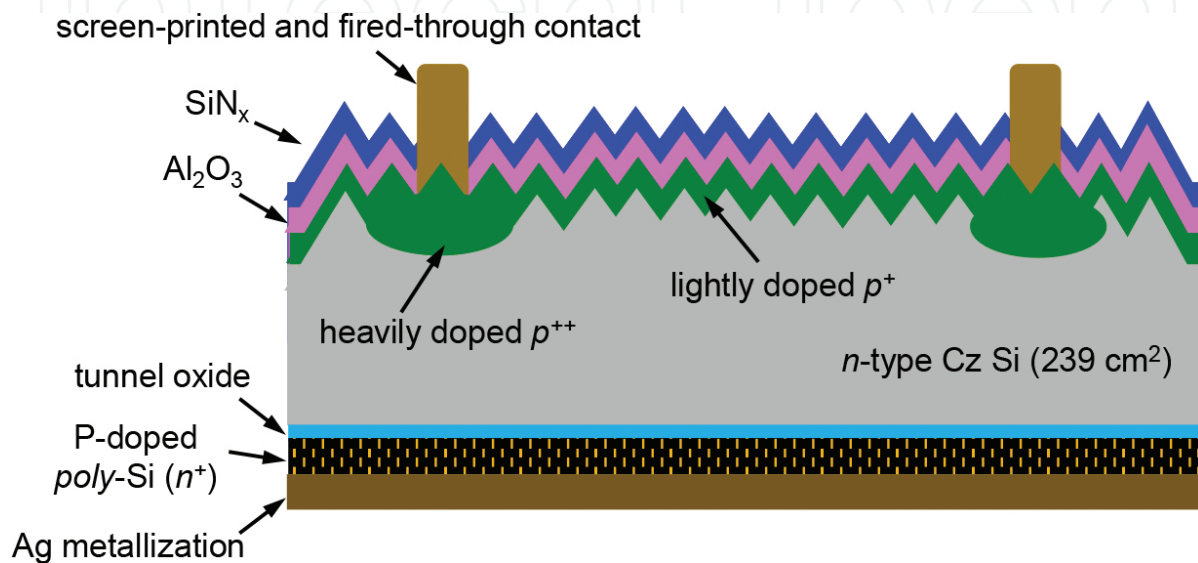
Figure 16. Schematic structure of a front junction *n*-type silicon solar cell (not to scale), with screen-printed and fired-through contact on a selectively doped front emitter, and tunnel oxide passivated rear contact.

Acknowledgements

Author details

Yuguo Tao[*]

Address all correspondence to: yuguo.tao@ece.gatech.edu

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

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