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Chapter 8

Theoretical Derivation of Junction Temperature of Package Chip

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Additional information is available at the end of the chapter

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Abstract

Junction temperature is the highest operating temperature of the actual semiconductor in an electronic device. In operation, junction temperature is higher than the case temperature and the temperature of the part's exterior. The difference is equal to the amount of heat transferred from the junction to case multiplied by the junction-to-case thermal resistance. When designing integrated circuits, predicting and calculating the chip junction temperature is a very important task. This chapter describes how to derive the junction temperature from the thermal transport model.

Keywords: junction temperature, thermal resistance, thermal conduction, thermal convection, thermal radiation

1. Introduction

From the small integrated circuits in 1960 to the development of today's large and ultra-high-speed integrated circuits, the package density has increased from only several electronic components to billions of electronic components per chip. Because of this high package density, the combination directly causes a serious designing problem, and it will also increase the heat dissipation of the chip per unit volume or area. If the cooling method is not properly designed, this overheated high-density package chip will result in a high junction temperature. As a result, it will have a negative effect on the functions, the reliabilities, and the life of the electronic chip. Usually, a high-speed integrated circuit is the most expensive element of the whole package. If the chip continues to suffer from the effect of high heat, it will cause the speed to slow down or be damaged; therefore, the solution of the heat-dissipated problem should not be underestimated. In electronics manufacturing, integrated circuit packaging is the final stage

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of semiconductor device fabrication, in which the tiny block of semiconducting material is encased in a supporting case that prevents physical damage and corrosion. The case, known as a "package," supports the electrical contacts that connect the device to a circuit board. The junctions of the chip are used by wire connecting on the package housing. These wires are then connected to other components through the wire on the printed circuit board (PCB). Therefore, for many integrated circuit products, packaging technology is a very important stage. Using chip as the main product such as random access memory (RAM) or dynamic RAM (DRAM), packaging technology not only can guarantee the separation of the chip and the outer world but also can prevent chip circuit from losing its function caused by the corrosion of the impurities in the air; also, the wellness of the packaging technology directly concerns the designing and producing of the PCB connected with the chip. This leads to the deeply influential of the chip's performance. However, if the thermal impedance of the package is too high, the junction temperature will also be raised to a high level. According to the report, once the junction temperature is raised to approximately 10°C, half of the component life will be reduced [1]. if the average life span is 30,000 to 50,000 hours, it is also implied that 15,000 to 25,000 hours of usage time will be decreased and result in the chip efficiency's sharp decline. This chapter is mainly focused on the theoretically export system manufacturers' topmost concern, junction temperature (T_J). Sometime in 1980, PC is still in 386 and 486, and the CPUs' permitted temperature could be up to 90°C; until the 21st century, all the semiconductor chip junction temperature (including LED) has been asked not to surpass 70°C. Some of them are not even allowed to exceed 50°C. Therefore, the purpose of this chapter is how to simply use a theoretical calculation to derive the chip junction temperature (T_J) without using software package (Code).

2. Theoretical derivation of the junction temperature

The following are the logical ways to think of the solutions to counter heat-dissipated problems.

2.1. Questions in Table 1

Step	Questions
A	What is the thermal model in this problem? Is it thermal conduction in [2]? Or thermal convection in [3]? Or thermal radiation in [4]?
B	Fluid? Is liquid? Or gas?
C	Can the fluid be compressed or not [5]? We usually supposed it is not compressible fluid.
D	Are the fluid properties related to the temperature?
E	What is the status of the fluid?

Step	Questions
	Is it laminar flow [6] or period cycle flow in [7]?
	Or turbulent flow in [8]? Or transient in?
F	What is the length of calculating Re's characteristic?
	By tube diameter or by plate length or by obstacle height? Or others
G	What is the effect of the viscosity in this problem [9]?
	How about the boundary layer [10]? What is mechanical loss? And others?

Table 1. Steps of finding the solutions of heat-dissipated problems.

At this step, readers should have a good physical explanation for solving the questions. From steps A to G, we can be closer and see clearly the answer to the question.

2.2. Quantization and removal of unimportant parameters

The goal of this step is to think about every item of the question (or concept) to gain a deeper understanding. For example, $Q=hA(T_s-T_f)$; in this phase, notice the correct use of the unit (usually in SI unit). Make sure not to compare apple and orange, making correct assumptions necessary. Thus, when making any item negligible, we need to provide a scientific proof. We cannot directly ignore an item because it is small. Take the temperature, for example, when finding the answer to the question on temperature. We need to ask if we are looking for the temperature distribution or the end point. What is the accuracy? Is there anything else that can be simplified?

2.3. Establishment of the governing equation

The definition of the governing equation is using other variables to define an unknown item. If we only consider the heat transfer mechanics of the single chip on the PWB, take **Figures 1** and **2**, for example, during the heat transfer mechanism. The chip and the board both have thermal conductance, thermal convection, and thermal radiation. At this point, we can notice some of the characteristics of the heat transfer processes: (A) Multiple heat transfer processes, a high level of thermal coupling (heat source and sink). (B) Large-scale thermal spreading effect. If we consider all the heat transfer mechanism between each PWB, such as in **Figure 3**, then we need to also consider the thermal conductance coupling problem from the PCB. Among thermal convection, they include (i) material on the board, (ii) thermal convection and thermal radiation between each adjacent boards, and (iii) thermal coupling between the main board and the daughter card. Among radiation coupling, they include (a) material on the board and (b) adjacent boards. What needs to be paid attention of is when there is thermal coupling between the outer heat source and the chip heat itself. The heat received from the critical chip is not less than the heat source chip itself. **Figure 4** presents a schematic diagram between the heat source chip and the critical chip of the motherboard and the outer heat source. Thus, to solve the heat-dissipated problem, we should not only pay attention to the temperature on the heat source of chip itself but also need to know problems such as the heat accumulation locations and the other chip influences.

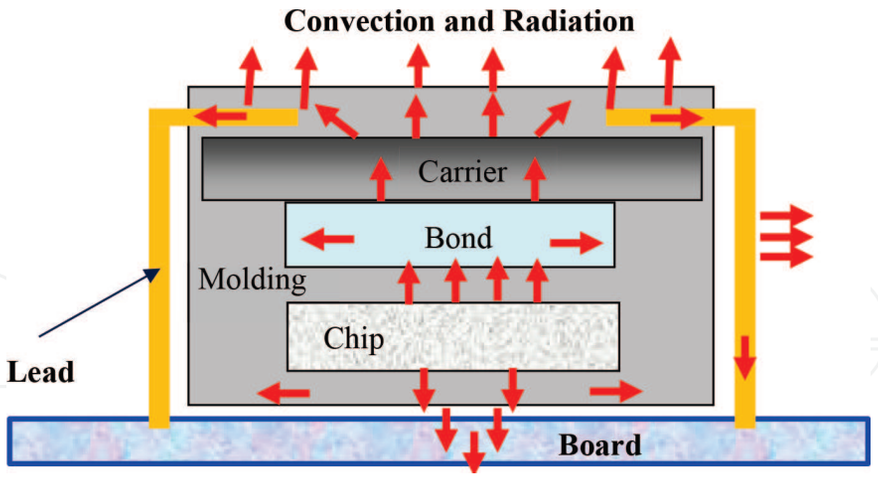


Figure 1. Heat transfer mechanism process of the chip for the upper part.

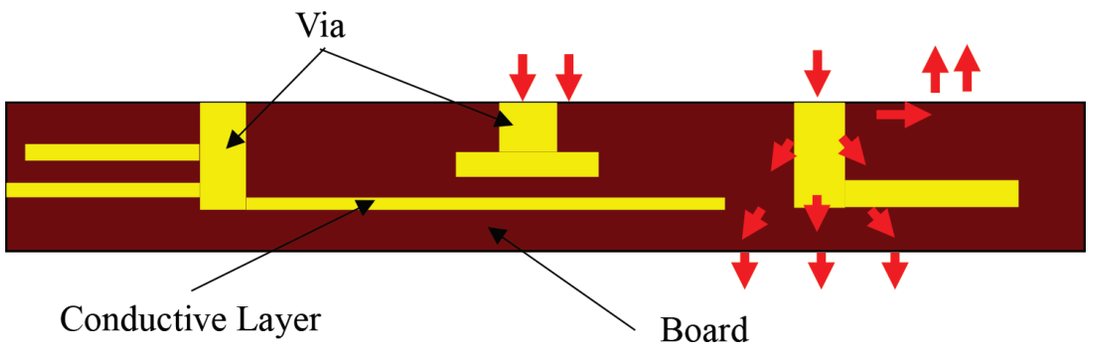


Figure 2. Heat transfer mechanism process of the chip for the lower portion.

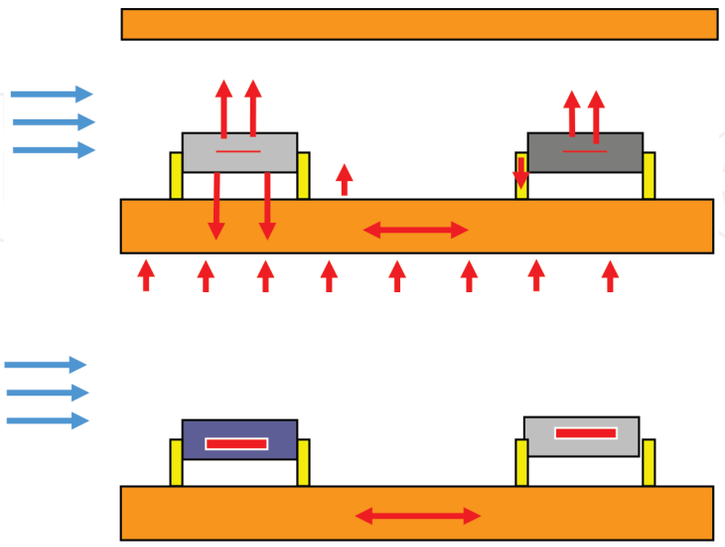


Figure 3. Heat transfer mechanism between each PWB.

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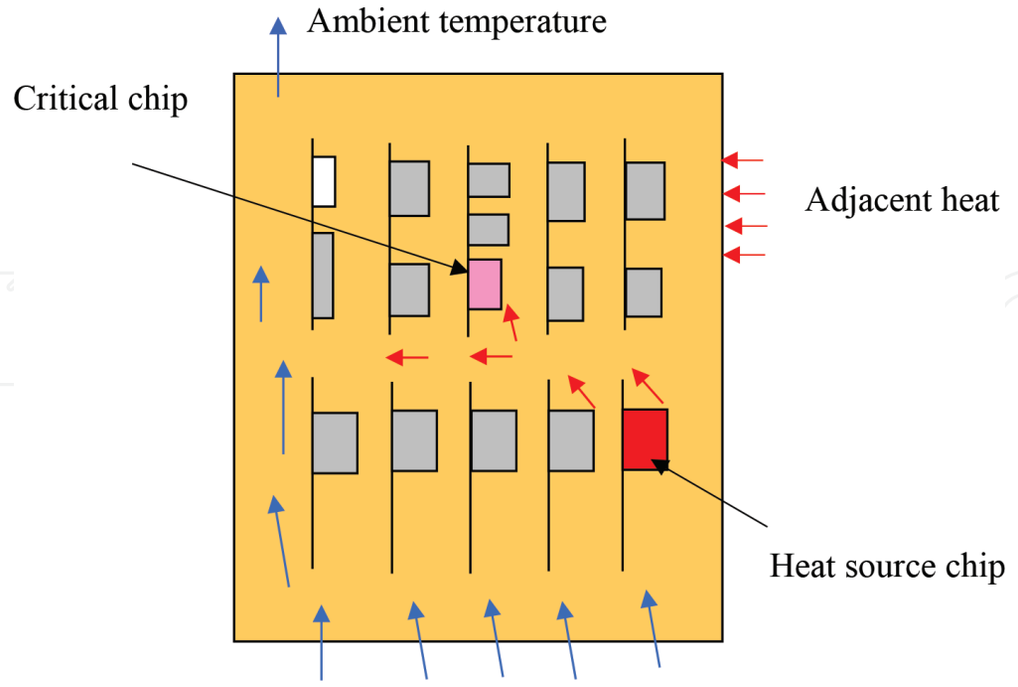


Figure 4. Schematic diagram between the heat source chip and the critical chip of the motherboard and the outer heat source.

2.4. How to analyze the influences of the thermal coupling

Thermal coupling makes it hard to analyze, if we do not include the thermal coupling in the calculation, and the results will not be accurate. Because of the thermal coupling natural properties, we need to consider the environment, chassis, PWB, component (module), chip, and parts (diodes, transistor) etc., when analyzing conducting a solution that can explain the thermal effect. Usually, there are three ways to solve either the key component or the heat source chip's heat-dissipated problem (see **Figure 5**). One of them is using the integral method, that is, a closed-form solution. However, this method can necessarily not be used on every energy conservation. The second method is using the differential method, the so-called numerical analysis. Numerical analysis needs a special mathematical skills technique. It needs someone who has studied numerical analysis to write a program that includes grids definition, module establish, numerical analysis model, converging problem, boundary condition definition, etc. This needs to educate talented people, and most of the companies are unwilling to invest in here. But on the other hand, usually there are also software packages in the market, such as ice pack, fluent, ANSYS, and Flotherm. However, all these software packages cost more than USD 30,000 or 40,000. Not everyone can afford it, and most companies cannot even buy it—these are some of the difficulties what companies are facing. The third solution is measure it by experiment. The experiment is then separated into two kinds. One is the actual measurement that uses the real system with the samples attached to it to measure the data such as temperature. Although this is a very reliable way, it spends a lot of manpower and time, and the cost is expensive. Cooler manufacturers commonly do not use this solution. For example, Intel published the next-generation CPU, but there are supplier problems on these equipment,

such as power supply, main board, south bridge, north bridge, hard disk, and DRAM. Cooler manufacturers can only solve the CPU's heat-dissipated problems, and they really cannot wait until all these peripheral accessory devices are ready because it will take too much time and cost too much. Therefore, the actual measurement is only used in system manufacture, such as in HP, DELL, ASUS, ACER, and Lenovo. The second way of the experiment is the Dummy experiment, also known as Dummy heater. It is commonly used by the industry. For example, because we wanted to know what the thermal resistance of the cooler is, we only have to place the cooler on the heating copper block with which it has the same area and then measure the difference temperature between the heat copper block and ambient temperature then divide by the input power to get the thermal resistance of the cooler. The experiment does not have any complex problems. The only thing that we need to be aware of is the sensors' correction, measuring the position and boundary condition.

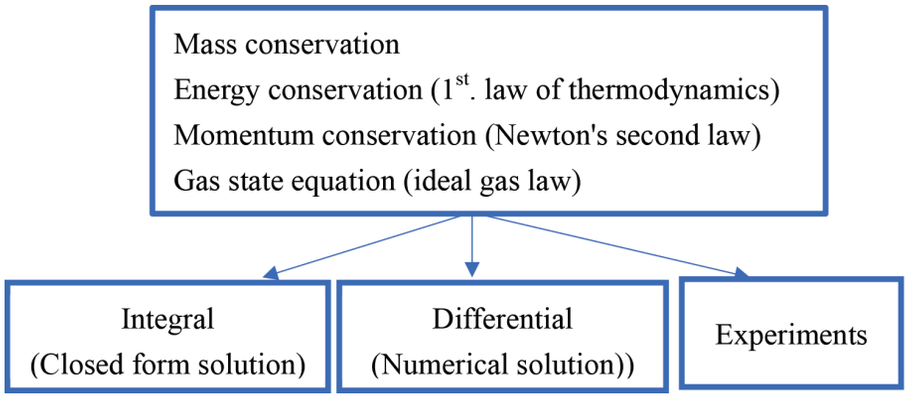


Figure 5. Three methods for solving heat-dissipated problems.

2.5. Theoretical derivation of the junction temperature (T_J)

2.5.1. Consider a control volume around the outside of the component and lead pin

Take the control volume on the external chip and wire as in **Figure 6**.

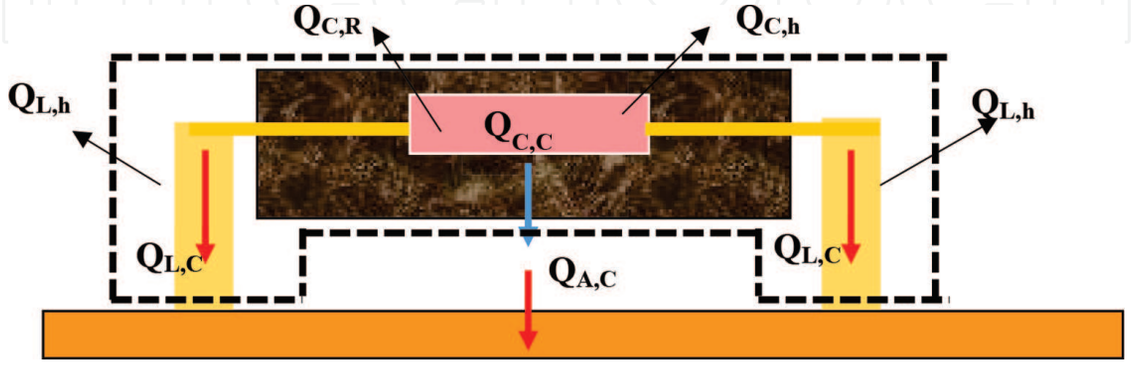


Figure 6. Heat transfer diagram outside the chip.

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Let us apply the energy balance equation to the body of the component and device power dissipation is "P_{tot},

$$\begin{aligned} P_{tot} &= Q_{C,R} + Q_{C,h} + Q_{L,h} + Q_{C,C} \\ &= Q_{C,R} + Q_{C,h} + Q_{L,h} + Q_{L,C} + Q_{A,C} \end{aligned} \tag{1}$$

where $Q_{C,R}$=radiation heat transfer from component (W), $Q_{C,H}$=convection heat transfer from component (W), $Q_{L,h}$=convection heat transfer from lead (W), $Q_{C,C}$=conduction heat transfer through component (W), $Q_{L,C}$=conduction heat transfer through lead (W), and $Q_{A,C}$=conduction heat transfer through air gap under the component (W).

Converting all the Q's in Eq. (1) in terms of the temperature definitions, we have

2.5.1.1. Using Stefan-Boltzmann's law to change the thermal radiation of the chip into temperature

$$Q_{C,R} = \sigma \in_C f_{C,ref} A_{C,C} \left(T_C^4 - T_{ref}^4\right) = \left(\frac{1}{R_{th,CR}}\right)\left(T_C^4 - T_{ref}^4\right)$$

$$= \sigma \in_C f_{C,ref} A_{C,C} \left(T_C^4 - T_a^4\right) = \left(\frac{1}{R_{th,CR}}\right)\left(T_C^4 - T_a^4\right) \tag{2}$$

where σ=Stefan-Boltzmann's constant=5.669×10^{-8} W/m^2 K^4,ε=material emissivity, $f_{c,ref}$=shape factor for component, $A_{C,C}$=upper surface area of the chip=bottom surface area of the chip (m^2), T_C=upper surface temperature of the chip (K), h_C=heat transfer coefficient of the chip (W/m^2 K), and T_{ref}=reference temperature where the component radiates to generally can be assumed to be T_a (K).

$$Q_{C,h} = h_C A_{C,C} \left(T_C - T_a\right) \tag{3}$$

$$R_{th,Ch} = \frac{1}{h_C A_{C,C}} = \frac{T_C - T_a}{Q_{C,h}} \tag{4}$$

2.5.1.2. Using Newton's cooling law to change the thermal convection of the chip into temperature

$$Q_{L,h} = h_L A_{L,S} \left(T_L - T_a\right)$$

$$R_{th,Lh} = \frac{1}{h_L A_{L,S}} = \frac{T_L - T_a}{Q_{L,h}} \tag{5}$$

where h_L=heat transfer coefficient of the wire (W/m^2 K) and $A_{L,S}$=surface area of the wire (m^2).

2.5.1.3. Using Newton's cooling law to change the thermal convection of the lead into temperature

$$Q_{L,C} = \frac{k_L A_{L,C}}{L_L}\left(T_L - T_b\right)$$

$$R_{th,LC} = \frac{1}{k_L A_{L,S}} = \frac{T_L - T_b}{Q_{L,C}} \tag{6}$$

where $A_{L,C}$=cross-sectional area of the lead (m^2), k_L=lead thermal conductivity (W/m K), L_L=length of the lead outside of the component (m), and T_L=lead average temperature (K).

2.5.1.4. Using Fourier's cooling law to change the thermal conduction of the chip into temperature through air gap between chip and board

$$Q_{A,C} = \frac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right)$$

$$R_{th,CA} = \frac{1}{k_A A_{C,C}} = \frac{T_C - T_b}{Q_{A,C}} \tag{7}$$

where k_A=air thermal conductivity (W/m K), t_A=thickness of the layer of air underneath the component (m), T_b=board temperature (K), and $A_{C,C}$=assumed component top surface is the cross-sectional area of the air gap (m^2).

Substitute the above into Eq. (1):

$$\begin{aligned} P_{tot} &= Q_{C,R} + Q_{C,h} + Q_{L,h} + Q_{C,C} \\ &= Q_{C,R} + Q_{C,h} + Q_{L,h} + Q_{C,C} + Q_{L,C} + Q_{A,C} \end{aligned}$$

$$\begin{aligned} &= \sigma \in_C f_{C,ref} A_{C,C}\left(T_C^4 - T_{ref}^4\right) + h_C A_{C,C}\left(T_C - T_a\right) \\ &+ h_L A_{L,S}\left(T_L - T_a\right) + \frac{k_L A_{L,C}}{L_L}\left(T_L - T_b\right) + \frac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right) \end{aligned} \tag{8}$$

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In Eq. (8), T_L, T_b, and T_C are unknown, but we do not know the junction temperature (T_J) yet. Therefore, we need seek another control volume to get T_J.

2.5.2. Consider a control volume around the inside of the component

Assume a chip inside as shown in **Figure 7**, according to energy conservation

$$P_{tot} = Q_{C,R} + Q_{C,h} + Q_{C,J} + Q_{A,C} \tag{9}$$

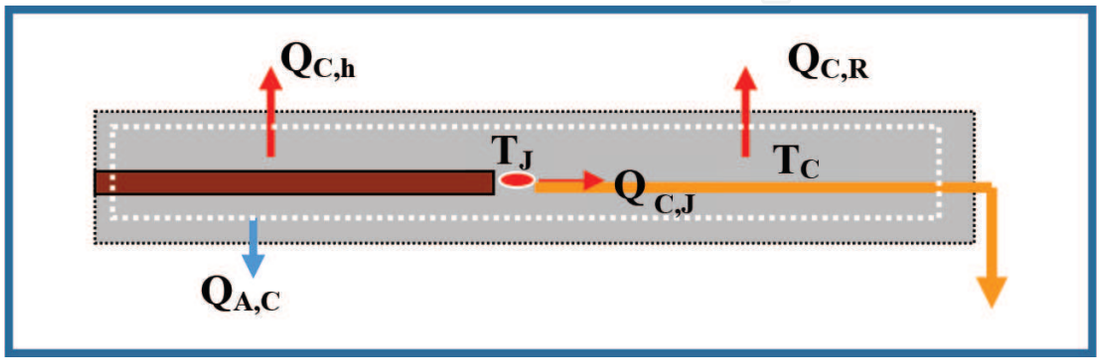


Figure 7. Case temperature and heat transfer diagram inside the chip.

2.5.2.1. Using Fourier's cooling law to change the inner thermal conduction of the chip into temperature

$$Q_{C,J} = (-\frac{k_L A_{L,C}}{L_L})_{eff}(T_C - T_J) = (\frac{k_L A_{L,C}}{L_L})_{eff}(T_J - T_C) \tag{10}$$

where $Q_{C,J}$=conduction heat transfer within the body of the component (W), $A_{L,C}$=effective lead cross-sectional area inside the component (m^2), $L_{L,eff}$=effective lead length inside the component (m), $k_{L,eff}$=effective thermal conductivity of the lead (W/m K).

2.5.2.2. Using Fourier's cooling law and Newton's cooling law to change the thermal conduction and thermal convection of the chip and lead into temperature

Compare Eq. (1) with Eq. (9).

$$P_{tot} = Q_{C,R} + Q_{C,h} + Q_{L,h} + Q_{L,C} + Q_{A,C} \tag{1}$$

$$P_{tot} = Q_{C,R} + Q_{C,h} + Q_{C,J} + Q_{A,C} \tag{9}$$

As shown in **Figure 8**, the conduction heat transfer within the body of the component $Q_{C,J}$ is the sum of the thermal convection from lead to ambient $Q_{L,h}$ and lead thermal conductance to board $Q_{L,C}$:

$$Q_{C,J} = Q_{L,h} + Q_{L,C}$$

Plugging all the thermal conduction equation and thermal convection into above equation, we obtain:

$$\left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}\left(T_J - T_C\right) = h_L A_{L,S}\left(T_L - T_a\right) + \frac{k_L A_{L,C}}{L_L}\left(T_L - T_b\right) \tag{11}$$

Plug Eq. (11) into Eq. (8):

$$\begin{aligned} P_{tot} &= \sigma \in_C f_{C,ref} A_{C,C}\left(T_C^4 - T_{ref}^4\right) + h_C A_{C,C}\left(T_C - T_a\right) \\ &\quad + h_L A_{L,S}\left(T_L - T_a\right) + \frac{k_L A_{L,C}}{L_L}\left(T_L - T_b\right) + \frac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right) \end{aligned}$$

$$\begin{aligned} &= \sigma \in_C f_{C,ref} A_{C,C}\left(T_C^4 - T_{ref}^4\right) + h_C A_{C,C}\left(T_C - T_a\right) \\ &\quad + \left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}\left(T_J - T_C\right) + \frac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right) \end{aligned} \tag{12}$$

Solve for T_J from Eq. (12):

$$T_J = T_C + \left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}^{-1}\left\{P_{tot} - \left[\begin{array}{l} \sigma \in_C f_{C,ref} A_{C,C}\left(T_C^4 - T_{ref}^4\right) \\ + h_C A_{C,C}\left(T_C - T_a\right) + \dfrac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right) \end{array}\right]\right\} \tag{13}$$

In Eq. (13), the junction temperature is what we need, but there are two unknown temperatures, such as T_b and T_C. Therefore we must seek another two equations to obtain T_b and T_C.

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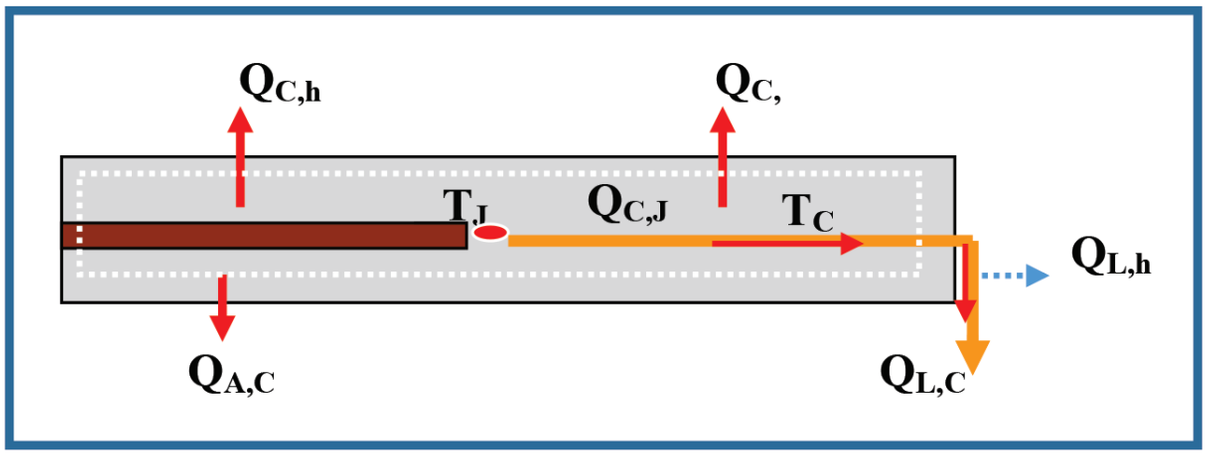


Figure 8. Junction temperature and heat transfer diagram inside the chip.

2.5.3. Consider a control volume around the air flow channel without considering adjacent heat source

Consider a control volume around the air flow channel as shown in **Figure 9**. The conduction heat transfer from component to board $Q_{C,C}$ is the sum of $Q_{L,C}$, $Q_{A,C}$, and $Q_{N,C}$, where $Q_{L,C}$=conduction heat transfer through lead, $Q_{A,C}$=conduction heat transfer through air gap under the component, and $Q_{N,C}$=adjacent heat input.

$$Q_{C,C} = Q_{L,C} + Q_{A,C} + Q_{N,C}$$

Neglect $Q_{N,C}$ heat conduction from neighbor and consider a control volume shown as in **Figure 9**. Chip heat conductance power $Q_{C,C}$ is then the sum of $Q_{b,h}$, $Q_{bb,h}$, $Q_{b,R}$, and $Q_{bb,R}$, where $Q_{b,h}$=convection heat transfer from board top surface, $Q_{bb,h}$=convection heat transfer from board bottom surface, $Q_{b,R}$=radiation heat transfer from board top surface, and $Q_{bb,R}$=radiation heat transfer from board bottom surface.

$$Q_{C,C} = \left(Q_{b,h} + Q_{bb,h}\right) + \left(Q_{b,R} + Q_{bb,R}\right) \tag{14}$$

From Eq.(1), with energy conservation of airflow channel:

……With energy conservation of air flow channel:

$$Q_{b,h} + Q_{b,R} + Q_{C,R} + Q_{C,h} + Q_{L,h} = m_{air} C_{p,air} \left(T_o - T_i\right) \tag{15}$$

Plug Eq. (15) into Eq. (1) and obtain Eq. (16):

$$
\begin{aligned}
P_{tot} &= Q_{C,R} + \left(Q_{C,h} + Q_{L,h}\right) + \left(Q_{L,C} + Q_{A,C}\right) \\
&= Q_{C,R} + \left[m_{air} C_{p,air} \left(T_o - T_i\right) - Q_{b,h} - Q_{b,R} - Q_{C,R}\right] + \left(Q_{L,C} + Q_{A,C}\right) \\
&= \left[m_{air} C_{p,air} \left(T_o - T_i\right) - Q_{b,h} - Q_{b,R} + \left(Q_{L,C} + Q_{A,C}\right)\right.
\end{aligned} \tag{16}
$$

$$
\text{Science } Q_{C,C} = Q_{L,C} + Q_{A,C} = \left(Q_{b,h} + Q_{bb,h}\right) + \left(Q_{b,R} + Q_{bb,R}\right) \tag{14}
$$

Plug Eq.(14) into Eq.(16), and solve for it, i.e.,

$$
P_{tot} = m_{air} C_{p,air} \Delta T + Q_{bb,h} + Q_{bb,R} \tag{17}
$$

Assuming $Q_{bb,h}$ and $Q_{bb,R}$ can be ignored, Eq. (17) turns out to be:

$$
P_{tot} = m_{air} C_{p,air} \left(T_o - T_i\right) \tag{18}
$$

It is reasonable that all the power generation from the component should be carried away by the air flow. If not, the board temperature, the case temperature, and the junction temperature will be increased. However, Eq. (18) cannot help to solve the board temperature; therefore, we need to seek another control volume to solve $T_{b.}$

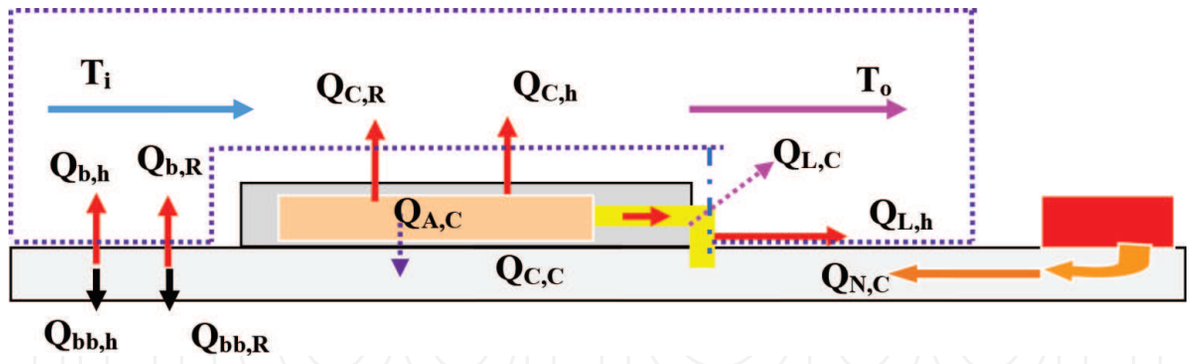


Figure 9. Schematic diagram for airflow channel.

2.5.4. Consider a control volume around the board

Consider a control volume around the board as in **Figure 10**, where T_b=board temperature (K), $Q_{C,C}$=conduction heat transfer from component to board (W), $Q_{b,h}$=convection heat transfer from board top surface (W), $Q_{bb,h}$=convection heat transfer from board bottom surface (W), $Q_{b,R}$=radiation heat transfer from board top surface (W), $Q_{bb,R}$=radiation heat transfer from board bottom surface (W), and $Q_{N,C}$=conduction heat transfer from neighboring component (W).

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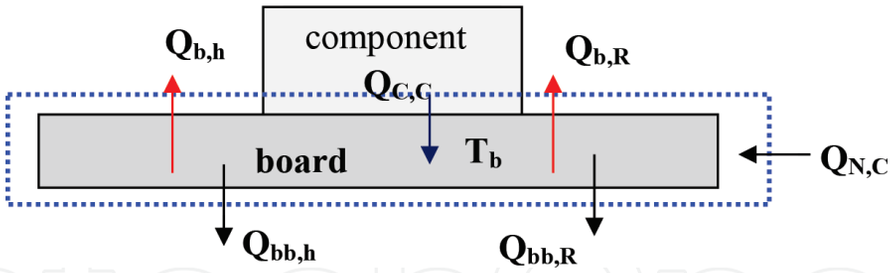


Figure 10. Schematic of chip on board.

Energy balance for the steady-state condition:

$$Q_{in} = Q_{out}$$

$$Q_{C,C} + Q_{N,C} = Q_{b,h} + Q_{bb,h} + Q_{b,R} + Q_{bb,R} \tag{19}$$

If neglect the bottom back board thermal convection and radiation effects, then $Q_{bb,h} = Q_{b,R} = 0$. Assume $Q_{N,C}$=0 and simplify Eq. (19) to be Eq. (20):

$$Q_{C,C} = Q_{L,C} + Q_{A,C} = Q_{b,h} + Q_{b,R} \tag{20}$$

where $Q_{L,C}$=conductance heat transfer from lead (W) and $Q_{A,C}$=conduction heat transfer through air gap under the component (W).

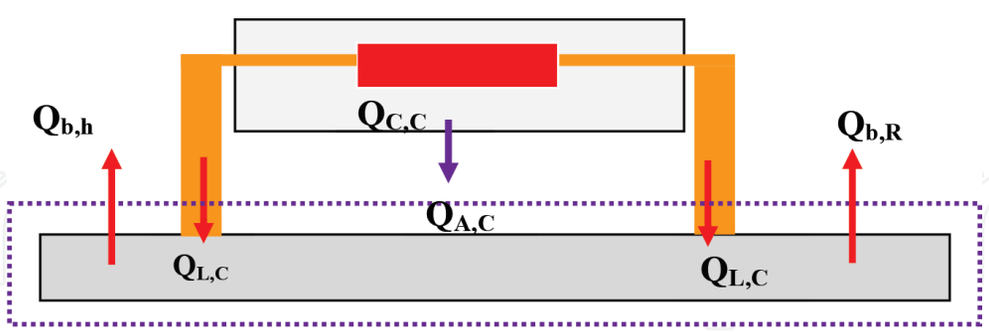


Figure 11. Schematic of heat transfer from lead to board.

In **Figure 11**, the conduction heat transfer from component to board $Q_{C,C}$ is the sum of the conductance heat transfer from lead $Q_{L,C}$ and the conduction heat transfer through air gap under the component $Q_{A,C}$. If we neglect the convection heat transfer from board bottom surface $Q_{bb,h}$ and the radiation heat transfer from board bottom surface, then the power $Q_{C,C}$ should also equal to the sum of convection heat transfer from board top surface $Q_{b,h}$ and radiation heat transfer from board top surface $Q_{b,R}$. Therefore,

$$P_{tot,board} = Q_{C,C} = Q_{L,C} + Q_{A,C} = Q_{b,h} + Q_{b,R}$$

$$= h_b\left(A_b - A_{C,C}\right)\left(T_b - T_a\right) + \sigma\grave{o}_b f_{b,ref}\left(A_{b-}A_{C,C}\right)\left(T_b^4 - T_a^4\right) \quad (21)$$

where h_b=heat transfer coefficient of air flow associated with the board, A_b=board upper surface area, and $A_{C,C}$=component top surface area=bottom surface area.

After obtaining a first estimate of the board temperature and assuming that the heat is uniformly distributed over the board, neglect $Q_{b,R}$ and thus obtain an initial average board temperature:

$$P_{tot,board} = h_b\left(A_b - A_{C,C}\right)\left(T_b - T_a\right) \quad (22)$$

Solve T_b from Eq. (22):

$$T_b = \frac{P_{tot,board}}{h_b\left(A_b - A_{C,C}\right)} + T_a \quad (23)$$

Hence, we have a first estimate of T_b.

where P_{tot}=total power generation from chip and $P_{tot,board}$=total power conduction to the board.

Remember, P_{tot} is different from $P_{tot,board}$. In general, under the forced convection condition, the heat conductance into the board is around 20–30%, $P_{tot,board}$=0.2P_{tot} ~ 0.3P_{tot} whereas, under the natural convection condition, the heat conductance into the board is only 70–80%, $P_{tot,board}$=0.2P_{tot} ~ 0.3P_{tot}

2.5.5. Solve for T_C, T_b, and T_J

2.5.5.1. Method 1

2.5.5.1.1. If $R_{th,JC}$ can be obtained from the vendor:

$$R_{th,JC} = \frac{T_J - T_C}{P_{tot}} \quad (24)$$

Combining Eqs. (13), (23), and (24), T_J, T_b, and T_C can be solved.

$$T_J = T_C + \left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}^{-1} \left\{ P_{tot} - \left[\begin{array}{l} \sigma \in_C f_{C,ref} A_{C,C} \left(T_C^4 - T_{ref}^4\right) + \\ h_C A_{C,C} \left(T_C - T_a\right) + \frac{k_A A_{C,C}}{t_A} \left(T_C - T_b\right) \end{array} \right] \right\} \tag{13}$$

$$T_b = \frac{P_{tot,board}}{h_b \left(A_b - A_{C,C}\right)} + T_a \tag{23}$$

2.5.5.1.2. If $R_{th,JC}$ is unknown

Assume that P_{up} is uniformly spread over the entire upper surface of the component. Therefore,

$$P_{up} = h_C A_{C,C} \left(T_C - T_a\right) \tag{25}$$

$$P_{tot} - P_{tot,board} = P_{tot} - h_b \left(A_b - A_{C,C}\right)\left(T_b - T_a\right)$$

$$T_C = \frac{P_{up}}{h_C A_{C,C}} + T_a \tag{26}$$

From Eqs.(13), (23), and (26), solve for T_j, T_b and T_c.

$$T_J = T_C + \left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}^{-1} \left\{ P_{tot} - \left[\begin{array}{l} \sigma \in_C f_{C,ref} A_{C,C} \left(T_C^4 - T_{ref}^4\right) + \\ h_C A_{C,C} \left(T_C - T_a\right) + \frac{k_A A_{C,C}}{t_A} \left(T_C - T_b\right) \end{array} \right] \right\} \tag{13}$$

$$T_b = \frac{P_{tot,board}}{h_b \left(A_b - A_{C,C}\right)} + T_a \tag{23}$$

In the case of duct flow, from Eq. (26), we need to obtain T_a. Let us reconsider the airflow over the component in a channel. If we neglect the radiation effect, the heat transported by the air is obtained from

$$T_C = \frac{P_{up}}{h_C A_{C,C}} + T_a \tag{26}$$

$$Q_{up,C} = \dot{m} C_{p,air} \left(T_o - T_i \right) \tag{27}$$

T_o is air exit temperature of the flow channel, whereas T_i is the air inlet temperature of the flow channel. T_o can be obtained from Eq. (28):

$$T_o = \frac{Q_{up,C}}{\dot{m} C_{p,air}} + T_i \tag{28}$$

In duct flow, the ambient temperature is the average temperature of the air inlet temperature and air exit temperature:

$$\begin{aligned} T_a &= \frac{\left(T_o + T_i \right)}{2} = \frac{1}{2} \left(\frac{Q_{up,C}}{\dot{m} C_{p,air}} + 2T_i \right) \\ &= \frac{Q_{up,C}}{2\dot{m} C_{p,air}} + T_i = \frac{P_{up}}{2\dot{m} C_{p,air}} + T_i \end{aligned} \tag{29}$$

Plug Eq. (29) into Eq. (26) and then obtain chip case temperature T_C:

$$T_C = \frac{P_{up}}{h_C A_{C,C}} + T_a = P_{up} \left(\frac{1}{h_C A_{C,C}} + \frac{1}{2\dot{m} C_{p,air}} \right) + T_i \tag{30}$$

However, in Eq. (30), the heat transfer coefficient h_C is still needs to be obtained.

2.5.5.2. Method 2

If h_C is not readily available, let us use the junction-to-ambient and junction-to-case thermal resistance for the component as shown in **Figure 12**, the schematic diagram of thermal resistance in flow channel.

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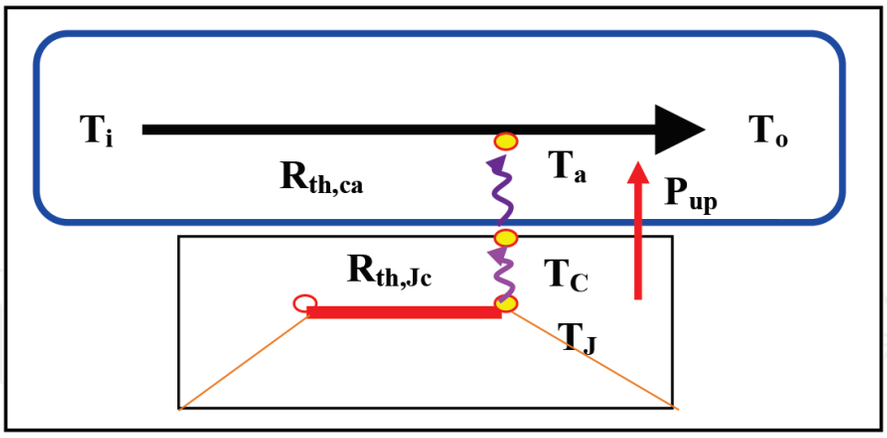


Figure 12. Schematic diagram of thermal resistance in flow channel.

The definition of thermal resistance $R_{th,JC}$ is the junction temperature (T_J) minus the chip case temperature T_C divided by power input as shown in Eq. (31):

$$R_{th,JC} = \frac{T_j - T_C}{P_{up}} \tag{31}$$

The thermal convection resistance from chip surface to ambient $R_{th,Ca}$ is shown in Eq. (32):

$$R_{th,Ca} = \frac{1}{h_C A_{C,C}} \tag{32}$$

Therefore, the total thermal resistance $R_{th,Ja}$ is the sum of $R_{th,JC}$ and $R_{th,Ca}$, shown as in Eq. (33):

$$R_{th,JC} + R_{th,Ca} = R_{th,Ja} \tag{33}$$

The thermal resistance $R_{th,Ch}$ (or $R_{th,Ca}$) can be represented by Eq. (34):

$$R_{th,Ch} = R_{th,Ca} = \frac{T_c - T_a}{P_{up}} = \frac{T_c - \frac{P_{up}}{2\dot{m}C_{p,air}} - T_i}{P_{up}}$$

$$= \frac{T_c}{P_{up}} - \frac{1}{2\dot{m}C_{p,air}} - \frac{T_i}{P_{up}} \tag{34}$$

The case temperature T_C can be represented by Eq. (35):

$$T_c = P_{up}\left(R_{th,Ca} + \frac{1}{2\dot{m}C_{p,air}}\right) + T_i \tag{35}$$

$$R_{th,Ch} = R_{th,Ca} = \frac{1}{h_C A_{C,C}} = \frac{T_c - T_a}{Q_{C,h}} \tag{4}$$

Plug Eq. (4) into Eq. (35) and obtain Eq. (36):

$$T_c = P_{up}\left(\frac{1}{h_C A_{C,C}} + \frac{1}{2C_p\left(\rho_{air} V_{air} A_{channel}\right)}\right) + T_i \tag{36}$$

Eqs. (36) and (30) are the same.

$$T_c = P_{up}\left(\frac{1}{h_C A_{C,C}} + \frac{1}{2\dot{m}C_{p,air}}\right) + T_i \tag{30}$$

Basically, we can solve for T_J, T_b, and T_C from Eqs. (13), (23), and (26).

2.5.6. Consider a control volume around the air flow channel with adjacent heat source

Now, if we want get a more accurate expression for the board temperature T_b, then we can reconsider the energy balance for the board, as shown in **Figure 13**. Because the value for T_C is known from Eqs. (26) and Eq. (30) from Eq. (17):

$$P_{tot} = m_{air} C_{p,air} \Delta T + Q_{bb,h} + Q_{bb,R} \tag{17}$$

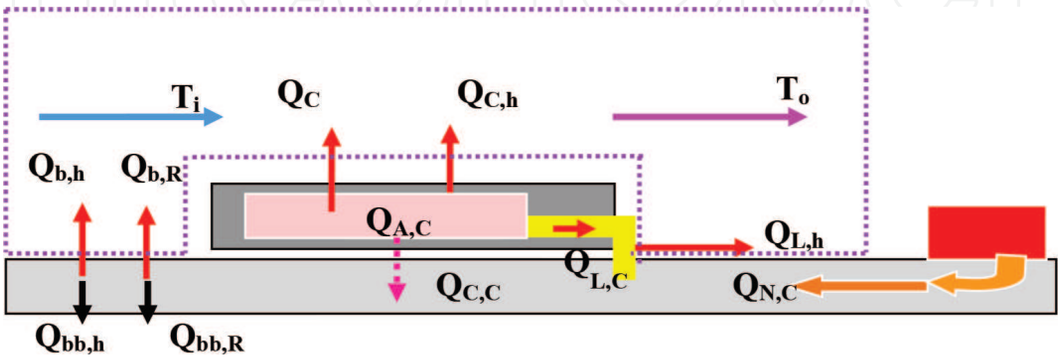


Figure 13. Schematic of chip thermal resistance and thermal resistance from adjacent heat source in the flow channel.

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Total power P_{tot} thus can be represented in terms of temperature:

$$P_{tot} = \dot{m}C_{p,air}\left(T_o - T_i\right) + h_{bb}A_{bb}\left(T_b - T_{amb,bb}\right) + \left(\frac{1}{R_{th,bbR}}\right)\left(T_b^4 - T_{N,bb}^4\right) \tag{37}$$

where $T_{N,b}$=neighboring board temperature where the component top surface sees for radiation exchange (K),h_{bb}=heat transfer coefficient from the backside of the board (W/m K), A_{bb}=back surface area associated with above convection loss (m^2), $R_{th,b,R}$=radiation heat transfer resistance with respect to the board (K/W), $R_{th,bb,R}$=radiation heat transfer resistance with respect to the back of the board (K/W), and $T_{N,bb}$=board temperature of the neighboring board where the radiation exchange takes place with back of the board where the component of interest resides.

Solve for T_b in Eq. (37); theoretically, we need more accuracy equation such as Eq. (38). In fact, it is not easy to solve for Eq. (38); sometimes, we need numerical analysis. In addition, there are some variables that could affect its accuracy, such as h_{bb} and $T_{N,b}$.

$$\left(\frac{1}{R_{th,bbR}}\right)T_b^4 + h_{bb}A_{bb}T_b$$

$$= P_{tot} + \left(\frac{1}{R_{th,bbR}}\right)T_{N,b}^4 + h_{bb}A_{bb}T_{amb,b} - \dot{m}C_p\left(T_o - T_i\right) \tag{38}$$

Because we have T_b, T_C, and T_a, T_J can be calculated from Eq. (13).

$$T_J = T_C + \left(\frac{k_L A_{L,C}}{L_L}\right)_{eff}^{-1}\left\{P_{tot} - \left[\begin{array}{l}\sigma\grave{o}_C f_{C,ref}A_{C,C}\left(T_C^4 - T_{ref}^4\right) + \\ h_C A_{C,C}\left(T_C - T_a\right) + \dfrac{k_A A_{C,C}}{t_A}\left(T_C - T_b\right)\end{array}\right]\right\} \tag{13}$$

Figure 14 shows the flow chart solution for T_J. (i) Consider a control volume around the outside of the component and lead pin for the first. Get a chip power P_{tot} as a function of (T_L, T_b, T_C, T_a). (ii) Consider a control volume around the inside of the component and get junction temperature (T_J) as the function of (T_b, T_C, T_a). (iii) Consider a control volume around the air flow channel, and the total power P_{tot} is equal to $mC_p(T_o - T_i)$. (iv) Consider a control volume around the board and assume that the power input to the board $P_{tot,board}$ is n times of the total power P_{tot}, $P_{tot,board}=nP_{tot}$. The average board temperature T_b obtained at this time is the function of $P_{tot,board}$ and T_a. (v) If the vendor can provide $R_{th,JC}$ data, then T_J, T_b, T_C, and T_a can be calculated. (vi) Calculate $Q_{L,C}$ and $Q_{A,C}$. Calculate $P_{tot,board}=Q_{L,C}+Q_{A,C}$, and $(P_{tot,board}/P_{tot})=n'$; if $(n'-n)/n>5\%$,

take new n for n=(n'+n)/2, back to (iv) using iterative method, and recalculate until (n'-n)/n<5%. Remember, the goal is to solve for T_J,Therefore, to ensure $\eta = \frac{\Delta T_{J,calc}}{\Delta T_{J,spec}} = \frac{T_{J,calc} - T_\infty}{T_{J,spec} - T_\infty} \leq 0.9$.

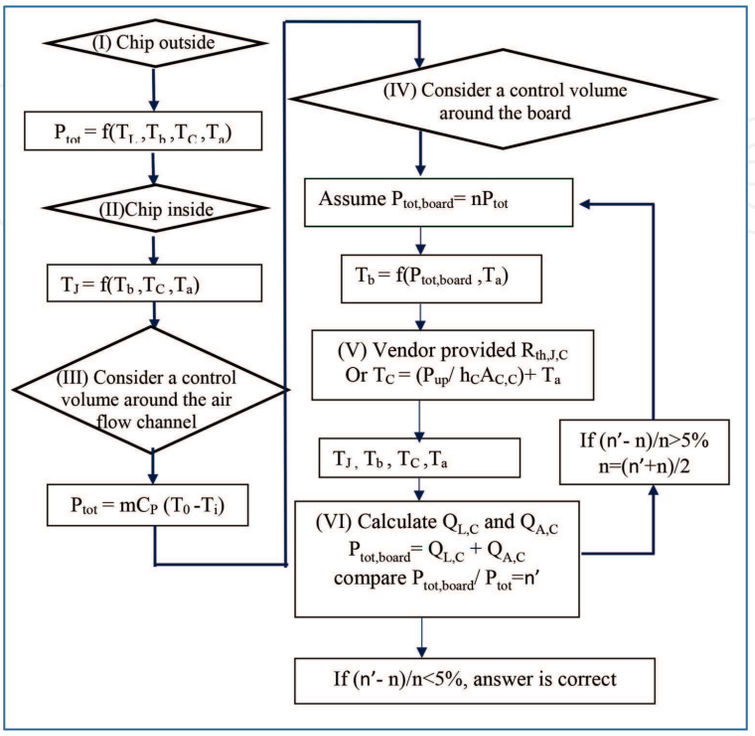


Figure 14. Flow chart of junction temperature calculation using the iterative method.

3. Summary

The goal of the thermal designer is to minimize the thermal resistance of the chip. Equations and analysis procedures are provided in this chapter to assist the designer in understanding the thermal characteristics of chip devices and the thermal performance of related materials. The methods are useful for the approximations of the chip junction temperature. In the meantime, the permissible dissipated powers of chip can be estimated as well.

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