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The Fabrication of High Aspect Ratio Nanostructures on Quartz Substrate

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1. Introduction

Recent developments in nano-scale devices have imposed many complex patterns with high aspect ratio nanostructures in its design. High aspect-ratio nanostructures have many applications such as X-ray diffractive optical elements [1,2], nano-electro-mechanical-system (NEMS), fuel cell electrodes [3] and nanoimprint molds [4]. However, fabricating the high aspect-ratio nanostructures is still a challenging problem. For silicon technology, Bosch process [5] which is based on alternating multiple steps of etching and sidewall passivation is normally employed to achieve a high aspect ratio nanostructure. Other alternative is the cryogenic process [6] which is cooling the silicon substrates to cryogenic temperature using liquid nitrogen in order to achieve vertical sidewall profiles during etching. These processes however are not suitable for quartz.

In addition, although a large number of articles on high aspect-ratio silicon structures have been reported, limited information is available for quartz etching process in achieving high aspect-ratio nanostructures. Fabricating high aspect-ratio nanostructures on glass or quartz would open several new possibilities in the MEMS/NEMS field and especially in BioMEMS.

In this chapter, we explained the pattern transfer process required on quartz substrate using CHF_3/Ar reactive ion etching (RIE) technique. The fabrication of feature sizes below 100 nm on quartz substrates will be demonstrated by understanding first the etching mechanism of quartz and then finding an optimised RIE process.

2. The fabrication method

Quartz is an insulating and hard substrate material in which patterning on top of its surface using electron beam lithography (EBL) is very challenging. Surface charging is the major issue

for pattern writing on the insulating substrates using an EBL technique. The trapped and built-up charges by the e-beam exposure on the insulating substrates surface may deflect or distort the e-beam positioning, and eventually may cause undesired effects. A conductive layer is required to ground the trapped charges in minimising the surface charges. There are several ways to suppress the charging effects by draining the charges to the ground, such as thin metallic or carbon coating on top or underneath the resist layer [7].

This chapter presents a number of approaches attempted for grounding the trapped charges for suppressing the surface charging effects during the pattern definition on quartz substrate. This also applies in fabricating three-dimensional nanostructures on insulating substrates [8]. The deposition of thin metallic layer on top of imaging resist layer is a common practise but requires wet etching process using acidic solution to remove the metallic layer in post e-beam exposure process. Most lithographers will avoid this technique as this process is the source of particles contamination and other incomplete removal issues.

We developed and investigated two methods of charge suppression using a thin metallic coating on quartz substrate and a conductive polymer coating on top of the imaging resist layer. The processes involved in each method are illustrated in Figure 1(a) and (b).

2.1. Thin metallic coating on quartz substrate

In this technique as illustrate in Figure 1(a), a cleaned quartz substrate was firstly sputtered with a 5 nm thick Tungsten (W) as a charge dissipation layer using Edward Auto500 Magnetron Sputtering system prior to the poly-methyl-methacrylate (PMMA) bi-layer resist coating. The thin Tungsten layer can be stripped off easily using a short sulphur hexafluoride (SF_6) plasma etching at a later stage.

A positive PMMA bi-layer resist was spun coated onto the tungsten coated quartz substrate. Each layer of PMMA was spun coated at spinning speed of 4000 rpm for one minute. The first layer of 4% low molecular weight (LMW) PMMA was spun followed by hard baking at 185°C for 30 minutes and then allowed to cool down to room temperature. Then the second layer of 2.5% high molecular weight (HMW) PMMA was spun and hard baked at 185°C for 30 minutes. The LMW PMMA layer thickness was 80 nm and the HMW PMMA was 120 nm when measured using a Dektak surface profiler system. The total PMMA bi-layer thickness was approximately 200 nm.

Pattern definition using single pass line (SPL) method of e-beam exposure was carried out using Raith-150 EBL tool with voltage acceleration of 10 keV, an aperture size of 30 microns and e-beam dosage of 110 $\mu\text{C}/\text{cm}^2$. The e-beam exposed sample was then developed in a MIBK:IPA 1:3 developer at a temperature of 23 °C for 30 seconds. Short O_2 plasma is recommended for descumming the residual resist layers. The O_2 plasma exposure duration of 15 seconds at 100 W of O_2 plasma power should be appropriate to clear the residual layer of 10 nm to 20 nm for 100 nm feature, however, longer O_2 plasma exposure may enlarge the pattern size.

A 40 nm thick of nichrome (NiCr) 80/20 99.999% was then thermally deposited on the developed sample using a thermal metal evaporator system. The lift-off process was carried out to

remove the unwanted resist and metal layers by soaking the sample in acetone for about three hours. A very short (about 10 seconds) RIE plasma process with SF_6 etchant gas was utilized to remove the exposed tungsten layer.

Finally an RIE process with CHF_3/Ar chemistry was used to etch the quartz substrate anisotropically. By using this technique, two metal layers (NiCr and W) were left on the top of the fabricated nanostructures. Another technique of fabricating nanostructures on quartz substrate is explained next.

2.2. Conductive polymer coating on top of resist

The nanofabrication process using this technique is illustrated in Figure 1(b). In this technique, a water soluble conductive polymer, poly (3,4 – Etylenedioxythiophene) / poly(styrenesulfonate) (PEDOT/PSS) was used as the charge dissipation layer [8].

A positive PMMA bi-layer resist was spun coated onto the cleaned quartz substrate as explained in previous section. PEDOT/PSS was then spun coated on top of PMMA bi-layer at spinning speed of 5000 rpm for one minute to achieve a 30 nm layer thickness.

The only issue with PMMA bi-layer resist was that its hydrophobic surface caused great difficulties for the watery solution to adhere to its surface. One well-known method of reducing the hydrophobicity or in other words, increasing the wettability of the PMMA bi-layer surface is by O_2 plasma surface treatment. Only very short O_2 plasma was needed to improve the wettability of the PMMA bi-layer surface.

The sample was then e-beam exposed using Raith-150 EBL system for pattern definition process as explained in previous section. Prior to the pattern development process, the unexposed PEDOT/PSS layer was removed by rinsing with deionised water (DIW) at room temperature for one minute.

In pattern definition process for feature size larger than 100 nm, the PEDOT/PSS layer was exposed with larger e-beam bombardment on a larger area which leads to the diffusion of PEDOT/PSS molecules into PMMA layer. This made the removal of PEDOT/PSS layer using DIW at room temperature became difficult. One option to resolve this issue is by increasing the DIW temperature to 45 °C and placed in ultrasonic bath for a couple of seconds.

The e-beam exposed samples were then developed in MIBK:IPA 1:3 at a temperature of 23 °C for 30 seconds and followed by metallization process. In additive pattern transfer employed, a 40 nm NiCr 80/20 99.999% layer was deposited as a pattern masking layer using thermal evaporator as explained in previous section. In order to realize the pattern, the unwanted NiCr layer was lifted off by soaking in acetone for about 3 hours.

At final stage, RIE process with CHF_3/Ar chemistry was used to etch the quartz substrate anisotropically. Using this technique, only a NiCr masking layer is left on top of the fabricated nanostructure. This metal layer can later be removed by the Chrome etch acidic solution.

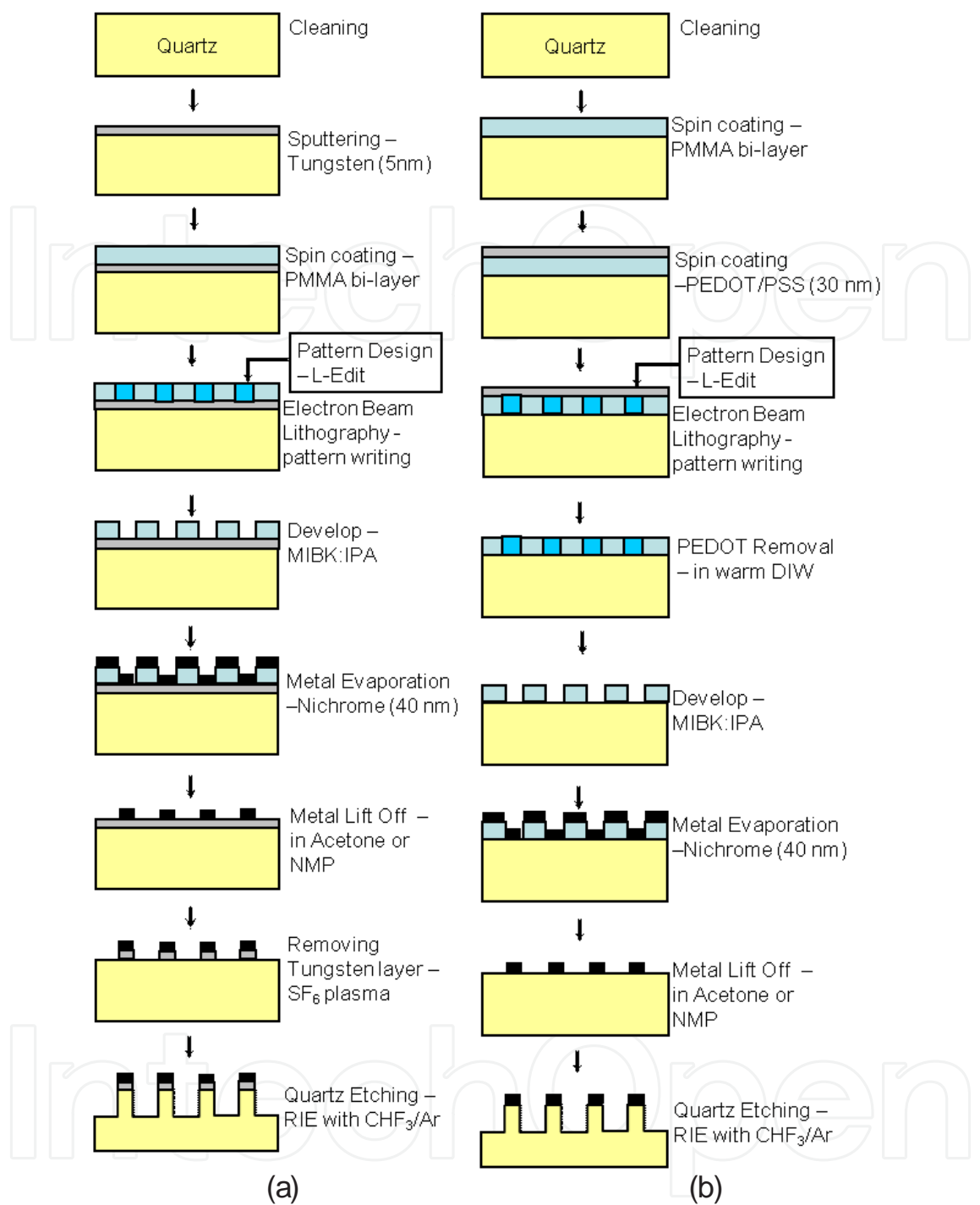


Figure 1. The fabrication process of nanostructures on quartz substrate using various charge suppression method (a) thin metallic coating (tungsten) on quartz substrate and (b) conductive polymer (PEDOT/PSS) coating on top of the resist.

3. The pattern transfer process

The RIE pattern transfer process employing CHF₃/Ar gas mixture was carried out using Oxford Plasmalab 80Plus etcher. A 100 nm diameter silicon wafer with a thick NiCr coated layer was

clamped physically onto the power electrode as a sacrificial masking layer. The electrical power was supplied to the electrode at a radio frequency (RF) of 13.56 MHz to produce plasma discharge.

Trifluoromethane (CHF_3 or Freon 23, sometimes called Halocarbon 23) was used as the main processing gas owing to its moderate F/C ratio resulting in a moderate etching rate which is essential in controlling the etching profiles. For etching the narrow high aspect ratio nanostructures, there are limited ions and neutral transport present within the trench which limits the chemical reactions. Hence, large aspect ratio and dense nanostructures are etched more slowly than low aspect ratio nanostructures [9]. Moderate to low etching rate is appropriate for this work.

Oxide such as silicon dioxide (quartz) etching using CHF_3 etchant can only take place for RF bias values above 55 V at 1 mTorr etching pressure [10]. A higher RF bias value is required for quartz etching if operating at a higher etching pressure. A bias voltage of -330 V was achieved by this work showing good directionality of the plasma bombardments onto substrate surface.

An additive inert gas argon (Ar) was added to stabilize plasmas and to add inert ion bombardment of a surface, resulting in more directional or anisotropic etching [11] for a steep sidewall profile. The pattern transfer onto quartz substrates is obtained by CHF_3/Ar RIE with the optimised parameter as in Table 1.

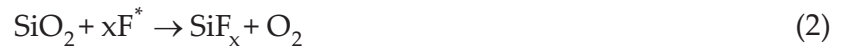
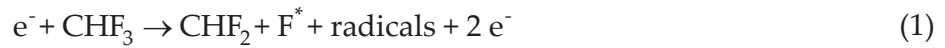
RIE Parameter	Setting/measured
Gases	CHF_3/Ar
Flow rate	50/30 sccm
Pressure	20 mTorr
Temperature	295 K
RF Power	200 W
RF Power density	2.5 W/cm ²
Bias Voltage	-330 V
Etch rate	10 nm/min

Table 1. An optimized CHF_3/Ar RIE parameter for 2D pattern transfer onto quartz substrate

3.1. The etching chemistries

In fluorine-containing plasma for example, surface reaction, etching and polymerization can occur at the same time. The domination of certain reactions is dependent on the gas feed, the operating parameters and the chemical nature of the polymer/substrate and electrode material and geometry [12].

In a quartz etching process using CHF_3 etchant, the free fluorine radical, F^* and radicals such as CF_x are created by the plasma discharge and the etching chemistries can be described as follows;



F^* is the reactive fluorine atom and SiO_2 is the quartz.

RIE plasma generates the reactive fluorine atom F^* , radicals and ions from the supplied etchant gas CHF_3 (Eqn. 1). The bombardments of the heavy argon ions break the Si-O bonds and then the disassociated silicon ions react with F free radicals to form a SiF_x . The etching of quartz consumes the F atom to form SiF_x and oxygen radicals (Eqn. 2). The resultant CF_x radicals tend to deposit polymer film on all surfaces, but the oxygen liberated in the etching of quartz reacts with the CF_x radicals to form volatile CO, CO_2 and COF_2 (Eqn. 3)[13]. Thus, both F and C are consumed but the polymer deposition releases the F atoms that enrich the F content hence, increasing the F/C ratio.

When the F concentration in the plasma is high, the CF_x radicals are destroyed by recombination at various surfaces of the plasma reactor and probably lead to the re-creation of volatile CF_4 . When the F concentration is low, surface production mechanism dominates the production of CF_2 which leads to the formation of a polymer layer at the surface (polymerization) [14]. The vertical sidewalls are created by the polymerization of the CF_x passivation layer.

In anisotropic etching, vertical sidewalls are the location where chemical reaction less occur and less exposure to ions bombardments, hence polymerization will build up on these locations. This process is called sidewall passivation in which the undercut etchings are prevented and steep sidewall profiles are realized.

3.2. The etching mechanism

The etching mechanism can be described as illustrated in Figure 2. There are two steps involved in the CHF_3/Ar RIE plasma process. Firstly the bombardment of heavy inert ions of argon mechanically breaks the bond of the substrate elements (Si-O). The high energy and heavy argon ions are accelerated by RIE plasma and act as bullets in bombarding substrate and mask surfaces. Si-O bonds are very strong and could only be dissociated by high energy plasma bombardment using heavy inert ions such as argon.

Then ion-induced chemical reaction at horizontal surface created the etching reaction products. The chemistry reactions will only take place when the freed ions/atoms are available after the breakage of the Si-O bonds.

The combination of these actions resulted in highly selective anisotropic etching of the substrate material. The etching selectivity of Chromium or NiChrome (NiCr) mask to quartz

substrate is about 18:1 [15]. Hence, the sample requires a NiCr masking layer of at least 35 nm thick to mask the pattern structures to achieve a 600 nm structure height on quartz substrate.

The etching process of quartz is the combination of physical etching by ions bombardment to break the bonding and chemical etching where the freed ions/atoms react to each other to create by-products and sucked away by the vacuum system. As the etching pressure used in this work are very low (< 30 mTorr), physical bombardment reactions are expected to dominate and less chemical reactions are involved in the etching process.

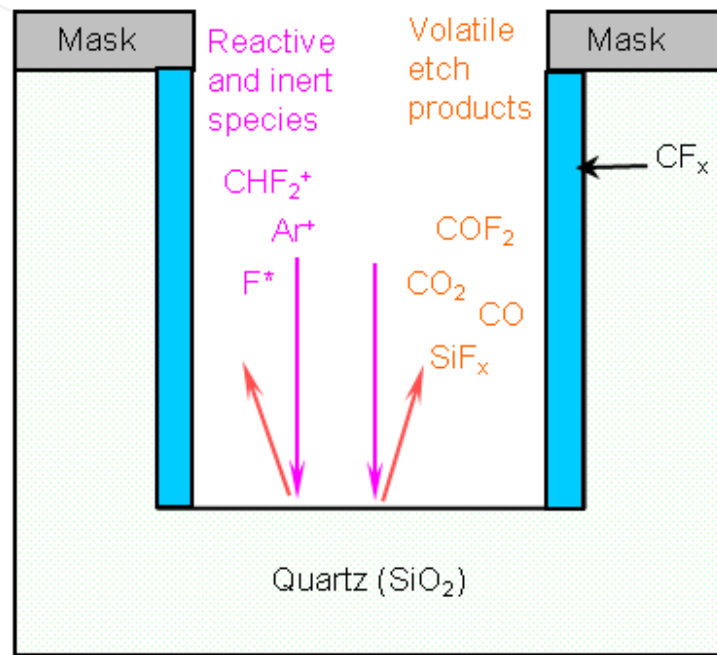


Figure 2. The schematic diagram of plasma etching mechanism, showing the fluorinated reactive gases and the by-products generated during the quartz etching process.

3.3. The etching cycle

Deep etching on quartz substrate requires a long etching time owing to very low etching rate of about 10 nm/min. Continuous heavy ions bombardments on the substrate surface for long period of time may result in increase of surface temperature. When the surfaces heat up, the F/C ratio could decrease, which would decrease the etching reactions as well. The etching rate could decrease to the point where the quartz etching may actually stop [16]. This can be avoided by etching in a short interval of time and repeat the etching cycle after the samples have cooled down.

In this research work, five minutes of cooling intervals on every 15 minutes of plasma etching process was employed to achieve a vertical sidewalls profile. This 'duty cycle' etching method as illustrated in Figure 3 has shown beneficial to minimise heat generation effects and achieve high aspect ratio nanostructures with vertical sidewalls.

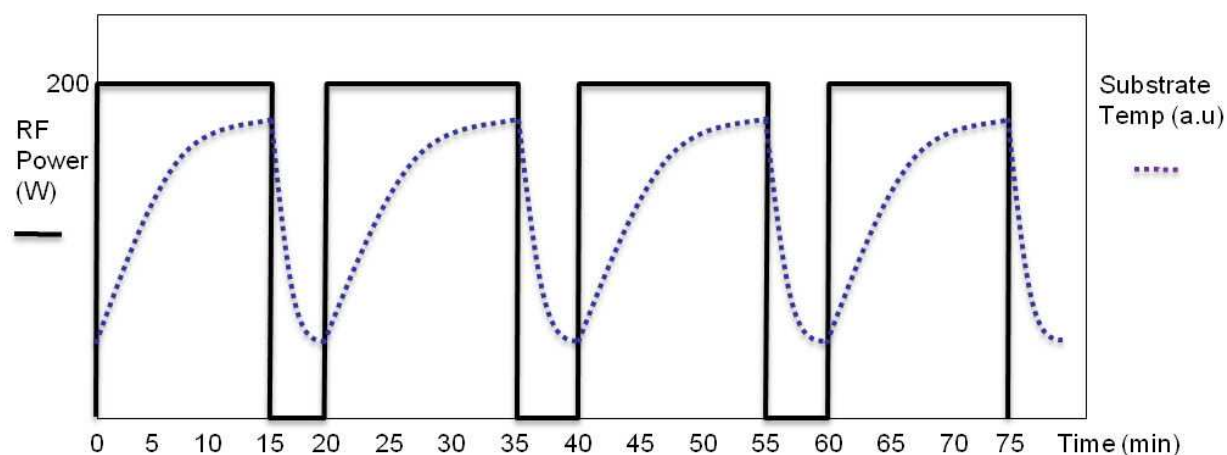


Figure 3. The profiles of the RIE RF power and the substrate temperatures in the 'duty cycle' etching method.

4. The fabrication results

Nanostructures with feature sizes of 20 nm, 40 nm, 50 nm, 60 nm, 70 nm and 90 nm have been attempted by this work. However, only the high aspect ratio nanostructures with feature sizes above 60 nm have been successfully fabricated on quartz substrates [17]. The subsequent figures show the SEM images of the results of the developed nanofabrication process in isometric angle.

Figure 4 shows an SEM image of the fabricated high aspect ratio structures on quartz substrate with dimensions of 60 nm lines width, 600 nm in height and 120 nm spacing. Hence, high aspect ratio nanostructures of up to 1:10 and sound vertical sidewall profiles have been demonstrated by this work. The second line from left is a bit shifted in the middle because of the presence of thin residual layer during metal deposition process and later shifted during the lift-off process.

Figure 5 shows another SEM image of high aspect-ratio nanostructures with dimensions of 90 nm lines width, 600 nm in height and 180 nm spacing. It has better sidewall, fine surface and flat top profiles as compared to 60 nm feature sizes nanostructure.

Figure 6 shows the SEM image of various high aspect-ratio nanostructures with feature sizes above 60 nm fabricated by this work. We have demonstrated various vertical sidewall nanostructures such as elbow corners, transistor-like profile and periodic lines. Almost all the nanostructures have vertical sidewall and flat top surface.

Figure 7 shows the line structures with width dimensions of 50 nm and 70 nm for comparison. The nanostructures of 50 nm in width failed to preserve the flat top surface which leads to uneven profile of top surface as compared to the 70 nm nanostructures.

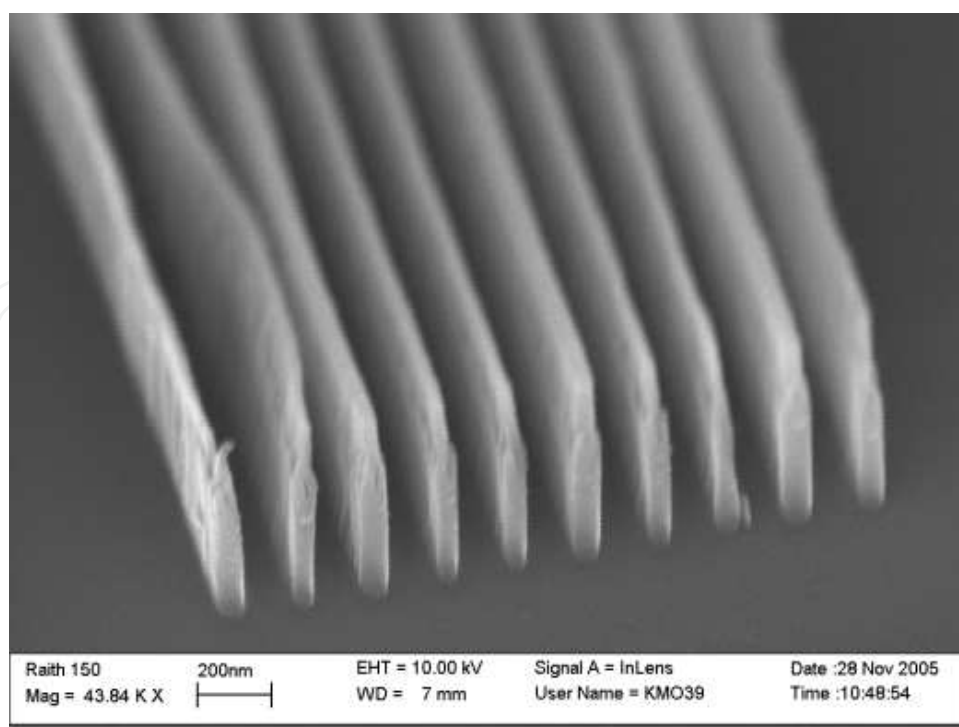


Figure 4. SEM images of the fabricated 2D high aspect-ratio nanostructures on quartz substrates showing the 60 nm lines structure with 600 nm height and 120 nm spacing.

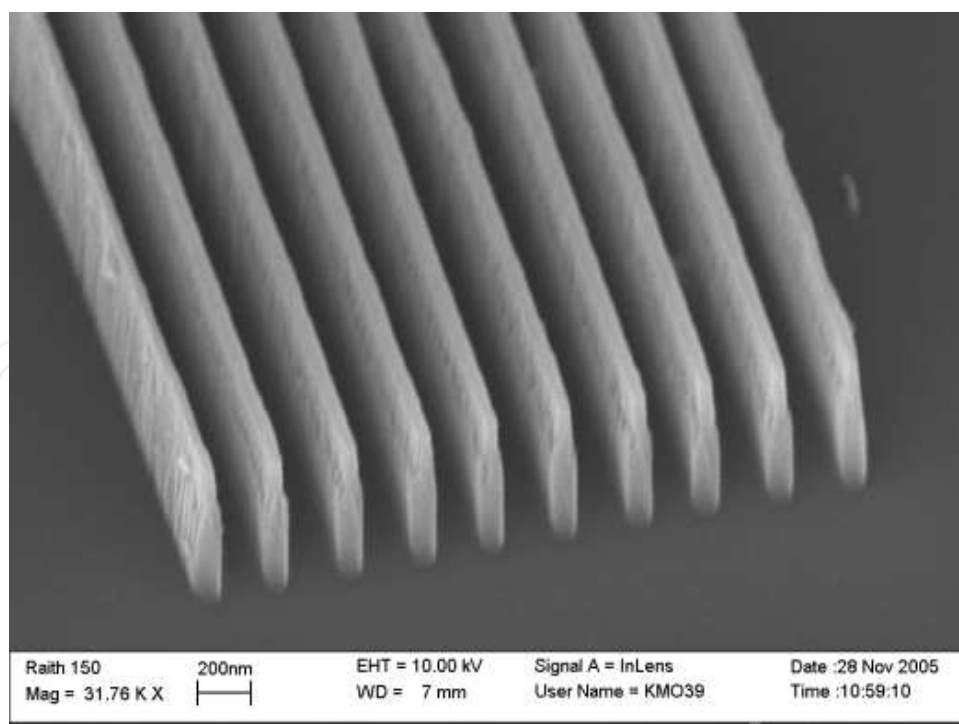


Figure 5. SEM images of the fabricated 2D high aspect-ratio nanostructures on quartz substrates showing the 90 nm lines structure with 600 nm height and 180 nm spacing

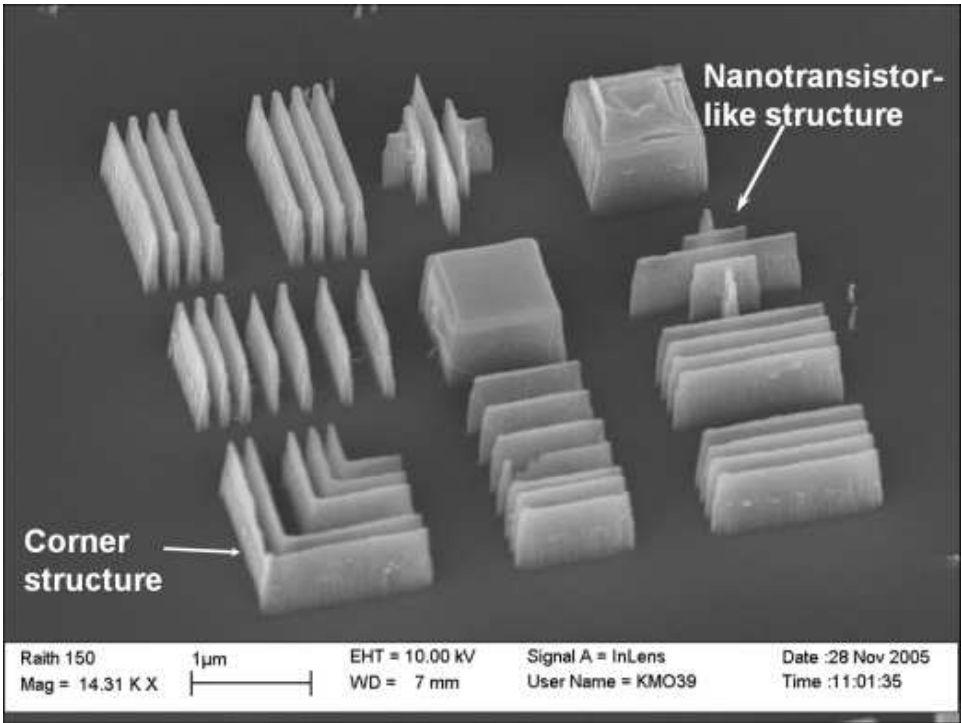


Figure 6. SEM image of the fabricated 2D high aspect-ratio nanostructures on quartz substrates with feature sizes of 60 nm width and 600 nm height lines, corner lines and transistor-like nanostructures.

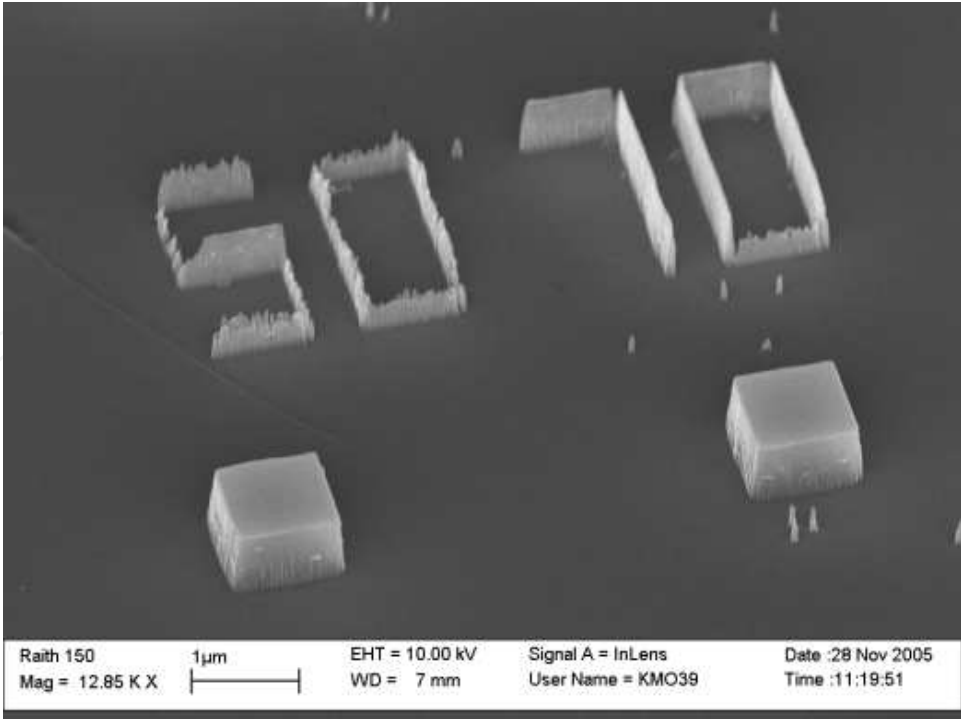


Figure 7. SEM image showing the comparison between the fabricated 50 nm and 70 nm nanostructures after the long etching process

5. Analysis and discussions

For feature sizes below 60 nm, the line structure failed to preserve the flat top surface as compared to the feature sizes above 60 nm. It could be to the insufficient of NiCr mask layer thickness in protecting or masking the top surface from ions bombardment. The NiCr masking layer was completely etched away earlier than the total etching time.

The uneven profile of NiCr masking layer could be due to blockage of the resist pattern during the metallization process. This could be explained schematically as illustrated in Figure 8, where it shows the diagram of metal deposition process for NiCr masking layer. During metal deposition process using thermal evaporator, depositing a metal layer through a narrow trench is difficult. Figure 8 also point out the location (at the entrance of the trench) of the shadowing effects and the difference between the measured coating thicknesses on top of the resist as compared to the actual NiCr mask thickness deposited on the substrate. This could be improved by using a thinner resist layer and a special developer that formulated for developing pattern with feature sizes less than 60 nm.

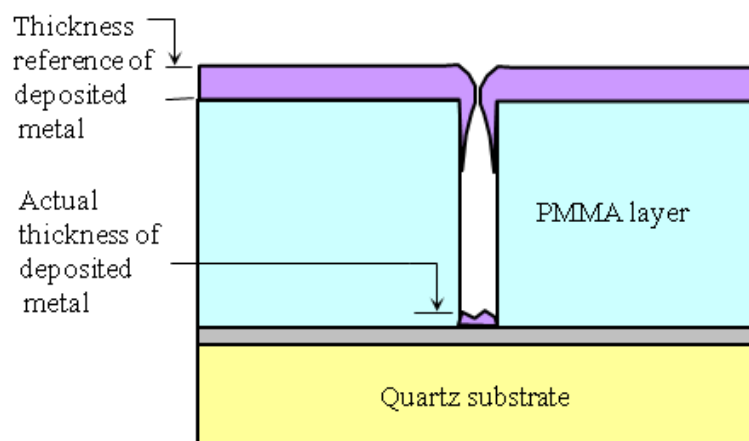


Figure 8. The schematic diagram describing the issue of metal deposition on feature sizes below 50 nm using PMMA bi-layer where shadowing effects causing insufficient metal deposition on fine feature sizes.

Figure 9 shows the SEM image of the deposited NiCr mask layer on quartz substrate where it shows 20 nm in width lines. The uneven brightness of the lines image could be due to uneven deposited thickness of NiCr mask layer. It has been observed that the NiCr layer thickness is less than 1/3 of the estimated thickness by metallization process due to shadowing effects.

Figure 10 shows the SEM image the 40 nm lines nanostructures after the etching process. The 40 nm lines feature failed to preserve the flat top surface due to the uneven and insufficient NiCr mask layer thickness. The NiCr masking layer was etched away earlier than the total etching time.

Figure 11 shows the SEM image of 20 nm line feature with worse condition than 40 nm lines feature. The metal deposition process is more difficult for fine feature size which leads to lesser NiCr masking layer thickness. A new metal deposition method and new masking material could be attempted to resolve this issue.

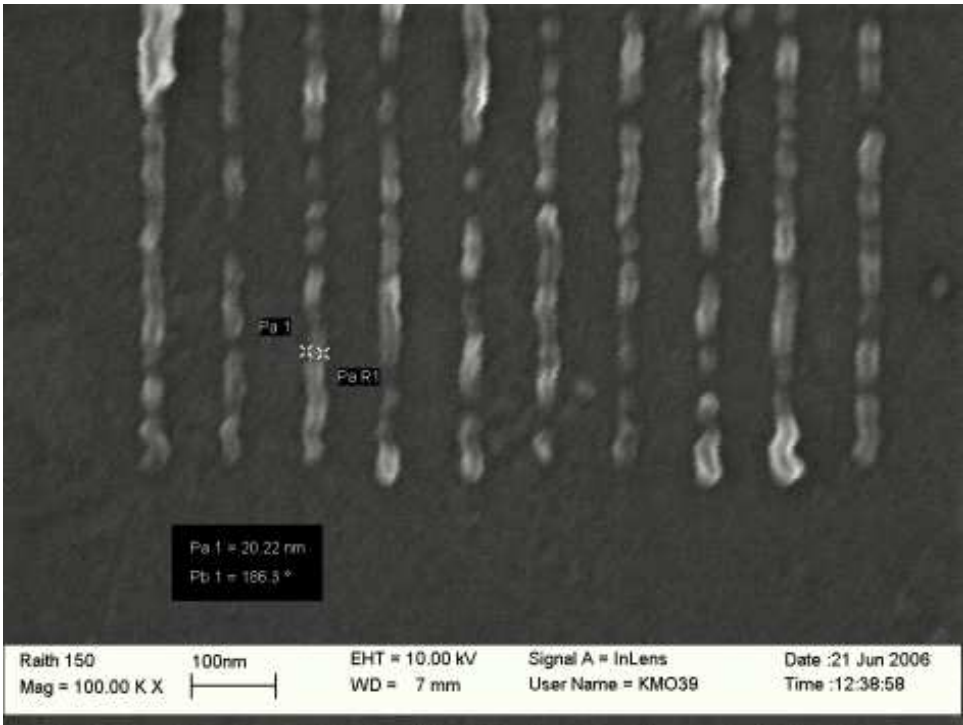


Figure 9. SEM image of 20 nm line pattern metallization (NiCr) on quartz substrate. The NiCr layer thickness is less than 1/3 of the estimated thickness by metallization process due to shadowing effects.

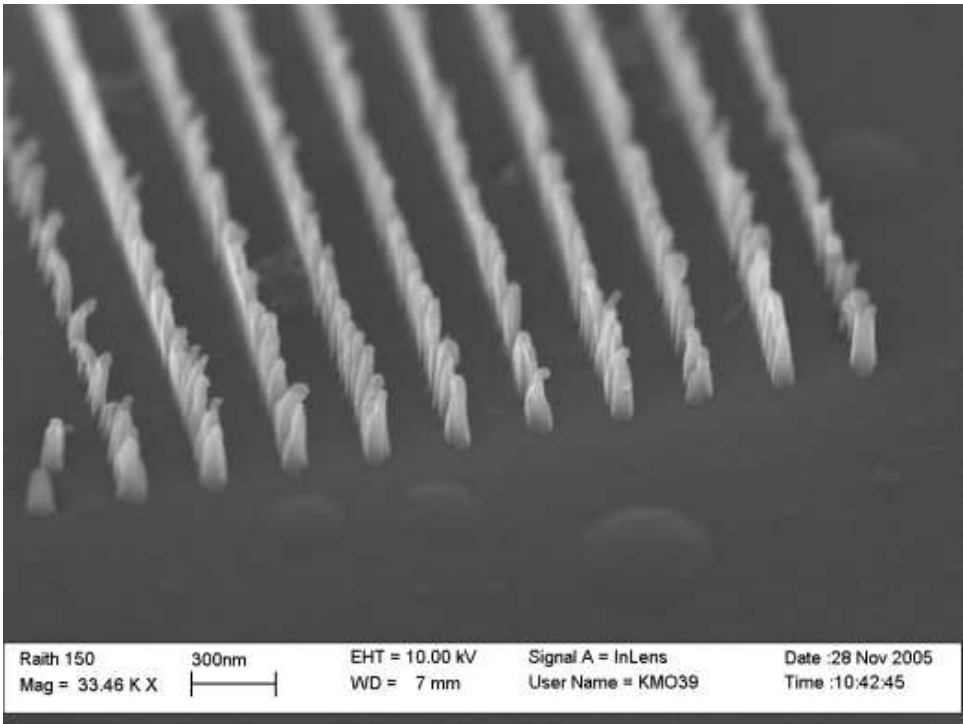


Figure 10. SEM images of the fabricated 2D nanostructure with feature sizes of 40 nm which failed to preserve the flat top profiles.

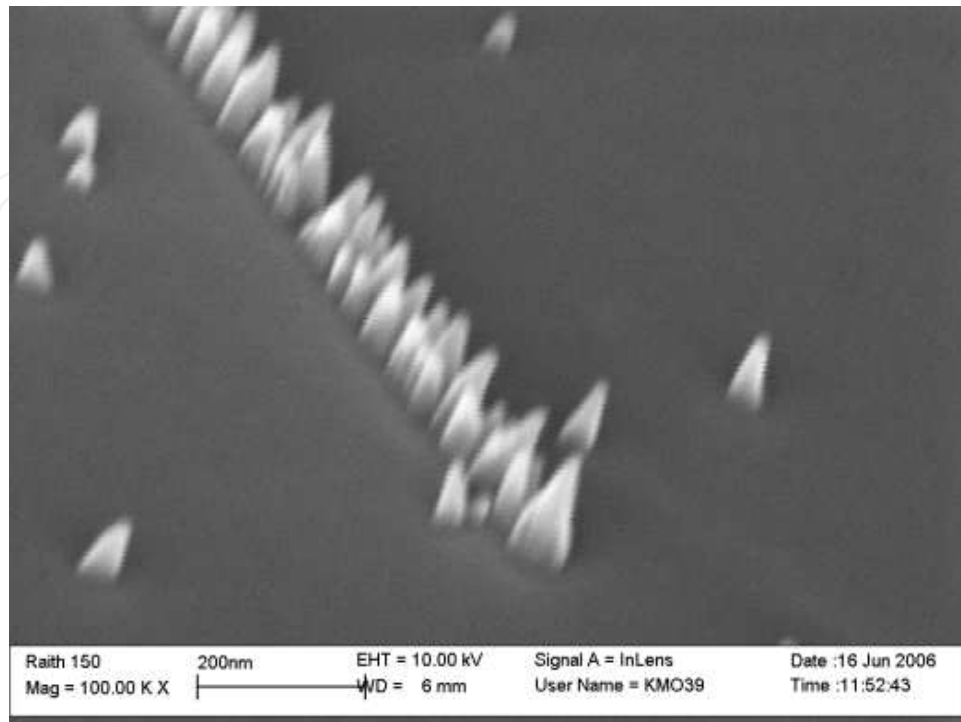


Figure 11. SEM images of the 20 nm lines structures which failed to preserve the flat top profiles after the etching process.

6. Conclusions

The fabrication of high aspect-ratio nanostructures on quartz substrates with feature sizes ranging from 60 nm to 100 nm has been demonstrated. The high aspect-ratio of up to 1:10 on 60 nm line nanostructures has been fabricated using the optimized CHF_3/Ar RIE plasma recipe. The fabrication of nanostructures with feature sizes below 60 nm was unsuccessful due to inadequate NiCr mask layer thickness. The five minutes cooling intervals on every 15 minutes of plasma etching process was found to achieve a 10 nm/min etch rate and steep vertical sidewalls profile.

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