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Chapter 9

Fundamental Aspects of Silicon Carbide Oxidation

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Additional information is available at the end of the chapter

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1. Introduction

Silicon carbide (SiC), which exhibits a wider band gap as well as a superior breakdown field and thermal conductivity over conventional Si, has gained considerable attention for future power electronics [1]. Among the various types of power devices, metal-oxide-semiconductor field-effect transistors (MOSFETs), which provide a normally-off characteristic, should become a key component for next-generation green electronics. As stated, with the exception of Si, SiC is the only compound semiconductor that yields SiO_2 insulators with thermal oxidation. This makes the device fabrication process easier compared with those for other wide band gap semiconductors. It is commonly believed that carbon impurities within the oxides diffuse out in the form of carbon oxides during high temperature oxidation, but a small amount of carbon impurities remains within the oxide and at the SiO_2/SiC interface. Consequently, the electrical degradation of SiC-MOS devices causing both deteriorated device performance and reliability is the most crucial obstacle to the implementation of SiC-based power electronics.

Unlike mature Si-MOS technology [2-5], a plausible oxidation model of a SiC surface and physical origin explaining electrical degradation of SiC-MOS devices have yet to be established. High-resolution transmission electron microscopy (TEM) observation reported several nm-thick transition layers with an extremely high excess carbon concentration around 20% beneath the SiO_2/SiC interface [6-8]. Although the non-stoichiometric bulk region seems to account for the mobility degradation of SiC-MOSFETs [8], a recent report based on an ion scattering technique pointed out a near-perfect stoichometric SiC region [9].

In addition, there still remain controversial issues of the energy band structure of SiO_2/SiC interfaces, despite the fact that a small conduction band offset significantly increases the gate leakage current, especially under a high electric field and high operation temperatures [10]. For example, while alternative channels, such as a 4H-SiC(000-1) C-face substrate, have

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proven to provide higher electron mobility than conventional devices on Si-face substrates [11], a further reduction in conduction band offset has been pointed out for the C-face channels [12]. However, details on the physical origins have not been clarified yet.

Furthermore, another important problem of SiC-MOS devices is poor gate oxide reliability, such as low dielectric breakdown field and threshold voltage instability. It has been reported that the location of dielectric breakdown is not correlated with any dislocations in SiC-MOS capacitors with gate oxides formed on 4º-off-angled 4H-SiC(0001) substrates by successive oxidation in N_2O and NO ambient [13]. Our conductive atomic force microscopy (AFM) study on a thermally grown SiO_2/4H-SiC(0001) structure has clearly demonstrated that dielectric breakdowns are preferentially induced at the step bunching [14]. It is generally accepted that the gate oxide breakdown is triggered when electrical defects generated in the oxide by a stress field are connected between the electrode and substrate (percolation model) [15]. Thus, we speculated that a local electric field concentration occurred around the step bunching, resulting in the preferential breakdown due to the acceleration of the defect generation. This suggests that oxidation behavior of step-bunched SiC surface induced by epitaxial growth and high-temperature activation annealing needs to be clarified from the macroscopic point of view, together with the atomic bonding features at SiO_2/SiC interface mentioned above.

This article provides an overview of our recent studies on the thermal oxidation of 4H-SiC substrates and the energy band structure of SiO_2/4H-SiC fabricated on (0001) Si-face and (000-1) C-face surfaces by means of high-resolution synchrotron x-ray photoelectron spectroscopy (XPS). We investigated the correlation between atomic structure and the electrical properties of corresponding SiC-MOS capacitors and discuss the intrinsic and extrinsic effects of the interface structure and the electrical defects on the band offset modulation. In addition, the surface and interface morphology of a thermally grown SiO_2/4H-SiC(0001) structure were systematically investigated using AFM and TEM to clarify the relation between step bunching and oxidation kinetics.

2. Initial oxidation of 4H-SiC(0001)

Synchrotron XPS analysis was performed using photon energy of 686.5 eV at BL23SU in the SPring-8 [16]. The starting substrate was as-grown 4º-off-angled 4H-SiC(0001) wafer with an n-type epitaxially grown layer. After RCA cleaning and subsequent native oxide removal with a diluted hydrofluoric acid (HF) solution, thermal oxidation was conducted in dry oxygen ambient using a conventional tube furnace at 1100ºC. To remove surface contamination due to air exposure, some of the samples were annealed in situ in an analysis chamber under an ultra-high vacuum condition.

Figure 1(a) represents changes in Si 2p core-level spectra as dry oxidation progresses on the 4H-SiC(0001) surface at 1100ºC [17]. Peak intensity was normalized with the bulk signal. Oxide growth on the SiC surfaces was confirmed with an increase in the chemical shift component in the Si 2p core-level spectra at around 104.5 eV. Capacitance-voltage (C-V)

measurement of the corresponding Al/SiO_2/SiC capacitors also revealed that oxidation for 10 and 30 min yielded roughly 3.5 and 5.7-nm-thick oxides, respectively. To investigate atomic bonding feature at SiO_2/SiC interfaces, Si 2p signals were analyzed by taking into account spin-orbit splitting. Figure 1(b) shows typical deconvoluted Si $2p_{3/2}$ and $2p_{1/2}$ peak components obtained with the manner adopted in the previous research on SiO_2/Si interfaces [3, 4]. Then, the Si $2p_{3/2}$ spectra taken from SiO_2/SiC were deconvoluted into five components originating from bulk SiC and SiO_2 portions together with intermediate oxide states (Si^{1+}, Si^{2+}, Si^{3+}). High-resolution XPS analysis allows us to detect small amount of intermediate states from an atomically abrupt oxide/substrate interface, and, in addition, these intermediate components can be a good indicator of structural imperfection at SiO_2/SiC interfaces. As shown in Fig. 1(c), we obtained a reasonable curve fitting with these components and confirmed that the total amount of the intermediate states is sufficiently small compared with that of thin thermal oxides. From these results, it is concluded that the physical thickness of the transition layer is as thin as a few atomic layers, which corresponding to areal density of Si-O bonds in the range of a few times 10^{15} cm^{-2}. This indicates formation of a near-perfect SiO_2/SiC interface and coincides well with a recent report based on high-resolution medium energy ion scattering [9].

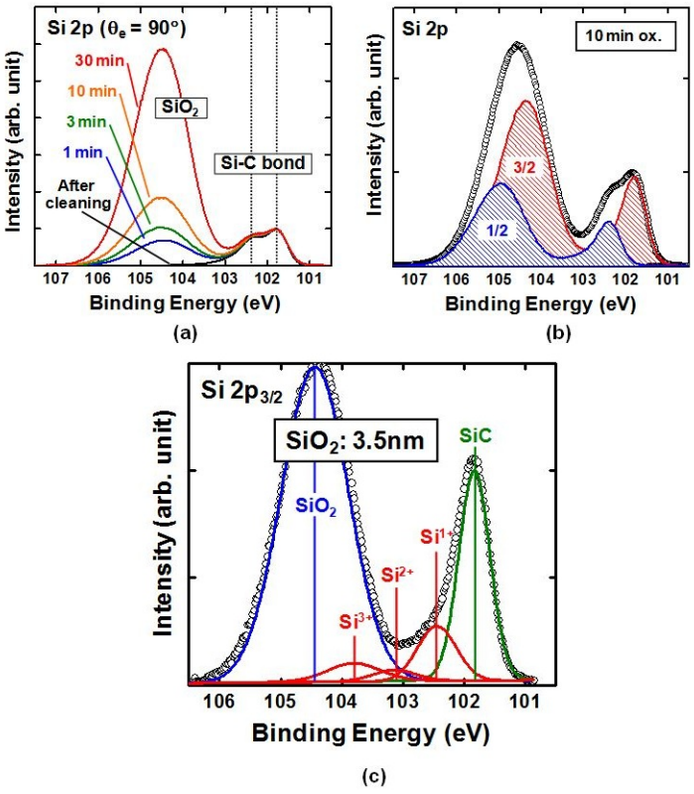


Figure 1. Synchrotron XPS spectra taken from the cleaned and oxidized 4H-SiC(0001) surfaces; (a) change in Si 2p core-level spectra as dry oxidation progresses, (b) peak deconvolution with $2p_{3/2}$ and $2p_{1/2}$ components, (c) result of curve fitting of Si $2p_{3/2}$ core-level with bulk SiC and SiO_2 signals and intermediate oxide states for the SiO_2/SiC sample prepared by 10-min oxidation.

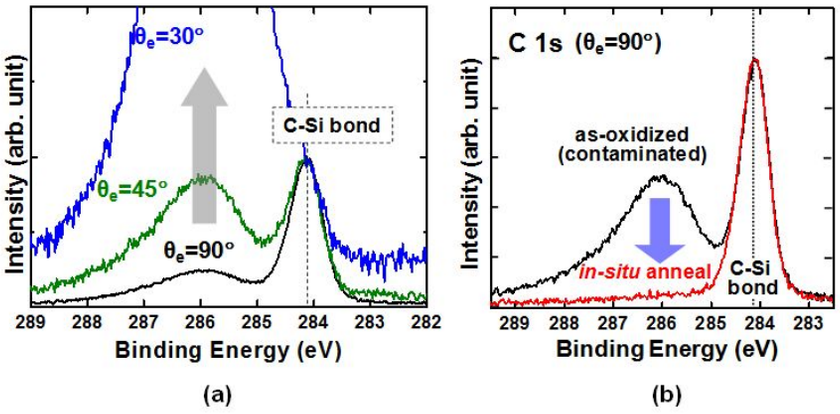


Figure 2. C 1s core-level spectra taken from the oxidized 4H-SiC(0001) surface using synchrotron radiation; (a) angle-resolved XPS analysis, (b) results of in situ vacuum annealing at 500ºC.

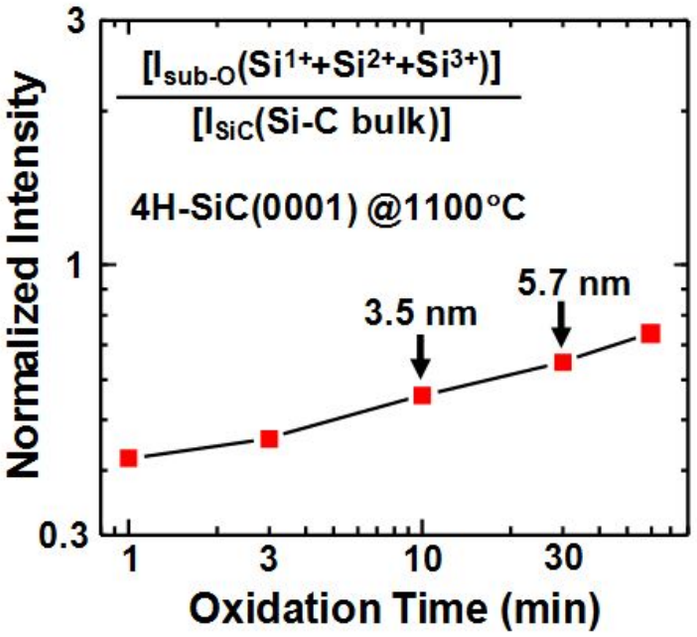


Figure 3. Change in the total amount of intermediate oxide states in Si $2p_{3/2}$ spectra, in which the intensity ratio between the intermediate state and the bulk signal was plotted as a function of oxidation time.

As previously reported, ideal hydrogen passivation of a SiC surface with a diluted HF solution was barely obtained, and the initial sample surface after wet cleaning was partially oxidized and contaminated with adsorbates [18]. This implies that a chemical shift component of C 1s core-level spectra involves unavoidable signals due to surface contamination. Thus, we performed angle-resolved XPS and in situ vacuum annealing prior to XPS analysis in the analysis chamber. Figure 2 represents C 1s core-level spectra taken from the oxidized 4H-SiC(0001) surface [17]. As shown in Fig. 2(a), the chemical shift component originating from carbon-oxides (CO_x) increased with respect to the bulk signal (C-Si bond) under the surface

sensitive conditions (at small take-off angle (θ_e)). In addition, it was found that the chemical shift component originating from carbon-oxides was totally removed by vacuum annealing at 500ºC (see Fig. 2(b)). Since stable chemical bonds existing at the SiO_2/SiC interface are hard to decompose under a moderate annealing temperature, we attributed the carbon-oxide signal to surface contamination. This clearly demonstrates that atomic bonding at the thermally grown SiO_2/SiC(0001) interface is dominated by Si-O bonds and that carbon impurity with its oxide form located near the interface is below the detection limit of XPS analysis (about sub-1 atomic percent in general).

Figure 3 shows the change in the total amount of intermediate oxide states in Si $2p_{3/2}$ spectra (Si^{1+}, Si^{2+}, Si^{3+}) [17]. Although a thick transition layer at SiO_2/SiC interface was ruled out, we observed a slight increase in the intermediate oxide states with an increase of the oxide thickness, unlike in the SiO_2/Si interface, which exhibits a perfect interface regardless of oxide thickness [4].

3. Interface structures beneath thick thermal oxides grown on 4H-SiC(0001) Si-face and (000-1) C-face substrates

Figures 4(a) and 4(b) represent typical deconvoluted Si $2p_{3/2}$ spectra obtained from the 40-nm-thick SiO_2/SiC(0001) Si-face and (000-1) C-face substrates, respectively, in which the thick thermal oxides were thinned using a diluted HF solution prior to synchrotron XPS analysis [19]. Similar to the thin thermal oxides (see Fig. 1), the Si $2p_{3/2}$ spectra were fitted well with five components originating from bulk SiC and SiO_2 portions together with intermediate oxide states. It's obvious that, for both cases, the total amount of the intermediate states was sufficiently small compared with that of the remaining oxides (about 3 nm thick). This implies that the physical thickness of the transition layer on the oxide side is as thin as a few atomic layers even for the thick thermal oxides. These experimental results clearly indicate formation of a near-perfect SiO_2/SiC interface with conventional dry oxidation regardless of the substrate orientation and oxide thickness.

Furthermore, for the thick thermal oxide on Si-face substrate, the composition of the bulk SiC region beneath the oxide was estimated from the intensity ratio ([Si 2p]/[C 1s]). We obtained an identical intensity ratio to that of the initial as-grown SiC surface [17]. These experimental results mean that, despite previous literature based on TEM observation [6-8], there exists no thick carbon-rich layer of a high atomic percentage at the SiO_2/SiC interface and that a near-perfect interface dominated by Si-O bonds is formed even for the thick thermal oxidation of the SiC(0001) surface.

Figure 5 compares the change in the total amount of intermediate oxide states in Si $2p_{3/2}$ spectra obtained from SiO_2/SiC interfaces. The intensity ratios between the intermediate states and the bulk signals for thin and thick thermal oxides grown on (0001) Si-face and (000-1) C-face substrates were plotted. Despite that the minimal intermediate oxide states again imply abrupt interface, we observed a slight increase in the intermediate states espe-

cially for thick thermal oxide interface on C-face substrates, which suggesting degradation of interface electrical properties of SiC-MOS devices formed on C-face substrates [20].

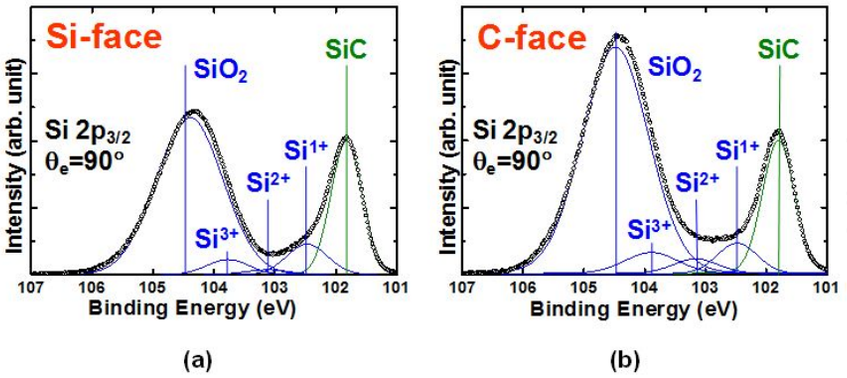


Figure 4. Si $2p_{3/2}$ core-level spectra obtained from the oxidized (a) 4H-SiC(0001) Si-face and (b) (000-1) C-face substrates. Before synchrotron XPS measurement, 40-nm-thick oxide layers were thinned using HF wet etching. The remaining oxide thickness was about 3 nm for both cases.

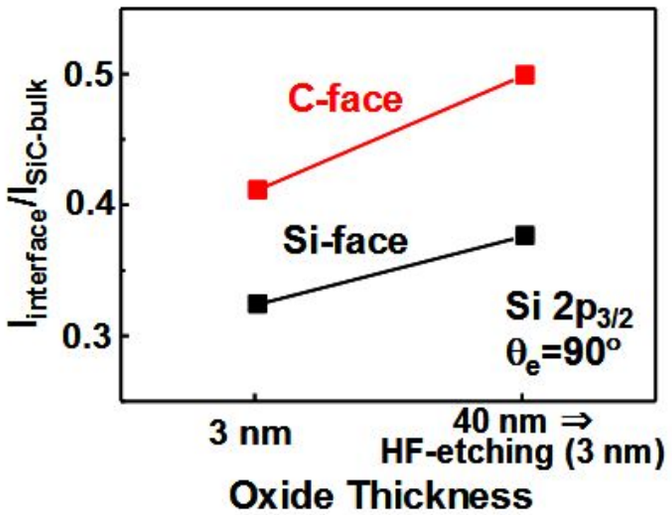


Figure 5. Change in the total amount of intermediate oxide states in Si $2p_{3/2}$ spectra taken from the oxide interfaces grown on SiC(0001) Si-face and C-face substrates.

4. Correlation between atomic structure and electrical properties of SiO_2/SiC interface

Corresponding SiC-MOS capacitors were fabricated with the top aluminum electrode evaporated through a shadow mask after post oxidation annealing at 900ºC in argon ambient. Electrical properties, such as the interface state density (D_{it}) and fixed oxide charge den-

sity (Q_{ox}) of the SiO_2/SiC interface, were extracted from the high-frequency C-V characteristics of SiC capacitors. The D_{it} value was extracted with the Terman method, and the Q_{ox} was deduced from the flatband voltage (V_{fb}) shift that depends on the oxide thickness [21]. Figure 6 summarizes the changes in D_{it} and V_{fb} values. Since post-treatment, such as nitrogen and hydrogen incorporation, was not conducted in this experiment, high D_{it} over 10^{12} $cm^{-2}eV^{-1}$ was extracted at an energy level of E_c - E = 0.36 eV. The high D_{it} value indicates degradation of the electrical properties of the SiO_2/SiC interface, especially for thick thermal oxides. In addition, the positive V_{fb} shift in the C-V curves implies the existence of a negative fixed charge within the gate oxides. Assuming that the fixed charge is located at the SiO_2/SiC interface, the Q_{ox} of the SiC-MOS devices estimated from the thickness-V_{fb} slope was 2.3 x 10^{11} cm^{-2} for oxides thinner than 20 nm and 1.2 x 10^{12} cm^{-2} for thick oxides, meaning that the fixed charges also accumulated at the interface probably due to the suppressed out-diffusion of carbon impurities as dry oxidation progressed.

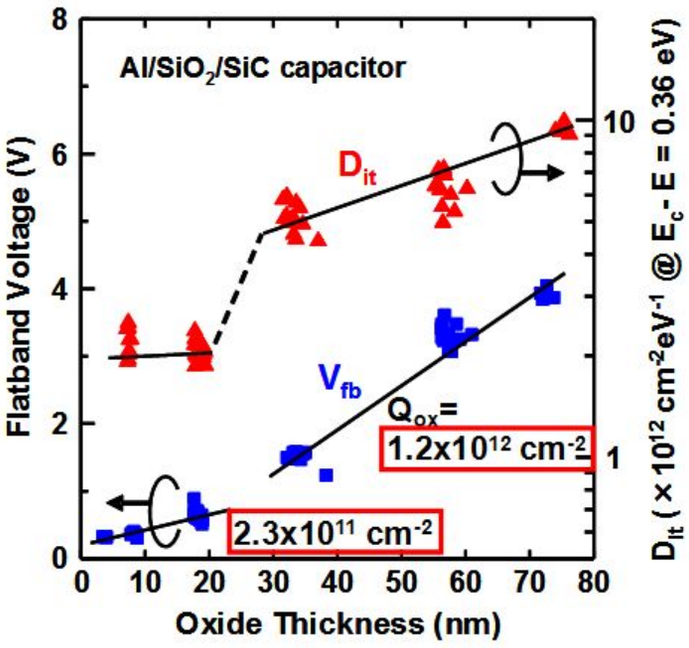


Figure 6. Summary of electrical properties of SiC-MOS capacitors fabricated by dry oxidation. Horizontal axis represents oxide thickness extracted from measured maximum capacitance. The D_{it} and Q_{ox} were estimated using Terman method and V_{fb} shift in C-V curves, respectively.

The correlation between electrical degradation and the atomic bonding feature of the SiO_2/SiC interfaces raises the intrinsic problem of SiC oxidation. This is consistent with the common understanding of SiC-MOS devices, whereas our synchrotron XPS analysis excludes the several-nm-thick transition layer having excess carbon as a physical origin of the electrical degradation. Instead, we think that the electrical defects at the interface, such as D_{it} and Q_{ox}, are partly ascribed to the atomic scale roughness and imperfection identified with the intermediate oxide states in the Si 2p spectra. Moreover, considering the significant mobility reduction in SiC-MOSFETs, we should take into account the various forms of carbon

interstitials forming local C-C dimers located on the SiC bulk side as a possible origin of the electrical defects [22]. Therefore, it is concluded that, for improving the performance of SiC-based MOS devices, we should focus our attention on the atomic bonding feature and carbon impurities within the channel region rather than the thick transition layer near the SiO_2/SiC interface.

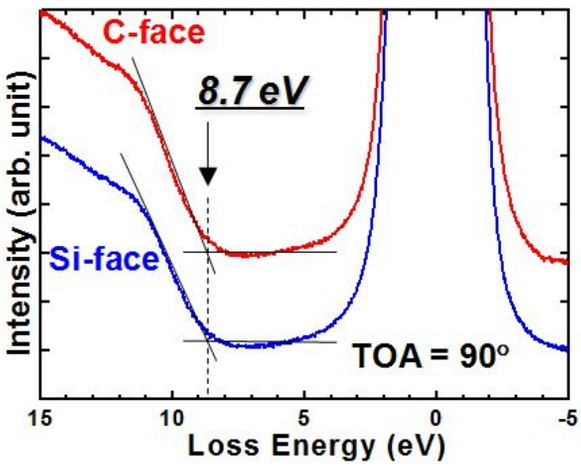


Figure 7. O 1s energy loss spectra for thermal oxides on (0001) Si-face and (000-1) C-face 4H-SiC substrates. The onset of the excitation from the valence to conduction bands (band gap) can be determined from the energy loss.The valence band maximum of SiC substrates and the oxides was determined by the valence spectra taken from SiO_2/SiC structures and a reference SiC surface [24]. Figure 8 represents measured and deconvoluted valence spectra obtained after 3-nm oxidation of the Si-face and C-face substrates, in which the valence band maximum of the thermal oxides was estimated by subtracting the reference SiC spectra (□) from the measured SiO_2/SiC spectra (□) both for the Si- and C-face substrates (see

5. Energy band structure of SiO_2/4H-SiC interfaces and its modulation induced by intrinsic and extrinsic interface charge transfer

The energy band structure and interface quality of SiO_2/4H-SiC fabricated on (0001) Si-face and (000-1) C-face substrates was also investigated by means of synchrotron XPS. Thermal oxidation was conducted using a conventional furnace at temperatures ranging from 1000 to 1100ºC. Thin and thick oxide layers of about 3 and 40 nm were prepared by choosing the oxidation temperature and time appropriately for Si-face and C-face substrates. For the thick oxide samples, the oxide layers were thinned to about 3 nm thick by a diluted HF solution. To determine band structures of SiO_2/SiC, we examined the band gap of the thermal oxides and valence band offset at the interface. The energy band gap of these oxides grown on Si-face and C-face substrates was first estimated from O 1s energy loss spectra. Because the photoelectrons generated in oxides suffer energy losses originating from plasmon and electron-hole excitations, the energy band gap can be determined by the threshold energy of an energy loss spectrum for an intense O 1s signal [23]. As shown in Fig. 7, O 1s energy loss spectra for thermal oxides on the Si-face and C-face substrates clearly indicate that the energy band gap of the oxides is identical

regardless of substrate orientation (8.7 eV) [24]. Considering the high oxidation temperatures over 1000˚C and low concentration of residual carbon impurities within thermally grown oxides on SiC [17], these results seem to be quite reasonable.

spectra ◎-◎). These results demonstrated that the valence band offset of the SiO_2/SiC for the C-face substrate was about 0.4 eV larger than that for the Si-face. In addition, we conducted similar synchrotron XPS analysis for thick oxide samples to examine the effects of interface defects on energy band modulation as the oxide thickness increased.

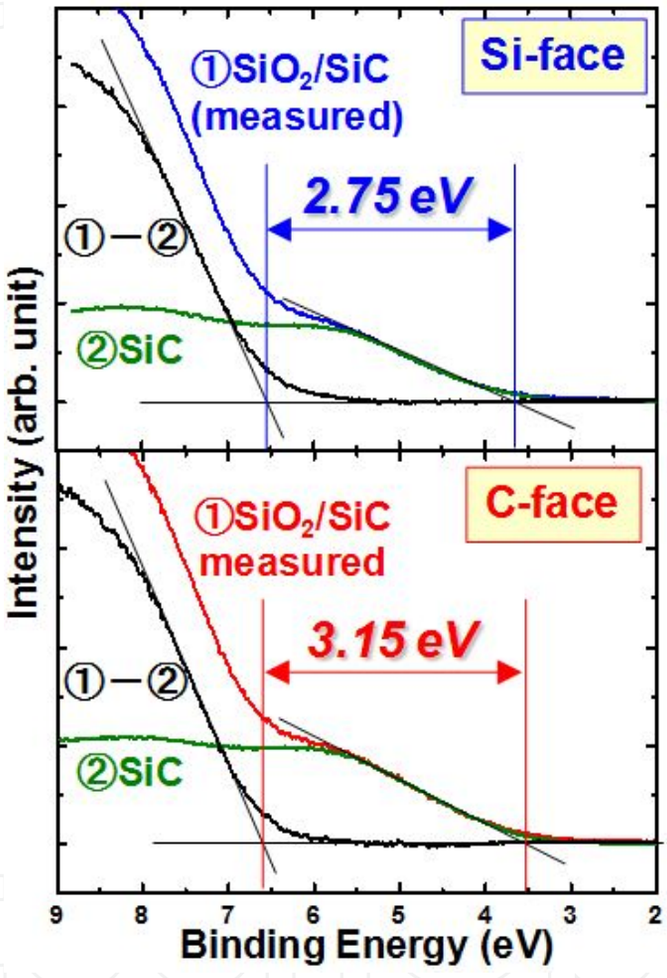


Figure 8. Measured and deconvoluted valence band spectra for SiO_2/SiC structures formed on (0001) Si-face and (000-1) C-face 4H-SiC substrates.

By taking these measured values and the reported energy band gap of 4H-SiC substrate (3.26 eV) into account, we obtained the energy band structures for SiO_2/SiC structures fabricated under various conditions and summarized them in Fig. 9 [24]. Note that the conduction band offset that determines gate leakage current and resultant gate oxide reliability of SiC-MOS devices crucially depends on the substrate orientation and oxide thickness. Since the thin oxide on the C-face substrates exhibits smaller conduction band offsets than those on the Si-face substrates, we conclude that the degraded reliability of SiC-MOS devices fab-

ricated on the C-face surface is an intrinsic problem, which is probably due to the difference in the electronegativity between Si and C atoms bonded with O atoms at the interface.

Furthermore, considering the accumulation of negative fixed charges at the SiO_2/SiC interface, the increase in the conduction band offset for thick oxides both on the Si-face and C-face substrates can be explained by an extrinsic energy band modulation due to the interface defects. This enlarged band offset for the thick MOS devices is preferable from the viewpoint of reducing gate leakage, but electrical defects should negatively impact on the device performance and reliability. Therefore, fundamental tactics, such as applying deposited gate oxides and band engineering by utilizing stacked structures, are indispensable to take advantage of C-face SiC-MOS devices [25-28].

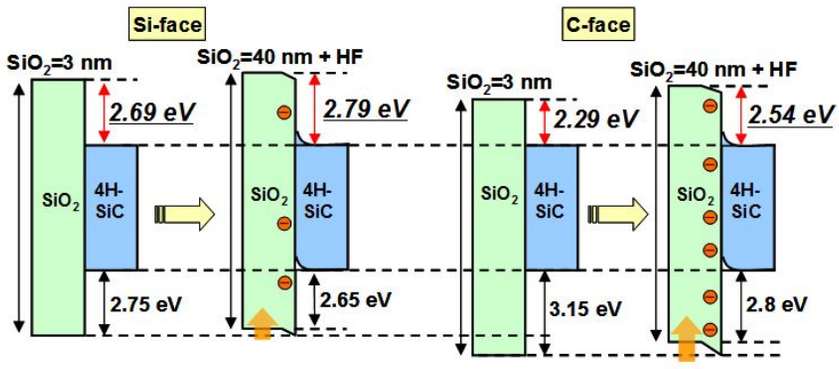


Figure 9. Energy band diagrams of SiO_2/4H-SiC(0001) structures obtained by synchrotron XPS analysis. The measured values of the valence band offsets for SiO_2/SiC interfaces formed under various conditions are indicated.

We also evaluated the modulation of energy band alignment of SiO_2/4H-SiC(0001) structures due to the interface defect passivation [29]. It was found that, although the hydrogen incorporation into the SiO_2/SiC interface is effective in improving the interface property, both XPS analysis and electrical measurements revealed that interface defect passivation induces a reduction of conduction band offset. This indicates that the larger conduction band offset at the as-oxidized SiO_2/SiC interface is attributed to the high density of interfacial carbon related defects.

6. Surface and interface morphology of thermally grown SiO_2 dielectrics on 4H-SiC(0001)

Finally, surface and interface morphology of thermal oxides grown on 4H-SiC(0001) substrates was investigated using AFM and TEM [30]. Thermal oxidation of 4º-off-angled 4H-SiC(0001) Si-face substrate with an n-type epilayer was carried out in dry O_2 ambient at 1100ºC for 12 hours. The root mean square (RMS) roughness of the as-grown surface was estimated to be 0.23 - 0.26 nm (see Fig. 10(a)), suggesting that it is an almost step-bunching-free substrate. However, in some locations, step bunching was observed, and the RMS

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roughness of the area, including step bunching, was about 2.3 nm. For some samples, high-temperature annealing was performed in an inert ambient at 1700ºC to intentionally emphasize the step bunching prior to the dry oxidation.

As shown in Fig. 10(b), the RMS roughness value of the oxide surface was about 0.36 nm, which is slightly higher than that of the as-grown epilayer surface. In addition, it seems that steps on the oxide surface are more rounded than the initial surface. Figure 11 shows cross-sectional TEM images of as-grown and oxidized samples. Single steps are observed at the SiO_2/4H-SiC interface in contrast to multiple-layer steps for the initial epilayer surface. These findings indicate that the step-terrace structure of an epilayer is enormously transferred to the SiO_2 surface, while the interface roughness decreases by smoothening step bunching. Since the oxidation rate for C-face 4H-SiC is much higher than that for Si-face, it is considered that the step edges will be rounded by enhanced oxidation and that the resulting oxide near the steps will be thicker due to a volume expansion from SiC to SiO_2.

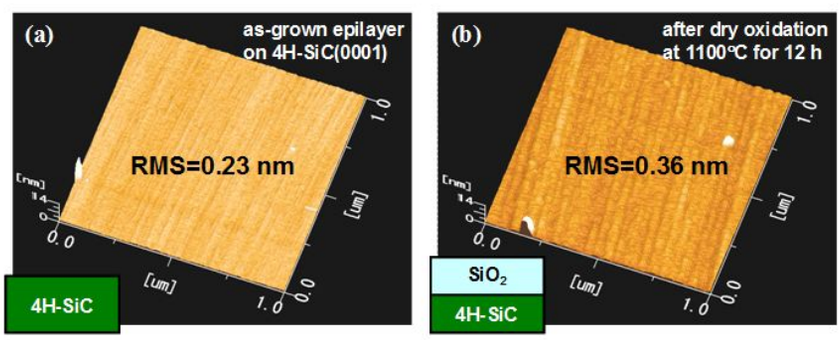


Figure 10. AFM images of (a) as-grown 4H-SiC(0001) epilayer surface and (b) SiO_2 surface formed on sample shown in (a) by dry O_2 oxidation at 1100ºC for 12 h.

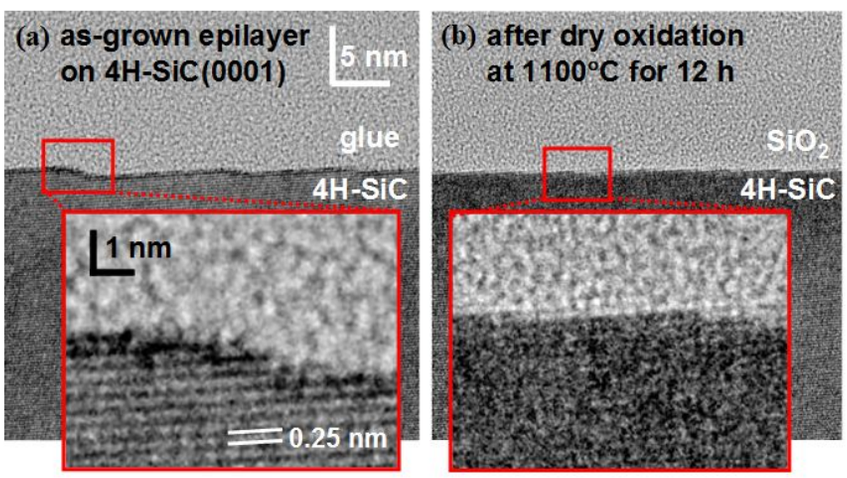


Figure 11. Cross-sectional TEM images of (a) as-grown 4H-SiC(0001) epilayer surface and (b) SiO_2/4H-SiC interface formed on sample shown in (a). The oxide thickness was about 35 nm.

To verify this hypothesis, a large step bunching was intentionally formed by high temperature annealing. As shown in Fig. 12(a), AFM observation of the 4H-SiC(0001) surface annealed at 1700ºC showed that the height of the step bunching ranged from 10 to 20 nm, while the RMS roughness within the terrace was 0.19 nm. After oxidation, a similar step-terrace structure to the one observed in Fig. 12(a) is preserved on the oxide surface, except for the bumps around the step bunching (see Fig. 12(b)). However, the RMS roughness in the flat region that was originally a terrace remains unchanged (<0.19 nm). This result strongly suggests significantly enhanced oxidation at the step face.

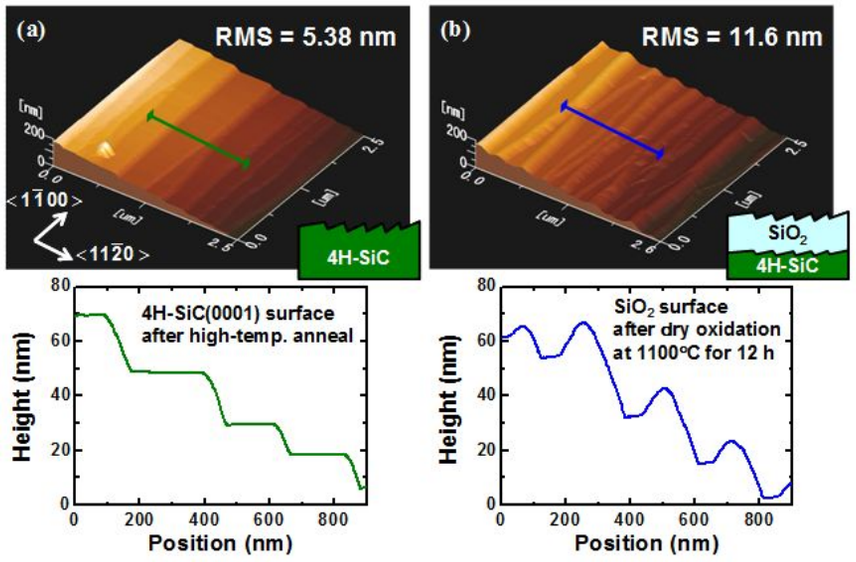


Figure 12. AFM images and cross-sectional profiles of (a) 4H-SiC(0001) surface after annealing at 1700ºC and (b) SiO_2 surface formed on the sample shown in (a) by dry oxidation at 1100ºC for 12 h.

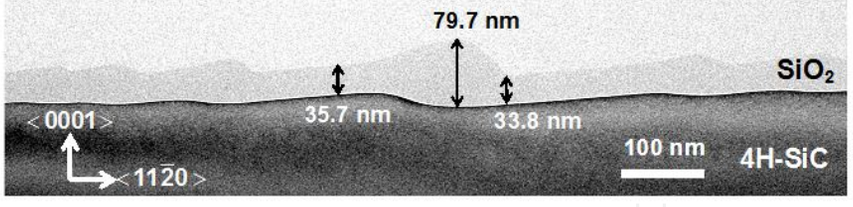


Figure 13. A cross-sectional TEM image of SiO_2/SiC structure shown in Fig. 12(b).

Furthermore, as shown in Fig. 13, a cross-sectional TEM image of the sample shown in Fig. 12(b) also clearly indicates pronounced oxidation at the step bunching. On the other hand, SiO_2/4H-SiC interface morphology is clearly more moderated than that of the SiO_2 surface, implying that the step bunching at the oxide interface became smooth by oxidation. The maximum SiO_2 thickness (~80 nm) was located facing the step, which is more than double that on the terrace. Since the oxidation reaction is controlled by the amount of oxygen molecules diffused through the SiO_2 layer, step edges will become rounded because of the thin-

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ner oxide on the terrace. The large oxide thickness fluctuation surely leads to the local electric field concentration around the step bunching during the electrical stressing, thus resulting in a preferential breakdown. Therefore, we can conclude that the surface morphology of the channel region before gate oxide formation is important for improving reliability of SiC-MOS devices.

7. Summary

We have investigated the fundamental aspects of SiC oxidation and SiO_2/SiC interfaces. Despite the literature based on TEM observation, we found that a near-perfect interface dominated by Si-O bonds is formed by dry oxidation of 4H-SiC(0001) substrates. However, atomic scale roughness and imperfection causing electrical degradation of SiC-MOS devices was found to be introduced as oxide thickness increases. We also pointed out the problems regarding oxide reliability originating from the gate leakage. It was found that, although negative fixed charges due to the interface defects enlarge the conduction band offset of SiC-MOS devices, small conduction band offset leading to increased gate leakage is an intrinsic feature, especially for the SiC(000-1) C-face substrates. We have also examined surface and interface morphology of thermally grown oxides to clarify the relation between step bunching and oxide breakdown. Multiple-layer steps as well as step bunching on the wafer surface lead to oxide thickness fluctuation due to the difference in oxidation rate between the terrace and the step face. The bump-like structure of the SiO_2 layer near the step bunching and the relatively thinner oxide on the terrace will cause a local electric field concentration, which enhances the generation of electrical defects in the oxide, indicating that an atomically-flat surface needs to be formed before gate oxide formation.

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