Chapter 10

Electrical Characterization of High-K Dielectric Gates for Microelectronic Devices

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Additional information is available at the end of the chapter

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1. Introduction

The continuous miniaturization of complementary metal-oxide-semiconductor (CMOS) technologies has led to unacceptable tunneling current leakage levels for conventional thermally grown SiO_2 gate dielectrics [1,2]. During the last years, many efforts have been devoted to investigate alternative high-permittivity (high-k) dielectrics that could replace SiO_2 and SiON as gate insulators in MOS transistors [3]. The higher dielectric constant provides higher gate capacitances with moderated thickness layers; however, other requirements such as lower leakage currents, high breakdown fields, prevention of dopant diffusion, and good thermodynamic stability must also be fulfilled. A number of high-k materials have been investigated as candidates to replace the SiO_2 as gate dielectric, being Al_2O_3 and HfO_2 among the most studied ones [3–5], since both have a larger permittivity than SiO2 and are thermodynamically stable in contact with silicon. The electrical characteristics of the as-deposited layers of these materials, however, exhibit large negative fixed charge and interface state densities and charge trapping as compared to SiO_2, although these characteristics can be improved by including an intermediate oxide between the high-k layer and the silicon substrate [6–8] or by high-temperature post-deposition processes.[9–13]. In addition to binary oxides, laminates of them show an improvement of the electrical characteristics as compared to the single oxide layers [14]. In particular, Al_2O_3–HfO_2 laminates and alloys benefit from the higher k of HfO_2 and the higher crystallization temperature of Al_2O_3 [15,16]

In this chapter we review the standard techniques as well as the new ones which we have developed for the electrical characterization of very thin insulating films of high k dielectrics for metal-insulator-semiconductor (MIS) gate and metal-insulator-metal (MIM) capacitor applications. These techniques have been conceived to provide detailed information of defects existing in the insulator bulk itself and interface traps appearing at the insulator-

semiconductor substrate interface. Several methods exist to obtain defect densities at insulator/semiconductor interface, such as deep level transient technique (DLTS), high and low (quasi static) frequency capacitance-voltage measurements and admittance spectroscopy.

However, the study of defects existing inside the gate dielectric bulk is not so widely established. Two techniques have been developed by us to accomplish it: conductance transient technique (GTT) and Flat-Band Voltage transients (FBT) measurements.

GTT is very useful when exploring disordered-induced gap states (DIGS) defects distributed inside the dielectric. This technique has been successfully applied to many high-k dielectric films on silicon. From conductance transient measurements we have obtained 3D profiles or contour maps showing the spatial and energetic distribution of electrically active defects inside the dielectric, preferentially located at regions close to the dielectric/semiconductor interface.

The FBT approach consists of a systematic study of flat-band voltage transients occurring in high-k dielectric-based metal-insulator-semiconductor (MIS) structures. While high-k material can help to solve gate leakage problems with leading-edge processes, there are still some remaining challenges. There are, indeed, several technical hurdles such as threshold voltage instability, carrier channel mobility degradation, and long-term device reliability. One important factor attributed to these issues is charge trapping in the pre-existing traps inside the high-k gate dielectrics. Dependencies of the flat-band voltage transients on the dielectric material, the bias history, and the hysteresis sign of the capacitance-voltage (C-V) curves are demonstrated. Flat bat voltage transients provide the soft optical phonon energy of dielectric thin-films. This energy usually requires chemical-physical techniques in bulk material. In contrast, FBT provides this magnitude for thin film materials and from electrical measurements, so adding an extra value to our experimental facilities.

Throughout the chapter we will give detailed information about the theoretical basis, experimental set-up and how to interpret the experimental results for all the above techniques.

Another topic widely covered will be the current mechanisms observed on high k materials. The above-mentioned methods allow determining the density and location of defects on the dielectric. These defects are usually responsible for the conduction mechanisms. The correlation between conduction mechanisms, defect location and preferential energy values provides very relevant information about the very nature of defects and how these defects can be removed or diminished.

We have studied many high-k materials during the last years, covering all proposed around the world as gate dielectric on silicon. These dielectrics consist of single layers of metal oxides and silicates (e.g.: HfO_2, ZrO_2, $HfSiO_x$, Gd_2O_3, Al_2O_3, TiO_2, and much more) directly deposited on n- and p- type silicon, combination of them in the form of multilayers, and gate stacks with silicon oxide or silicon nitride acting as interface layers which prevent from thermodynamic instabilities of directly deposited high-k films on silicon substrates. Figure 1

summarizes the atomic elements used as precursors of the high-k dielectrics we have studied in our laboratory. An extended summary of the more relevant results obtained will be also included in the chapter. Another topics covered in this chapter include: high-k fabrication methods: ALD, CVD, High Pressure Sputtering, etc., influence of the process parameters on the quality of as-grown and thermally annealed materials, or charge trapping at the inner interface layers on gate-stacks and multilayer films.

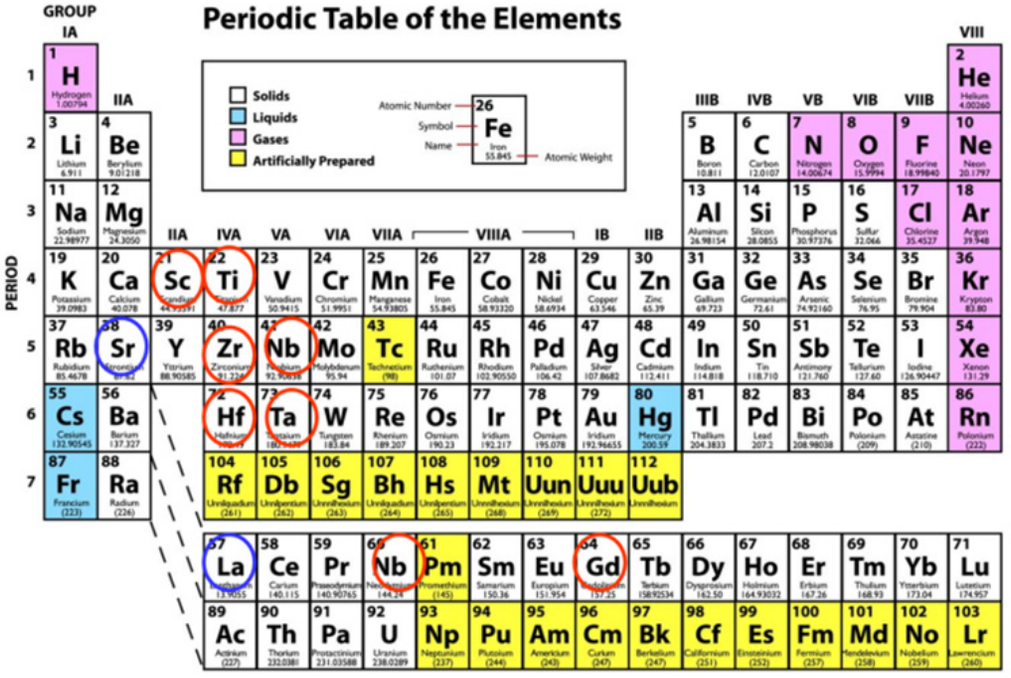

Figure 1. Periodic table with marks on the atomic elements from which high-k materials (mainly oxides and silicates) have been fabricated.

2. Standard characterization methods

2.1. Capacitance-Votage measurements

Capacitance-Voltage is the most frequently used electrical technique to assess the properties of both the thin oxide layer and its interface with the semiconductor substrate. In thicker oxide layers (more than 4-5 nm) C–V curves can be fitted satisfactorily with classical models, described in textbooks. The C–V technique can be used to determine flatband and threshold voltage, fixed charge, and interface state density. It is also often used to calculate the oxide thickness.

The ideal expression of a MIS structure in accumulation regime is: $C_{ac} = \frac{k\varepsilon_0 A}{t_{ox}}$. Non-ideal effects in MOS capacitors include fixed charge, mobile charge and surface states. Performing a capacitance-voltage measurement allows identifying all three types of charge. Charge existing in the dielectric film shifts the measured curve. Trapping and detrapping of defects

inside the insulator produce hysteresis in the high frequency capacitance curve when sweeping the gate voltage back and forth.

Finally, surface states at the semiconductor-insulator interface also modify the CV curves. As the applied voltage varies the Fermi level at the interface changes and affects the occupancy of the surface states. The interface states cause the transition in the capacitance measurement to be stretched out In Figure 2 we show experimental high frequency C-V results for hafnium oxide MIS structures measured at room temperature. Atomic Layer Deposition technique was used to grow these 20 nm-thick HfO_2 films

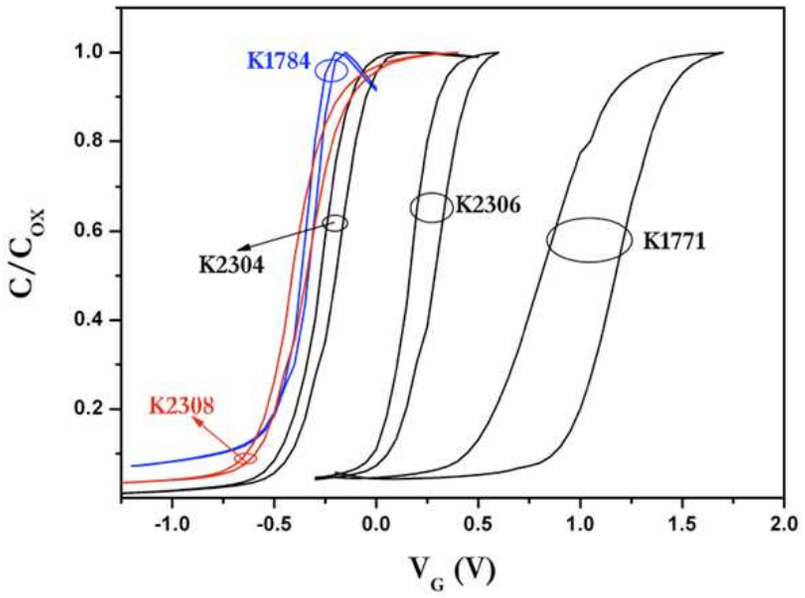

Figure 2. 1MHz C-V curves of Al/HfO_2/n-Si capacitors obtained by Atomic Layer Deposition

The combination of the low and high frequency capacitance (HLCV) [17] allows calculating the surface state density. This method provides the surface state density over a limited (but highly relevant) range of energies within the bandgap. Measurements on n-type and p-type capacitors at different temperatures provide the surface state density throughout the bandgap. A capacitance meter is usually employed to measure the high-frequency capacitance, C_{HF}. The quasi-static measurement of the low frequency capacitance, C_{LF}, consists on recording the gate current whereas a ramp-voltage is applied to the gate terminal. Interface state density is obtained according the following expression:

$$D_{it}=\frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox}-C_{LF}}-\frac{C_{HF}}{C_{ox}-C_{HF}}\right) \quad (1)$$

In sub-4 nm oxide layers, C–V measurements provide the same information, but the interpretation of the data requires considerable caution. The assumptions needed to construct the ‘‘classical model’’ are no longer valid, and quantum mechanical corrections become mandatory, thus increasing the complexity of the analytical treatment: Maxwell–Boltzman statistics no longer describe the charge density in the inversion and accumulation layers satisfactorily, and should be replaced by Fermi–Dirac statistics. In addition, band

bending in the inversion layer near the semiconductor–insulator interface becomes very strong, and a potential well is formed by the interface barrier and the electrostatic potential in the semiconductor. The correct analytical treatment requires solving the complex coupled effective mass Schroedinger and Poisson equations self-consistently.

2.2. Current measurements and conduction mechanisms

The performance of MOS devices strongly depends on the breakdown properties and the current transport behaviors of the gate dielectric films. The conduction mechanisms are very sensitive to the film composition, film processing, film thickness, and energy levels and densities of trap in the insulator films. Therefore, the analysis of the dominant conduction mechanisms may provide relevant information on the physical nature of the dielectric film and complements other characterization techniques when optimizing fabrication process. The most commonly found mechanisms as well as the voltage and temperature laws for each one are summarized in Figure 3.

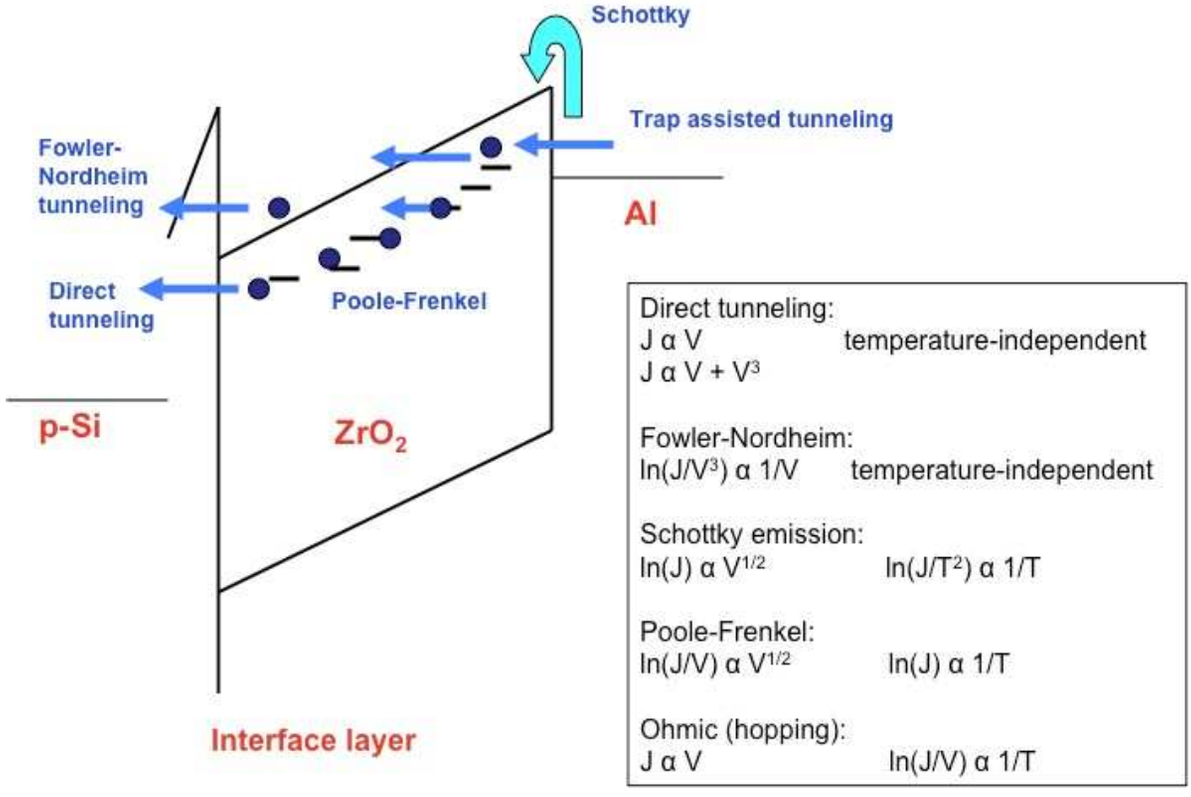

Figure 3. Main conduction mechanisms on Metal-Insulator- Semiconductor devices

- **Electrode-limited mechanisms**: When the dielectric has high bandgap, high energy barrier with electrodes and low trap density, conduction is more electrode-limited than bulk limited. For a large applied bias, the silicon surface is n-type degenerated regardless of the bulk doping. Hence, for a large applied voltage the current is limited by tunneling (independent of the temperature) from the vicinity of the silicon conduction band edge through the triangular barrier into the oxide conduction band

(*Fowler-Nordheim effect*). When barriers are no so high, conduction may occur when electrons or holes are promoted from the corresponding band to the insulator bands (*Schottky effect*). That occurs at lower voltages than Fowler-Nordheim mechanisms.

- **Bulk limited mechanisms:** As the insulators become more defective, as is the case of practically all high-k dielectrics, bulk-limited conduction predominates due to traps inside the insulator. Sometimes current density is due to field enhanced thermal excitation of trapped electrons into the conduction band. This process is known as the *Internal Schottky or Poole Frenkel effect*. The *hopping* of thermally excited between isolated states gives an ohmic I–V characteristic, exponentially dependent on temperature.
- **Tunnel limited mechanisms**: As dielectric films become thinner, tunneling conduction gradually dominates the conduction mechanisms. It may occur via defects in a two-step (or trap-assisted) tunneling or by direct tunneling from one electrode to the other.

In Figure 4 we draw the I-V characteristics at different temperatures of an Al_2O_3–based MIS sample fabricated by Atomic Layer Deposition. Leakage current clearly increases with temperature at lower gate voltages. I-V curves of all the samples were fitted according to the Poole-Frenkel emission, so indicating that the main conduction mechanism is bulk related.

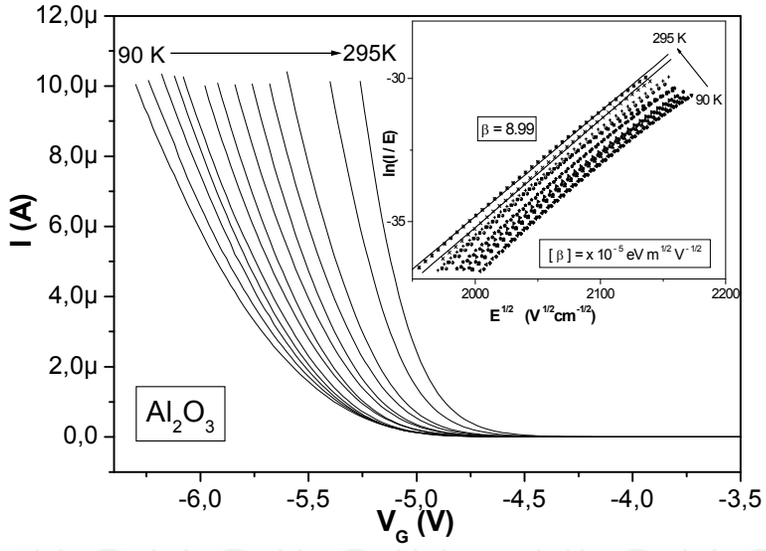

Figure 4. I-V curves at several temperatures and Poole-Frenkel fitting of an ALD Al_2O_3–based MIS sample

2.3. Admittance spectroscopy

The admittance spectroscopy or conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [18]. Interface trap densities of 10^9 cm^{-2} eV^{-1} and lower can be measured. It is also the most complete method, because it yields *Dit* in the depletion and weak inversion portion of the bandgap, the capture cross-sections for majority carriers, and information about surface potential fluctuations. The technique is based on measuring the equivalent parallel conductance of an MIS capacitor as a function of bias voltage and frequency. The conductance, representing

the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density. Interface traps at the insulator-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G}{\omega}=\frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2}$$

where $\tau_{it}=\left[v_{th}\sigma_p N_A\ exp\left(-\frac{q\Phi_S}{kT}\right)\right]^{-1}$ is the emission time constant of interface traps with energy Φ_S.

The conductance is measured as a function of frequency and plotted as G/ω versus ω. G/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G/q\omega$. For equation (2) we find $\omega \approx 2/\tau_{it}$ and $Dit = 2.5\ G/q\omega$ at the maximum.

It is also possible to make measurements by varying the temperature and keeping the frequency constant [19], instead of changing the frequency at constant temperature. This has the advantage of not requiring measurements over a wide frequency range and one can chose a frequency for which series resistance is negligible. Elevated temperature measurements enhance the sensitivity near mid-gap allowing the detection of trap energy levels and capture cross sections [20]. It also is possible to use transistors instead of capacitors and measure the transconductance instead of the conductance but still use the concepts of the conductance method [21]. This allows interface trap density determination on devices with the small gate areas associated with transistors without the need for capacitance test structures.

2.4. Other thecniques

In this section we include several electrical characterization techniques that are useful for probing microscopic bonding structures, defects, and impurities in high-k dielectrics, as described in [22].

2.4.1. Inelastic electron tunneling spectroscopy (IETS)

IETS is a novel technique that can probe phonons, traps, microscopic bonding structures, and impurities in high-k gate dielectrics with a superior versatility and sensitivity when compared with other techniques. This technique basically takes the second derivative of the tunneling I–V characteristic of an ultrathin MOS structure. The basic principle of the IETS technique is illustrated in Figure 5. Without any inelastic interaction, the I–V characteristic is smooth and its second derivative is zero. When the applied voltage causes the Fermi-level separation to be equal to the characteristic interaction energy of an inelastic energy loss event for the tunneling electron, then an additional conduction channel (due to inelastic tunneling) is established, causing the slop of the I–V characteristic to increase at that voltage, and a peak in its second derivative plot, where the voltage location of the peak corresponds

to the characteristic energy of the inelastic interaction, and the area under the peak is proportional to the strength of the interaction.

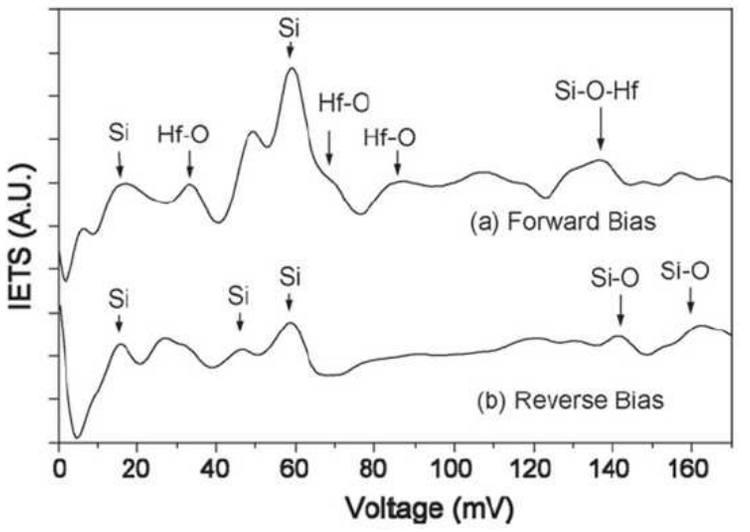

Figure 5. Principles of IETS technique [22].

In a typical MOS sample, there are more than one inelastic mode, as a wide variety of inelastic interactions may take place, including interactions with phonons, various bonding vibrations, bonding defects, and impurities. Figure 6 shows an actual IETS spectrum taken on an Al/HfO2/Si sample, where the features below 80 meV correspond to Si phonons and Hf–O phonons, and the features above 120 meV correspond to Hf–Si–O and Si–O phonons. The significance of this IETS spectrum is that it confirms the strong electron–phonon interactions involving optical phonons in HfO_2, and that the Hf–O phonons have very similar energy range as Si phonons which we know are a source of scattering centers that degrade the channel mobility.

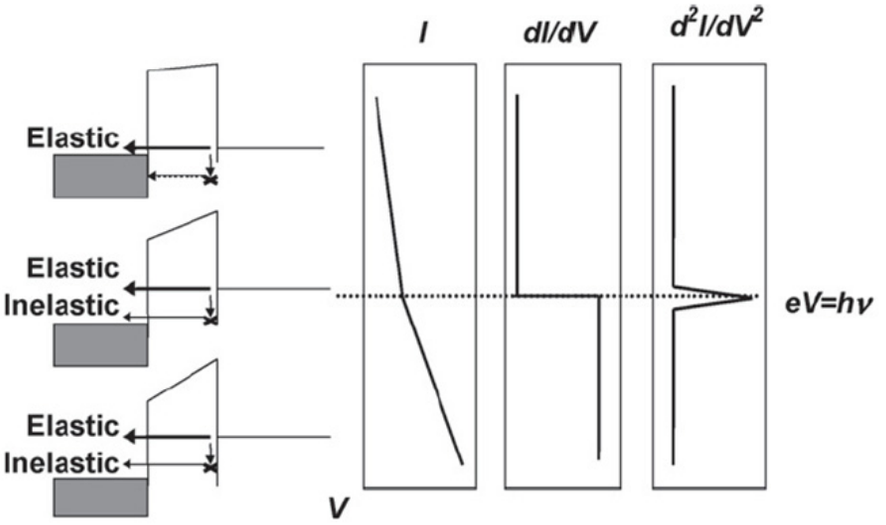

Figure 6. IETS for HfO2 on Si under different bias polarities: (a) forward bias (gate electrode positive), (b) reverse bias (gate electrode negative) [22].

2.5. Lateral profiling of threshold voltages, interface traps, and oxide trapped charge

Lateral profiling is a charge-pumping technique that enables one to profile the lateral distribution of threshold voltages of a MOSFET, and the lateral distributions of interface traps and oxide trapped charge generated by hot-carrier damage [23-24]. Figure 7(a) shows the I_{cp}–V_h curves for the source (curve 1) and the drain junction (curve 2) prior to hot-carrier damage, from which one can obtain the threshold voltage distributions near the two junctions (Figure 7(b)) using the V_h-$V_t(x)$ relationship as described in [25, 26]. Then a channel hot-carrier (CHC) stressing for 300 s to damage the device is used. Comparing curves 2 and 1 in Figure 8(a), one can see that the CHC stressing is not only generated N_{it} but also caused by positive charge inside the insulator gate, Q_{ot}. Therefore, one must neutralize this Q_{ot} before proceeding, and this was accomplished by a light hot electron injection as shown by curve 3 in Fig. 8. Note that this step did not cause any increase in N_{it} as evidenced by the unchanged $I_{cp,max}$.

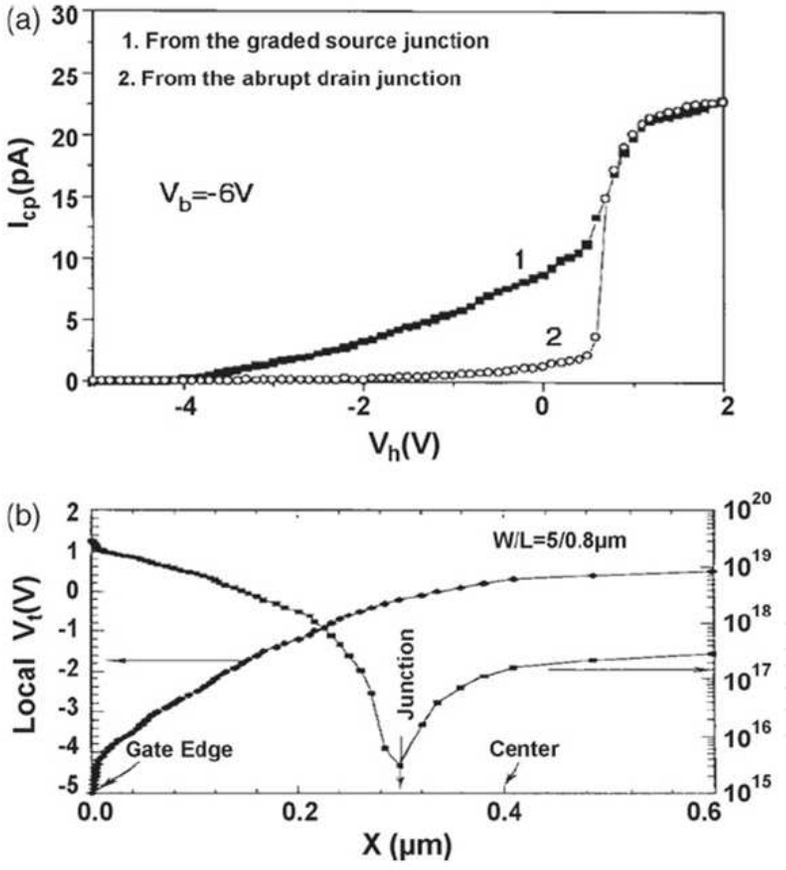

Figure 7. (a) Single-junction charge pumping curves measured either with the source floating (curve 1) or with the drain floating (curve 2). (b) Local Vt distribution across the channel as deduced from the data in (a).(From Reference [22])

These three I_{cp} curves were then used to extract the $N_{it}(x)$ from the difference between curves 3 and 1 at a given V_h, and $Q_{ot}(x)$, from the voltage shift between 2 and 3 at a given I_{cp} (Figure 8(b)).

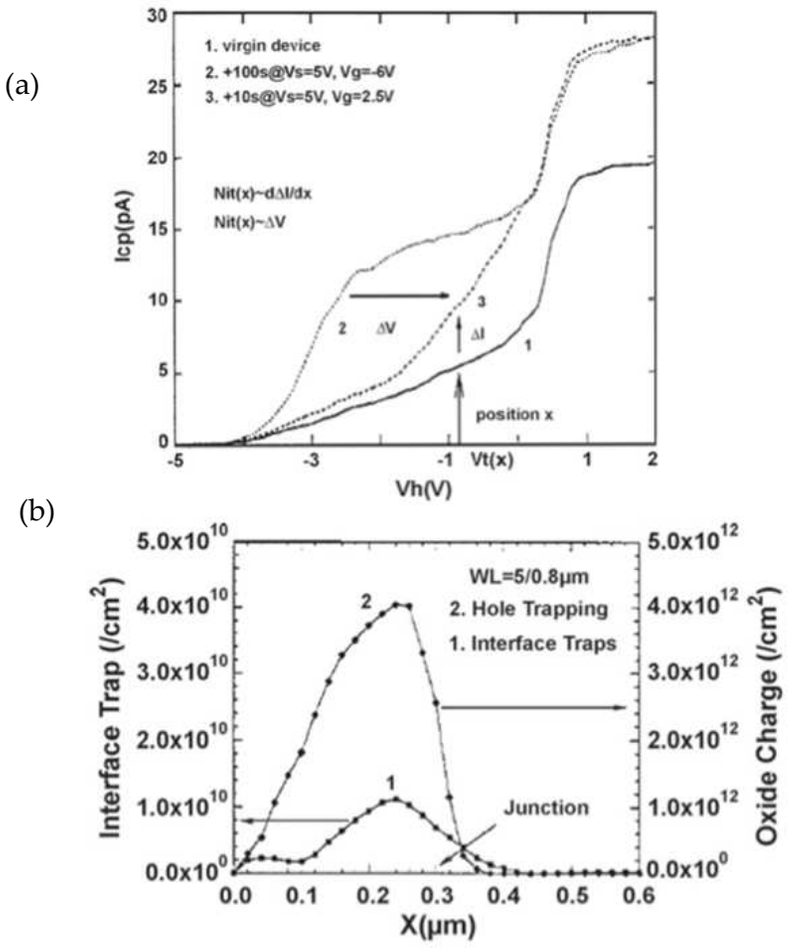

Figure 8. (a) Three charge pumping curves measured for the purpose of directly profiling the erase-induced damage, and graphically illustrating the direct lateral profiling principle. (b) Lateral profiles of both positive oxide charge and interface traps near the source junction, transformed from the three charge pumping curves in (a).(From Reference [22]).

2.6. Pulse agitated substrate hot electron injection (PASHEI) technique for studying trapping parameters

PASHEI technique [27, 28] can be used to study charge trapping in the gate dielectric of an MOSFET under low gate biases. The commonly used carrier injection techniques, such as Fowler–Nordheim (FN) tunneling, and CHC techniques require high gate field to obtain high injection flux, which makes it impractical to study trapping effects under low gate fields when the injection flux is extremely low. Another technique, the substrate hot-electron injection (SHEI) technique, does allow high flux injection at low gate fields, but it requires a separate p–n junction injector in the vicinity of the MOSFET being tested, which rules out most of the devices available for test. In contrast, the PASHEI technique, which will be described below, allows substrate hot-electron injection with just an ordinary MOSFET without a separate injector. The PASHEI technique relies on properly timed pulse sequences to achieve SHEI, as illustrated schematically in Figure 9 for an n-MOSFET. As shown in Figure 9(b), during the electron-emitting phase, the S/D junction is forward biased, and

electrons are injected into the substrate. Subsequently, the S/D is reverse biased to create a deep depletion region, which will cause the previously injected electrons in the substrate (those that have not recombined away) to be accelerated across the depletion region and injected into the gate dielectric. This period is called the collecting phase, during which the emitting voltage can control the gate voltage, and large injection current can be achieved with low V_g. Figure 10 illustrates the use of the ΔV_{th} vs. N_{inj} curve, obtained by the PASHEI technique, to extract trap parameters. For this particular sample, we obtained a trap density of 2.7 $x10^{12}$ cm^{-2}, and capture cross-section of 7.7 10^{-19} cm^2, by fitting the trapping theory presented by Zafar [29].

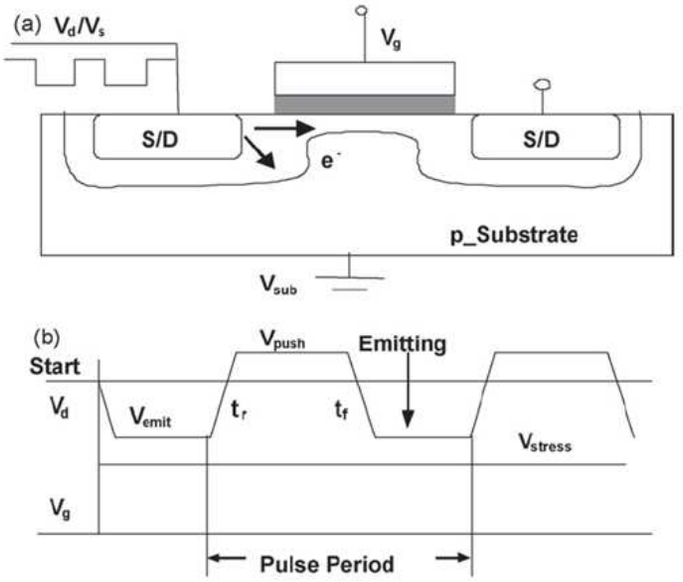

Figure 9. (a) Schematic description of PASHEI. (b) Pulse sequence for PASHEI. (From Reference [22])

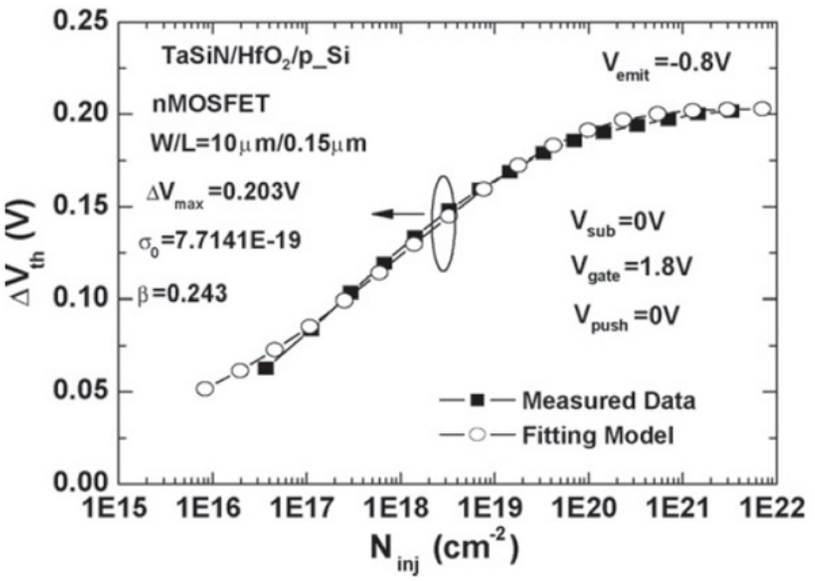

Figure 10. ΔV_{th} vs. N_{inj} curve obtained by the PASHEI technique, to extract trap parameters. (From Reference [22])

3. Advanced techniques

In this section we show three techniques set up in our laboratory: Single shot DLTS , which provides interface state densities), Conductance transient technique used to profile disorder induced gap states in the insulator zones close to the interface, and Flat-band voltage transient technique from which slow traps distribution inside the insulator is obtained.

3.1. Single shot deep-level transient spectroscopy

Deep-level transient spectroscopy (DLTS) has been widely used to characterize localized deep levels in semiconductor junctions. This technique is also useful to measure interface traps in the insulator-semiconductor interface. The instrumentation for interface trapped charge DLTS is identical to that for bulk deep level DLTS. However, the data interpretation is different because interface traps are continuously distributed in energy through the band gap, whereas bulk traps have discrete energy levels.

Single-shot DLTS measurements consist on recording and processing 1-MHz isothermal capacitance transients at temperatures from 77 K to room temperature. A programmable source is used together with a pulse generator to introduce the quiescent bias and the filling pulse, respectively. D_{it} is obtained by first applying a pulse which drives the MIS capacitor to accumulation, in order to fill the interface traps. Afterwards, the bias quickly returns to the limit between depletion and weak inversion, then traps formerly filled are emptied yielding the capacitance transients which are recorded for the DLTS processing. The isothermal capacitance transients are captured by a 1 MHz capacitance meter and a digital oscilloscope. The digital oscilloscope allows us to record the entire capacitance transient and, in this way, we can process the entire energy spectrum with only one temperature scan.

Once the capacitance transients have been captured, we process them as follows: we chose two times t_1 and t_2 (the window rate). The difference in the capacitance value at these times is the DLTS correlation signal which is given by [30, 31]:

$$\Delta C = - \frac{C(t_1)^3}{\varepsilon_S N_D} \frac{1}{C_{ox}} \int_{E_F^{t1}}^{E_F^{t2}} \left[\exp\left(-e_n t_1\right) - \exp\left(-e_n t_2\right) \right] D_{it} \tag{3}$$

The emission rate, e_n, depends on temperature and on energy, E_T, according the well-known Arrhenius law:

$$e_n = \sigma_n v_n N_c \exp\left[\frac{E_T - E_C}{kT}\right] \tag{4}$$

Where σ_n is the capture cross section, v_n is the electron thermal velocity and N_C is the efective state density at the silicon conduction band. According equation (3), all the interface states contribute to the correlation function, but only those with emission rates in the range of the window rate have non negligible contribution. Indeed, the correlation function has a maximum for:

$$e_n^{\max} = \frac{\ln\left(\frac{t_2}{t_1}\right)}{t_2 - t_1} \tag{5}$$

If we assume that capture cross section has not strong variations with energy, we can find the energy of interface traps which have the maximum contribution to the correlation function:

$$E_T^{\max} = E_C - kT\ln\left[\frac{\sigma_n v_n N_C (t_2 - t_{1)}}{\ln\left(\frac{t_2}{t_1}\right)}\right] \tag{6}$$

$\Delta C(E_T)$ has a maximum at the energy given by equation (6) and decays very sharply when energy varies from the maximum. Only interface traps with energies close to the maximum contribute to the DLTS signal, and a more simple form equation (3) can be obtained:

$$\Delta C = -\frac{C(t_1)^3}{\varepsilon_S N_D}\frac{kT}{C_{OX}} D_{it}\left(E_T^{\max}\right)\ln\left(\frac{t_2}{t_1}\right) \tag{7}$$

And the interface state density at the energy of the maximum:

$$D_{it}\left(E_T^{\max}\right) = -\frac{\varepsilon_S N_D}{kT\ln\left(t_2 / t_1\right)}\frac{C_{OX}}{C(t_1)^3}\Delta C \tag{8}$$

Equation (6) indicates that for a given window rate the energy is proportional to temperature. Therefore, low temperature transients provide D_{it} for states close to the majority carriers semiconductor band (conduction band for n-type or valence band for p-type). As temperature increases deeper states densities are obtained. Equation (8) says that D_{it} is proporcional to $\Delta C/T$, that is, the sensitivity is lower for deeper states. Since SS-DLTS is a differential technique, its sensitivity is much higher than Capacitance-Voltage or Conductance-Voltage Techniques. Typical sensitivities are in the range of 10^9 eV^{-1} cm^{-2}, which are lower than the state-of-the-art of thermal silicon oxide with silicon interface. Figure 11 is an example of SS-DLTS applied to the case of a hafnium silicate/silicon oxide on n-type silicon. The silicate was deposited by atomic layer deposition. In this case, we studied the effect of post deposition thermal annealing on the quality of the interface.

3.2. Conductance transient technique

All gate dielectrics exhibit conductance transients in MIS structures when are driven from deep to weak inversion [32]. This behavior is explained in terms of disorder-induced gap states (DIGS) continuum model suggested by Hasegawa et al.[33]. These authors proposed that lattice breaking at semiconductor/insulator interface causes defects with a continuous

distribution both in energy and in space. Conductance transient phenomena are due to charge and discharge of DIGS states assisted by majority carriers coming from the corresponding semiconductor band by means of a tunneling assisted mechanism. Transients can be understood looking at Figure 12 which is referred to a MIS structure over an n-type semiconductor substrate. When the bias pulse is applied, empty DIGS trap electrons coming from the conduction band (n-MIS structure). E_F and E' are the locations of the Fermi level before and after the pulse. Capture process is assisted by tunneling and is, thus, time consuming, so empty states near the interface capture electrons before the states deep in the dielectric. x_C is the distance covered by the front of tunneling electrons during the time t . It is important to note here that only those states with emission and capture rates of the same order of magnitude than the frequency have non-zero contributions to the conductance [34]. If an experimental frequency ω_b is assumed, only those states with emission rates in the range $\omega_b \pm \Delta\omega$ can contribute to the conductance (those located over equiemission line $e_n = \omega_b$), so only when the front of tunneling electrons reaches point A conductance increases. Then, when point B is reached, conductance transient follows the DIGS states distribution which is typically decreasing as we move away from interface, in agreement with Hasegawa's model [33]. Finally, conductance returns to its initial value when the front reaches point C, since after this point DIGS states susceptible to contribute to the conductance signal have energies strongly apart of the Fermi level and, then, they remain empty. Figure 12 is a schematic of the conductance transient principle.

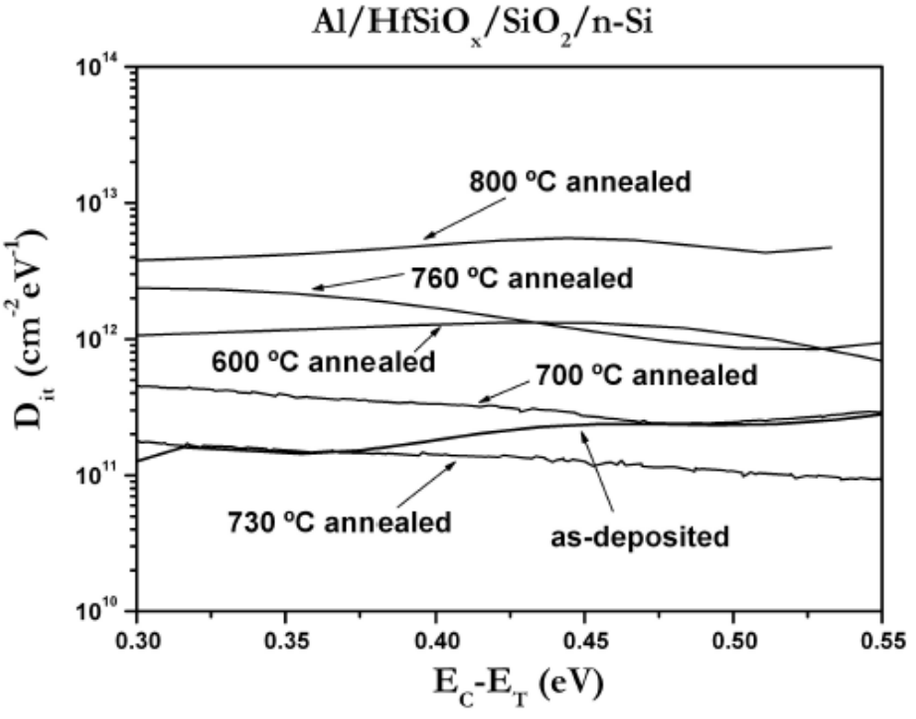

Figure 11. Interface state profiles for *Al/HfSi$_x$O$_y$/SiO$_2$/n-Si* capacitors.

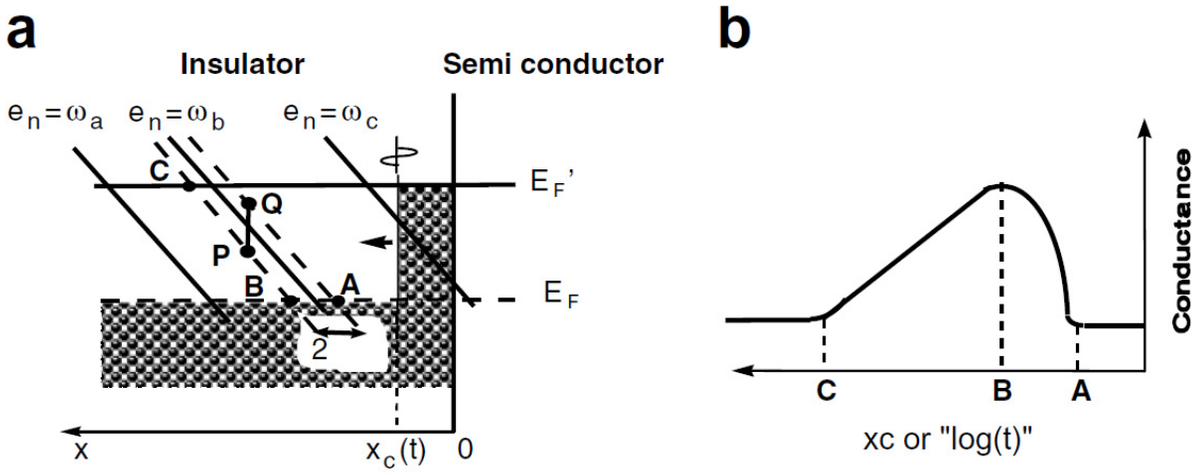

Figure 12. (a) Schematic band diagram of an I–S interface illustrating the capture electrons by DIGS continuum states during a conductance transient. (b) General shape of the conductance transient.

In the following, we show the model developed by us [35] to obtain DIGS states as a function of the spatial distance to the interface and the energy position by measuring conductance transients at different frequencies and temperatures. The calculation details presented here are for the case of an n-MIS structure. Similar equations can be derived for p-MIS devices. Our model departs from the conductance method typically used to obtain the interface state density, D_{it} , in MIS devices. For an angular frequency, ω, D_{it} is related to conductance by $D_{it}=\frac{G_{SS}}{0.4qA\omega}$ [36] where G_{SS} is the stationary value of the conductance. Variations of this value are due to the DIGS contribution to the conductance:

$$N_{DIGS}(E(t),x_C(t))=\frac{\Delta G_{SS}(t)}{0.4qA\omega} \tag{9}$$

where $E(t)$ is the energy of the DIGS states which a given time t during the transient contribute to the conductance variation. $x_C(t)$ is the distance covered by the front of tunneling electrons during the time t, *and* is given by $x_c(t)=x_{on}\ln(\sigma_o v_{th} n_s t)$, where $x_{on}=\frac{h}{2\sqrt{2m_{eff}H_{eff}}}$ is the tunneling decay length, σ_0 is the carrier capture cross-section value for x = 0, v_{th} is the carrier thermal velocity in the semiconductor, and n_s is the free carrier density at the interface. Finally, m_{eff} is the electron effective mass at the dielectric and H_{eff} is the insulator semiconductor energy barrier for majority carriers, that is, the dielectric to semiconductor conduction band offset. Figure 13 shows x_{on} for some high-k dielectrics (electron effective mass and barrier height values have been obtained from References [3] and [37] respectively). One can see that x_{on} is higher for dielectrics in which H_{eff} and m_{eff} are low. In these cases, the tunneling front x_C is faster and, consequently, transients reach deeper locations in the dielectric. An important trend can be derived from this figure: as permittivity increases, tunneling decay length increases providing deeper DIGS profiles.

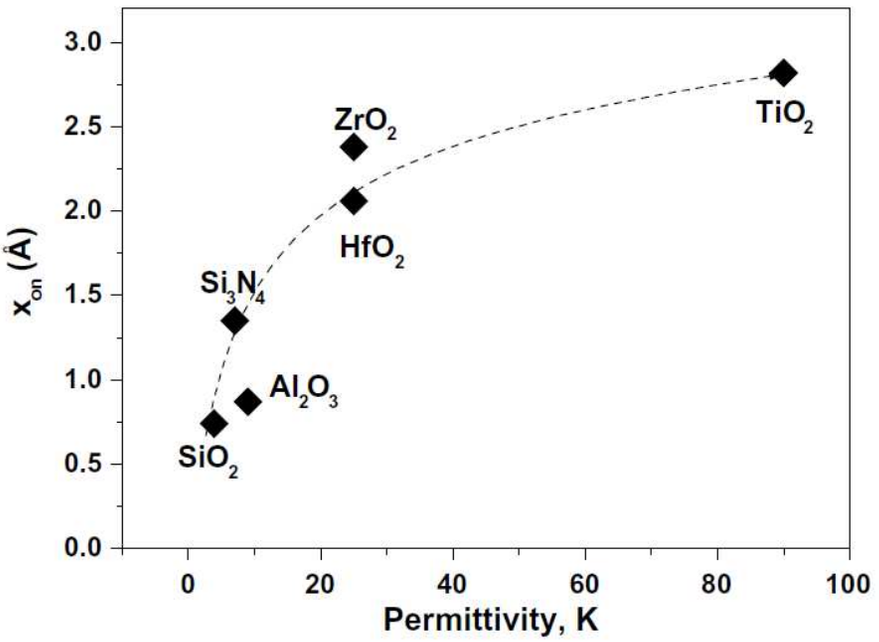

Figure 13. Tunneling decay length versus permittivity for several dielectrics.

Finally, to obtain the energy position of DIGS states in the band gap of the dielectric, we use equi-emission line equations [33] , and considering that the measurement frequency is related to emission rate by $e_n = \omega / 1.98$ [36] , we obtain the following equation:

$$E' - E(x_C, t) = H_{eff} + kT \ln \frac{\sigma_0 v_{th} N_C}{\omega / 1.98} - \frac{kT}{x_{on}} x_C(t) \tag{10}$$

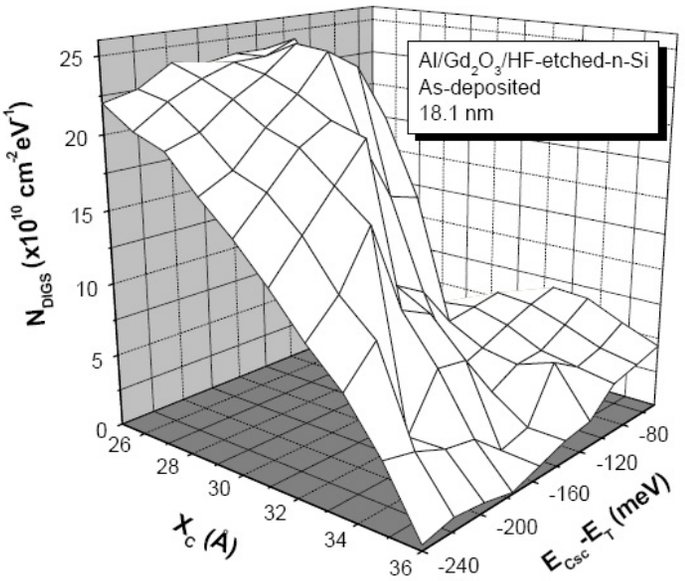

Figure 14. Example of DIGS profile: atomic layer deposited Gadolinium oxide films.

When temperature decreases the emission rates of all interface states exponentially decrease, and the equi-emission lines shift approaching the interface. Thus, transients are modified in a similar way as when frequency is increased while keeping constant the temperature. DIGS three-dimensional profile or contour line maps can be obtained using Equations (9) and (10). As for the experimental sensitivity, temperature measurement involves an error of 0.1 K. Estimated errors of energy and defect concentration values on DIGS profiles are of about 10 meV and $5x10^9$ $eV^{-1}cm^{-2}$, respectively. Estimated precision on DIGS depth is of about 2 Å.

The experimental set-up consists of a pulse generator to apply bias pulses, a lock-in analyzer to measure the conductance, and a digitizing oscilloscope to record conductance transients. Samples are cooled in darkness from room temperature to 77 K in a cryostat. Figure 14 is an example of DIGS profiles obtained from conductance transients on MIS structures fabricated with ALD Gadolinium oxide as dielectric.

In section IV.C we review results obtained for several high-k dielectrics grown by atomic layer deposition (ALD) under different processing conditions.

3.3. Flat-Band Transient Technique (FBT)

Several problems must be fixed before the high-k dielectric materials could be extensively used in fabrication. One of them is the instability caused by charge trapping and detrapping inside the dielectric. Fixed and trapped charges cause serious performance degradation by shifting the threshold voltage, limiting transistor mobility and reducing device lifetimes. Threshold voltage shifts are observed under positive bias, negative bias and hot-carrier stressing in high-gate stacks. Charge trapping under positive bias stressing is known to be more severe compared to conventional SiO_2-based gate dielectrics [38]. It is believed to happen due to filling of pre-existing bulk traps. Charge trapping causes threshold voltage shifts and drive current degradation over device operation time. It also precludes accurate mobility (inversion charge) measurements due to a distortion of C-V curves. Negative bias temperature instability (NBTI) induced threshold voltage shifts in high-k devices are also observed and are comparable to those observed for silicon-based oxide devices.

In a previous work [39], we showed the existence of flat band voltage transients in ultra-thin high-k dielectrics on silicon. To obtain these transients, we recorded the gate voltage while keeping the capacitance constant at the initial flat band condition (C_{FB}). Therefore, samples were kept under no external stress conditions: zero electric field in the substrate, darkness conditions and no external charge injection. Under these conditions, the only mechanism for defect trapping or detrapping is thermal activation, that is, phonons. We proved that the energy of soft-optical phonons in high k dielectric is obtained with this experimental approach.

The flat-band voltage, V_{FB}, of a MIS capacitance is given by:

$$V_{FB}(t) = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{tox} \rho_{ox}(x,t) x dx \tag{11}$$

When the charge density inside the insulator film, $\rho_{ox}(t)$, varied with time, t, or with the distance from the interface, x, the flat band voltage varies. In particular, trapping and detrapping on defects existing inside the dielectric will produce transient variations of the flat-band voltage. According equation (11) these variations are oposite in sign to the charge variation. As it has been suggested elsewhere [40] at flat-band voltage conditions there are not electrons or holes directly injected form the gate or semiconductor, i.e., free charges move by hopping from trap to trap. Moreover, since no optical neither electrical external stimulus are applied, free charges must be originated from trapping or detrapping mechanisms of defects existing inside the dielectric and the energy needed to activate this mechanisms only can be provided as thermal energy, that is, phonons.

The experimental setup of this technique is identical to that used to capacitance-voltage technique. The only difference is that in order to obtain the flat-band voltage transients, a feedback system that varies the applied gate voltage accordingly to keep the flat-band capacitance value was implemented.

The experimental flat band voltage transients become faster when the dielectric thickness diminishes. Time dependences appear to be independent of the temperature. These two facts suggest that there are tunnelling assisted process involved. The amplitude of the transients is thermally activated with energies in the range of soft-optical phonons usually reported for high-k dielectrics. We have proved that the flat-band voltage transients increase or decrease depending on the previous bias history (accumulation or inversion) and the hysteresis sign (clockwise or counter-clockwise) of the capacitance-voltage (C-V) characteristics of MOS structures. In the next section we illustrate all these finger prints.

To illustrate the technique, we have included in Figure 15 some experimental results for the case of a sample of a 20 nm film of hafnium oxide deposited by ALD on silicon. The amplitude of the flat-band voltage transients depends on temperature according an Arrhenius type law:

$$\Delta V_{FB}(T,t)\,\alpha\,\exp-\left(\Phi_{ph}\Big/kT\right) \tag{12}$$

where Φ_{ph} is the energy of the soft optical phonons of the dielectric.

4. Some examples

This section includes a selection of different cases to show the applicability of our techniques.

4.1. Effect of interlayer trapping and detrapping on the determination of interface state densities on high-k dielectric stacks

HfO_2 is among the most promising high-k dielectrics, but before qualifying, the nature and formation of electrically active defects existing in these emerging materials should be

known. In fact, hafnium based high-k dielectris are already in production [41-43]. While not identified, it is most likely the dielectrics used by these companies are some form of nitrided hafnium silicates (HfSiON). HfO_2 and HfSiO are susceptible to crystallize during dopant activation annealing. However, even HfSiON is susceptible to trap-related leakage currents, which tend to increase with stress over device lifetime. This drawback increases with the hafnium concentration. It is known that defects in SiO_2 are passivated by hydrogen, but this can cause some problems in HfO_2 [44]. Moreover, as most of the high-k materials, when HfO_2 is deposited in direct contact with Si a silicon oxide (SiO_x) interfacial layer (few nanometres thick) is formed [45, 46]. Because of the non-controlled nature of this silicon dioxide layer, its quality is poor and the interfacial state density (D_{it}) and leakage current increase. Moreover, this barrier layer leads to a reduction of the dielectric constant and, hence, to the effective capacitance of the gate dielectric stack. The use of silicon nitride instead of silicon oxide as barrier layer can improve the effective capacitance of the gate dielectric stack, since silicon nitride has a higher permittivity (≈ 7) than silicon oxide (≈ 3.9). Moreover, SiN_x is stable when deposited on Si, preventing the growth of silicon oxides, and the use of nitrides greatly reduces boron diffusion from the heavily doped poly-Si gate electrode to the lightly doped Si channel [3].

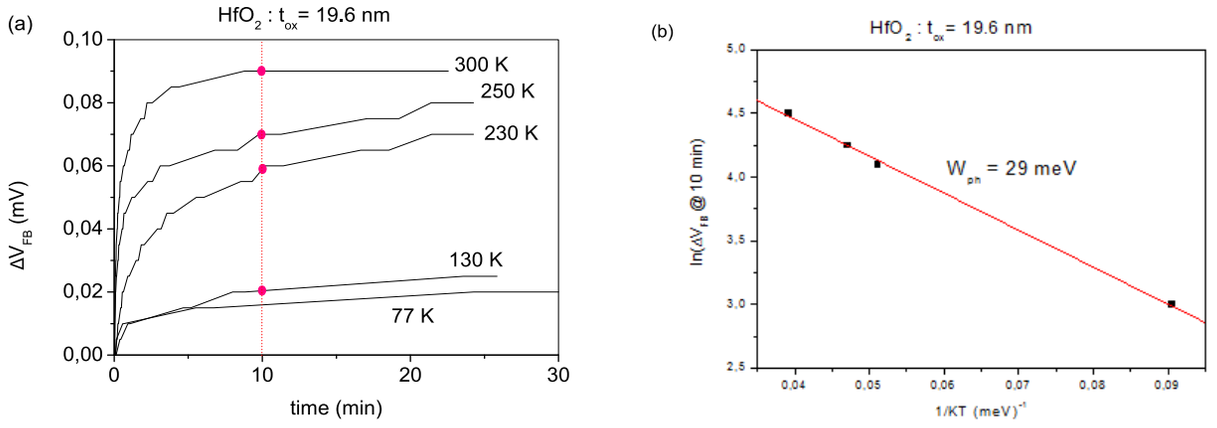

Figure 15. Example of DIGS profile: Atomic Layer Deposited hafnium oxide films.

In a previous work [47] we studied the influences of the silicon nitride blocking-layer thickness on the Interface State densities (D_{it}) of HfO_2/SiN_x:H gate-stacks on n-type silicon. The blocking layer consisted of 3 to 7 nm thick silicon nitride films directly grown on the silicon substrates by electron-cyclotron-resonance assisted chemical-vapour-deposition (ECR-CVD). Afterwards, 12 nm thick hafnium oxide films were deposited by high-pressure reactive sputtering (HPS). Interface state densities were determined by deep-level transient spectroscopy (DLTS) and by the high and low frequency capacitance-voltage (HLCV) method. The HLCV measurements provide interface trap densities in the range of 10^{11} cm^{-2} eV^{-1} for all the samples. However, a significant increase of about two orders of magnitude was obtained by DLTS for the thinnest silicon nitride barrier layers. In this work we probe that this increase is an artefact due to the effect of traps located at the internal interface existing between the HfO_2 and SiN_x:H films. Because charge trapping and discharging are

tunnelling assisted, these traps are more easily charged or discharged as lower the distance from this interface to the substrate, that is, as thinner the SiN_x:H blocking layer. The trapping/detrapping mechanisms increase the amplitude of the capacitance transient and, in consequence, the DLTS signal, which have contributions not only from the insulator/substrate interface states but also from the HfO_2/SiN_x:H interlayer traps.

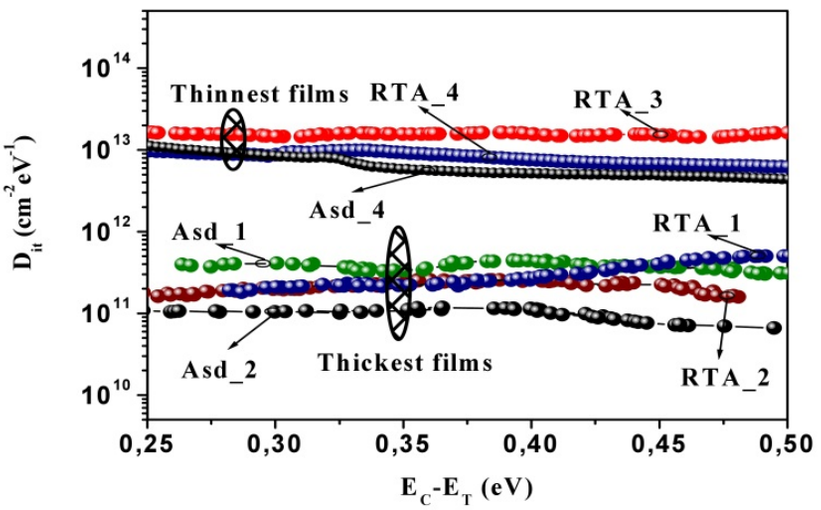

Figure 16. Interface state density measured by DLTS

To determine the interface trap densities we used DLTS and HLCV techniques in order to contrast the results obtained by the two techniques. HLCV measurements are summarized in table 1. This technique provides similar interface density (D_{it}) values (2-4 × 10^{11} $cm^{-2}eV^{-1}$) for all the samples, regardless the silicon nitride layer thickness. Therefore, interface quality seems not to depend on the blocking layer thickness, as one could expect for these not ultrathin films. In contrast, DLTS results (Figure 16) can be clearly separated in two groups: one corresponding to the thickest samples which has D_{it} densities from 9 × 10^{10} $cm^{-2}eV^{-1}$ to 4 × 10^{11} $cm^{-2}eV^{-1}$, in good agreement with HLCV results, and the other group corresponding o the thinnest samples wit D_{it} values (from 6×10^{12} $cm^{-2}eV^{-1}$ to 2×10^{13} $cm^{-2}eV^{-1}$) much higher than those obtained by HLCV. In order to explain these discrepancies we carried out an exhaustive analysis which leads us to conclude that charging and discharging mechanisms of inner traps existing at the HfO_2/SiN_x interface affect the DLTS results.

Figure 17 plots the normalized C-V curves measured at room temperature for the as-deposited samples. The stretch-out is similar for all the samples, meaning a similar trap density, contrary to the DLTS results. Vuillame et al. [48] reported variations in the DLTS signal due to slow traps located inside the insulator, but these changes are only observed for very short filling accumulation pulses times under 50 μs, much lower than the 15 ms used in our experiments. On the other hand, changes were much smaller than those observed in this work. Moreover, slow traps induce hysteresis at the C-V curves and conductance transients. However, a clockwise hysteresis is observed only in the thickest samples and conductance transients have not been detected in any of the thinnest samples. The only difference between the samples is the HfO_2/SiN_x:H interface distance from the substrate, so that we

focused our attention in the traps existing at the surface between the SiN_x:H interface layer and the HfO_2 film.

Sample	ECR-CVD time (s)	Silicon nitride Tickness (nm)	RTA	D_{it} from DLTS $\times 10^{11}$ ($cm^{-2}eV^{-1}$)	D_{it} from HLCV $\times 10^{11}$ ($cm^{-2}eV^{-1}$)
Asd_1	90	6,6 ± 0,4	As-deposited	3 – 5	3.0
RTA_1			600 ºC – 30s	2 - 5	2.2
Asd_2	60	5,9 ± 0,4	As-deposited	0.8 – 1	1.3
RTA_2			600 ºC – 30s	1 - 2	2.7
Asd_3	30	3,9 ± 0,2	As-deposited	Not measured	4.5
RTA_3			600 ºC – 30s	100 - 200	4.4
Asd_4	15	3,0 ± 0,4	As-deposited	50 - 100	2.0
RTA_4			600 ºC - 30s	50 - 100	1.9

Table 1. ECR-CVD deposition time, silicon nitride thickness and interface state densities provided by DLTS and HLCV measurements.

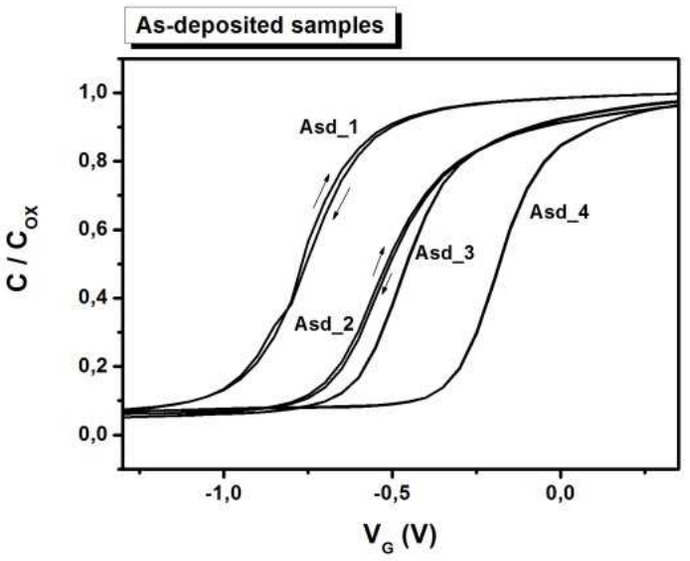

Figure 17. 1 MHz C-V curves measured for the as-deposited samples at room temperature.

To study these discrepancies in depth, we have focused our attention on the sample showing the biggest discrepancies on the D_{it} values measured by HLCV and DLTS. The one selected was the Asd_4 sample, which has the lowest barrier layer thickness (3 nm). First, we recorded the interface state density profiles obtained by DLTS when varying the bias conditions. Figure 18(a) shows important variations in the D_{it} profiles when the accumulation filling pulse voltage is varied while keeping constant the reverse voltage. On the contrary, no significant differences are obtained when varying the reverse voltage (Figure 18(b). Therefore, the mechanisms responsible for these variations must occur during the trap-filling pulse but not under reverse (detrapping) bias conditions, when the capacitance transients are recorded.

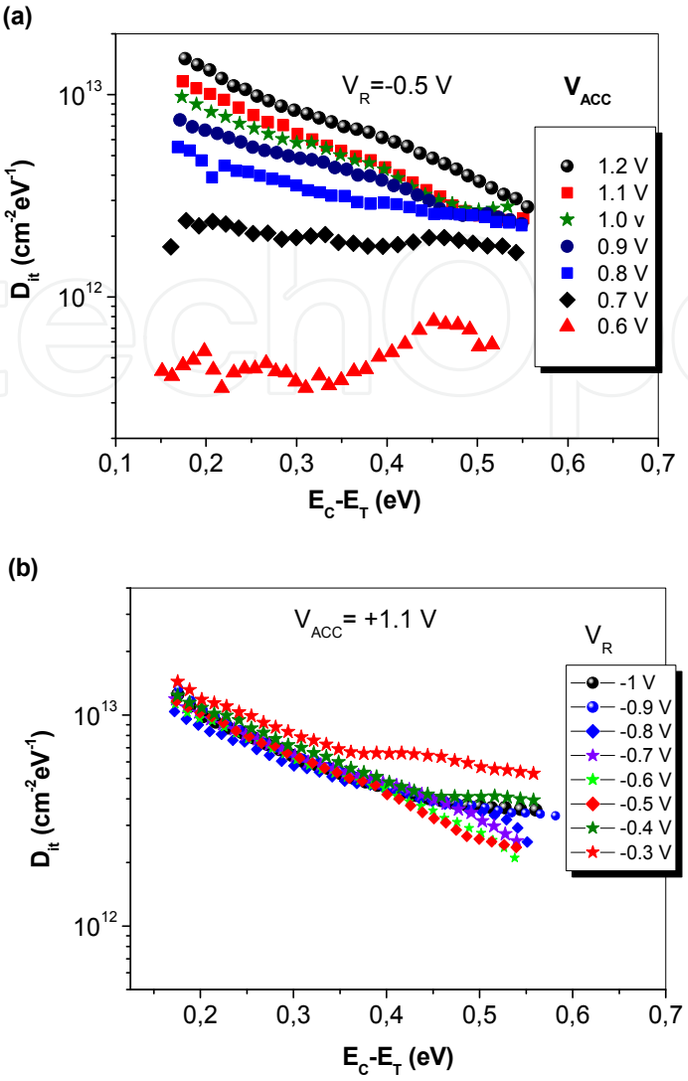

Figure 18. DLTS profiles obtained keeping constant the voltage of the reverse-emptying-pulse (a) and the accumulation-filling pulse (b).

In Figure 19 we show the DLTS values obtained for different energies as a function of gate voltage and the electric field at the Silicon Nitride film. The electric field has been evaluated according the expression:

$$F_{SiNx} = \frac{V_G - V_{FB}}{\frac{\varepsilon_{SiN_x}}{\varepsilon_{HfO_2}} t_{HfO_2} + t_{SiN_x}} \tag{13}$$

We clearly observed that for all the energies the relationship between D_{it} and electric field is linear:

$$\frac{dD_{it}}{dF_{SiNx}} = \eta(E_c - E_T) \tag{14}$$

The slope of Equation (14) is a function of energy. This dependency is plotted in Figure 20 and we have observed that the experimental points fit very well the following dependency.

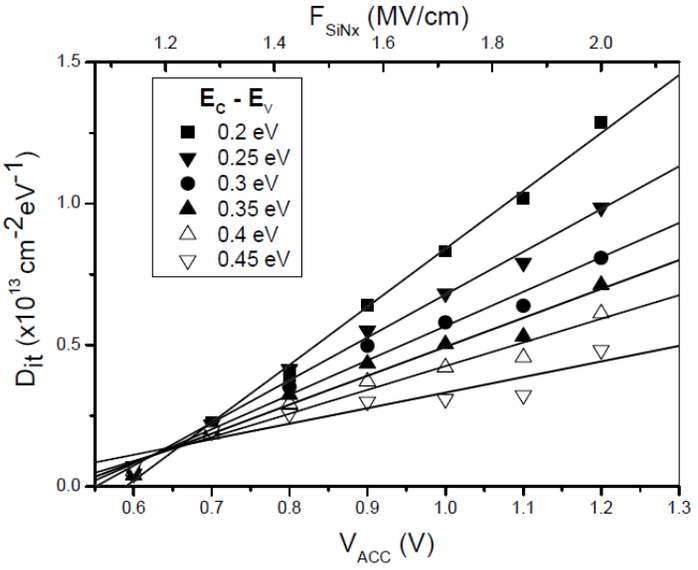

Figure 19. Experimental DLTS signal as a function of accumulation voltage and SiN_x electric field for different energies.

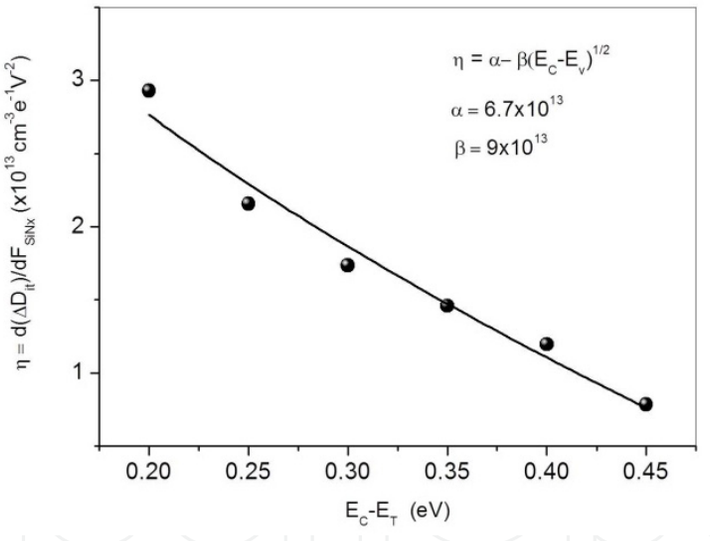

Figure 20. Variation with energy of the electric field barrier lowering parameter, η.

$$\eta(E_c - E_T) = \alpha - \beta\sqrt{E_C - E_T} \tag{15}$$

In summary, we can state that experimental DLTS profiles obey the following expression:

$$D_{it}^{*} = D_{it} + \eta F_{SiNx} = D_{it} + \left(\alpha - \beta\sqrt{E_c - E_T}\right) F_{SiNx} \tag{16}$$

where *Dit** is the as-measured apparent interface state profile. Dit is the true trap interface state density profile that is the obtained at low electric filed values. η is a parameter

associated to the electric field lowering of the energy barrier between the silicon conduction band and traps located at the inner layer interface. This barrier is lower as higher the energy of the traps at the inner interface layer and this fact is included at the second term of parameter η.

The true interface state density, *Dit*, is plotted at Figure 21 as obtained for the lowest accumulation voltage values. These values do agree with those obtained when using HLCV technique. Moreover, this distribution show a profile consisting on broad gaussian peaks, as is usually reported for silicon nitride films [49-53].

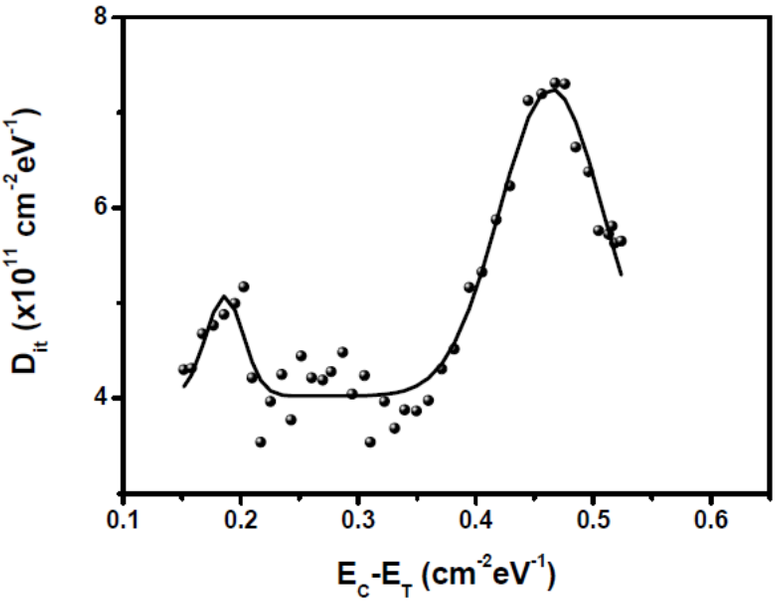

Figure 21. True interface state density profile as obtained at low electric fields (<1 MV.cm-1)

4.1.1. Band energy model

The energy diagrams of the MIS structures under accumulation and inversion are displayed in Figure 22. To construct them, we have included the published values of the bandgap and the conduction and valence band offsets of hafnium oxide and silicon nitride relative to silicon [54]. We also assume that defects exist at the HfO2/SiN_x:H inner layer interface (IL). DLTS measurements consist of applying accumulation pulses to fill the interface states in the upper half of the semiconductor bandgap followed by reverse pulses in which the interface states emit electrons to the conduction band yielding capacitance transients that are conveniently recorded and processed to obtain the D_{it} distribution. If the SiN_x:H film is thin enough, tunnelling between the semiconductor and the inner layer interface (IL) may occur. At accumulation, capturing electrons coming from the semiconductor band by direct tunnelling fills IL states. Then, when the reverse pulse is applied these defects emit the captured electrons to the semiconductor band. The emission process may occur in two different ways: IL states with energies above the silicon conduction band (light grey area) emit electrons by direct tunnelling (A). On the other hand, for energies ranging from the Fermi level to the semiconductor conduction band (dark grey area) tunnelling between the

IL states and the interface states (B). These interface states can emit electrons to the conduction band in a similar way as occurs in conventional DLTS (C). Electrons emitted according the (B)+(C) sequence increase the capacitance transient, obtaining an apparent increase in the measured interfacial state densities. Since all these mechanisms are tunnelling assisted, as thinner the silicon nitride films as higher their probability. In our experiment, the SiN_x:H layer thickness has been varied from around 3 to 6.6 nm. To roughly estimate the relationship between the tunnelling charging/discharging probabilities for two samples with different silicon nitride thickness (t_1 and t_2), we can use the following quantum mechanics expression:

$$\frac{p_1}{p_2} = \exp\left[\frac{2\pi\sqrt{2m_h\overline{\phi_V}}}{h}\left(t_1 - t_2\right)\right] \tag{17}$$

where m_h is the hole effective mass inside the barrier, $\overline{\phi_v}$ is the mean barrier height, t_1 and t_2 are the barrier thickness and h is the Plank's constant. For the h-well triangular barrier, $\overline{\phi_v}$ = $\Delta E_V/2$, where ΔE_V is the valence band offset of silicon nitride relative to silicon. Gritsenko et al. [55] reported values of $\Delta E_V \approx 1.5$ eV and $m_h/m_0 = (0.3 \pm 0.1)$. Here m_0 is the free electron mass. These values yield a relation of $p_1/p_2 = 10^{-4}$ for two layers of 6 and 3 nm, respectively, so indicating that the IL trapping/detrapping mechanisms effect is negligible for thicker samples in comparison with the 3 nm-thick blocking layer samples where the very thin silicon nitride layer allows electron tunnelling from IL traps to the channel interface, so increasing the total charge emitted during the DLTS reverse pulses.

Moreover, as higher the electric field In Figure 22(b) higher filling-pulse (higher bias in the accumulation regime). In this case, a larger number IL traps has been filled. When biasing the sample in the inversion regime, a higher number of IL traps can contribute to the capacitance transient by direct tunnelling. This result agrees with results shown in Figure 18(a): the higher the filling pulse the higher the DLTS *Dit* results.

On the contrary, variations of the inversion bias do not change the total filled traps, and the emitted charge from the IL traps does not change significantly. The results shown in Figure 18(b) confirm this hypothesis: the measured D_{it} values hardly change when varying the reverse bias.

In samples with thicker SiN_x:H layer, IL traps cannot contribute to the DLTS capacitance transients, which take place in a relatively short time. However, the IL traps in these samples do exchange charge with the substrate in longer times, giving rise to the hysteresis phenomena not observed in the two thinnest samples. In fact, we can measure slow states inside the MIS insulator by the conductance transient technique (GTT) [56]. We measured the slow states inside the insulator and we observed only slow states in the two thickest samples: if these slow states were due to traps in the bulk SiN_x:H, they would appear in all the samples.

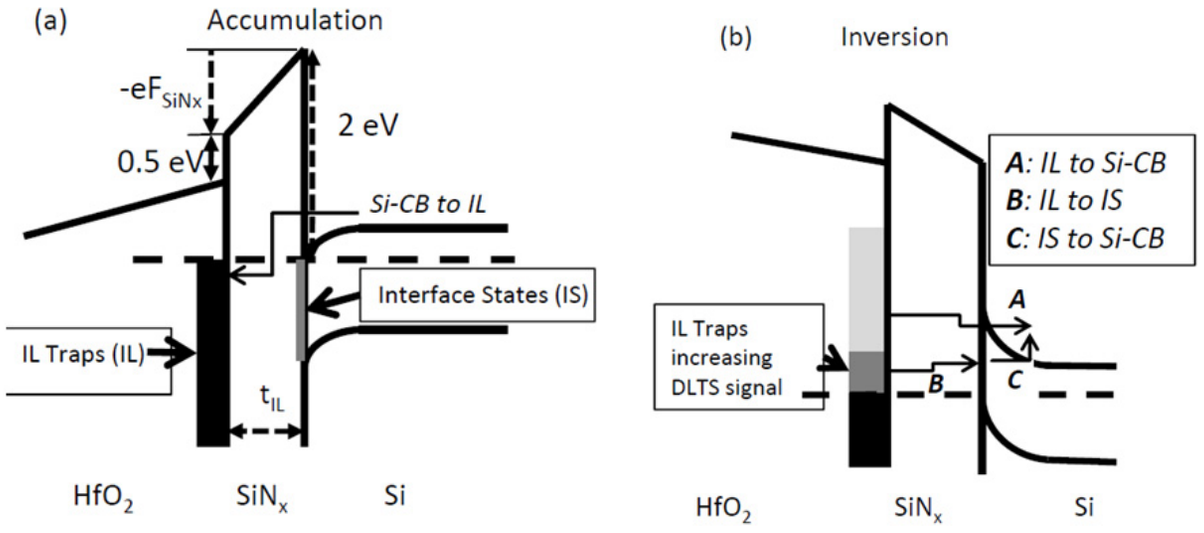

Figure 22. Energy band diagram of the HfO_2/SiN_x:H/n-Si MIS structures under accumulation (a) and inversion (b)

4.2. Flat-band voltage transients: Main fingerprints

In this section we summarize the main finger-prints of the flat-band voltage transients. We have obtained V_{FB} transients for many high-k dielectrics (HfO_2, hafnium silicate, Al_2O_3, TiO_2 and Gd_2O_3). In all cases, there is a direct relationship between the C-V curve hysteresis and the transient amplitude. Here we present a selection of our experimental work to show the information that can be extracted from the transients as well as the parameters affecting to their amplitude, shape, and time constant. We have observed that the main parameters affecting the transients are the experimental temperature, the dielectric film thickness, the dielectric material itself and, finally, the bias voltage and the setup time just before the flat band voltage condition is established in the sample.

4.2.1. Temperature and thickness dependencies

Figure 23 shows capacitance-voltage curves obtained at room temperature for as-deposited Al/Gd_2O_3/HF-etched-Si (a) and Al/Gd_2O_3/SiO_2/Si (b) MIS structures with different Gd_2O_3 thickness. V_{FB} is negative in all cases indicating the existence of positive charge in the dielectric. In Figure 23(a) we see that V_{FB} moves to less negative values with thickness indicating that the charge centroid is closer to the interface for thicker films. That means that traps are preferentially created in the very first dielectric layers. Moreover, in Figure 23(b) we see that when a SiO_2 film is present, V_{FB} shows more negative values and weaker thickness dependence than when Gd_2O_3 films are directly deposited on HF-etched silicon. That must be due to the existence of non-mobile charge trapped at the interface between the high-k and SiO_2 films. V_{FB} transients for different thicknesses (Figure 24(a)) reveal time constants increasing with thickness below 5.7 nm. That indicates the existence of charge displacement mechanisms: the thinner the films the lower the distances to be covered for the mobile charges to reach the gate and/or the insulator-semiconductor interface.

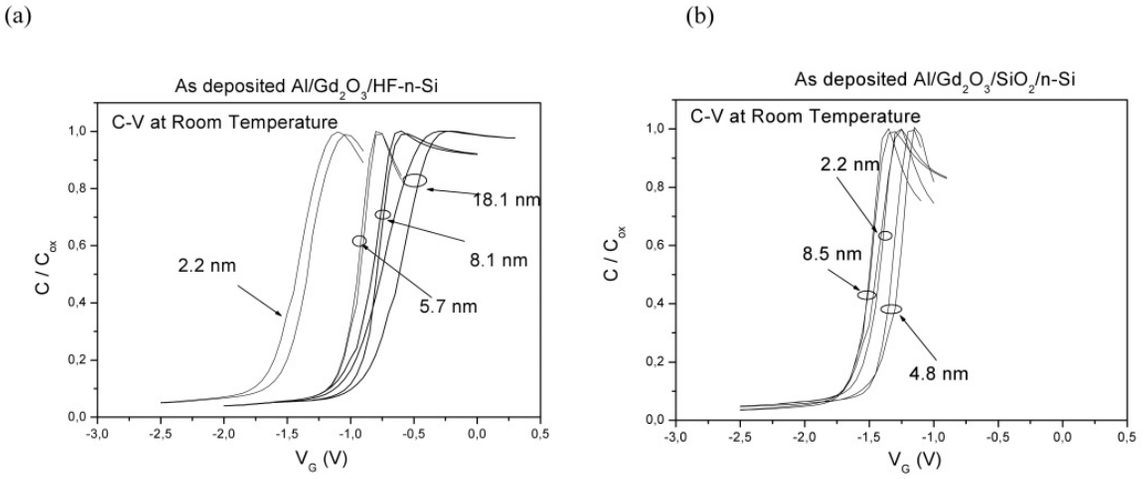

Figure 23. Normalized C-V curves of Al/Gd_2O_3/HF-etched-Si (a) and Al/Gd_2O_3/SiO_2/Si (b) with different Gd_2O_3 thicknesses, measured at room temperature.

To characterize the time dependence of the transients, we have normalized them (Figure 24(b)) by dividing the experimental values by their value at 600 seconds. It is clear that the time constant is independent of the temperature, indicating that tunnelling mechanisms are involved in the conduction. As for temperature dependency of V_{FB} transients, we recorded transients at several temperatures (Figure 25(a)) and we observed that their magnitude follows an Arrhenius plot (Figure 25(b)) with activation energy in the range of the soft-optical phonon energies (W_{PH}) usually reported for high-k dielectrics. From our fits for different samples we have obtained that for Gd_2O_3 these energies are of about 55±10 meV. These values were obtained for both annealed and as-deposited samples and for Gd_2O_3 film thicknesses from about 2 to 20 nm.

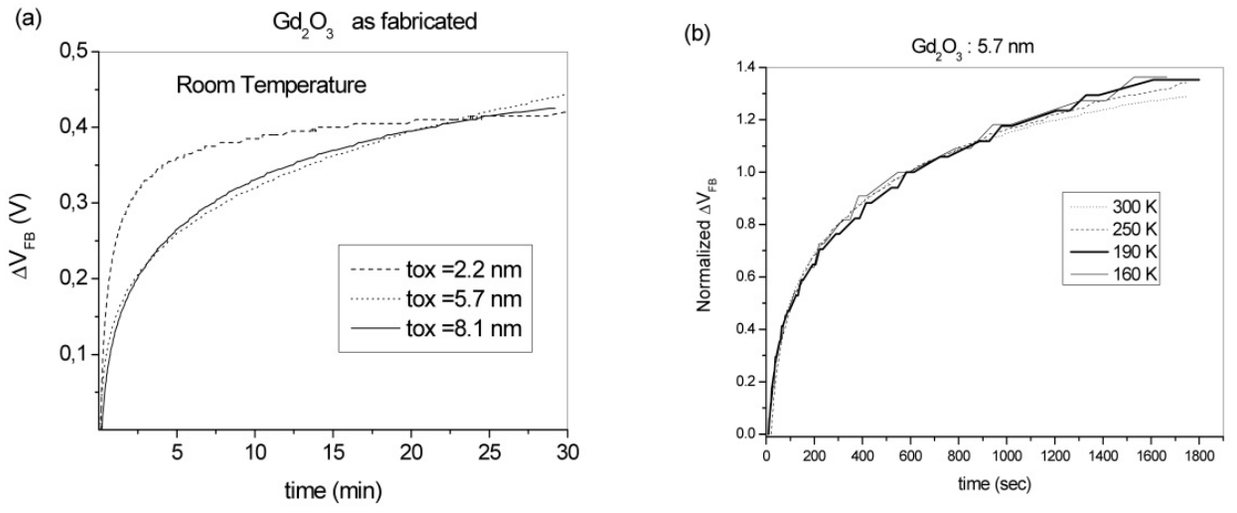

Figure 24. Flat-band voltage transients at different Gd_2O_3 thickness, t_{ox}, (a) and temperature (b) of Gd_2O_3-based MIS structures.

From all these observations we concluded that the flat band voltage transients under conditions without external stress are originated by phonon-assisted tunnelling between

localized states: Phonons produce the ionization of traps existing in the bandgap of the insulator. Electrons and/or holes generated in this way move by hopping from trap to trap until they reach a defect location and neutralize the charge state of this defect. It is important to point out that the electrons (or holes) do not enter the conduction (or valence) band of the dielectric and the conduction takes place within the band gap.

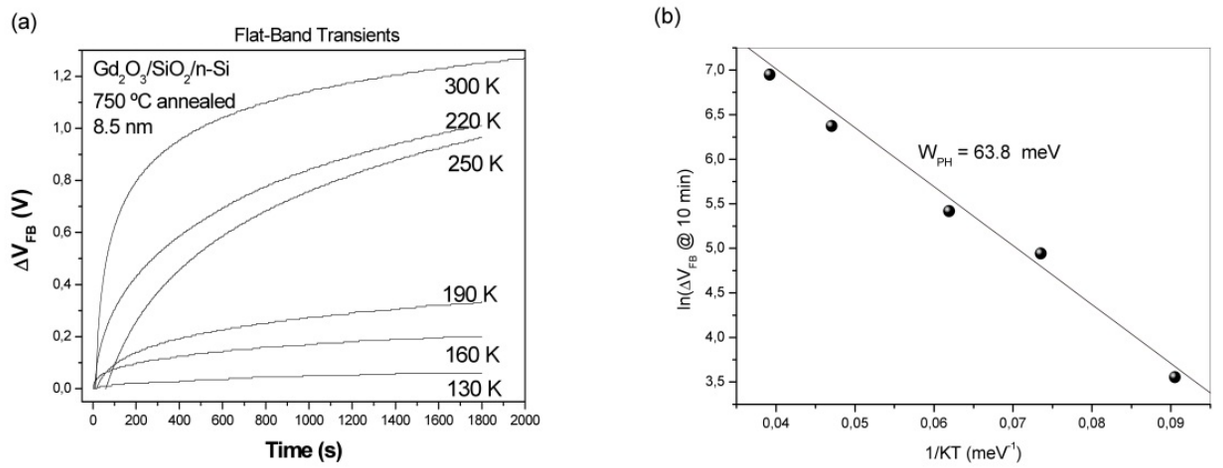

Figure 25. Flat-band voltage transients at different temperatures (a) and Arrhenius plot of the transient amplitude at 10 minutes (b) for an Al/Gd_2O_3/SiO_2/Si sample.

4.2.2. Influence of the setup conditions

In this section we show how the V_{FB} transients are different depending on the bias regime of the sample just before the transient were recording. Transients are different depending if the samples are biased in accumulation or in inversion regimes. Setup time under these previous conditions also affect to the transient amplitude. To illustrate these influences we analyze here two cases based in HfO_2 films. The first one is an HfO_2 film directly grown on n-type silicon, and the second is a HfO_2/SiO_2 stack deposited on n-type silicon. Figure 26(a) shows the C-V curves at room and low temperature for an Al/HfO_2/Si sample with a 250 Å HfO_2 layer grown by atomic layer deposition (ALD). We observe that blat band voltage is positive in all curves indicating the existence of negative charge in the dielectric. Moreover, C-V shows hysteresis at both temperatures. Both flat band voltage and hysteresis are bigger for low temperature. The amount of negative charge and hysteresis are higher at low temperature.

To explain that we suggest that there are positive and negative charges inside the dielectric having different activation energies. At low temperatures positively charged traps (PCT) are not ionized, whereas this temperature is high enough to ionize traps yielding negative charge (NCT). When temperature increases positive traps are ionized by emitting electrons that moves by hopping to the gate or to substrate, so partially compensating the total negative charge. Another point is that hysteresis is clockwise at all temperatures, that is, accumulation bias give places to an increase of the total negative charge. When sample is in accumulation, detrapping mechanisms occurs and traps remain ionized. At inversion, PCT trap electrons coming from the gate and NCTs trap holes coming from the inversion layer at

the substrate. Since NCTs predominates the whole effect is that negative charge increases during accumulation and decreases at inversion. These arguments are also observed in the flat-band voltage transients (Figures 26(b) and (c)).

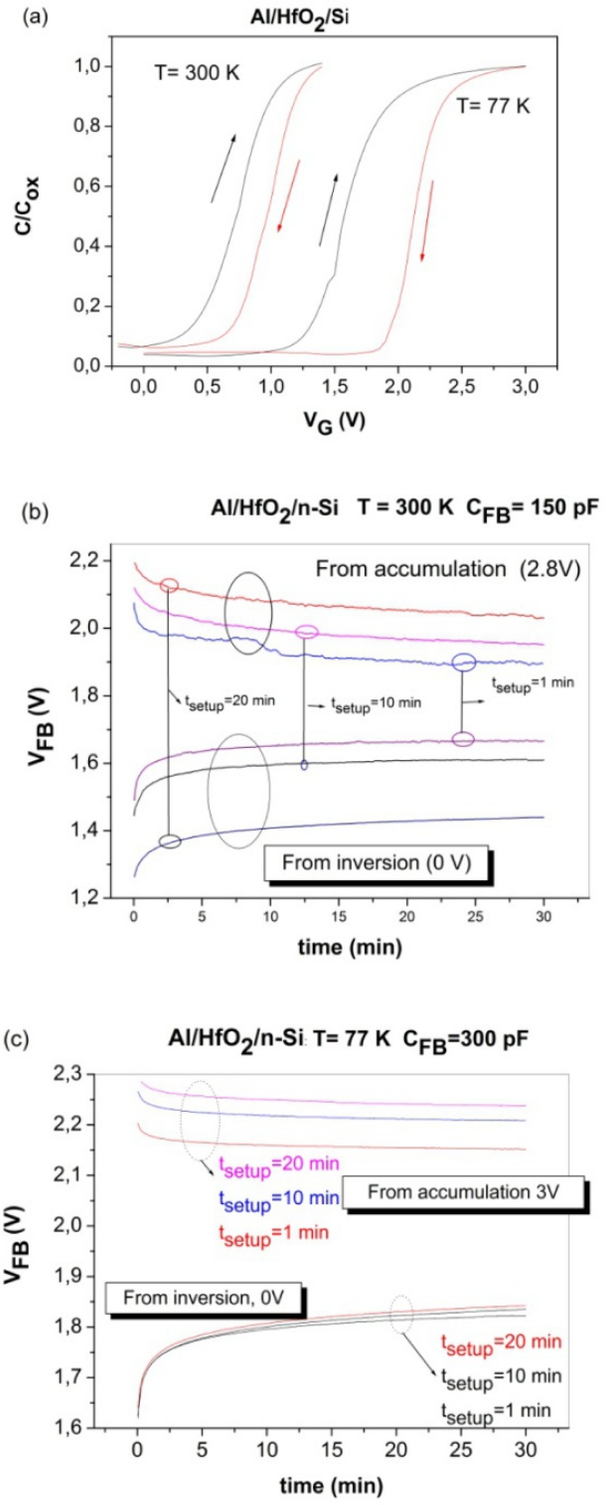

Figure 26. Normalized C-V curves (a) and Flat-band voltage transients at room temperature (b) and 77 K (c) of an Al/HfO_2 /Si sample grown by ALD

We see that transients are decreasing when coming from accumulation and increasing when the sample is previously biased in inversion. At flat-band conditions traps previously charged (PCTs in accumulation and NCTs at inversion) can emit the trapped charge giving place to the corresponding flat-band voltage variation. We see also that these effects are more important as the setup time is higher indicating that trapping and detrapping are not instantaneous because the time needed by free carriers to reach the trap locations. Another important point is that decreasing and increasing transients seem to reach the same final values but after very long times (very much longer than those used in our experimental records).

The second case presented here is a sample in which the dielectric is a stack of an 21 nm HfO_2 film grown by High-Pressure Reactive Sputtering (HPRS) and a SiO_2 buffer layer (3.4 nm-thick). In this case (Figure 27), C-V curves indicate that at room temperature there is positive charge at the dielectric, that is PCTs predominates over NCTs. Consequently, in accumulation the positive charge increases and decreases in inversion regime, giving place to the counter clock-wise hysteresis cycle observed at room temperature. At 77 K the PCTs are not ionized and the hysteresis cycles are due only to NCTs and, then, a clock-wise hysteresis cycle is obtained. This model is confirmed by the opposite trends shown by the flat-band voltage transients obtained at room and low temperature (Figures 27(b) and (c)). Low temperature curves are similar to those obtained in the previous case (Figure 26).

4.3. Conduction transient profiles of high-k dielectrics

In this section we review results obtained for several high-k dielectrics grown by atomic layer deposition (ALD) under different processing conditions. The most noticeable results provided by the experimental contour maps are outlined.

4.3.1. Hafnium-based dielectrics

HfO_2 is a promising gate dielectric material due to its high dielectric constant and excellent thermal stability. Figure 28 shows three-dimensional DIGS plots for HfO_2 atomic layer deposited on n-Si and over p-Si using chloride as metal (Hf) precursor. DIGS states are located at energies close to the majority band edge of the semiconductor. This can be explained in terms of the very nature of the conductance transient technique: majority band edges have the maximum majority carrier concentration, so states located at energies close to this position have the maximum probability to capture majority carriers. On the other hand, no conductance transients were observed for ultrathin samples (less than 40 Å). Kerber et al. [57] proposed the existence of a defect band in the HfO_2 layer. We find spatially distributed defect bands for films on both types of silicon substrates. These defect bands could be due to oxygen vacancies: when the capacitor structure is terminated by the oxide-Si interface, the electric field existing in the dielectric film makes oxygen vacancies (positively charged) to move towards locations farther away from the interface. That occurs in samples deposited on n-type silicon f the difference in semiconductor band bending at the interface [58]. Forming gas annealings (FGA) are usually employed in integrated circuit technology

for passivation of defects (dangling bonds) on Si surface. Figure 29(a) shows DIGS density corresponding to post-metallization annealed (400ºC, 30 min) Al/HfO_2/p-Si sample. Lower DIGS density is achieved, but D_{it} density is increased in this sample [59], indicating that thermal treatment partially moves the insulator defects to the interface. Ioannou-Sougleridis et al. [60] attributed instabilities observed in as-grown Y_2O_3 samples to slow traps, which were mostly removed after FGA. The same behaviour can affect our results.

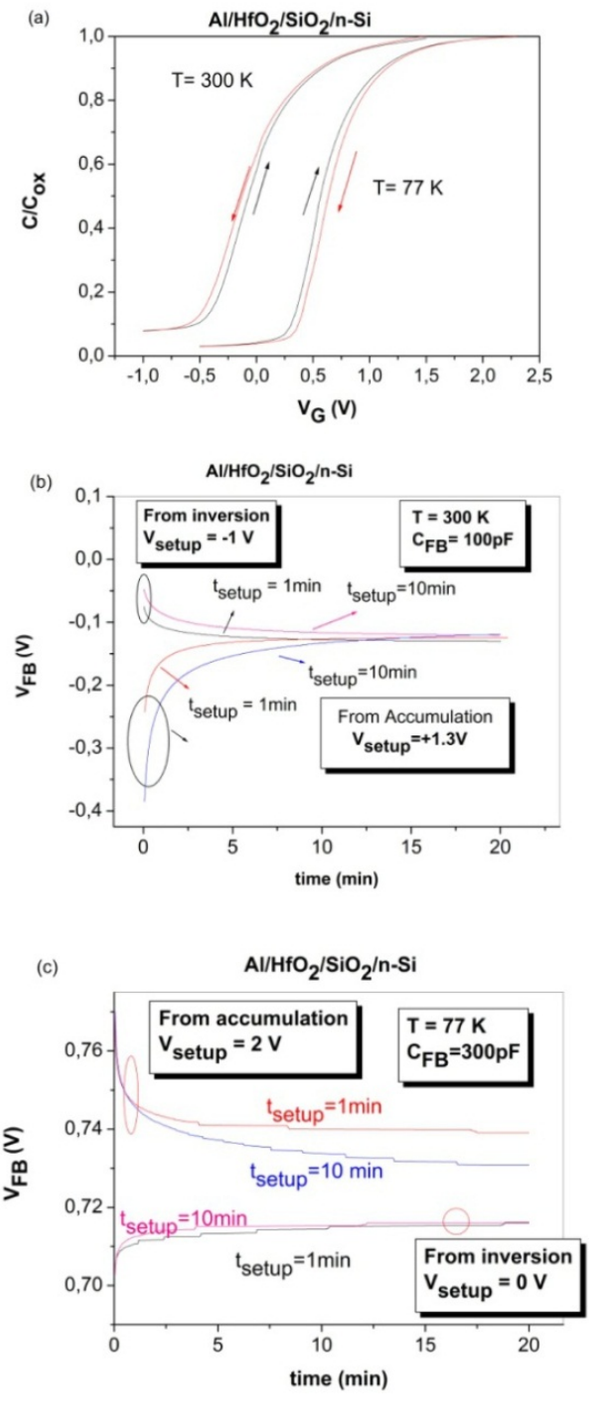

Figure 27. Normalized C-V curves and Flat-band voltage transients at room temperature (b) and 77 K (c) for an Al/HfO_2/SiO_2/n-Si sample grown by HPRS

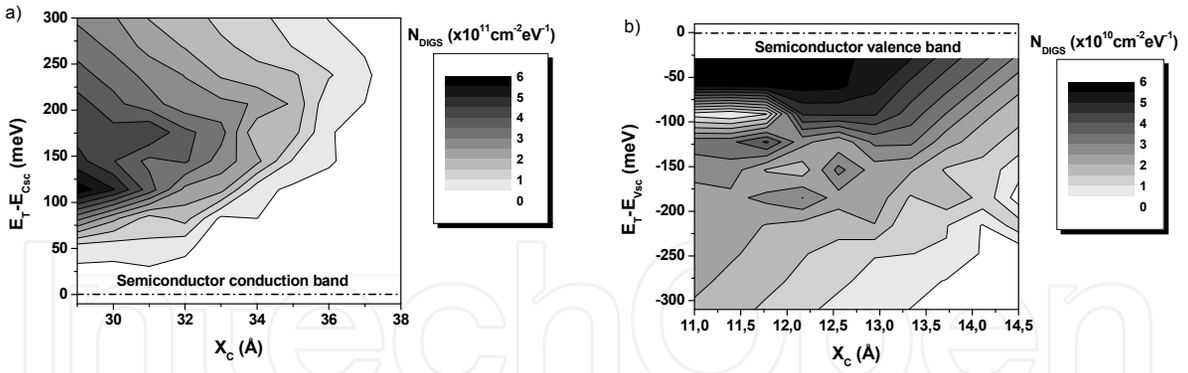

Figure 28. Three-dimensional DIGS plots for unannealed HfO2 atomic layer deposited on n-Si (a) and over p-Si (b)

Transition metal silicates, such as hafnium silicate, have also been the object of a considerable number of studies to replace SiO_2 because of their higher crystallization temperature. Figure 29(b) shows DIGS states obtained from as-deposited Al/$HfSi_xO_y$/n-Si structures grown using HfI_4 and $Si(OC_2H_5)_4$ as precursors. In this case contour lines have a more anisotropic shape than those for HfO_2 indicating less homogeneous distribution of DIGS defects. In fact, we can see two different local ordering at zones A and B. The boundary between these zones approximately follows the line $E_{Csc} - E_T = 588.22 - 15.42 x_C$. Contour lines are parallel in zone A and perpendicular to this boundary, indicating some regularity in the defect distribution. On the other hand, DIGS density rapidly decreases to lower values in zone B, where uniformity is higher. When this sample is submitted to a post-deposition annealing at temperatures ranging from 700 to 800ºC, this two-region structure does not change [61].

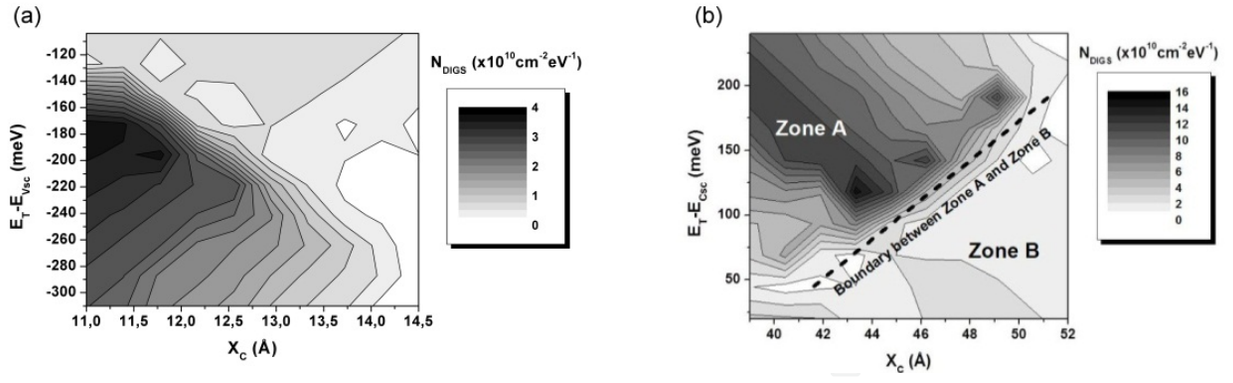

Figure 29. Contour plots of DIGS density obtained to 400 ºC-30 min. annealed Al/HfO_2/p-Si (oxide grown at 450 ºC) and Al/$HfSi_xO_y$/n-Si (silicate grown at 400 ºC)

4.4. Al_2O_3

The importance of Al_2O_3 as an insulating dielectrics is due to its large band gap (8.8 eV), excellent stability when deposited over silicon and its amorphousness (Al2O3 is a good glass former). We have studied Al/Al_2O_3/n-Si structures grown by atomic layer deposition at temperatures ranging from 300 ºC to 800 ºC. $AlCl_3$ and H_2O were used as precursors. DIGS

states densities are listed in Table 2. The measured value is similar in all samples, but non measurable at 500 ºC. It is possible that Al_2O_3 grown at this temperature is free of residual defects and moreover, the amorphousness, high purity and structural homogeneity achieved cause low defect densities, making the conductivity signal difficult to measure. In Figure 30 one can see the contour plot corresponding to the sample grown at 300 ºC. The shape is similar to HfO_2 sample deposited on n-Si, but in the case of Al_2O_3 the maximum density appears near the interface which might cause faster defect detrapping. The highest quality sample in terms of DIGS states is that grown at 500 ºC, but if we consider also interface states densities obtained for these samples [62] the best sample would be that grown at 300 ºC. It is important to consider both D_{it} and DIGS densities before concluding the quality of the samples.

Growth temperature	**Maximum DIGS ($\times 10^{10}$ cm^{-2} eV^{-1})**
300	12
400	19
500	Undetectable
600	15
800	25

Table 2. DIGS densities obtained to Al/Al_2O_3/n-Si structures grown at different temperatures.

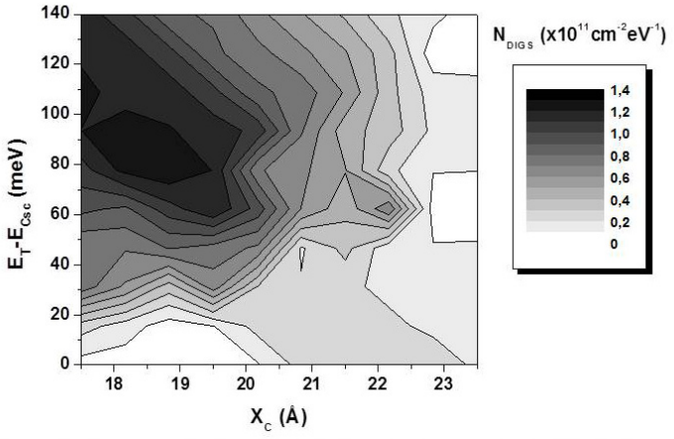

Figure 30. Contour plot of DIGS density obtained to Al/Al_2O_3/n-Si (oxide grown at 300 ºC).)

4.5. TiO_2

TiO_2 is being extensively studied for memory and logic applications, because of its high dielectric constant, ranging from 40 to 86. We have studied TiO_2 atomic layer deposited on etched n-silicon and high-pressure reactive sputtered over SiO_2–covered Si. DIGS state densities and other growth parameters are listed in Table 3. All ALD samples have been annealed at 750 ºC, so the only differences are growth temperature and chemical precursors. H_2O seems to be more adequate as a precursor than H_2O_2 for the two grown temperatures. On the other hand, when titanium precursor is $Ti(OC_2H_5)$, carbon remains uniformly distributed in the film bulk [63]. In contrast, when $TiCl_4$ is used, chlorine remains in the film and accumulates near the interface [64]. Because of that, higher D_{it} and lower DIGS values

are seen in the films grown with $TiCl_4$. To compare with the previous results, we grew TiO_2/SiO_2 dielectric thin films stacks on n-type silicon substrates. A 7 nm layer of SiO_2 was deposited by an Electron Cyclotron Resonance (ECR) oxygen plasma oxidation. Afterwards, 77.5 nm TiO_2 films were grown in an HPRS system at a pressure of 1 mbar during 3 hours and at a temperature of 200ºC. Finally, some samples were *in situ* annealed in oxygen atmosphere at temperatures ranging from 600 to 900ºC. Sputtered films exhibit lower DIGS densities, but the large band gap buffer layer (SiO_2) interposed between substrate and TiO_2 inhibits trap displacements from the interface to the dielectric bulk.

Figure 31 shows two contour maps corresponding to ALD sample grown from TiO_2 (Figure 31(a)) and to sputtered (600 ºC annealed) sample (Figure 31(b)). Defects are located closer to the interface in ALD films because the wider band gap SiO_2 interface layer is not present in this case.

4.6. Other materials: Mixtures

Mixtures, ternary or quaternary oxides are also studied in order to find replacement for SiO_2. Aluminum is a good glass former, so it can induce other dielectric layers to be amorphous, but at the expense of reducing the dielectric film permittivity. To avoid this fact, niobium is also mixed with dielectrics, due to its high permittivity. We have studied Hf-Al-O, Zr-Al-O, Hf-Al-Nb-O and Zr-Al-Nb-O mixtures.Ta_2O_5 layers have also been compared to Ta-Nb-O mixture. All these materials can be grown by ALD on p-silicon, using chlorides as precursors of hafnium and zirconium, $Al(CH_3)_3$ as aluminium precursor, and ethoxides for niobium and tantalum. Table 4 shows DIGS densities of these dielectric layers. In all cases niobium possibly acts as a barrier which inhibits trap displacement from the interface: in fact interface state densities are larger when Nb is incorporated and at the same time, DIGS state densities are reduced [65, 66]. Hf-Al-O behaves like Zr-Al-O due to the similarity between hafnium and zirconium. DIGS density for Ta_2O_5 has an intermediate value (~ 10^{11} cm^{-2} eV^{-1}), as seen in the contour plot in Figure 32. By comparing this plot with $Al/HfO_2/p\text{-}Si$ plot, we realize that maximum DIGS reach deeper locations and lower energies for Ta_2O_5. This can be explained in terms of the larger valence band offset for HfO_2 or ZrO_2 with respect to Ta_2O_5.

TiO_2 atomic layer deposited over n-Si		
Precursors	T_G (ºC)	Maximum DIGS ($\times 10^{11}$ cm^{-2} eV^{-1})
$Ti(OC_2H_5)$, H_2O	275	0,1
$Ti(OC_2H_5)$, H_2O_2	225	3,5
$Ti(OC_2H_5)$, H_2O_2	275	1
$TiCl_4$, H_2O	225	2

TiO_2 sputtered over SiO_2	
Annealing	Maximum DIGS ($\times 10^{11}$ cm^{-2} eV^{-1})
No	Not detected
600 ºC	0,5
700 ºC	2,6
800 ºC	1,2
900ºC	Not detected

Table 3. DIGS densities obtained to TiO_2 deposited over n-silicon and over SiO_2

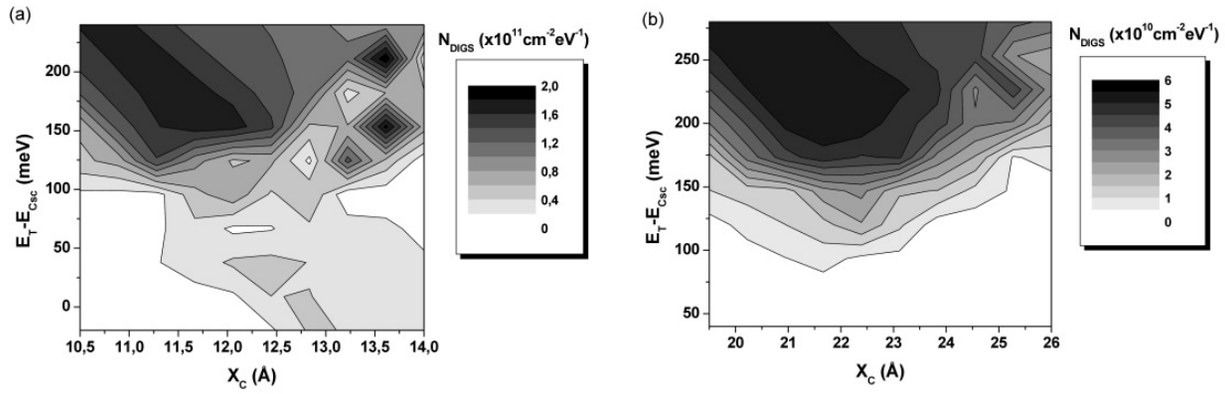

Figure 31. Contour plots of DIGS density obtained to ALD TiO_2 sample grown at 225 ºC from $TiCl_4$ on etched silicon (a) and TiO_2 sputtered on SiO_2–covered silicon (600 ºC annealed) (b).

	Maximum DIGS (x10^9 cm^{-2} eV^{-1})
Hf-Al-O	1200
Hf-Nb-Al-O	2
Zr-Al-O	2000
Zr-Nb-Al-O	Not detected
Ta_2O_5	120
Ta-Nb-O	Not detected

Table 4. DIGS densities obtained for different high-k dielectric mixtures

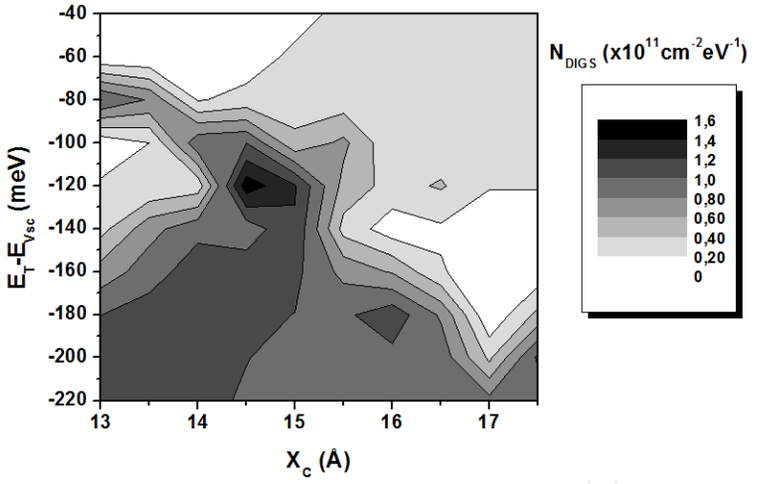

Figure 32. Contour plot of DIGS density obtained to Al/Ta_2O_5/p-Si (oxide grown at 300 ºC).

5. Conclusions and future trends

In this chapter we review several experimental techniques which allow detecting, measuring and identifying traps and defects in metal insulator interface, and at the bulk of the dielectric. The correlation between conduction mechanisms, defect location and preferential energy values provides very relevant information about the very nature of defects and, eventually, how these defects could be removed or diminished. Our techniques

provide high resolution in two dimensions: defect energy (E) and depth relative to the interface (z). In the future, we want to combine these techniques with scanning probe microscopy in order to obtain high resolution in lateral dimensions (x,y) as well.

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