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Using Numerical Simulations to Study and Design Semiconductors Devices in Micro and Nanoelectronics

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1. Introduction

The survival of the integrated circuits(ICs) industries is directly linked to its ability to innovate in terms of the developing new semiconductor devices (planar and three-dimensional) and new manufacturing process technologies (Silicon-On-Insulator, etc), in theircapability to reduce the dimensions of semiconductor devices focusing on the increasing of integration capability of the devices into a single integrated circuit (IC) and in their efficiency to develop new digital and analog ICs applications to attend the market in different forms of consumption. In this context, the numerical simulators represent a very important role for the ICs industries and very high investments have been done in this area of the process and device simulation tools (Technology Computer-Aided Design, TCAD) in order to use the computer simulations to develop and optimize semiconductor processing technologies and devices [1-2].

Significant costs reductions can be achieved through the use of numerical simulators for developing new semiconductor manufacturing technologies and devices that are associated with ICs industries. Thinking on developing new devices, the numerical simulations are able to supply a lot of information about the devices in terms of theirs electrical characteristics curves (drain current as a function of gate voltage for the MOSFETs, etc) and mainly in terms of the internal electrical and physical behaviors of the semiconductor devices (current density, electric field density, potential distribution along of the device structure, mobile carriers density along of the channel width and length of a MOSFET, etc) previously to the physical implementation, which is impossible to be obtained, visualized and understood with only the electrical characterization of the physical devices [1-2]. The involved costs with numerical simulations are associated mainly with human resources and infra-structure (hardware and software) while that, if new devices developing were

associated only with the manufacturing process use, would involve very high production costs, very high lead time and many uncertainties about the efficiency of the proposed devices [1-2].

Currently there is two-pronged research in the world focusing on developing new semiconductor devices [3]. The first one is based on designing of the new tridimensional (3D) devices, such as the multi-gates MOSFETs (FinFETs, Three-gates, Four-gates, Surrounding-gate) that involve high cost and investments related to the new techniques of ICs manufacturing process andnew materials. The other tries to explore the many real improvement opportunities of the current planar ICs manufacture technology. One of them, it is to use the "drain/source and channel region interface engineering" (D/SCRIE) approach [4-6], where it can implement new and innovative layout styles with non-conventional geometries, focusing on enhancing the device performance and consequently the performance of analog and digital ICs applications [4-7]. An example is very promising of this layout approach is the "Diamond MOSFET" that it was carefully and specially designed to improve the longitudinal (parallel) electric field ($\vec{\varepsilon}_{//}$) in order to increase the mobile carriers drift velocity in the channel region ($\vec{v}_{//}$) and consequently the drain current (I_{DS}), transconductance (g_m) and to reduce the on-state drain/source series resistance (R_{DS_on}) by a simple changing of the gate geometry from the conventional (rectangular) to hexagonal, as illustrated in Figure 1, showing an example of a SOI nMOSFET3D structure [4-7].
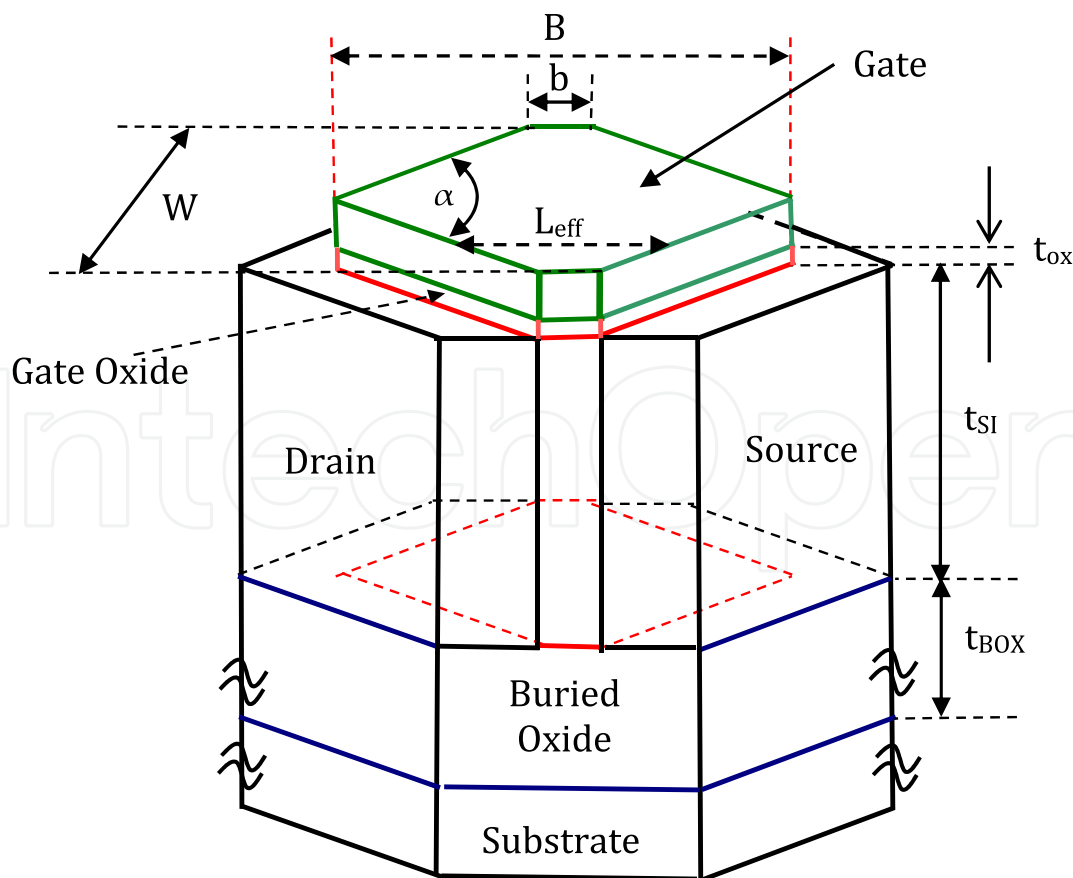

Figure 1. Example of a SOI nMOSFET 3D structure.

In Figure 1, the shorter and longer channel dimensions are represented by b and B, respectively, W is the channel width and L_{eff} is the effective channel length, α angle is the angle of the drain/channel and the channel/source interfaces due to hexagonal gate geometry, t_{ox}, t_{SI} and t_{BOX} are gate oxide, silicon film and buried oxide thickness, respectively.

Figure 2 presents the Diamond SOI nMOSFET layout style, where the longitudinal corner effect (LCE) acting in the point P in the channel is shown and the resultant longitudinal electric field ($\vec{\varepsilon}_{//}$) is given by the vector sum of the longitudinal electric field components ($\vec{\varepsilon}_{//1}$ and $\vec{\varepsilon}_{//2}$). Last is higher than the one observed in the conventional SOI nMOSFET counterpart. These longitudinal electric field components ($\vec{\varepsilon}_{//1}$ and $\vec{\varepsilon}_{//2}$) are generated by the drain bias (V_{DS}) and are perpendiculars to the metallurgical junctions of the drain/silicon film (channel region) [4-7].

The effective channel length (L_{eff}) of the Diamond SOI nMOSFET is given by the equation (1).
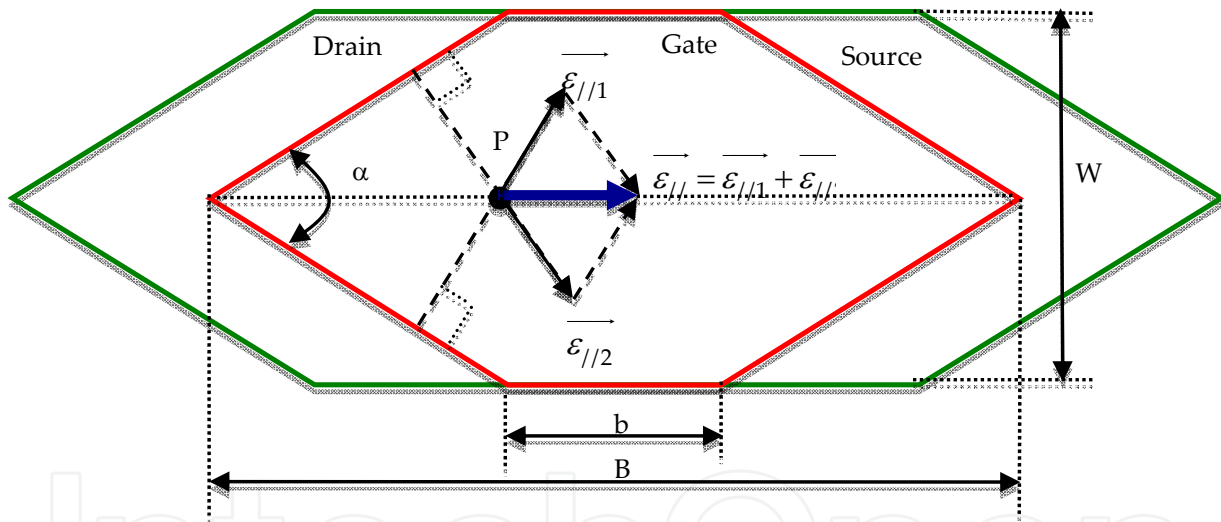
$$L_{eff} = \frac{B+b}{2} \tag{1}$$

Figure 2. Example of a SOI nMOSFET 3D layout showing the LCE acting in the point P.

In this structure, the resultant longitudinal electric field ($\vec{\varepsilon}_{//}$) in the center of the gate region is higher than the one observed in the edges of the gate region, due to the higher interaction between the longitudinal electric field components ($\vec{\varepsilon}_{//1}$ and $\vec{\varepsilon}_{//2}$) in the center of the device (LCE) [4-7] than the one found in the edges of the gate region, and therefore the drain current tends to flow more in the center of the gate region than in the edges of the gate region. Besides that, the Diamond structure can be electrically represented by the parallel association of the N transistors, where the channel width of each transistor of this parallel association is given by W/N and the channel length of these transistors varies from b to B. As a consequence of this last feature, the drain current tends to flow more by the edges than by the center of the gate region. This effect is defined here

by "Variable Channel Lengths of Transistors Associated in Parallel Effect" (VACLETAPE). So, in the Diamond structure occurs two effects at the same time, i.e., the LCE and the VACLETAPE generating a Diamond drain current higher than the one observed in the conventional (rectangular) SOI nMOSFET counterpart, regarding the same gate area (A_G) and bias conditions.

2. Devices used to perform the study

So, in order to qualify and quantify the benefits of Diamond layout style to improve the transistor performance, it were implemented three pairs of SOI nMOSFETs, being three Diamond transistors with different α angles and other three conventional SOI nMOSFETs counterparts, regarding the same gate area (A_G). Table I presents the devices dimensions used to implement these devices in the DevEdidt3D from (TCAD/Silvaco Inc) [8]. A similar TCAD to implement devices is the Sentaurus Structure Editor of the Synopsys, Inc [9].

Conventional SOI nMOSFET				Diamond SOI nMOSFET			
#	W (μm)	L (μm)	W/L	#	b (μm)	B (μm)	α (°)
CSM1	6.0	7.0	0.86	DSM1	1.0	13.0	53.1
CSM2	6.0	4.0	1.50	DSM2	1.0	7.0	90.0
CSM3	6.0	2.5	2.40	DSM3	1.0	4.0	126.9

Table 1. Devices Dimensions used to the study.

The constructive characteristics of these devices are: gate-oxide (t_{ox}), silicon-film (t_{SI}) and buried-oxide (t_{BOX}) thickness are 2 nm, 100 nm and 400 nm, respectively, and drain/source and channel doping concentrations are 5.5×10^{17} cm^{-3} and 1×10^{20} cm^{-3}, respectively.

3. Three-dimensional simulations results

The ATLAS (Device Simulation Software) [9] was used to perform the 3D numerical simulations of the Diamond and Conventional SOI nMOSFETs. The curves of I_{DS} versus gate voltage (V_{GS}) and I_{DS} versus drain voltage (V_{DS}) were obtained. Based on these curves, the main parameters of these devices were extracted and compared in order to verify the advantages and disadvantages of the Diamond layout style in relation to the conventional one counterpart.

Basically, the ATLAS device simulator uses two files inputs: the first one is the text file that contains commands for the ATLAS. Usually, these commands are to include a file that define the devices structure (usually built by using DevEdit3D [8]), to define the dimensions, the terminals and the meshof the structure of the device. The second one is responsible to define the physic phenomenon models (mobility, band width, impact ionizations, etc), the solution methods and the bias commands of the terminals that must be taking in account in the simulation of the device [1].

Besides that, ATLAS generates three types of output files. The first one is the "run-time output file" that provides all the error and warning messages. The second one is the "log files", which store allterminal voltages and currents of the device [direct current (DC), small signal alternate current (AC) and transient] generated the command SOLVE. This last file can be seen with the TonyPlot (visualization tool) to visualize the electrical behavior of the device. The last one is the "solution files", and it is responsible to stores the two-dimensional and three-dimensionaldata of the solution variables within the device for a single bias point (electric field, potential, etc.). This last file can be visualized by the use of TonyPlot too [1].

The following models are used to perform the 3D numerical simulations of the devices: I. Lombardi's vertical and horizontal electric-field-dependent mobility model, which includes effects of low (surface acoustic phonon scattering, optical inter-valley scattering and surface roughness) and high (Thonber's drift velocity model to calculate the velocity saturation) electric field; II. The Aurora model takes into account mobility degradation due to the lattice temperature; III. The Fowler-Nordheim Tunneling (electron and holes) model considersthe tunneling of electrons from the semiconductor Fermi level into the insulator conduction band, when high electric field across the gate is applied; IV. The Lucky-Electron Hot Carrier Injection model, considers the electrons emissions into the oxide by first gaining enough energy from the electric field in the channel to surmount the insulator/semiconductor barrier [1].

Figure 3 presents the three-dimensional numerical (3D) simulations results of the DSMs and CSMs I_{DS} as a function of V_{GS},for V_{DS} equal to 10 mV (Triode Region).
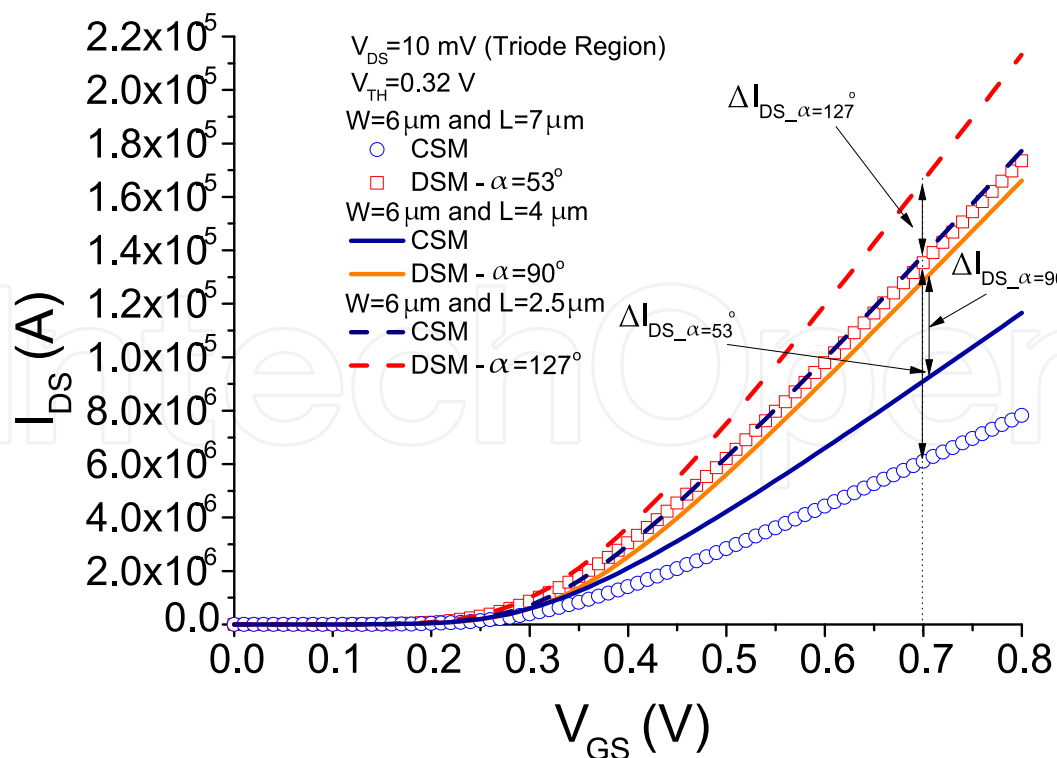

Figure 3. Curves of three-dimensional numerical simulations of the I_{DS} as a function of V_{GS} for V_{DS}=10mV.

In Figure 3, $\Delta I_{DS\_\alpha=127^o}$, $\Delta I_{DS\_\alpha=90^o}$ and $\Delta I_{DS\_\alpha=53^o}$ are respectively the differences between the I_{DS} of the DSMs with different α angles (127°, 90° and 53°) and the respective CSMs counterparts.

By analyzing the Figure 3, considering the same A_G and bias conditions in the Triode Region, it can be observe that DSMs I_{DS} with α angles equals to 127°, 90° and 53° are respectively 20.3 %, 37.2 % and 126.5 % (2.26 times) higher than those observed in the CSMs counterparts and these differences decreaseswhile the DSM α angle increases, due the two effects existents in the Diamond SOI nMOSFET (LCE and VACLETAPE). So, this innovative layout style can be used to increase the fun-out and fun-in capability of the logic gates.

Figure 4 presents the three-dimensional numerical (3D) simulations results of the DSMs and CSMs g_m as a function of gate voltage (V_{GS}),for drain voltage (V_{DS}) equal to 10 mV.
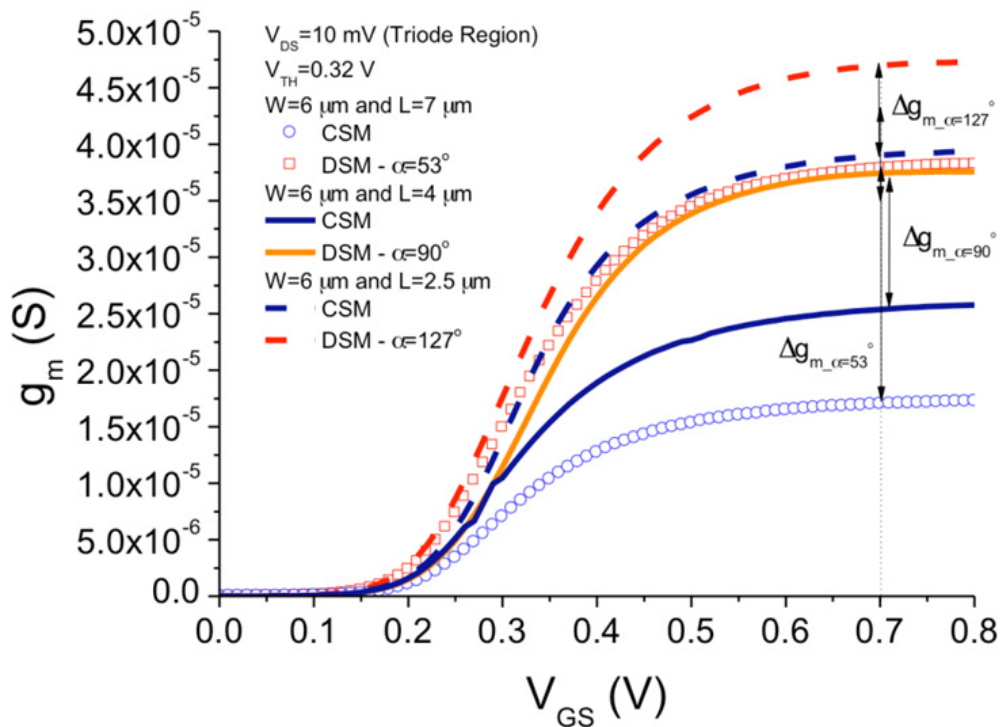

Figure 4. Curves of three-dimensional numerical simulations of the g_m as a function of V_{GS} for V_{DS}=10 mV (Triode Region).

In Figure 4, $\Delta g_{m\_\alpha=127^o}$, $\Delta g_{m\_\alpha=90^o}$ and $\Delta g_{m\_\alpha=53^o}$ are respectively the differences between the g_m of DSMs with different α angles (127°, 90° and 53°) and the respective CSMs counterparts.

Basing on Figure 4, we can see that, DSMs g_m with α angles equals to 127°, 90° and 53° are respectively 20.5 %, 47.6 % and 122.9 % (around 2.23 times) higher than those verified in the CSM counterparts and these differences also decreaseswhile DSM α angle increases, due the LCE and VACLETAPE,considering the same A_G and bias conditions.So, this Diamond structures can be used to improve significantly the voltage gain (A_V) and unit voltage gain frequency (f_T) of the amplifiers used in analog ICs.

Figure 5 presents the three-dimensional numerical (3D) simulations results of DSM (α=53°) and CSM counterpart Log(I_{DS}) as a function of gate voltage (V_{GS}),for drain voltage (V_{DS}) equal to 10 mV.

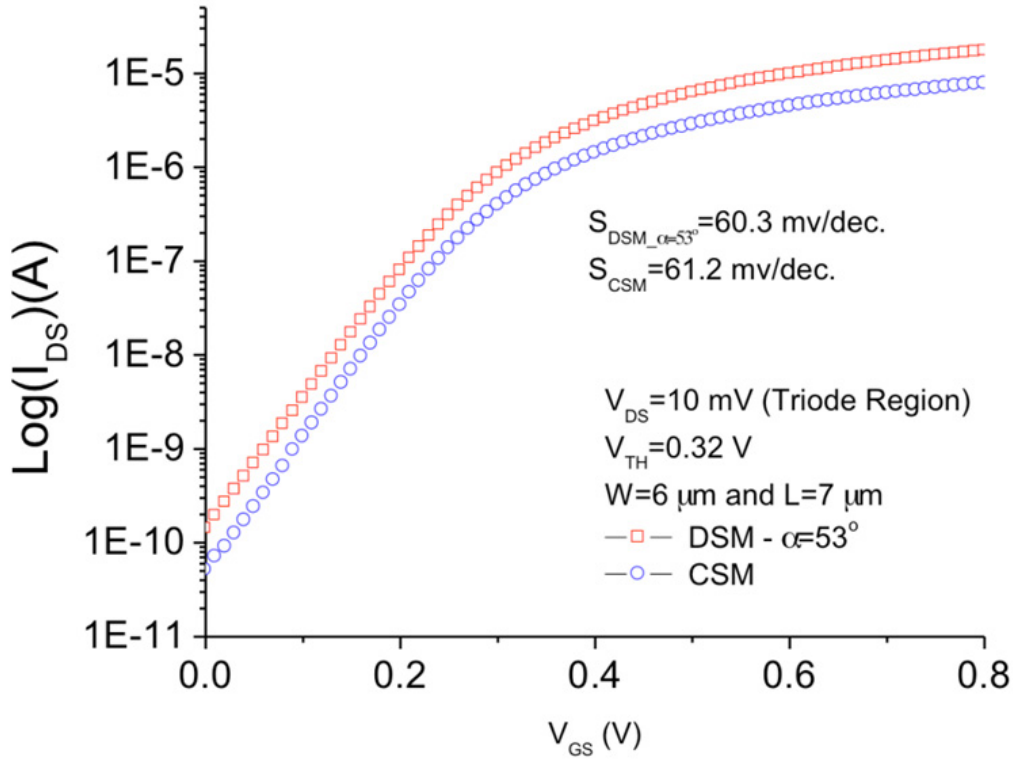**Figure 5.** Curves of three-dimensional numerical simulations of DSM (α=53°) and CSM Log(I_{DS}) as a function of V_{GS} for V_{DS}=10 mV.

Analyzing Figure 5, we can see that the subthreshold slopes (S) from of the both devices are practically similar around 60 mV/decade. Similar results are found to the others devices studied.

Figure 6 presents I_{DS} as a function of V_{DS} with V_{GS} equal to 0.4 V in the saturation region to DSM with α angles equals to 127° (Figure 6.a), 90° (Figure 6.b) and 53° (Figure 6.c) respectively.

Analyzing Figure 6, it is possible toobserve that always the I_{DS} in saturation region (I_{DSsat}) of all DSMs with different α angles are higher than those found in the CSMs counterpart, considering the same A_G, geometric factor and bias conditions. Besides that, I_{DS} of DSMs with α angles equals to 127°, 90° and 53° is higher 27%, 52% and 284% (1.84 times) than those observed in CSMs counterparts. This can be justified because of LCE and VACLETAPE effects present in the Diamond structure. Additionally, itcan see that DSMs Early voltages (V_{EA}) are strongly degraded in relation to CSMs counterparts, due to the high resultant longitudinal electric field in the drain region of the Diamond structures, as for example, DSM (α=53°) V_{EA} is approximately equal to 5V while CSM counterpart V_{EA} is approximately equal to 36V (around seven times smaller) and therefore can limit the use of this device to the output stages of analog ICs.
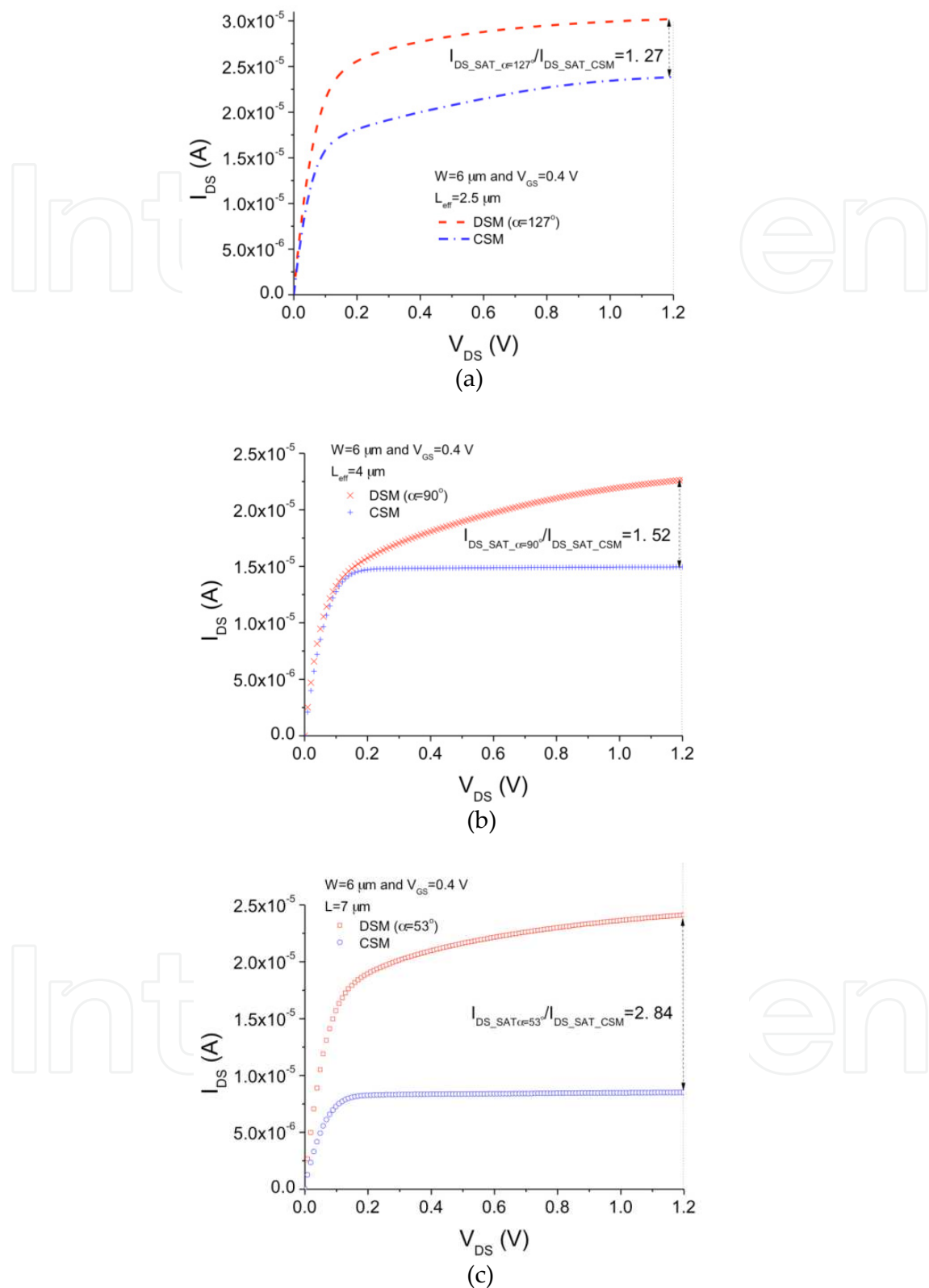
(a)

(b)

(c)

Figure 6. Curves of three-dimensional numerical simulations of I$_{DS}$ as a function of V$_{DS}$ for V$_{GS}$=0.4 V (saturation region) for DSMs with different α angles [127° (Figure 6.a), 90° (Figure 6.b) and 53° (Figure 6.c)and CSMs counterparts.

The on-state series resistance (R_{DS_on}) can be extracted from the Figure 6 in the linear region of the triode region. So, notice that, DSMs with different α angles R_{DS_on} are always higher than those observed in CSMs counterparts, as for example, DSM (α=53°) R_{DS_on} is around 82% (6 KΩ) smaller than the one found in CSM counterpart (110 KΩ) and therefore, by using DSM counterpart instead CSM, we can improve significantly the processing clock velocity of digital ICs.

4. Electrical and physical analysis

In order to understand the electrical and physical behavior of the Diamond structure in relation the to conventional one counterpart, the longitudinal electrical field vectors picture was extracted of DSM (α =90°) and CSM counterpart structures, regarding V_{GS} and V_{DS} equals to 0.4 V and 1.2 V, respectively, in saturation region, as illustrated in Figure 7.
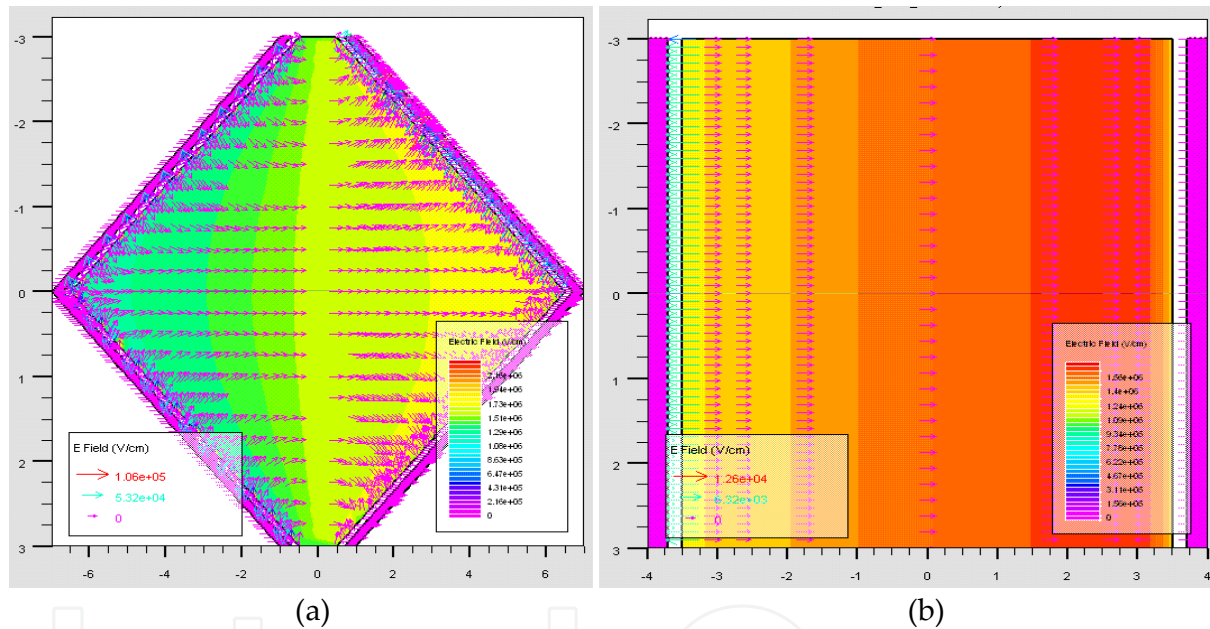

Figure 7. Vectors of the resultant longitudinal electric field of the DSM (α=90°) (Figure 7.a) and CSM counterpart (Figure 7.b) channel regions for V_{GS} and V_{DS} equal to 0.4 V and 1.2 V, respectively (saturation region).

With the use of TonyPlot3D (Silvaco Inc.) [1] and analyzing Figure 7, it is possible to see how is the behavior of DSM (α =90°) resultant longitudinal electric field ($\vec{\varepsilon}_{//}$) along of the channel length. Notice that, DSM (α =90°) resultant longitudinal electrical field ($\vec{\varepsilon}_{//}$) in the channel region edges (1.5×10^6 V/cm) is smaller than the one found in the center of the channel from of the middle of the channel length (2.0×10^6 V/cm), due to the smaller interaction between the longitudinal electric field components ($\vec{\varepsilon}_{//1}$ and $\vec{\varepsilon}_{//2}$) next to DSM edges regions. Besides that, it can beverify that DSM (α =90°) average resultant longitudinal electric field (1.9×10^6 V/cm) is higher than the one observed in CSM counterpart ($1.2.10^4$ V/cm), due to the presence of LCE and VACLETAPE in the Diamond structure.

Additionally, it is plotted a picture of the DSM (α =53°) total drain current density, considering V_{GS} and V_{DS} equals to 0.4 V and 1.2 V, respectively, in saturation region, as illustrated in Figure 8.
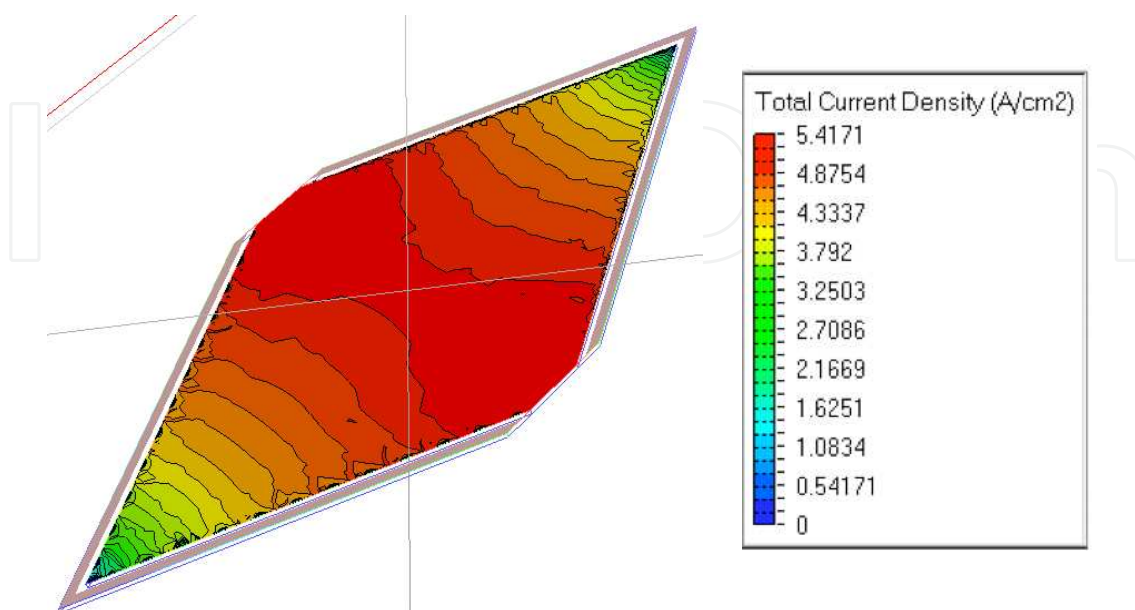

Figure 8. Curves of the total drain current density of DSM (α=53°) (Figure 8.a) and CSM counterpart (Figure 8.b) channel regions for V_{GS} and V_{DS} equal to 0.4 V and 1.2 V, respectively (saturation region).

Figure 8 shows that DSM (α =90°) total drain current density is higher in the center of the channel region than in the vertices (source/drain and channel regions interfaces) of the device, indicating that this layout style can be evolved to the octagonal gate geometric [10].

5. SOI MOSFEts investigationat high temperatures

Today, there are much electronic equipments that operate under high-temperature environment (from room temperature up to 300°C) such as avionics, automotive, aircrafts, spacecrafts, ships, train, among other [11-13], where conventional (bulk) CMOS integrated circuits can operate satisfactorily at moderate temperatures (up to 150°C), but when the temperature increses beyond this, the devices present failures arising the threshold voltage reduction and excessive drain leakage current increases [14-18].

Fortunately, thanks to the advantages of SOI CMOS technology, especially at high temperatures, their applications at high temperatures can be extended up to 300°C, where its electrical performance is less impaired than the one found in the conventional MOSFETs [18-20].

In this context, the drain leakage current (I_{DLeak}) of the Diamond SOI nMOSFET (DSM) is analyzed from room temperature up to 300°C by the three-dimensional numerical simulator ATLAS [1]. The DSM I_{DLeak} results are then compared to the one found in the SOI MOSFETs (CSM) counterpart, taking into account the same die area, geometric factor and bias and temperature conditions.

6. Three-dimensional numerical simulations results at high temperatures

To analyze DSM operating at high temperatures, from room temperature up to 300°C, CSM and DSM with different α angles are implemented by using DevEdit3D [8].

In order to investigate I_{DLeak} behavior, it is necessary to extract the I_{DS} as a function of V_{GS} curves, at high temperatures. Once I_{DLeak} is obtained in the subthreshold region. In this study, I_{DLeak} is extracted considering V_{GS} equal to -0.5V, as it can be seen in Figure 9, for different temperatures (27°C, 100°C, 200°C and 300°C) and for all devices under evaluation in this work.
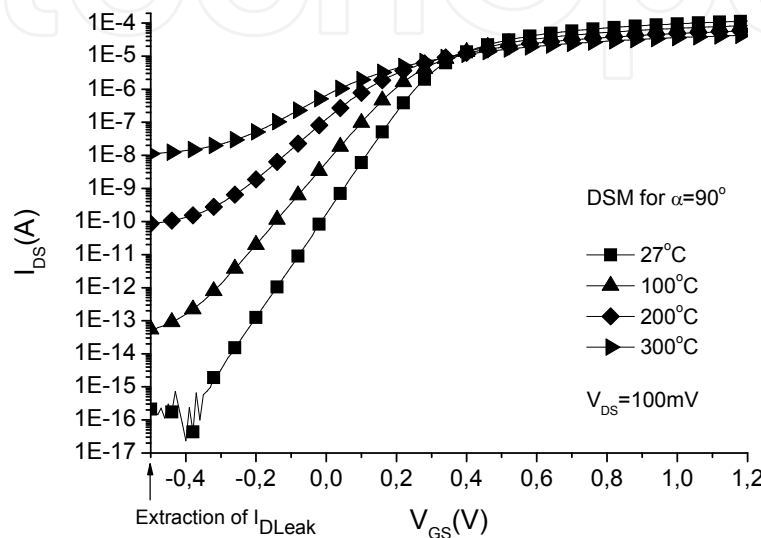

Figure 9. DSM (α=90°) Log(I_{DS}) as a function of V_{GS} with V_{DS} equal to 100 mV, considering different temperatures.

Figure 10 shows some results concerning I_{DLeak} as a function of the temperature, considering DSM with different α angles and the CSMs counterparts, operating at same bias and temperature conditions.
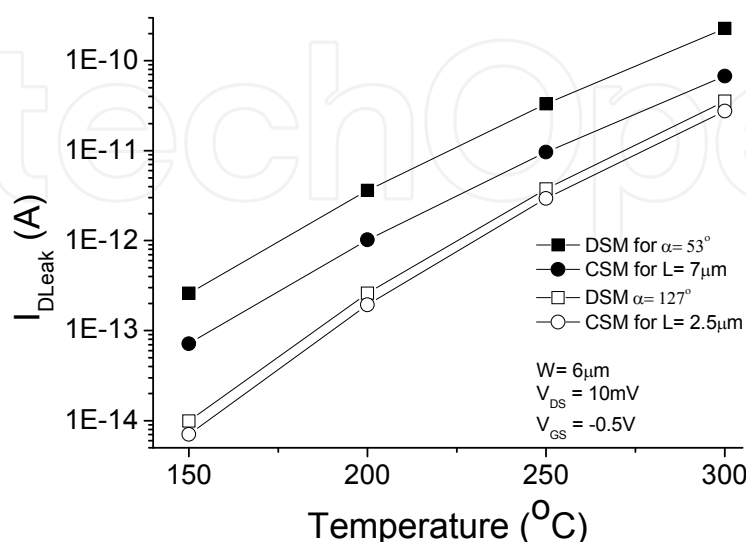

Figure 10. DSM and CSM counterpart I_{DLeak} as a function of the temperature.

From Figure 10, it is possible to observe that, as the temperature increases, I_{DLeak} also increases, as expected [11]. Besides that, I_{DLeak} is higher in DSM when compared to CSM devices, independently of the αangle and the temperature. It happens since the longitudinal electric field is higher in DSM when compared to CSMs and consequently, its drain leakage current (I_{DLeak}) is also larger. On the other hand, it worthwhile to describe that as α reduces, I_{DLeak} difference observed between both devices becomes higher. As for example, when αis equal to 127°, DSM I_{DLeak} is 20% higher than the one observed in the CSM counterpart (L= 2.5μm) for V_{GS}=-0.5 V, but providing an I_{DS} also 20% more than rectangular gate transistor, for V_{GS}=1.2V. These increasing proportions between I_{DLeak} and drain currents are maintained for all equivalent devices, i.e., for α = 53° and 127°.

Figure 11 shows DSM I_{DLeak} behavior as a function of the angle α. It is important to comment that this comparison is possible once I_{DLeak} is normalized with the geometric factor (W/L), thus providing a more realistic comparison of I_{DLeak} as α changes. Then, analyzing the results it is possible to observe that, for the same temperature, as α increase, I_{DLeak} becomes smaller. Otherwise, for the same α, I_{DLeak} also increases according to the temperature rises.
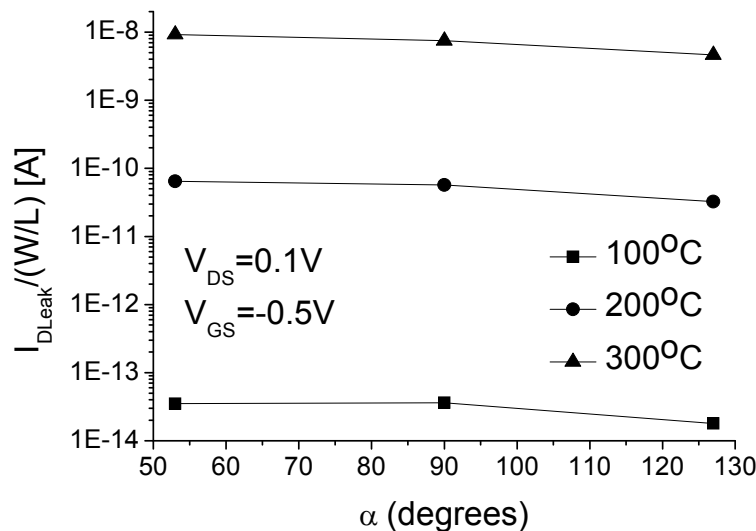

Figure 11. Diamond SOI nMOSFET I_{DLeak} behavior as a function of α, at high temperatures.

Anyway, for both CSM and DSM, I_{DLeak} increases when the temperature increases in the same proportion,mainly due to the thermal generation process [15], but in DSM I_{DLeak} is higher because the longitudinal electric field along the DSM channel length is higher than the one present in its CSM counterpart.

7. Conclusions

Comparative studies between Diamond SOI MOSFETs and Conventional ones counterparts by numerical simulations demonstrate that Diamond layout style can improve current drive, transconductance, on-state series resistance, frequency response (voltage gain and unit voltage gain frequency) when it is compared to the Conventional counterpart, considering the same gate area, geometry factor (aspect ratio) and bias conditions.

By using Diamond layout style, instead rectangular gate geometry, the die area of analog integrated circuits can be significantly reduced since the drain current of the Diamond structure is higher than the one observed in the Conventional counterpart, considering the same gate area, geometry factor (aspect ratio) and bias conditions.

Therefore, the Diamond layout style becomes an important device alternative to improve the performance of the transistors and consequently the performance of the analog and digital ICs.

This temperature studyin the Diamond layout structure shows the drain leakage current behavior in the Diamond SOI MOSFETs, in comparison to the conventional one counterpart, regarding these devices operating since room temperature (27°C) up to 300°C. From this investigation it is observed that I_{DLeak} in Diamond SOI MOSFETs is higher than the one observed in Conventional devices operating at same bias and temperatures conditions, because the longitudinal electric field along the Diamond channel length is higher than the one found in the conventional counterpart. On the other hand, the DSM drain current is increased in the same proportion of I_{DLeak}, regarding to the same die area, geometric factor and bias and temperature conditions. So, these results show that also it is possible to analyze and investigate the behavior of devices at high temperatures, through three-dimensional numerical simulations, in order to predict its performance in harsh environments before submit them in such real operation conditions, and thus, even get additional information to improve the design/performance of the ICs in harsh temperature conditions. Therefore, Diamond layout style I_{DLeak} (35 pA and 228 pA for α equals to 127° and 53°, respectively) presents practically the same magnitude order than the one observed in the CSM counterpart (67 pA and 28 pA for α equals to 127° and 53°, respectively) at 300 ^{o}C and therefore when it is used DSM instead of the conventional one, Diamond structure does not degrade the performance the battery time life of the portable electronics equipment operating in harsh (high temperature) environments.

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Acknowledgement

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