Chapter 12

Analytical Model and Numerical Simulation for the Transconductance and Drain Conductance of GaAs MESFETs

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Additional information is available at the end of the chapter

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1. Introduction

The analytical model and simulation numerical of semiconductor devices is one of the important steps for Integrate Circuit fabrication, verification and characterization. Each semiconductor device has models that satisfies the requirements to the device under different operating conditions. GaAs MESFET is a promising semiconductor device used in many applications in the microwave domain. The elements which compose the MESFET transistors can be gathered in two distinct categories. There are extrinsic and intrinsic elements; the first category represents the different structures of access like the side resistances *Rs* and *Rd*. The intrinsic elements like the transconductance g_m and drain conductance g_d translate by their nature and their behavior localized of the device physical structure. Our main aim in these sheets related on the one hand to the optimization of a two dimensional (2D) analytical model for the static characteristics of short gate-length GaAs MESFET's, this model takes into account the different physical specific phenomena of the device, and on the other hand to calculate the variation of some intrinsic elements (transconductance and drain conductance) as a function of the biasing voltages. The model suggested has enables to us to calculate and trace the different series from curves. The results obtained are well represented and interpreted.

2. General characteristics of the model

The major features of this study are:

To solve the system of the two dimensional partial differential equations, we based for the works of Chin and Wu (1992, 1993), the Green's function technique is used in these

references to solved the two dimensional Poisson's equation, this technique gives an acceptable distribution of the space charge and a form of the depletion area in agreement with the physical phenomena specific to this device.

To determine the depletion-layer width, we have considered first the one-dimensional approximation (Sze and Ng, 2007), then we add the corrective which results from the two-dimensional analysis.

To determine the electron mobility law in the semiconductor, we have considered that described by Chang and Day (1989).

To calculate the drain current expression as a function of the drain-source and gate-source voltages, we divided the channel under the gate in regions (linear, non-linear and saturated) according to the electric field.

In order to simplify the mathematical study and consequently the numerical simulation, we used some assumptions and approximations.

To determine the *I-V* extrinsic characteristics in different operations regimes, we used the iterative method.

To determine the transconductance and drain conductance as a function of the drain-source and gate-source voltages in different operations regimes, we based also for the numerical simulation methods.

2. Analytical model

2.1. Determination of the potential under the gate

The potential distribution in the active layer under the gate is modeled by solving the Poisson's equation with proper boundary conditions, in two-dimensions this equation is given by:

$$\Delta\psi(x,y) = \frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon} \tag{1}$$

where $\psi(x, y)$ is the potential in the active-layer.
$\rho(x, y)$ is the density of the majority carriers in the channel.
ε is the dielectric permittivity of semiconductor.

If the channel doping is homogeneous, the activity area density is written

$$\rho(x,y) = \rho(y) = eN_d(y) \tag{2}$$

where $N_d(y)$ is the doping profile in semiconductor.

To simplify the study, one considers that this equation is a superposition of two simple equations. In this connection, one can write:

$$\psi(x,y) = U(y) + \varphi(x,y) \tag{3}$$

where

$$U(y) = \iint \frac{-eN_d(y)}{\varepsilon} dy^2 \tag{4}$$

and

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = 0 \tag{5}$$

In such a way, according to formula (3 – 5) the process of solving the initial Poisson's equation consists of looking-for of solution to one-dimensional equation (Eq. 4) and solving the two-dimensional equation (Eq. 5).

2.2. Boundary conditions

The above solution of the Poisson's equation has to verify the equations and boundary conditions expressed as:

$$\psi(x,0) = 0 \tag{6}$$

$$\psi(0,y) = Vb - Vg \tag{7}$$

$$\psi(L,y) = Vd + Vb - Vg \tag{8}$$

where Vg is the intrinsic gate-source voltage, Vd is the intrinsic drain-source voltage and Vb is the built-in voltage of the Schottky barrier.

If the drain voltage is equal to zero, the symmetry between the two gate-sides leads to the following condition:

$$\psi(0,y)\big|_{Vd=0} = \psi(L,y)\big|_{Vd=0} \tag{9}$$

At the first point of the pinch-off, the electron velocity attains its maximum and the electric field with drain side's corresponds to the saturation field E_S.

$$\left.\frac{\partial \psi(x,y)}{\partial x}\right|_{(L,a)} = E_S \tag{10}$$

The electric field must vanish in the depletion-layer edges at both gate-sides; this field may cause a large current flow. Therefore, it may be written:

$$E_{\vec{n}}\big|_S = 0 \tag{11}$$

and

$$E_{\vec{n}}\big|_D = 0 \tag{12}$$

where $\vec{n}$ is the outward unit vector at the depletion-layer edge.

2.3. 1D approximation

By integrating the equation (4) from *0* to *h (x)*, we determine the term *U (y)*, and one obtains:

$$U(h) = \frac{eN_d}{2\varepsilon} h(x)^2 \tag{13}$$

The one-dimensional depletion layer width h_X at any x coordinate is given by the one-sided abrupt junction depletion approximation (Sze and Ng, 2007).

$$h_X = \sqrt{\frac{2\varepsilon\left(V(x) + Vb - Vg\right)}{eN_d}} \tag{14}$$

where *V(x)* is the potential of the neutral channel with *V(0) = 0* at the source-end and *V(L) = Vd* at the drain-end. So that the one-dimensional depletion widths at the source and drain ends given respectively by:

$$h_S = \sqrt{\frac{2\varepsilon\left(Vb - Vg\right)}{eN_d}} \tag{15}$$

$$h_D = \sqrt{\frac{2\varepsilon\left(Vd + Vb - Vg\right)}{eN_d}} \tag{16}$$

2.4. 2D analytical model

To determine the second term, we based for the works Chin and Wu (1992, 1993), Jit et al. (2003, 2011) and Morarka and Mishra. (2005), these studies are used the Green's functions and superposition techniques. In the homogeneous medium, the solution suggested is written in the following form:

$$\varphi(x,y) = \left[A_1^S \frac{\sinh\left(k_1(L-x)\right)}{\sinh\left(k_1 L\right)} + A_1^D \frac{\sinh\left(k_1 x\right)}{\sinh\left(k_1 L\right)} \right] \sin\left(k_1 y\right) \tag{17}$$

where

$$k_1 = \frac{\pi}{2a} \tag{18}$$

$$A_1^S = Vp\left[a_1 + b_1 \left(\frac{Vb - Vg}{Vp} - c_1 \right)^{1/2} \right] \tag{19}$$

and

$$A_1^D = Vp\left[a_1 + b_1\left(\frac{Vd + Vb - Vg}{Vp} - c_1\right)^{1/2}\right] \tag{20}$$

A^{S}_1 and A^{D}_1 are the first term of Fourier coefficient for the excess sidewall potential at the source and drain sides of the gate respectively.

a_1, b_1 and c_1 are constants related to the device structure.

From (13) and (17), one obtains the expression of total tension $\psi(x, y)$:

$$\psi(x,y) = \frac{eN_d}{2\varepsilon}h^2(x)\left[A_1^S\frac{\sinh\left(k_1(L-x)\right)}{\sinh\left(k_1L\right)} + A_1^D\frac{\sinh\left(k_1x\right)}{\sinh\left(k_1L\right)}\right]\sin\left(k_1y\right) \tag{21}$$

2.5. Depletion-layer width

To calculate the two dimensional width of the depletion layer formed by the Schottky barrier W_X at any x coordinate, we have considered firstly the one-dimensional approximation h_X then we have added the corrective which results with the two-dimensional analysis. So the Eqs. (14 ~ 16) becomes respectively as follows:

$$W_X = \sqrt{\frac{2\varepsilon\left(V(x) + Vb - Vg - \varphi(x,h_X)\right)}{eN_d}} \tag{22}$$

$$W_S = \sqrt{\frac{2\varepsilon\left(Vb - Vg - \varphi(0,h_S)\right)}{eN_d}} \tag{23}$$

$$W_D = \sqrt{\frac{2\varepsilon\left(Vd + Vb - Vg - \varphi(L,h_D)\right)}{eN_d}} \tag{24}$$

where the correctives are determinate by:

$$\varphi\left(x,h(x)\right) = \left[A_1^S\frac{\sinh\left(k_1\left(L-x\right)\right)}{\sinh(k_1L)} + A_1^D\frac{\sinh\left(k_1.x\right)}{\sinh(k_1L)}\right]\sin\left(\frac{\pi}{2}\sqrt{\frac{Vb - Vg + V(x)}{Vp}}\right) \tag{25}$$

$$\varphi\left(0,h_S\right) = A_1^S\sin\left(\frac{\pi}{2}\sqrt{\frac{Vb - Vg}{Vp}}\right) \tag{26}$$

$$\varphi\left(L,h_D\right) = A_1^D\sin\left(\frac{\pi}{2}\sqrt{\frac{Vd + Vb - Vg}{Vp}}\right) \tag{27}$$

and the pinch-off voltage:

$$Vp = \frac{eN_d}{2\varepsilon} a^2 \tag{28}$$

2.6. The electron mobility law

For gallium arsenide GaAs, the analytical expression of the electron mobility dependence of the electric field which used in this study is a simplified mathematical relation (Chang and Day, 1989; Shin and Klemer 1992) given as follows:

For the feeble electric fields where $E < E_0$, the electrons are in thermodynamic balance with their mobility, the later is constant and independent of the electric field, in this connection:

$$\mu(E) = \mu_0 \tag{29}$$

As the electric field becomes more growth where $E \geq E_0$ the interactions of the carriers with the vibrations of the network involve a reduction in the mobility of the electrons. The law of this mobility in this case is given by:

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\frac{E - E_0}{E_C}\right)^2\right]^{\frac{1}{2}}} \tag{30}$$

where

$$E_C = \frac{v_S}{\mu_0} \tag{31}$$

$$E_0 = \frac{1}{2}\left[E_S + \left(E_S^2 - 4E_C^2\right)^{\frac{1}{2}}\right] \tag{32}$$

$$\left.\frac{dv(E)}{dE}\right|_{E=E_S} = 0 \tag{33}$$

2.7. I-V caractéristics

In general, it is possible that the channel current is expressed as a function of the intrinsic grille-source and drain-source voltages in terms of physical dimensions. The basic equation used to derive the *I-V* relationship (Sze and Ng, 2007) is given by:

$$Id = \frac{Zq^2 N_d^2 \mu(E)}{\varepsilon L} \int_{W_S}^{W_D} \left(a - W\right) W dW \tag{34}$$

By simple integration, *Id* becomes as:

$$Id = Ip\left[\left(u_D^2 - u_S^2\right) - \frac{2}{3}\left(u_D^3 - u_S^3\right)\right] \tag{35}$$

where

$$Ip = \frac{Zq^2 N_d^2 \mu(E) a^3}{2\varepsilon L} \tag{36}$$

$$u_D = \frac{W_D}{a} \tag{37}$$

$$u_S = \frac{W_S}{a} \tag{38}$$

u_D and u_S are the normalized dimensionless units.

The mobility law makes it possible to obtain the different expressions of the drain-current in the different operation regimes (linear, non-linear and saturated). Fig. 1 shows the structure of a MESFET with the channel under the gate. It can be divided in general into three regions (L_A, L_B and L_C) depending upon the magnitude of the electric field (Shin and Klemer, 1992; Khemissi et al. 2004, 2006). In the region L_A the electric field is below E_0, and the electron mobility is given by equation (29), region L_B correspond the electric field is between E_0 and E_S and the electron mobility is given by equation (30), the last L_C is the high field region in which the electric field exceeds E_S and the mobility is given by equation (30).

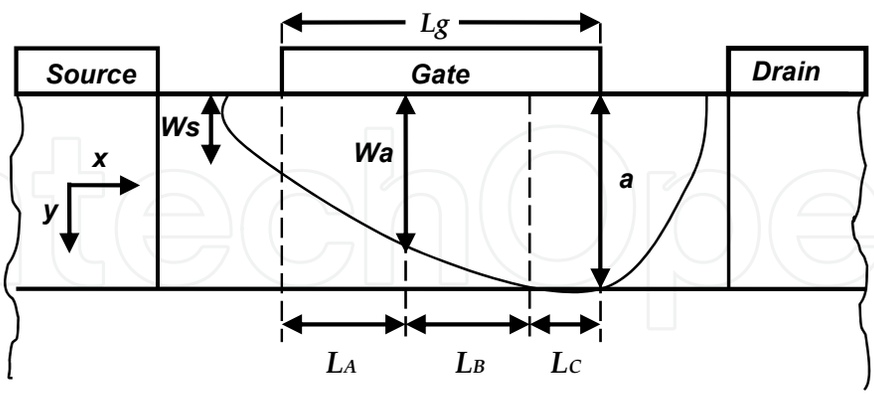

Figure 1. A cross-sectional view of a biased MESFET channel

2.8. Linear regime

This regime exists when the applied drain-source voltage is sufficiently low such that the electrical field under the gate is both smaller than E_0, the mobility is equal to μ_0 and the channel is described by L_A. The expression of the drain current in this regime is given by:

$$Id = Ip_0\left[\left(u_D^2 - u_S^2\right) - \frac{2}{3}\left(u_D^3 - u_S^3\right)\right] \tag{39}$$

where

$$Ip_0 = \frac{Zq^2N_d^2\mu_0 a^3}{2\varepsilon L} \tag{40}$$

2.9. Pinch-off regime

As the drain-source voltage increases, the electric field in the channel is not entirely below E_0. For this case, the channel under the gate consists of two regions: One of the lengths L_A with the field is below E_0 and the mobility is equal to μ_0. The other region of the length L_B with E is between E_0 and E_S and the mobility is given by equation (30). The expression of the current in this regime can be obtained by:

$$Id = Ip_0\left[\left(u_A^2 - u_S^2\right) - \frac{2}{3}\left(u_A^3 - u_S^3\right)\right] + Ipn\left[\left(u_D^2 - u_A^2\right) - \frac{2}{3}\left(u_D^3 - u_A^3\right)\right] \tag{41}$$

where

$$Ipn = \frac{Zq^2N_d^2\mu_0 a^3}{2\varepsilon L\left[1 + \left(\frac{E - E_0}{E_C}\right)^2\right]^{1/2}} \tag{42}$$

and u_A is the normalized dimensionless unit which corresponds to the drain bias equal to ($E_0.L$).

2.10. Saturation regime

As the electric field at the drain side becomes larger than E_S, the channel is divided into three regions: The first of the length L_A, the second of the length L_B and the last of the length L_C in which the depletion-layer reaches the interface between the activate area and the semi-insulator substrate. The expression of the current in this regime can be obtained by

$$Id = Ip_0\left[\left(u_A^2 - u_S^2\right) - \frac{2}{3}\left(u_A^3 - u_S^3\right)\right] + Ips\left[\frac{1}{3} - \left(u_A^2 - \frac{2}{3}u_A^3\right)\right] \tag{43}$$

where

$$Ips = \frac{Zq^2N_d^2\mu_0 a^3}{2\varepsilon L\left[1 + \left(\frac{E_S - E_0}{E_C}\right)^2\right]^{1/2}} \tag{44}$$

2.11. Effect of parasitic resistances

The characteristics which we have calculated are those of the intrinsic values (*Vg, Vd* and *Id*). To obtain the extrinsic characteristics (*Vgs, Vds,* and *Ids,*) of the device it is necessary to take into account the effect of parasitic resistances (*Rs, Rd* and *Rp*) and substitute the intrinsic terms by the extrinsic terms in all the previous expressions. In this case *Vgs, Vds* and *Ids* can be respectively expressed as

$$Vgs = Vg + RsId \tag{45}$$

$$Vds = Vd + RdId \tag{46}$$

$$Ids = Id + \frac{Vds}{Rp} \tag{47}$$

where *Rs* is the resistance of the region from the source contact to the source side of the gate, *Rd* is the resistance of the drain region outside the gate and *Rp* is the parallel resistance associated with the buffer layer.

It is obviously necessary to implement an iterative technique to obtain the extrinsic drain current *Ids* for given values of the gate-source and drain-source voltages *Vgs* and *Vds* respectively.

2.12. Transconductance and drain conductance

The expression of the intrinsic drain current "*Id*" makes it possible to determine the mathematical expressions of the transconductance and the drain conductance. When the transistor is polarized at a point of operation given by the biasing, the expression of the current "*Id*" can be written as follows:

$$dId = \frac{\partial Id}{\partial Vg} dVg + \frac{\partial Id}{\partial Vd} dVd \tag{48}$$

$$dId = g_m dVg + g_d dVd \tag{49}$$

The expression of the transconductance is defined by the equation:

$$g_m = \left.\frac{\partial Id}{\partial Vg}\right|_{Vd=cst} \tag{50}$$

And the expression of the drain conductance is given by the equation:

$$g_d = \left.\frac{\partial Id}{\partial Vd}\right|_{Vg=cst} \tag{51}$$

After simple derivations of the current drain expressions in the different operation regimes, one obtains the expressions of the transconductance and the drain conductance.

3. Numerical methods

3.1. Calculation of the drain current

To calculate the extrinsic characteristics *Ids (Vds, Vgs)*, one needs to put in consideration the effect of parasitic resistances, this effect which is not negligible, is very significant for the exactitude of the analytical model, but the problem of this type of models (model analytical) is that, the effect of parasitic resistances in the hand is requires to calculate the expressions of the drain current and on the other hand the mathematical relations which express this effect are determined also by the drain current. To solve this problem, are thus needed used a sophistical numerical methods. In this study, we used the iterative method represented by the following relations:

At the beginning, the initial extrinsic drain current *Ids* is considered equal to intrinsic current *Id*.

$$Ids^{(0)} = Id \tag{52}$$

Consequently, $$Ids^{(1)} = Ids^{(0)} + \Delta Ids^{(1)} \tag{53}$$

where: $\Delta\ Ids^{(1)}$ is on a side the difference between $Ids^{(1)}$ and $Ids^{(0)}$ and on the other side it results on the effect of parasitic resistances for $Ids = Ids^{(0)}$.

$$\begin{aligned} Ids^{(2)} &= Ids^{(1)} + \Delta Ids^{(2)} \\ &\cdot \quad \cdot \quad \cdot \\ &\cdot \quad \cdot \quad \cdot \\ &\cdot \quad \cdot \quad \cdot \\ Ids^{(n)} &= Ids^{(n-1)} + \Delta Ids^{(n)} \end{aligned} \tag{54}$$

The operation is stopped when: $$\Delta Ids^{(n)} = 10^{-3}\, Ids^{(n-1)} \tag{55}$$

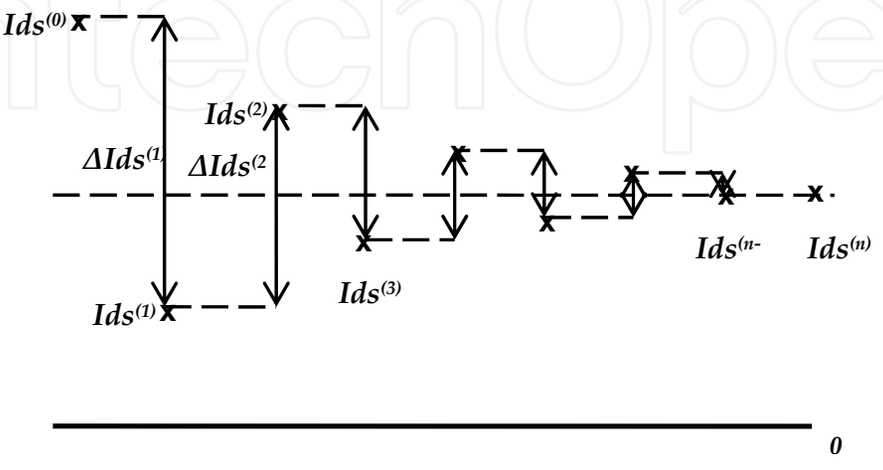

Figure 2. Diagram representative of the method

3.2. Calculation of transconductance and the drain conductance

The expressions of the transconductance and the conductance of drain are simple derivations of the drain current as a function as the drain and gate intrinsic voltages (Eqs. 50, 51), to obtain the values of these significant parameters, we based on numerical calculation as follows:

For the transconductance:

After the fixing of the drain voltage to the given value, the transconductance is obtained from the following relation:

$$g_m^{(k)} = \left.\frac{\Delta Ids^{(k)}}{\Delta Vg^{(k)}}\right|_{Vd=cst} = \left.\frac{Ids^{(k+1)} - Ids^{(k)}}{Vg^{(k+1)} - Vg^{(k)}}\right|_{Vd=cst} \tag{56}$$

where:

$$Vg^{(k+1)} - Vg^{(k)} = 0,01 \tag{57}$$

Same manner as the transconductance, the drain conductance is obtained after fixing of the gate voltage and after the following relation:

$$g_d^{(k)} = \left.\frac{\Delta Ids^{(k)}}{\Delta Vd^{(k)}}\right|_{Vg=cst} = \left.\frac{Ids^{(k+1)} - Ids^{(k)}}{Vd^{(k+1)} - Vd^{(k)}}\right|_{Vg=cst} \tag{58}$$

where:

$$Vd^{(k+1)} - Vd^{(k)} = 0,01 \tag{59}$$

4. Simulation results

In order to illustrate the exposed model, we elaborated simulation software based on different formulas and mathematical equations previously obtained and by using the numerical methods. The study carried out on a submicron gate length GaAs MESFET transistors which parameters shown in the table 1. The results obtained are exposed and interpreted in this section.

L (μm)	a (μm)	Z (μm)	Nd (At / cm^3)	μ_0 (cm^2/ Vs)	E_0 / Em
0,3	0,145	100	1,2. 10^{17}	3400	0,25
Rs (Ω)	Rd (Ω)	Rp (Ω)	a_1	b_1	c_1
6	6	600	- 0,06	0,12	0,10

Table 1. Summary of device dimensions

In the fig. 3, we have presented the network of the static characteristics in the case of the preceding device. These characteristics illustrate the relation between the extrinsic drain

current *Ids* and the bias voltages *Vds* and *Vgs*. We notice the presence of three regions which correspond to the three operation regimes (linear, non-linear and saturated).

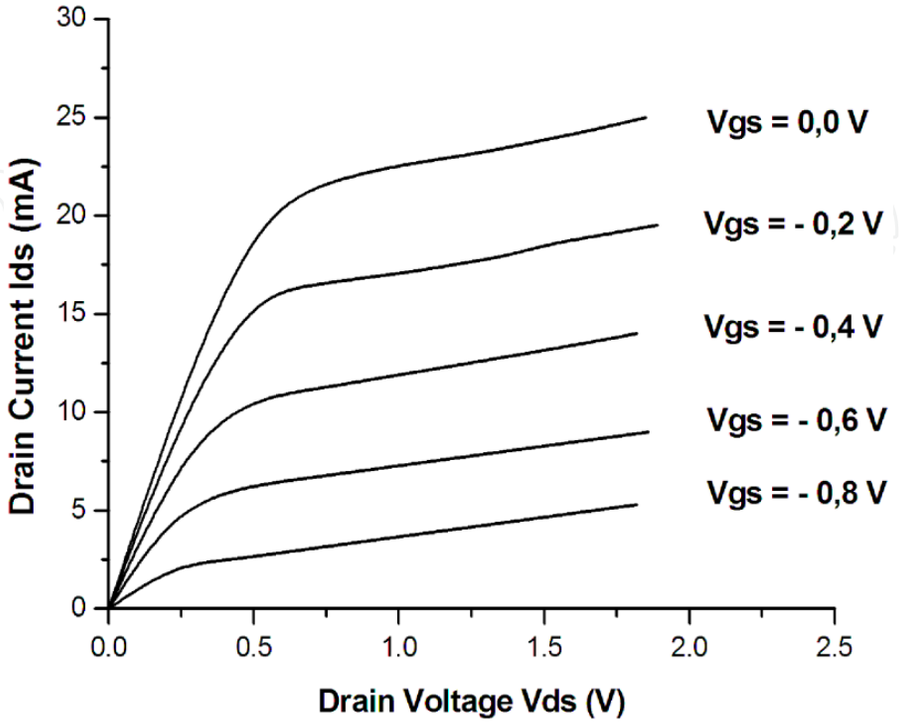

Figure 3. Drain current versus drain-source voltage at a different gate-source voltages for GaAs MESFET with parameters and device dimensions are listed in Table 1.

To demonstrate the validity of the developed model and to compare its performance with the experimental data reported in the literature (Chin and We, 1993) a submicron GaAs MESFET having the parameters and device dimensions selected in Table 2. Fig. 4 represented a comparison between the proposed model and the experimental *I-V* characteristics for this device. It is clearly seen that good agreement between the model and the experimental data are obtained, this is quite interesting to argue the validity of the mathematical analysis and the proposed numerical methods for practical short gate-length GaAs MESFET devices.

L (μm)	a (μm)	Z (μm)	Nd (At / cm^3)	μ_0 (cm^2/ Vs)	E_0 / Em
0,5	0,143	100	$1{,}31.\ 10^{17}$	3600	0,25
Rs (Ω)	Rd (Ω)	Rp (Ω)	a_1	b_1	c_1
6	6	1000	- 0,06	0,12	0,10

Table 2.

Fig. 5 and Fig. 6 represent the transconductance as a function of the intrinsic drain voltage *Vd* for a series of intrinsic gate voltage *Vg*. In these figures, we noticed that the transconductance increases on the one hand as the absolute value of the voltage gate decreases, and on the other hand with the increase in the drain voltage until the saturation regime where the transconductance is saturated. This is explained because, more the gate voltage increases in absolute value, more the width of space charge area increases. The

extension of this area ends when this one occupies all the width of the channel. No passage of the current is then theoretically possible.

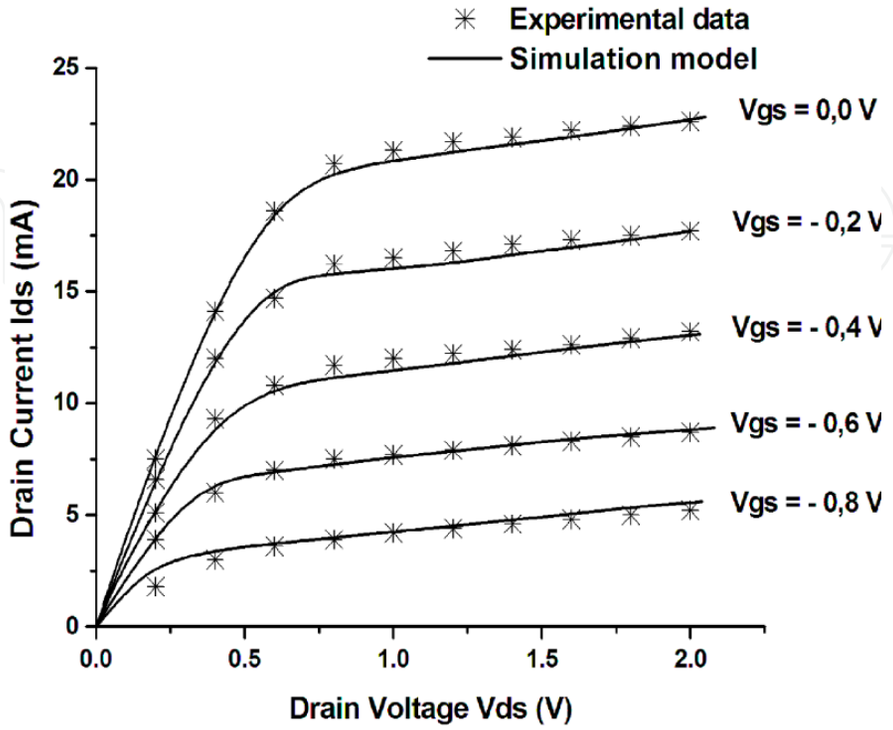

Figure 4. Comparisons of the *I-V* characteristics between the proposed model (solid line) and the experimental data (asterisks) (Chin and Wu, 1993) for the device with dimensions are listed in Table 2.

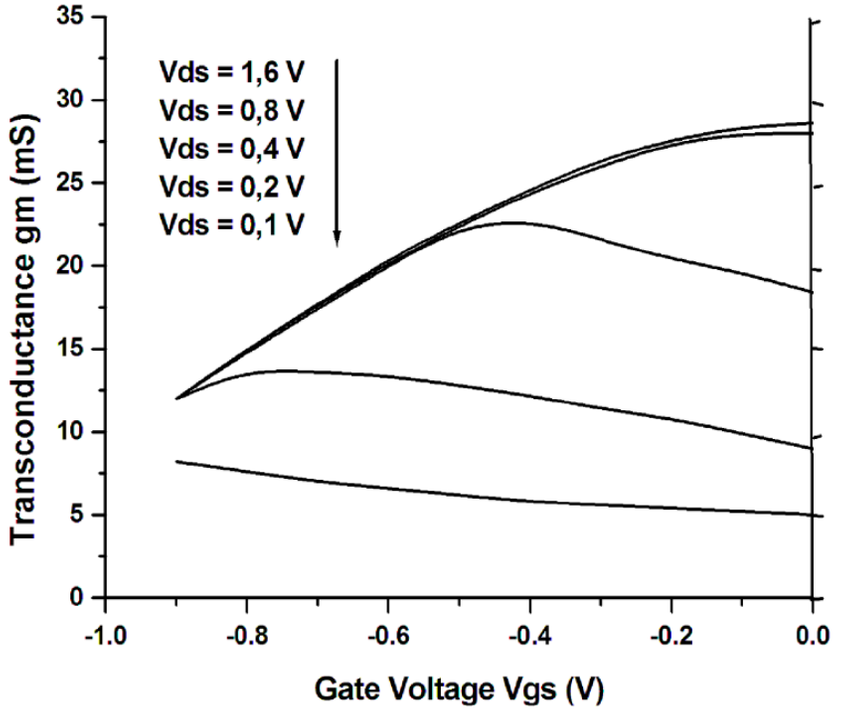

Figure 5. Variation in transconductance as a function of gate-source voltage at different drain-source voltages for a device with parameters and dimensions are listed in Table 1.

Fig. 7 represents the drain conductance as a function of the drain voltage for a series of gate voltage. We notice that the drain conductance is decreases on the one hand as the drain

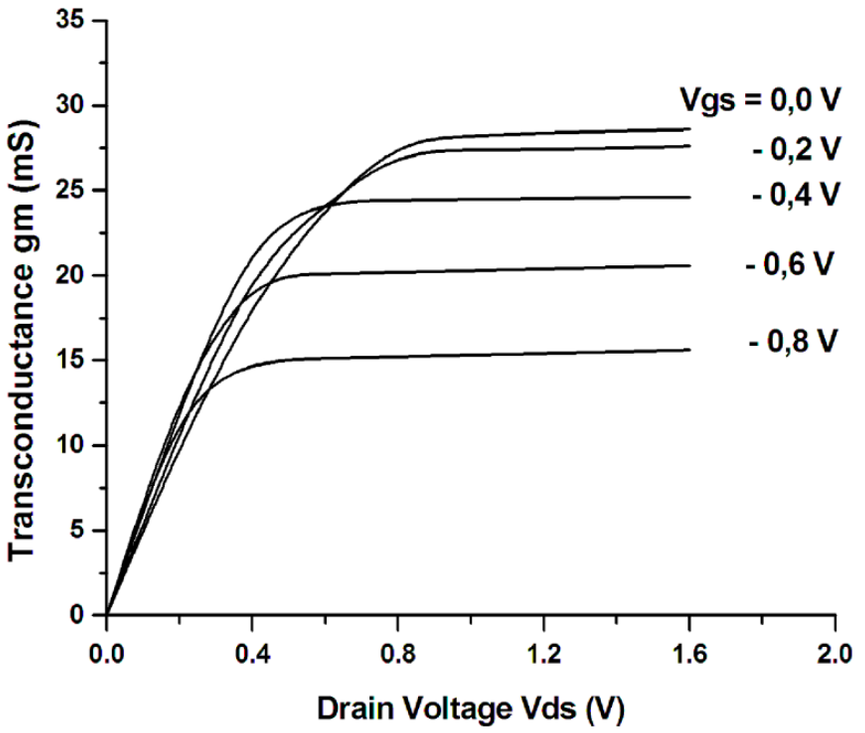

Figure 6. Variation in transconductance as a function of drain-source voltage at different gate-source voltages for a device with parameters and dimensions are listed in Table 1.

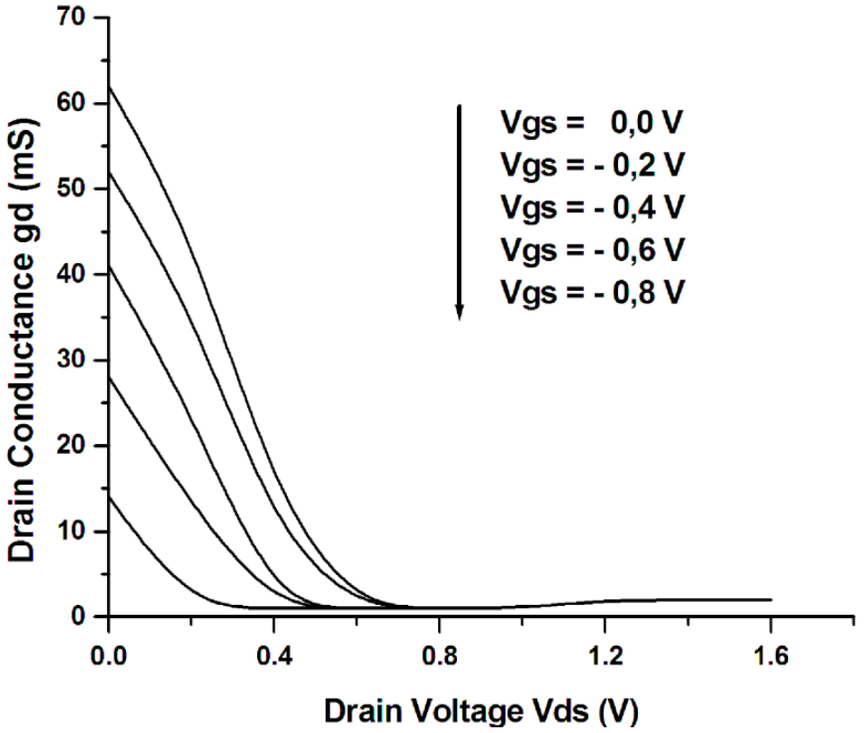

Figure 7. Variation in drain conductance as a function of drain-source voltage at different gate-source voltages for a device with parameters and dimensions are listed in Table 1.

voltage increases and on the other hand when the absolute value of the gate voltage increases. It takes its maximum value in linear regime, and is cancelled in regime of saturation. This explains why, in linear mode, the electrons available for conduction and present in the channel do not reach their speed limit. Also the drain current *Ids* varies in an important and quasi linear way with the drain voltage. On the contrary, for the strong values of *Vd* in the saturated regime, the electrons reached their speed limits and the current *Ids* progresses slightly with *Vd*.

5. Conclusion

During this work, a comprehensive new model is developed to simulate the static characteristics of short gate-length GaAs MESFET. The validity of the model is established by simulating *Ids*, *gm* and *Gd* characteristics. The performance of the model is compared with experimental results existing in the literature by calculating the I-V characteristics of a device with the gate length is equal to 0,5 μm. It has been demonstrated that the proposed model is a comprehensive one capable of simulating DC characteristics of short gate-length GaAs MESFETs. The transconductance and drain conductance curves obtained by the model have the same behavior with those of the theory, so that it has been shown that proposed model could be a useful tool for device simulators involving short channel MESFETs.

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