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Low Temperature Wafer-Level Metal Thermo-Compression Bonding Technology for 3D Integration

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1. Introduction

1.1. Background of 3D integration

The past few decades have seen the rapid development in computing power and wireless communication achieved through invention of new technologies, discovery of new semiconductor materials and application of new fabrication processes. These innovations have enabled the placement of large number of high performance transistors which are commensurate with scaling on an integrated circuit and the transistor count doubles approximately every 18 months, which is famously known as Moore's law as described by Gorden Moore (Moore, 1998) and modified by Davide House (Kanellos, 2003). Since small and efficient system is always the ultimate objective for semiconductor industry development, 3D integration emerges as a suitable candidate for mainstream packaging and interconnection technology in the future as geometrical scaling is faced with unprecedented scaling barriers from the fundamental and economics fronts.

The development of vertically integrated devices could date back to the early 1980s (Pavlidis&Friedman, 2009). One of the first successful 3D structure just includes a positive-channel metal oxide semiconductor (PMOS) and a negative-channel metal oxide semiconductor (NMOS) transistors which share the same gate electrode to reduce the total area of the inverter (Gibbons&Lee, 1980; Goeloe et al., 1981). After 30 years of continuous development, 3D integration technology has infiltrated into all the domains of semiconductor, such as combination of logic and memory circuit (Beyne, 2006), sensor packaging (Yun et al., 2005), heterogeneous integration of MEMS and CMOS (Lau et al., 2009), etc. More importantly, 3D integration technology is not only used for form-factor miniaturization, but also for achieving excellent performance, low power consumption, high integration capability, and low cost (Tan et al., 2011).

1.2. Motivation for research in 3D integration

In order to keep up with the needs of the astonishing development in the functionality of portable devices and of computational systems, integration technology has been investigated over the past three decades. 3D integration technology is widely defined as the technology which can integrate the disparate device layers in a multi-strata vertical stacking way (Young&Koester, 2010) with electrical interconnects by vertical inter-layer vias. Fig. 1 schematically presents the concept of 2D and 3D integration circuit. Further requirements on form factor reduction, performance improvement, and heterogeneous integration will make 3D integration a plausible choice as the next generation of microsystem manufacturing technology, as it can provide an excellent connection density higher than $10^4/\text{mm}^2$ (Beyne, 2006) for developing “More than Moore” scaling.

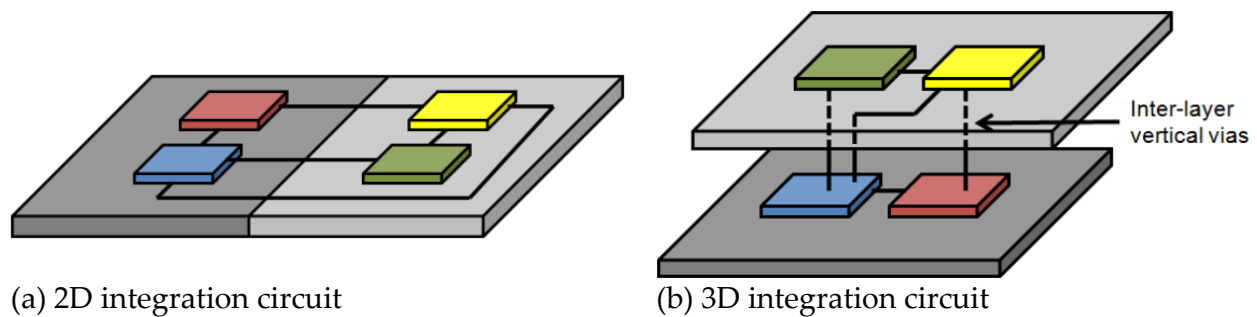


Figure 1. Different approaches of integration technology.

The original purpose of 3D structure is system-size reduction. Traditional 2D integration technologies individually assemble different functional dies on a planar substrate or in a printed circuit board. The packaging area of individual die is generally needed and an additional spacing between disparate functional blocks is typically required, thus reducing the integration density to a very low level. By stacking the device layers in a vertical way, a highly integrated circuit can be achieved. Since the substrate area is the first consideration, high integration density can increase the number of devices or functional blocks per chip area, which in turn miniaturizes the form-factor.

High performance requirement is another important reason for research in 3D integration. As the dimension of functional blocks continues to shrink and the emergence of large scale integration (LSI) technology, or even very large scale integration (VLSI) technology in recent years, the interconnects in an integrated circuit has begun to dominate the overall circuit performance. As a result of long interconnect length, interconnect latency and power consumption will increase. Therefore, the number of long wires is identified as the bottle-neck in the planar (2D) integration. In comparison with 2D design, 3D integration technology based on flip-chip, micro-bump connection and through silicon via (TSV) technologies can ease this interconnect bottle-neck and thus results in a lower propagation delay and power consumption. More importantly, in one synchronous operation mode, on-chip signal can only propagate in a limited distance. In other words, large chip size usually requires more clock cycles for on-chip signal to travel across the entire circuit. Using 3D

stacking technology, more functional devices can be integrated in one synchronous region, thus increasing the computational speed.

The third, and maybe the most attractive, advantage of 3D integration technology is heterogeneous integration (Beyne, 2006). Although system-on-a-chip (SoC) is an attractive solution to integrate multiple functionalities on a single chip, specific optimization for each functional blocks on the same substrate may make SoC devices with large numbers of functional blocks very difficult to achieve. Furthermore, compatibility between different substrates might cause potential contamination or signal corruption. If high density 3D integration technology is available, it is a very attractive method for a “3D-SoC” device manufacturing. With this method, each functional block can be optimized separately and assembled in a vertical fashion. Since there is no common substrate, the problems caused by compatibility between different substrates are expected to be less severe. Fig. 2 shows an example for heterogeneous TSV-less integration method of CMOS and MEMS whereby the CMOS layer can be used as an ‘active capping’ layer for the sensitive MEMS layer. In order to provide a hermetic ambient for proper operation, the seal ring is formed in the trench of SOI MEMS wafer during the device layer DRIE etching. The electrode pad of MEMS is bonded to a connection pad on the CMOS die and will be routed to external by using lower metal layers in the CMOS chip. Metallization process can be realized during the SOI MEMS fabrication.

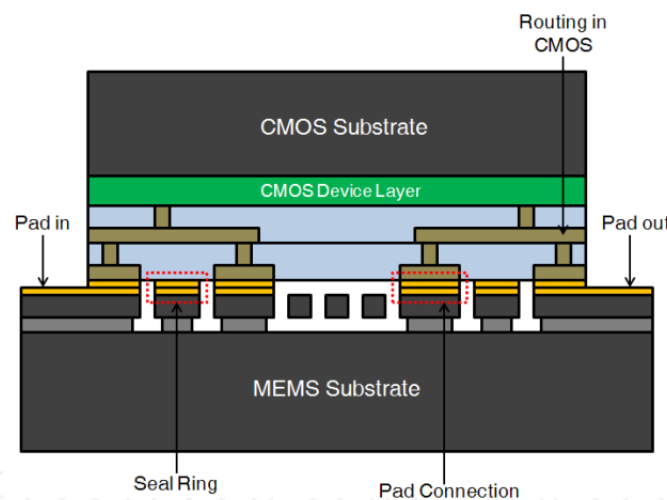


Figure 2. TSV-less 3D integration heterogeneous of MEMS and CMOS (Nadipalli et al., 2012).

2. Overview on bonding technologies in 3D integration

Bonding technologies have been reported as an imperative packaging and integration method for 3D IC stacking. It can be split into three schemes according to the fabrication approach: wafer to wafer, chip to wafer and chip to chip, as shown in Fig. 3. The ability of wafer to wafer bonding technology can effectively increase the throughput, making it a cost-effective manufacturing approach, but the unstable number of known-good-die (KGD) which is determined by the device layer might be the a drawback for this stacking method. Therefore, chip to wafer bonding and chip to chip bonding can assure that the vertical stacking will be only executed with the good dies. Since mass production is the primary commercial and

manufacturing consideration in future, both chip-to-wafer and wafer-to-wafer technologies will gradually become the mainstream for 3D stacking and packaging (Ko&Chen, 2010).

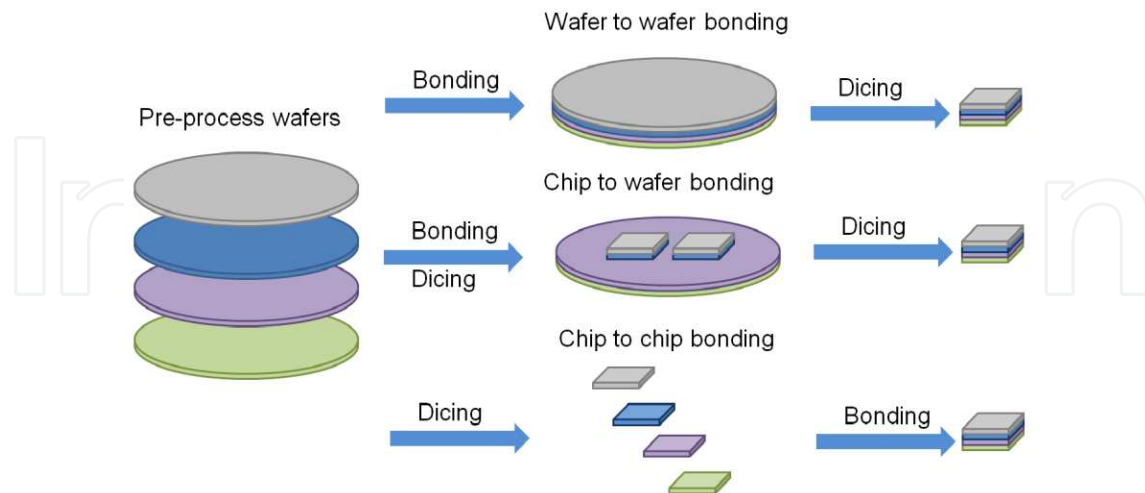


Figure 3. Different bonding technologies for 3D Integration circuit according to fabrication approach.

Based on the bonding materials, bonding technology can fall into dielectric bonding and metallic bonding. Since the dielectric materials are used, the device layers are isolated from each other and a “via-last” process is followed. Devices layers are firstly bonded in a vertical stack, and then the vertical vias are etched through the devices layers for vertical interconnects between each layer. Therefore, high aspect ratio vias are usually needed. The most leading dielectric bonding methods used in 3D integration include adhesive bonding and oxide fusion bonding.

Adhesive bonding, also known as polymer bonding, usually uses polymers and inorganic adhesive as the intermediate bonding materials. Since a layer of polymer or inorganic adhesive is always spun before bonding, it is very suitable for non-uniform surfaces and for bonding at low temperature. Benzocyclobutene (BCB) and SU-8 are the most common materials used in 3D integration, since high bonding strength can be easily achieved with these two polymer materials (Niklaus et al., 2001; Pan et al., 2002).

Oxide fusion bonding requires a very low surface roughness (root mean square roughness < 1 nm) and the process is often followed by a post-bonding annealing. The bonding step for fusion bonding refers to spontaneous adhesion process of two wafers when they are placed in direct contact. The surface activation which enables the wafer pair to have a stronger spontaneous adhesion is usually applied before bonding. This bonding technology is not only limited between Si-to-Si and SiO₂-to-SiO₂, but some high-*k* dielectric materials, such as Al₂O₃, HfO₂, and TiO₂ (Chong&Tan, 2009) are also employed to achieve a higher bonding strength for a given anneal temperature and duration.

Device layers bonded with a conductive metallic layers is a very attractive choice, as it allows “via-first” and “via-middle” approaches for 3D IC integration. Therefore, the requirement for high aspect ratio via can be relaxed. On the other hand, metal is a good heat conductor which will help to circumvent the heat dissipation problem encountered in 3D ICs. At the same time, the use of metal as bonding material in 3D applications allows the

electrical contact and mechanical support to be formed between two wafers in one simultaneous step. Examples of such bonding technology include metal diffusion bonding and eutectic bonding will be presented in details in next section.

Dielectric bonding and metallic bonding can be combined to one emerging approach for 3D integration as well. The research work by McMahon *et al.* (McMahon et al., 2005) presents a wafer bonding of metal/adhesive damascene-patterned providing inter layer electrical interconnects via Cu-Cu bonding and mechanical support via adhesive bonding (BCB) of two wafers in one unit processing step. IMEC (Interuniversity Microelectronics Centre, Belgium) developed this technology and was formally named as “Hybrid Bonding” (Jourdain et al., 2007; Jourdain et al., 2009).

3. Low temperature wafer-level metal thermo-compression bonding for 3D integration

Pure metal and alloy material are widely used in bonding technology for 3D integration. The description in this section is specific on two types of metal based low temperature thermo-compression bonding technologies: copper diffusion bonding and copper/tin eutectic bonding. The following description includes the comparison of different metal bonding materials, the principle of bonding process and performance of reported work. Oxide fusion bonding which is also widely investigated in 3D integration is included for comparison at the end of this section as well.

3.1. Why low temperature?

As the name implies, thermo-compression bonding contains two important elements: heat and pressure. Metal bonding surfaces are brought into contact with the application of force and heat simultaneously. Atomic motion (for metal diffusion bonding) or alloy formation (for eutectic bonding) will occur at the bonding interface during this process. Due to surface oxidation and some specific alloy formation, high temperature is usually required for achieving high bonding quality, but practical packaging and integration should be achieved at adequately low temperature (typically 300°C or below) for prefabricated devices which are sensitive to high temperature processing owing to thermal budget limitation, the post-bonding thermo-mechanical stress control, and alignment accuracy improvement (Tan et al., 2009). Although it is commonly known that the quality of thermo-compression bonding can usually be ameliorated when the bonding temperature increases, the current mainstream research focuses on achieving high bonding quality at temperature as low as possible for the considerations of cost reduction and high throughput manufacturing.

3.2. Metal diffusion bonding

Metal diffusion bonding is also referred as pressure joining, thermo-compression welding or solid-state welding. Bonding interfaces will fuse together due to atomic interaction under heat and pressure.

3.2.1. Comparison of different diffusion bonding materials

The common metal materials for metal diffusion bonding are aluminum (Al-Al), gold (Au-Au) and copper (Cu-Cu). Table 1 shows a comparison of physical properties of these metals in the context of metal diffusion bonding. Among these metals, Al-Al bonding is hard to achieve with low bonding temperature and low bonding force, most likely because it gets oxidized readily in ambient conditions. In addition, its relatively higher coefficient of thermal expansion (CTE) in comparison with that of silicon wafer will result in larger wafer bow during cooling. This poses difficulty in achieving high quality bonding for Al-Al especially across large area. On the other hand, even though the bonding temperature for Au-Au is generally about 300°C, its prohibitively high cost is the major roadblock for widespread use except for high end applications. Cu emerges as an attractive choice in terms of its lower cost and the ability to bond Cu at moderately low temperature. Furthermore, Cu presents a number of advantages in terms of its physical properties that suit the final application such as better electrical conductivity, mechanical strength and electro-migration resistance. Therefore, with these superior material properties, low temperature Cu bonding will be the candidate for mainstream 3D integration application.

Material	Al-Al	Au-Au	Cu-Cu
Temperature (°C)	450	~300	250/300
Resistivity (μΩcm)	2.67	2.20	1.69
Melting Point (°C)	660.4	1064.4	1083
CTE (×10 ⁻⁶ /K)	23.5	14.1	17.0
Thermal Conductivity (W/ m K)	237	318	401
Cost (US\$/LB)	1.1798	25881.44	4.4198

Table 1. Comparison of different metal diffusion bonding technologies (Fan et al., 2011).

3.2.2. Fundamentals of low temperature copper diffusion bonding

Fig. 4 illustrates the formation principle of low-temperature Cu diffusion bonding. In order to isolate the substrate from the Cu bonding film, a thin film of dielectric, such as SiO₂ is firstly deposited as the precursor (Fig. 4. a). Subsequently, the barrier layer, such as Ti or Ta which is used to thwart excessive Cu diffusion into Si and to ameliorate the adhesion between substrate and Cu film, and a thin Cu seed layer are deposited (Fig. 4. b). After that, Cu electroplating is applied to the required thickness of Cu layer depending on the applications (usually from several to a dozen of μm), followed by chemical mechanical planarization (CMP) (Fig. 4. c). Finally, the wafer pair is brought into contact in nitrogen (N₂) or vacuum ambient under a contact force (e.g. 2500 mbar for a 6 inch wafer) and held typically at 300°C (or 250°C) for some time (e.g. 30 min and above) (Fig. 4. d).

Since the bonding temperature is fixed at low level, key parameters of low temperature Cu diffusion bonding are bonding duration and bonding force. During bonding, Cu atoms

acquire sufficient energy to diffuse rapidly and Cu grain begins to grow. In order to obtain a higher bonding strength, Cu diffusion must happen across the bonding interface and the grain growth also needs to progress across the interface. If the bonding duration is insufficient (e.g. 10 min or below), the inter-diffusion of Cu atoms across the bonding interface is limited. Thus Cu grain formation stops at bonding interface and bonding strength is reduced. More importantly, Cu gain across the bonding interface will reduce the number of grain boundaries, which will provide a high conductivity at the bonding interface. However, this difficulty can be overcome by an anneal step after bonding. Fig. 5 presents the comparison of bonding strength, measured by die shear strength testing, without and with anneal step after a short bonding duration. The samples are bonded and annealed at 250°C for 15 min and 1hr, respectively. The bonding strength presents a significant improvement when short bonding duration is followed by an anneal process.

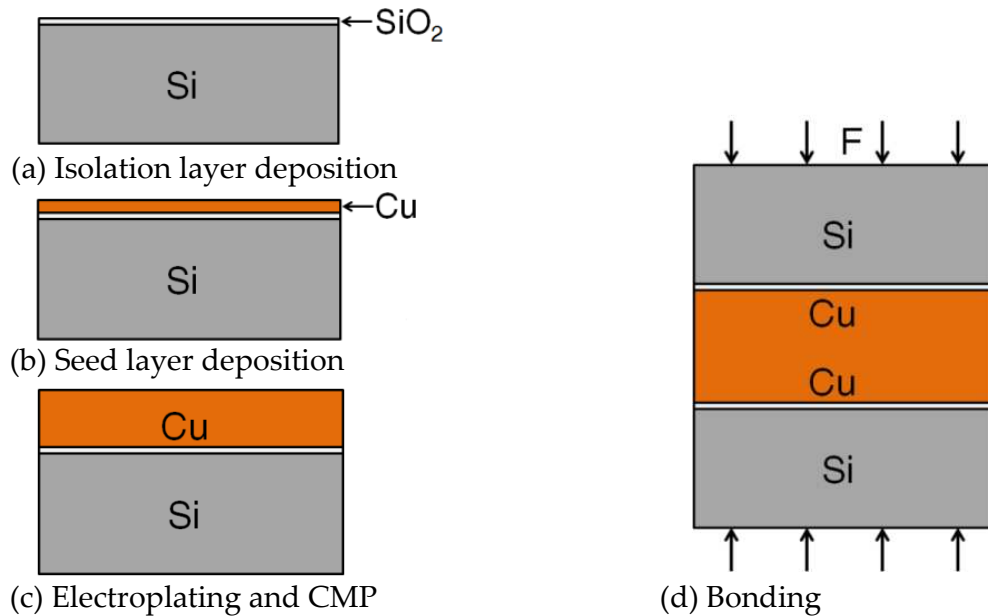


Figure 4. Schematic showing the principal of formation of Cu diffusion bonding.

Cu diffusion bonding is based on Cu atom migration and grain growth. Therefore, the wafer pairs must be brought into an intimate contact at the atomic level by a uniform bonding force. Wafer bow and surface contamination are the critical factors that affect the bonding uniformity. The surface contamination can usually be reduced with tighter particle control or some surface treatment before bonding which will be presented in next section. As shown in Fig. 6, a Cu-coated wafer exhibits a wafer bow of $\sim 15.9 \mu\text{m}$ based on wafer curvature measurement using a laser beam. This is a direct result of the huge difference in the CTE between Cu and Si (17 and $3 \times 10^{-6} / \text{K}$, respectively), and it might become bigger during the bonding process. Appropriate bonding force enables us to eliminate the drawback brought by the wafer bow and perform a highly uniform bonding. For the wafer pairs that exhibit wafer bow lower than $20 \mu\text{m}$, high bonding uniformity can usually be achieved under a contact pressure of ~ 2000 mbar at 300°C for 1 hour without post-bonding anneal.

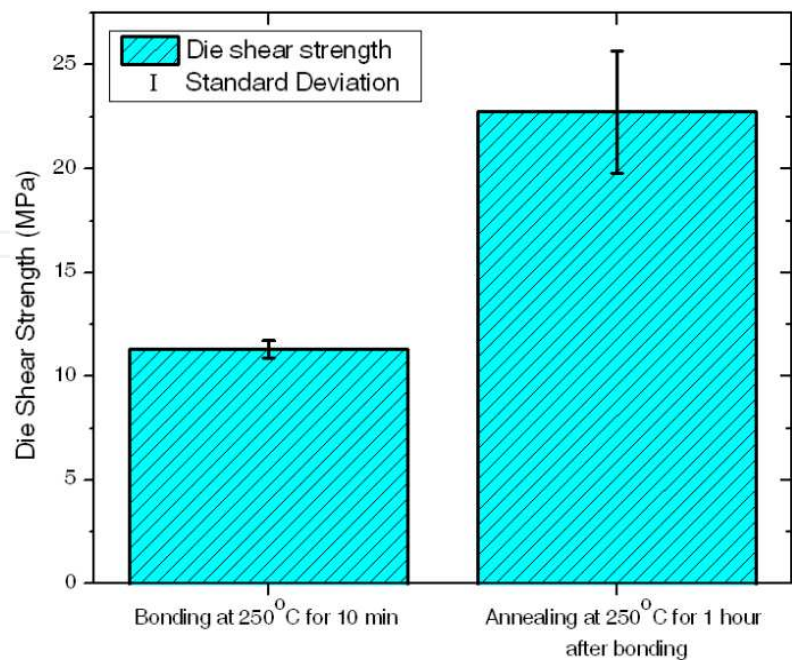


Figure 5. Comparison of bonding strength, without and with an anneal step after a short bonding duration.

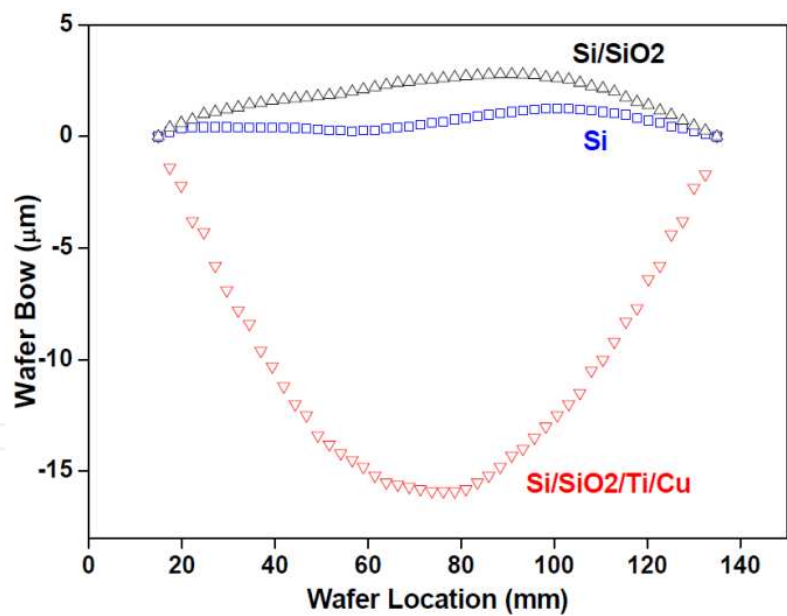


Figure 6. Pre-bonding wafer bow based on wafer curvature measurement (Tan et al., 2011).

3.2.3. Surface treatment before copper diffusion bonding

The surface condition often refers to the oxidation at the Cu bonding surface. Since Cu surface oxidizes readily in ambient air to form cuprous oxide (red oxide) and cupric oxide (black oxide). These oxide layers impose a barrier to successful diffusion bonding at low temperature.

3.2.3.1. Wet etch method

In order to remove the surface oxide, surface treatments by soaking the wafers in acetic acid or dilute hydrochloric acid and followed by a forming gas purge in the bonding chamber are usually applied immediately before bonding (Tadepalli&Thompson, 2003). This removal process can be described by the following chemical equations (1) and (2):



Since this reaction takes place very rapidly, the immersion is completed in a few minutes. The research work by Jang *et al.* (Jang et al., 2009) indicates that, for the consideration of bonding strength, the immersion time must less than 5 min for a thickness of bonding layer around 500 nm. If long time immersion is applied, the bonding strength will be reduced due to the decrease in plastic dissipation energy near the interfacial crack tips with thinner Cu film thickness caused by over etching.

3.2.3.2. Forming gas anneal

Oxygen content in the bonding layer can be reduced by pre-bonding forming gas anneal. Forming gas is a mixture of hydrogen and nitrogen (typically 5% H_2 :95% N_2 , by volume). The reactions with the Cu oxides are exothermic and can be principally represented as follows in (3) and (4):



This pre-bonding anneal is an *in-situ* clean process, which presents no re-oxidation risk before bonding. Compared with anneal at high temperature, long anneal duration (e.g. 1 hour) at low temperature (typically at 250 or 300 °C) is preferred to eliminate the oxygen in the bonding layer, as high temperature takes the potential risk of unwanted damage in the device layer.

3.2.3.3. Self-assembled monolayer (SAM) passivation

Even though the surface oxide removal by wet cleaning and oxide content reduction in the bonding layer by forming gas anneal have been widely investigated with some success, surface contamination of particles can still remain a challenge. Recently, a novel surface treatment using self-assembled monolayer (SAM) of alkane-thiol to passivate clean Cu surface immediately after metallization is applied. SAM application was first applied in wire bonding by IMEC in the area of microelectronic manufacturing (Whelan et al., 2003). Subsequently, this method is applied in the domain of fluxless solder, flip-chip bonding, and wafer-level Cu diffusion bonding. SAM of alkane-thiol formed by linear alkane-thiol molecules ($\text{CH}_3-(\text{CH}_2)_{n-1}-\text{SH}$, n = number of carbon), and it can be dissolved in ethanol to a concentration of 1 mM for the passivation application in wafer-level Cu diffusion bonding.

The process flow includes post-metallization adsorption and pre-bonding *in-situ* desorption to provide clean Cu surfaces for bonding.

Fig. 7 shows schematic of the process flow used in low temperature Cu diffusion bonding with SAM application. Wafers are immersed immediately into the solution of alkane-thiol after Cu metallization. Due to its specific high affinity functional head group (thiol, S-H) towards Cu surface, alkane-thiol can readily adsorb onto the Cu surface and rearranged into a uniform organic monolayer. This SAM layer provides temporary protection to the Cu surface. Subsequently, the SAM layer will be desorbed effectively with an annealing step in inert N₂ ambient to recover the clean Cu surface for the final bonding at low temperature. Research work in Nanyang Technological University (NTU) indicates that anneal for 30 min at 250 °C can efficiently desorb the SAM layer formed after 3 hr of immersion time in the solution.

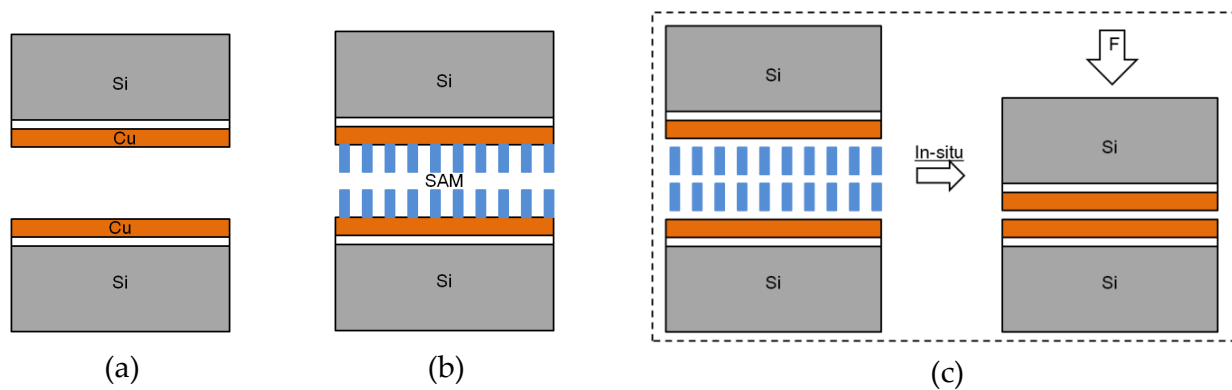
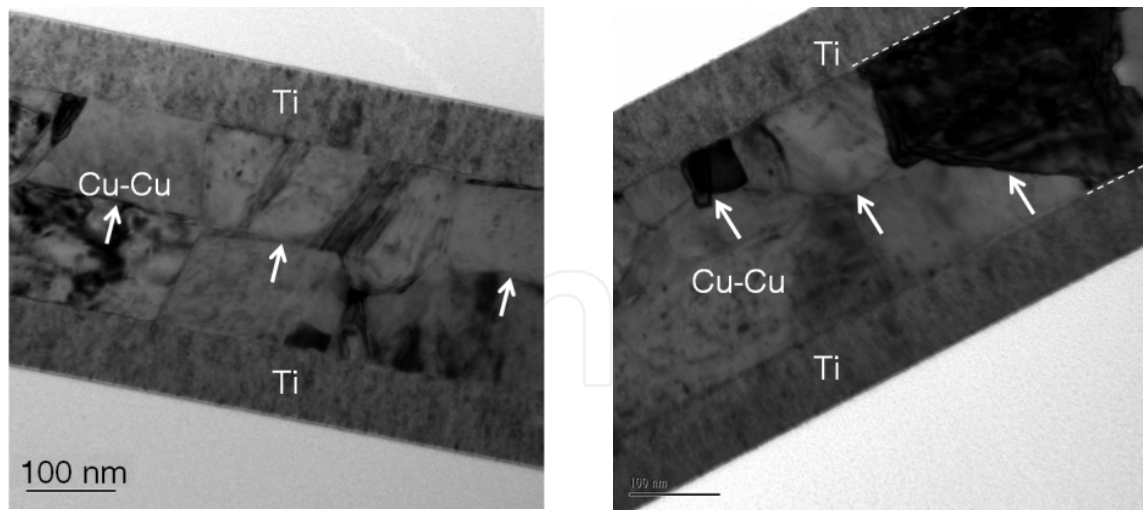


Figure 7. The application of self-assembled monolayer (SAM) as a passivation layer on Cu surface for bonding enhancement at lower temperature. (a) A pair of Si wafers with Cu metallization; (b) Immersion in alkane-thiol solution: SAM absorption; (c) Pre-bonding SAM desorption by thermal means and bonding (Tan et al., 2012).

Fig. 8 shows the cross-section TEM images of the bonded Cu layers. The micrographs clearly confirm the success of Cu–Cu bonding in both samples. Fig. 8(a) is taken from bonded sample without SAM treatment. There is limited grain growth across the bonding interface and the original bonding interface is clearly seen (marked with arrows). In Fig. 8(b) which is taken from bonded sample with SAM treatment, the original bonding interface has disappeared. Cu grains extend across the bonding interface and a wiggling grain boundary is observed (marked with arrows). As can be seen, one Cu grain even extends the entire bonded Cu layer thickness sandwiched by the Ti capping layers (marked with white dotted line).

3.2.4. Performance of state-of-the-art copper diffusion bonding

Low temperature Cu diffusion bonding is gradually becoming the mainstream bonding technology for 3D integration as it allows the formation of electrical contact, mechanical support, and hermetic seal in one simultaneous step. Therefore, these three parameters are usually presented as the key performance matrix for metal based bonding quality.



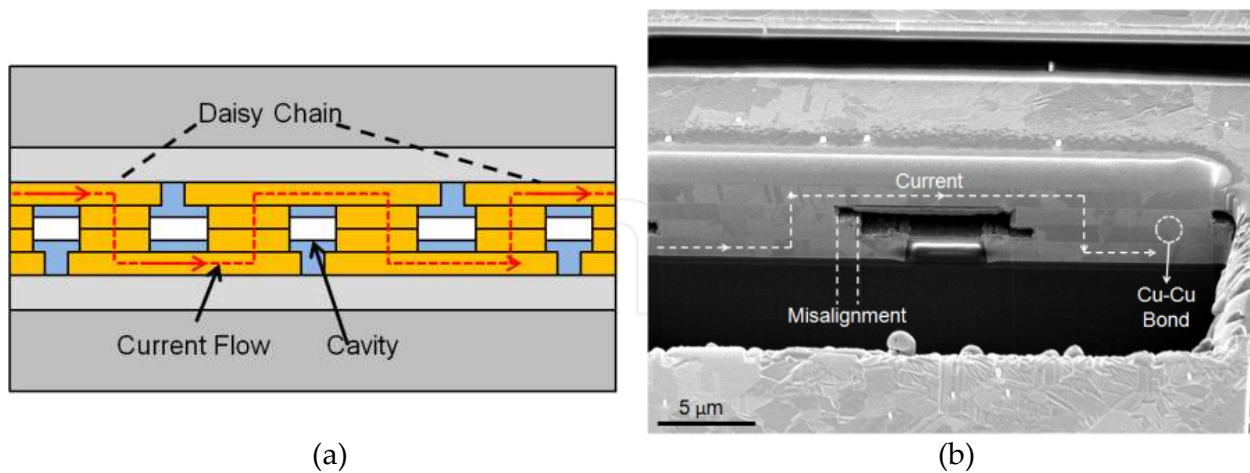
(a) Without SAM passivation

(b) With SAM passivation and desorption

Figure 8. TEM micrographs of bonded Cu layers (Tan et al., 2009).

3.2.4.1. Electrical characterization

Early study of contact resistance of bonded Cu interconnects is presented by Chen *et al.* (Chen et al., 2004) in MIT (Massachusetts Institute of Technology, USA). The measurement results using Kelvin structure indicate that a specific contact resistance of bonding interfaces of approximately $10^{-8} \Omega \cdot \text{cm}^2$ is obtained. A recent research by Peng *et al.* (Peng et al., 2011) demonstrate an excellent specific contact resistances of bonding interface using SAM as the surface treatment of about $2.59 \times 10^{-9} \Omega \cdot \text{cm}^2$. This work has also demonstrated a daisy chain of at least 44,000 contacts at $15 \mu\text{m}$ pitch connected successfully, and the misalignment of $\sim 2 \mu\text{m}$ (Fig. 9).



(a)

(b)

Figure 9. (a) Face-to-face daisy chain stacking architecture of two wafers using Cu-Cu bonding. (b) Cross sectional FIB image of the $15 \mu\text{m}$ pitch Cu-Cu bonding (Peng et al., 2011).

No open failure is detected during measurement up to 44,000 nodes, as shown in Fig. 10. a. The sample with 10,000 bonding nodes is subjected to temperature cycling test (TCT) with temperature ranging from -40°C to 125°C . It is observed that the electrical continuity is

maintained even after 1,000 thermal cycles (Fig. 10. b). In freshly bonded sample (before TCT test), the resistance of the daisy chain is estimated from I - V plot and each node (consists of Cu lines and contact) is estimated to have ~ 26.1 m Ω of resistance, and a slight increase of the node resistance up to ~ 29 m Ω at 1,000 temperature cycles. This slight increase is due to oxidation of the exposed Cu lines as a result of complete removal of the top wafer after bonding (since there is no TSV). The results suggest that the robustness of the Cu-Cu bond is maintained. This high connection density of up to $4.4 \times 10^5/\text{cm}^2$ and its reliability provides a feasible platform of high IC-to-IC connection density suitable for future wafer level 3D integration of IC to augment Moore's Law scaling.

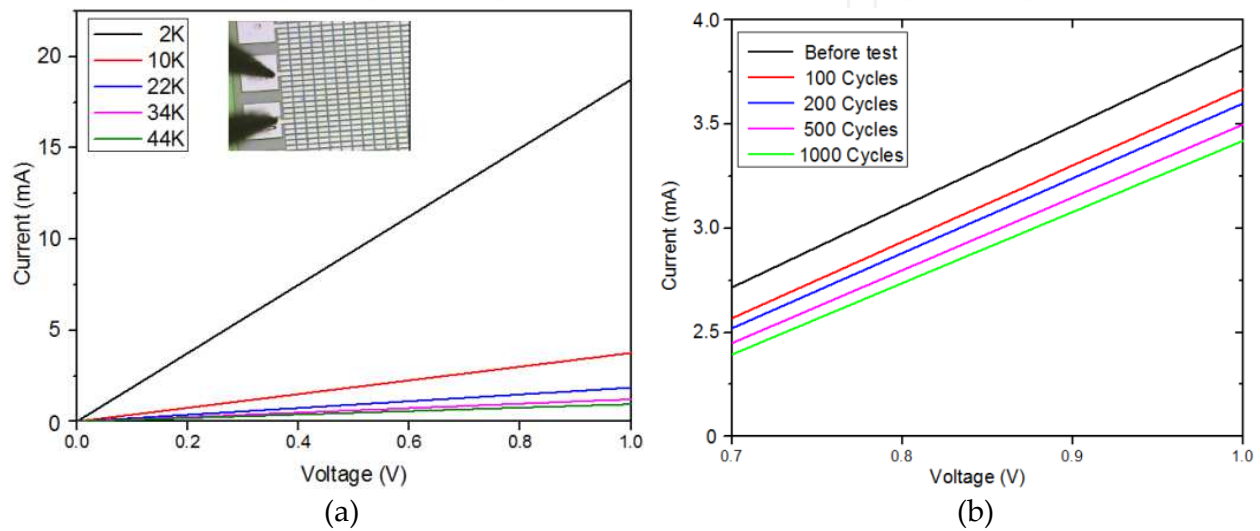


Figure 10. (a) I - V characteristic of the Daisy chain measured from 2,000 to 44,000 contacts (each interval = 2,000 contacts). The contacts are connected continuously and ohmic behavior is exhibited; (b) I - V characteristics of daisy chain before and after temperature cycling test (Peng et al., 2011).

3.2.4.2. Mechanical test

Besides the die shear strength test, four-point bending method is also widely employed for strength of mechanical support analysis (Huang et al., 2005). The interfacial adhesion energy between two bonded thin films can be qualitatively analyzed by this method. The earlier work by Tadepalli *et al.* (Tadepalli&Thompson, 2003) presents a superior interfacial adhesion energy of 11 J/m 2 at Cu diffusion bonding interface bonded at 300 °C and indicates that this value is superior than that of industry-standard SOI wafer. A recent work by Kim *et al.* (Kim et al., 2010) shows a short time bonding with post-anneal at 300 °C for 1 hour can also get a high interfacial adhesion energy around 12 J/m 2 which is much higher than critical bonding strength required (>5 J/m 2) by the subsequent processes such as grinding. A summary of interfacial adhesion energy achieved for wafer pairs with and without SAM passivation bonded at 250 °C for 1 hr is shown in Fig. 11. The average interfacial adhesion energy obtained with and without SAM passivation goes up to 18 J/m 2 and 12 J/m 2 , respectively. Compared with the results from other literature, this interfacial adhesion energy obtained at low temperature is comparable or even better. The daisy chain bonding presented earlier exhibits high bonding strength as well, since

bonded Cu structures need to provide sufficiently mechanical strength to sustain the shear force during wafer thinning.

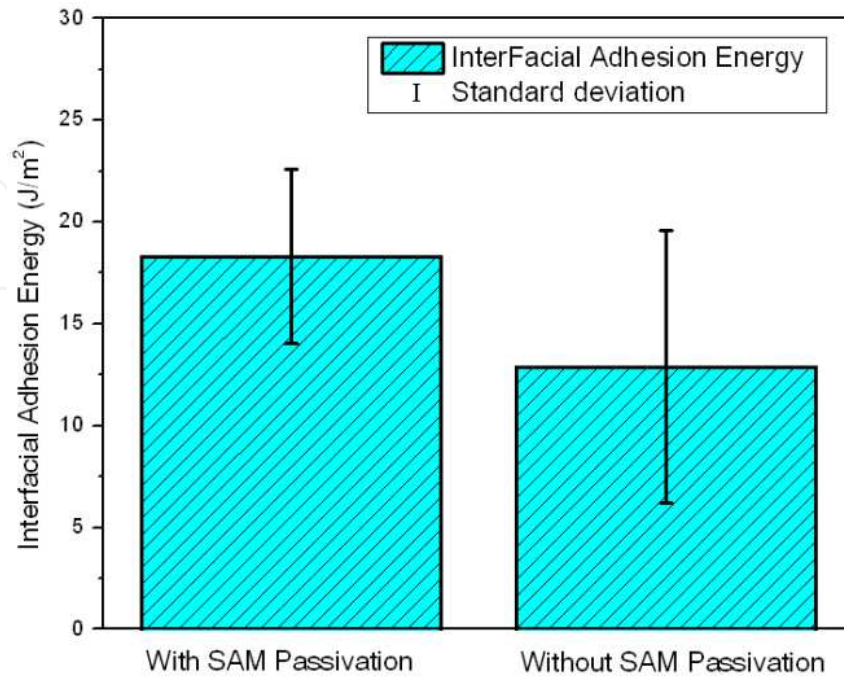


Figure 11. Interfacial adhesion energy for samples bonded at 250 °C.

3.2.4.3. Hermeticity detection

In an integrated 3D microsystems, micro- and nano-scale devices such as micro-electro-mechanical system (MEMS), microelectronic devices and optoelectronic devices, a hermetic ambient is commonly needed for proper operation with very low or without oxygen and water vapor content. The objective of hermetic packaging is to protect these devices against harsh environmental corrosion and potential damage during processing, handling and operation. Hermetic encapsulation can be also achieved by metal diffusion bonding. Hermeticity test, which consists of over-pressure storage in a helium bomb chamber and leak rate measurement with a mass spectrometer, is based on specifications defined in the MIL-STD, a standard commonly applied for microelectronics packaging. Hermetic packaging by Au diffusion bonding at 400°C demonstrated by Xu *et al.* (Xu et al., 2010) achieve a helium leak rate on order of 10^{-9} atm.cm³/sec based on the MIL-STD-883E method 1014.9 specification. A research of Al diffusion bonding at 450°C by Yun *et al.* (Yun et al., 2008) presents a excellent result of helium leak rate of the order of 10^{-12} atm.cm³/sec based on the MIL-STD-750E method 1071.8 specification.

The research work focusing on hermetic encapsulation with Cu diffusion bonding at low temperature in NTU exhibits outstanding helium leak rate based on the MIL-STD-883E method 1014.9 specification. Fig. 12 shows an average helium leak rate and standard deviation for cavities with the seal ring size of 50 μ m sealed by Cu diffusion bonding at 250 °C and 300 °C respectively with proper surface preparation and control. These values are at least one order of magnitude smaller than the reject limit (5×10^{-8} atm.cm³/sec) defined by the

MIL-STD-883E standard and is very attractive for packaging of devices that require high level of hermeticity and for heterogeneous integration of different micro-devices.

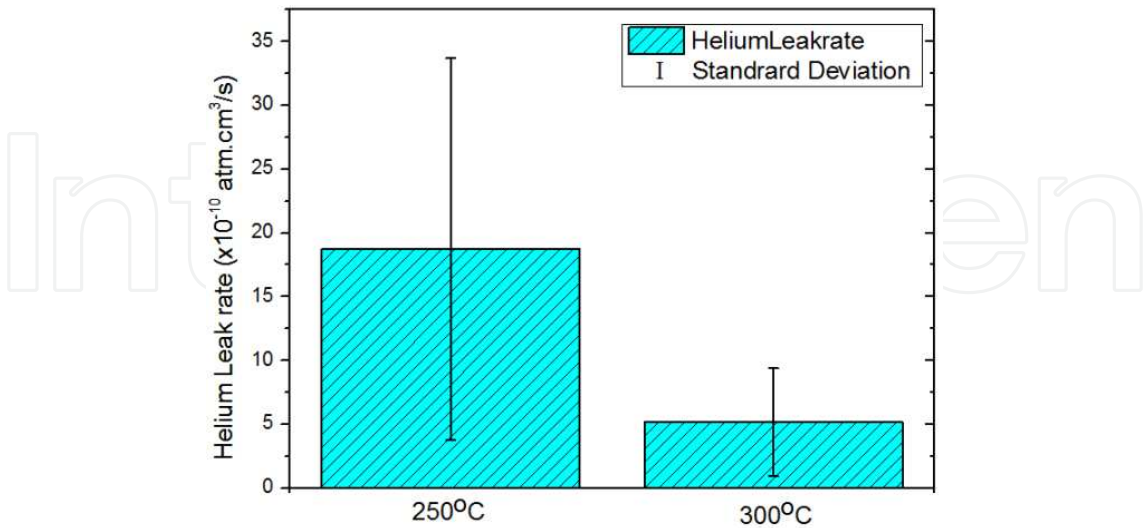


Figure 12. Average helium leak rate and standard deviation for cavities sealed at low temperature.

The reliability of Cu frame for hermetic packaging is also investigated through a temperature cycling test (TCT) from -40 to 125 °C up to 1000 cycles and a humidity test based on IPC/JEDEC J-STD-020 standard: (1) Level 1: 85°C/85%RH, 168hr; (2) Level 2: 85°C/60%RH, 168hr; and (3) Level 3: 30°C/60%RH, 192hr. The humidity test is applied from level 3 to level 1 in an ascending order in terms of rigor. In addition, an immersion in acid/base solution is applied to verify the corrosion resistance of the Cu frame for hermetic application. Table 2 shows some detected helium leak rate of sealed cavities with the seal ring size of 50 µm. Excellent reliability results of Cu-to-Cu wafer-level diffusion bonding at low temperature are maintained after a long term temperature cycling test with extreme low/high temperature swing, prolonged storage in humid environment, and immersion in acid/base solution.

TCT test	Before test	7.7×10 ⁻¹⁰ atm.cm ³ /sec
	After 500 cycles	7.9×10 ⁻¹⁰ atm.cm ³ /sec
	After 1000 cycles	7.9×10 ⁻¹⁰ atm.cm ³ /sec
Humidity test	Before test	6.0×10 ⁻¹⁰ atm.cm ³ /sec
	Level 3	7.5×10 ⁻¹⁰ atm.cm ³ /sec
	Level 2	7.0×10 ⁻¹⁰ atm.cm ³ /sec
	Level 1	8.0×10 ⁻¹⁰ atm.cm ³ /sec
Corrosion test	Before test	7.1×10 ⁻¹⁰ atm.cm ³ /sec
	Acid corrosion	5.9×10 ⁻¹⁰ atm.cm ³ /sec
	Base corrosion	5.4×10 ⁻¹⁰ atm.cm ³ /sec

Table 2. Detected helium leak rate after TCT test, humidity test, and corrosion test.

3.3. Eutectic bonding

Eutectic bonding is another metal based bonding technology for advanced MEMS packaging and for 3D integration. This technology, which is also referred as eutectic soldering and solid-liquid inter-diffusion bonding, stacks two wafers by intermediate eutectic compounds formation. The bonding interfaces will be fused together due to intermetallic phase formation. An important feature of eutectic bonding is the melting of intermediate eutectic metals and formation of the alloys that facilitate surface planarization and provide a tolerance of surface topography and particles.

3.3.1. Different alloy for eutectic bonding

The intermediate eutectic bonding layer is usually composed of a binary (or more) metal system. One with high melting point noble metal (like gold, silver and copper) and the other one with low melting point metal (like tin and indium) are used as intermediate eutectic metals which form intermetallic compounds during bonding. At present, the commonly used materials include Cu/Sn, Au/Sn, Au/Si, and Sn/Pb (Ko&Chen, 2010). Table 3 shows some eutectic metal system bonding temperature and their melting point. Since the eutectic point of two metals is lower than their melting points, the eutectic bonding can be usually achieved at low temperature. For example, in Cu/Sn, the bonding temperature is 150-280 °C. However, the temperature needed is still too high for some applications (e.g. Au/Si: 380 °C). The bonding temperature for Sn/Pb is only 183 °C, but this approach is not suitable for all electronic products due to the lead-free requirement.

Material	Bonding temperature	Material	Melting Point
Cu/Sn	150-280 °C	Cu	660.4 °C
Au/Sn	280 °C	Au	1064.4 °C
Au/Si	380 °C	Sn	213.9 °C
Sn/Pb	183 °C	Pb	327.5 °C

Table 3. Commonly used eutectic alloys bonding temperature and melting point of each metal

3.3.2. Fundamental of eutectic bonding

In following sections, the basic principles of eutectic bonding based on the binary metal systems Cu/Sn which is one of the best-investigated and well-established metal systems will be presented in detail.

3.3.2.1. Intermetallic compound formation

The bonding process relies on intermetallic compounds formed by inter-diffusion of the intermediate eutectic metal layers when they are brought into intimate contact at the specific bonding temperature. The first intermetallic compound formed between Cu and Sn is the metastable η -phase Cu_6Sn_5 , and then the Cu_3Sn ε -phase starts to form at Cu to Cu_6Sn_5

interface. Fig. 13 presents a typical intermetallic compound formation during bonding. This process is terminated when all Sn is consumed to form Cu_3Sn , since the binary metal systems is thermodynamically stable while no non-reacted Sn remains (Munding et al., 2008). If the bonding time is insufficient, the transformation fails to complete. The joint presents a potential risk of resistance in high temperature environment, as the melting point of Cu_6Sn_5 is 415°C , while that of Cu_3Sn is 676°C .

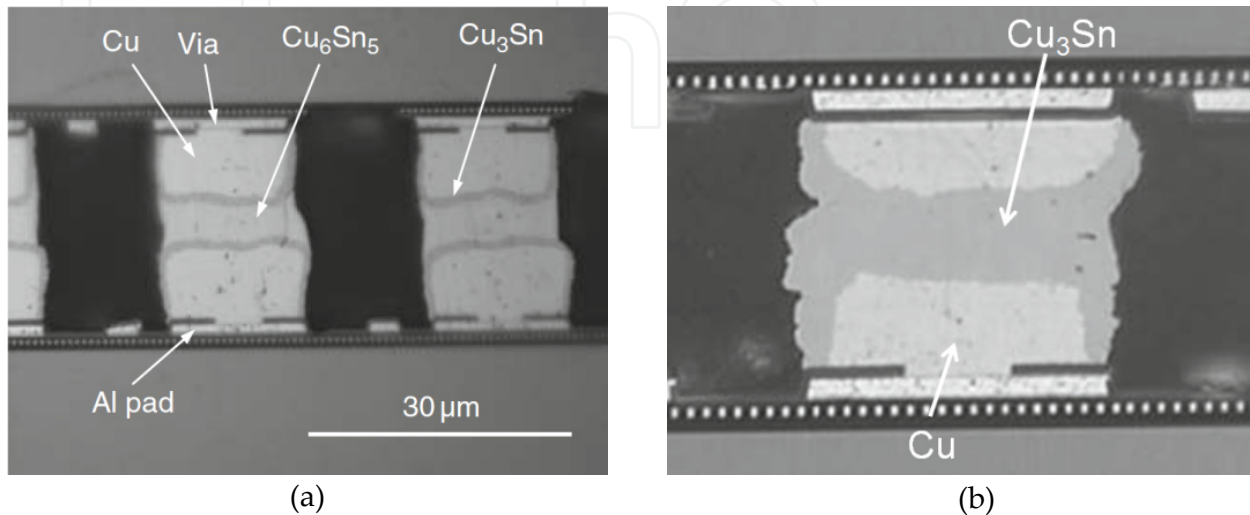


Figure 13. (a) Cross sectional view of typical intermetallic compounds formation, from η -phase Cu_6Sn_5 to ϵ -phase Cu_3Sn ; (b) Cross sectional view of completely alloyed joint, only ϵ -phase Cu_3Sn (Munding et al., 2008) [Copyright of Springer].

3.3.2.2. Temperature profile

A typical temperature profile for Cu/Sn eutectic bonding is shown in Fig. 14. Two bonding systems are widely used: Cu/Sn-Cu bonding and Cu/Sn-Sn/Cu bonding (Fig. 15). For Cu/Sn-Cu bonding system, the temperature ramping rate higher than 6°C/s (Munding et al., 2008) is preferred, since the fast ramping rate after contact is beneficial to preserve most of reactive Sn. If Sn would have reacted with Cu during this period in the Cu/Sn stack, the Sn may be insufficient at the bonding interface for subsequent Cu/Sn-Cu diffusion. In this case, the delay between Sn melting and molten Sn wetting Cu surface is the other key parameter for metal system design and determines the necessary amount of Sn in the bonding process. In general, the Cu and Sn thickness should be related as $d_{\text{Cu}} \geq 1.5d_{\text{Sn}}$. On the contrary, for Cu/Sn-Cu/Sn bonding, it is believed that a slow ramping rate is beneficial for reducing the flow of any excess Sn. More Sn would have reacted with Cu when temperature increases, and thus less pure liquid Sn is available at the bonding interface for combination (Lapadatu et al., 2010).

3.3.3. Performance of state-of-the-art eutectic bonding

The intermetallic compound formation is diffusion controlled which is directly related to the temperature. Below the melting temperature of Sn, the reaction is slow, but when the Sn begins to melt the reaction speed can be accelerated to an extremely high level. In order to control the diffusion of soldering process and to prevent solder consumption before

bonding, a thin buffer layer can be deposited between Cu and Sn. With a thin buffer layer, the bonding process begins with the slow reaction between buffer layer and the solder. Since the buffer layer is very thin, the Sn solder can diffuse into Cu in a short time. The research work by Yu *et al.* (Yu *et al.*, 2009) reports a 50nm Ni can be used as buffer layer during Cu/Sn/In eutectic bonding. A thin layer of Au has also been used for wetting and for metal layer surface protection from oxidation. During bonding, Sn and In will first wet and react with Ni layer. Alloy of Ni_3Sn_4 or NiInSn ternary phase is formed initially. Then, InSn solder starts to diffuse into Cu to form $\text{Cu}_6(\text{Sn},\text{In})_5$ compounds. Finally, all Ni atoms diffuse into $\text{Cu}_6(\text{Sn},\text{In})_5$ to form $(\text{Cu},\text{Ni})_6(\text{Sn},\text{In})_5$ phase, and $\text{Au}(\text{In},\text{Sn})_2$ is formed as a byproduct (Fig. 16). In addition, the TCT test is a very important examination for the reliability of eutectic bonding technology, since the compound has the potential risk of structural degradation caused by solder fatigue after a long term dramatic change in temperature or brittleness of the inter-metallic compound at low temperature.

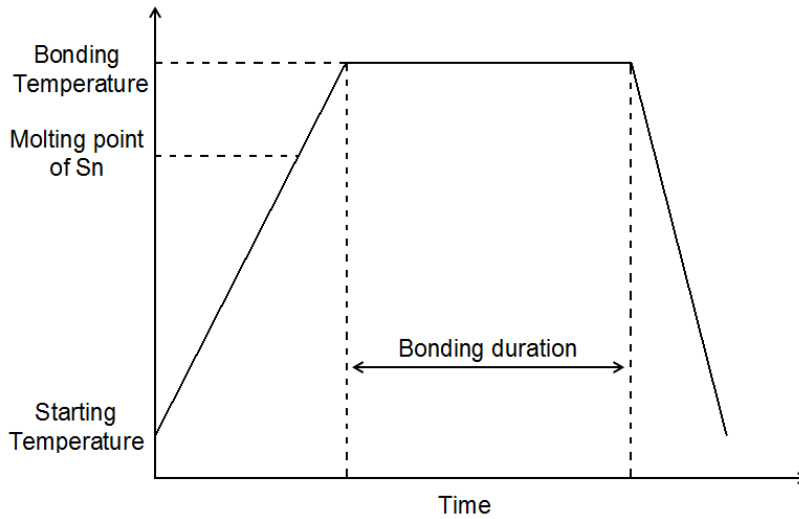


Figure 14. Schematic illustration of the temperature profile during eutectic bonding.

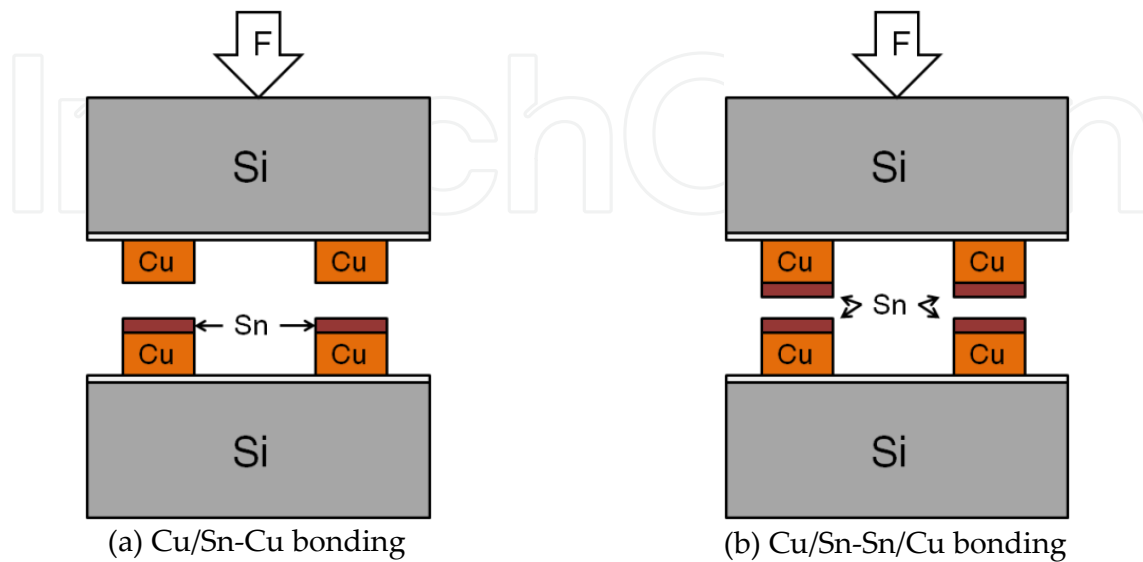


Figure 15. Different methods used in Cu/Sn eutectic bonding.

Good die shear strength and outstanding hermeticity have been obtained using Ni as the buffer layer. The average bonding strength can go up to 32 MPa and the helium leak rate with the seal ring size of 300 μm is smaller than 5×10^{-8} atm.cm³/sec which is defined as the reject limit for standard MIL-STD-883E method 1014.9. After temperature cycling test (from -40 °C to 125 °C up to 1,000 cycles) and high humidity storage (85 °C, 85% RH for 1000 hr), the bonding strength still remains above 15 MPa, and over 80% dies can still provide high hermeticity level. The research work by Liu *et al.* (Liu et al., 2011) has reported the resistance of bonded interconnects obtained by Cu/Sn bonding. The bonded interconnect shows the resistance of the order of 100 m Ω , and the excellent bonding strength of about 45 Mpa.

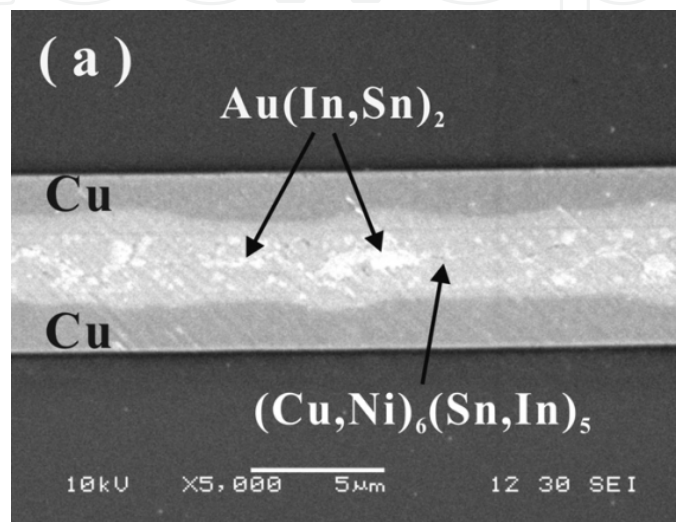


Figure 16. Interfacial microstructure of intermetallic compound joint (Yu et al., 2009) [Copyright of Elsevier].

3.4. Low temperature oxide fusion bonding

Oxide fusion bonding describes the direct bonding between wafers with or without dielectric layers. This bonding method has a stringent surface quality requirement, e.g. wafer surface needs to be smooth with small total thickness variation (TTV) and low roughness is also strictly required. Surface activation is usually performed before bonding. Subsequently, a spontaneous adhesion is firstly applied between the two wafers. Post-bond annealing allows the bonding interface to convert from hydrogen bonds to strong covalent bonds. Surface treatment method and post-bonding annealing process will be presented in detail in the following sections.

3.4.1. Surface activation before bonding

A number of surface activation methods have been investigated, include oxygen plasma bombardment, argon sputter-cleaning, and wet chemical methods with various reagent combinations such as RCA1 ($\text{H}_2\text{O} + \text{H}_2\text{O}_2 + \text{NH}_4\text{OH}$), RCA2 ($\text{H}_2\text{O} + \text{H}_2\text{O}_2 + \text{HCl}$), piranha ($\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$), etc. The original bonding surface is usually covered with a thin layer of native oxide and contaminant. When the surface is exposed to plasma or immersed in

chemical solution, the bombardment of energetic particles or the corrosion of ions removes the surface contamination. At the same time, a very thin high hydrophilic amorphous oxide layer can be formed. Following that, clean and activated surfaces are ready for subsequent hydrophilic bonding. Finally, hydrogen bonds are formed when the two surfaces are brought into contact.

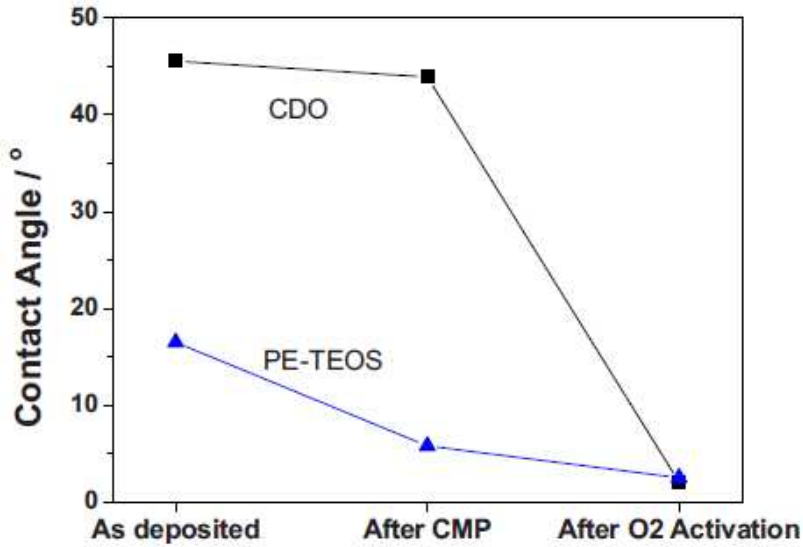
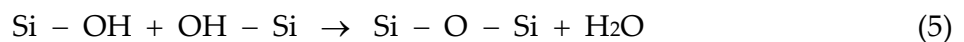


Figure 17. CA measurement for dielectric materials of PE-TEOS and low- k CDO under three different conditions, i.e., as deposited, polished, and O₂ plasma activated (Tan&Chong, 2010).

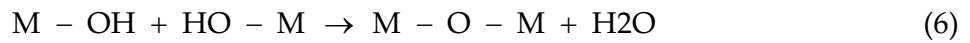
Fig. 17 shows the water droplet contact angle (CA) value of both plasma-enhanced tetraethyl orthosilicate (PE-TEOS) and carbon-doped oxide (CDO) samples for three different conditions, i.e., as deposited, after CMP, and after O₂ plasma activation with CMP. For hydrophilic wafer bonding, smaller contact angle corresponds to higher hydrophilicity of a surface, hence higher density of hydroxyl (OH) groups for hydrogen bond formation during bonding. With O₂ plasma surface activation, both PE-TEOS and CDO show a convergence of CA values to ~2.5°, resulting in a highly hydrophilic surface for fusion bonding.

3.4.2. Post-bonding anneal

For hydrophilic bonding, when two cleaned and activated wafers are brought into contact at room temperature, hydrogen bonds between hydroxyl (–OH) groups are established across the gap between the wafers. Anneal process must be applied after bonding in order to achieve a much higher bonding strength by converting the hydrogen bonds into a strong covalent bonds. The reaction of surface silanol (Si–OH) groups is enhanced during annealing based on the following equation and therefore more covalent bonds are formed:



For some high- k dielectric materials bonding, such as Al₂O₃, HfO₂, and TiO₂ which are used to achieve a higher bonding strength for a given anneal temperature and duration, their reaction during anneal can be presented as follows:



Where, M is the symbol for metal atom in high-*k* materials.

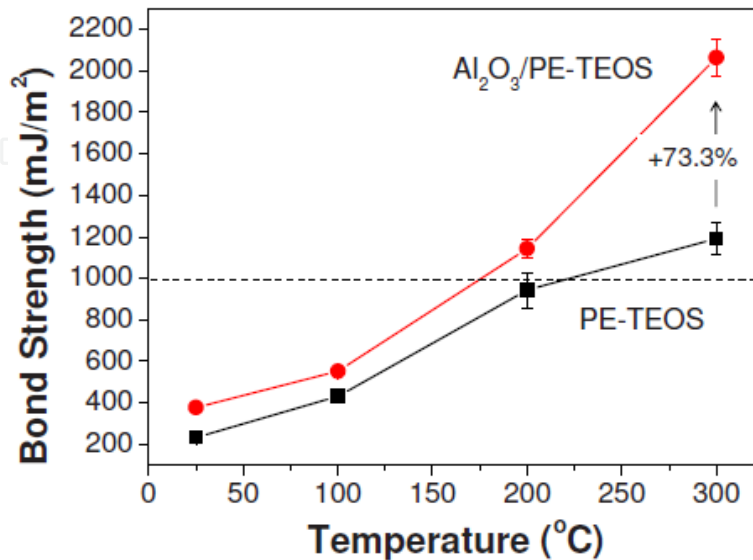


Figure 18. Variation in bond strength of PE-TEOS and Al₂O₃/PE-TEOS samples at various annealing temperatures (Chong&Tan, 2011).

Fig. 18 shows the variation in the bond strength of bonded wafers at various bonding temperatures as measured using the Maszara's crack opening method. The annealing duration is 3 hr. As expected, a higher bonding strength is achieved at a higher annealing temperature. Bonding strength is marginally improved for anneal temperature below 100°C. As the anneal temperature is increased to 200°C, significant improvements in the bonding strength are obtained. When the bonding temperature reaches 300°C, all samples present a bonding strength superior to 1 J/m² which is the minimum strength required to sustain post-bonding processes such as mechanical grinding and tetramethylammonium hydroxide (TMAH) etching (Tan&Reif, 2005). The enhancement in the bond strength value using a thin Al₂O₃ layer is most likely related to the different bond dissociation energy between Al-O-Al and Si-O-Si. Since the Si-O bond has lower bond dissociation energy (316 kJ/mol) compared with that of the Al-O bond (511 kJ/mol) at 298 K, a higher energy is required to debond wafers that are bonded with Al₂O₃.

4. Summary and conclusion

Over the past decades bonding technology has been used as the mainstream 3D integration method by various key players in America, Asia and Europe. Metal diffusion bonding and eutectic bonding are widely chosen for stacking of multiple chip layers in 3D integration as these methods allow simultaneous formation of mechanical, electrical and hermetic bonds. Although wafer-level stacking using via-first and face-to-face or face-to-back stacking method by Cu diffusion bonding technology has already been investigated with some success, high temperature (>300 °C) processing still remains a challenge. Meanwhile, a

number of research work on Cu/Sn eutectic bonding using chip-level stacking method have been demonstrated and provided high vertical interconnect density in 3D stacking. However, formation of inter-metallic compound weakens the quality and reliability of the bonds. As the metal based bonding technology can provide electrical contact, mechanical support and hermetic seal in one simultaneous step, low temperature wafer-level Cu diffusion bonding and Cu/Sn eutectic bonding technologies with inter-layer connection technology, such as TSV, present a very attractive prospect for 3D integration.

Technology development in the areas of 3D integration has resulted in a number of attractive stacking methods. In this chapter, fundamental of low temperature metal diffusion bonding and eutectic bonding technology are introduced. Cu diffusion bonding and Cu/Sn eutectic bonding are presented in details. Another bonding technology using oxide fusion between wafer pair is also exhibited, as it is widely use in the semiconductor industry. Excellent performances of these bonding technologies are shown in the chapter. Some details of processes and methodology used in the research work are included as well.

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