Chapter 3

Fabrication of Crystalline Silicon Solar Cell with Emitter Diffusion, SiNx Surface Passivation and Screen Printing of Electrode

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Additional information is available at the end of the chapter

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1. Introduction

The amount of solar energy incident on the earth surface every second (1650 TW) is higher than the combined power consumption by using oil, fossil fuel, and other sources of energy by the entire world community (< 20 TW) in 2005. The solar photovoltaic power generation are ever increasing in capacity, yet at a lower scale. Thus there is a scope of further use of solar energy to produce more electricity. For this purpose a demand for a large scale commercial production of solar cells have emerged. There is a large variety of solar cell structures proposed with various types of materials, of which p-type c-Si solar cell has been one of the most popular and widely used in commercial production with screen printing technique.

Looking back to the history of solar cell, one can find that, in 1839 Becquerel observed a light dependant voltage between two electrodes, that were immersed in an electrolyte. In 1941, first silicon based solar cell was demonstrated and 1954 is the beginning of modern solar cell research. Since then there has been several proposals for solar cell design, that can lead to various photovoltaic (PV) conversion efficiencies (η) of the solar cells. A conventional Si solar cell gives 14.7% PV efficiency[1], whereas other designs, for example, back surface field (BSF) 15.5% [2], rear local contact (RLC) solar cell efficiency ~20%, as reported by NREL. However these values are not the theoretical or experimental limit, and there is a continuous effort in improving the efficiency.

The c-Si solar cells fabricated on the high quality silicon wafers, having selective emitter on the front and local contact on the rear surface [3] shows higher η, but the required additional measures to be taken for the production of such solar cells may substantially increase the production cost.

Presently the cost of the silicon wafer alone covers >20% of the total cost of solar cell production, so there may be a technology available in future, by which a large scale production of silicon solar cells from a thin wafer (< 200μm) will be possible

2. Fabrication Process for Industrially Applicable Crystalline Silicon Solar Cells

The fabrication of our c-Si solar cell starts with a 300μm thick, (100) oriented Czochralski Si (or Cz-Si) wafer. The wafers generally have micrometer sized surface damages, that needs to be removed. After the damage removal, the wafer surface shows high optical reflectivity, for which an anti-reflection coating (ARC) is necessary. Furthermore, the top surface was textured by chemical etching before an ARC was deposited.

For a p-type c-Si substrate, an n-type top layer while for an n-type c-Si substrate a p-type top layer acts as emitter. A thermal diffusion is commonly used for emitter diffusion [4]. After the emitter diffusion, the edge isolation was carried out, as otherwise the top and the bottom surfaces of the wafers remain electrically shorted.

A suitable thin dielectric coating at the front and back of the wafers were given to passivate surface defects. As the wafer becomes covered with a dielectric layer, an electrical connection to the cell becomes necessary. Ag and Al metal electrodes were formed by using screen printing of Al pastes and co-firing at a suitable temperature.

2.1. Wafer Cleaning and Saw Damage Removal

In order to remove the organic contaminants from the c-Si wafer surfaces, we used 12% NaOCl solution and cleaned the wafers ultrasonically at room temperature (RT) for five minutes. This cleans the wafer surface with an approximate Si etching rate of 500nm/min [5]. The surface damages to the wafers were removed through isotropic etching with a concentrated solution of NaOH in de-ionized water (DI-W). DI-W helps the NaOH to break in Na+ and OH- ions in the solution. An 8% NaOH solution, at 80°C temperature for about 7 minutes of etching removes the surface damages. This saw damage removal step, etches out about 5 micro meter Si from wafer surface. After that the wafers were rinsed in HCl(10%) for 1 min, DI-W for 1 min, HF(10%) for 1 min, DI-W for 1 min.

2.2. Surface Texturing

Anisotropic chemical etching of Si (100) oriented wafers give rise to textured surface. The characteristics of the etching depends upon, time of etching, etching rate, temperature, com-

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ponents of the solution and its concentration. With a dilute NaOH solution containing isopropyl alcohol (IPA) and DI-W, the Si(100) oriented smooth wafers can grow pyramidal surface texture at 80°C temperature [6]. The surface texturing was performed by asymmetric etching of front surface of the wafers, in a dilute alkaline solution, as against the concentrated solution used for saw damage removal. The loss in mass of each wafer were estimated from the mass of the wafer measured with a microbalance before and after texturing, which subsequently led to the estimation of the etched thickness of the wafer and hence etch rate. Optical microscopic observations, SEM images, and laser scanning were the tools that were used for the characterization of the textured surface morphology. Ultraviolet visible (UV-Vis) spectrophotometry was used to estimate the retro-reflectivity of the textured surface.

The etching depends mainly on two processes. One is the rate of the reaction at the surface, and the other is the rate at which reactants diffuse into the surface. These two processes control the overall rate of the micro structural growth during the etching. The anisotropic etchants is expected to etch (110) plane at a faster rate than the (100) plane while the (111) plane etches at a slowest rate [7]. However if chemical composition of the etchant is such that some insoluble residue is formed during etching process (like oxides etc.) then diffusion of etchant into the Si will be hindered and hence etching will not happen as expected.

IPA enhances surface diffusion, so a rapid etching can take place in presence of IPA in the solution [8]. The NaOH etches silicon crystal planes differently, mostly because of different atomic concentration in different crystallographic planes. So, at a lower NaOH concentration the selective etching process helps to create textured surface of the wafer. The chemical reaction that takes place is as follows,

$$Si + 2NaOH + H_2O \rightarrow Na_2SiO_3 + 2H_2 \quad (1)$$

The sodium silicate (Na_2SiO_3) is soluble in water and thus Si surface remains devoid of any deposition. At 80°C temperature, (100) planes etch about two orders of magnitude faster than (111) planes [9]. For a (100) silicon wafer, a solution of NaOH, IPA, DI-W creates square based four sided pyramids consisting of sections of (111) planes which form internal angles of 54.7° with the (100) surface.

The degree of isotropy is sensitive to the concentration of the solution. While a 8% NaOH solution at 80°C temperature etches silicon isotropically to achieve a polished wafer surface, a 2% NaOH, 8% IPA solution at 80°C temperature etches anisotropically to a square based pyramidal surface texture.

2.3. Phosphorus Diffusion for p-n Junction Formation

The thermal diffusion of phosphorus is necessary to create an n-type emitter to the p-type wafer. The diffusion depends on various factors, of which temperature and gaseous environment is most important [10]. In oxygen environment and at 850°C temperature, the diffusion coefficient (D) can be approximated as D~0.0013μm^2/hr. The phosphorus diffusion

leads to formation of n+ type emitter at the top surface of the wafer. The diffusion was carried out in two stages, pre-deposition and drive-in [11-13]. At the pre-deposition stage, liquid $POCl_3$ was evaporated by bubbling N_2 gas into the liquid. The $POCl_3$ evaporates and gets deposited at the surface of the wafers. In presence of oxygen, phosphosilicate glass (PSG) is formed at the 850°C temperature. Phosphosilicate glass or PSG is phosphorus doped silicon dioxide, a hard material formed at the top surface of Si wafer. PSG formation rate is about 15nm in 30 minutes.

After that, in the drive-in stage, the wafers were heated at 850°C temperature for 7 mins, 0.3Torr pressure in presence of oxygen, when the P atoms from the n+-type top layer diffuses deeper into the wafer, forming a deeper junction. Details of the reaction is given below

$$POCl_3(\text{liquid}) + N_2(\text{bubble}) \rightarrow POCl_3(\text{vapor}) \quad (\text{pre}-\text{deposition}) \tag{2}$$

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \tag{3}$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \ (\text{drive-in}) \tag{4}$$

$$P + 3Si \rightarrow n-\text{type doped Si} \tag{5}$$

For gaseous diffusion with $POCl_3$, the p-type silicon wafers were loaded into a quartz boat, which was slowly moved into the middle of a fused quartz tube in a heated horizontal furnace. The boat, which can hold tens of wafers, was moved slowly into the tube so that the wafers do not suffer large temperature gradients and warping. Furnace temperature for the diffusion was held at about 800°C, with a variation across the length of the boat of not more than 2°C.

When the PSG was deposited in the pre-deposition stage, the dopant profile leads to a shallow junction depth and a high surface concentration. In the drive-in stage, a deeper junction was formed as phosphorus atoms diffuse deeper, thus thicker emitter and a lower surface concentration of dopant was achieved. The junction depth is defined as the depth where the phosphorus and boron concentrations are equal (as boron already existed in p-Si wafers).

Table 1 shows details of P-diffusion process. A shorter pre-deposition of only 7 minutes at 850°C and a drive-in of about 20 min at 850°C temperature, shows good result. It is to be noted that, a relatively deeper junction and the dead layer near the top wafer surface degrade blue response of solar cells. The PSG was removed by washing the wafer in a 10% HF solution for one minute.

The heated quartz tube, used for pre-deposition and drive-in, were periodically cleaned with HCl vapor in an N_2 stream.

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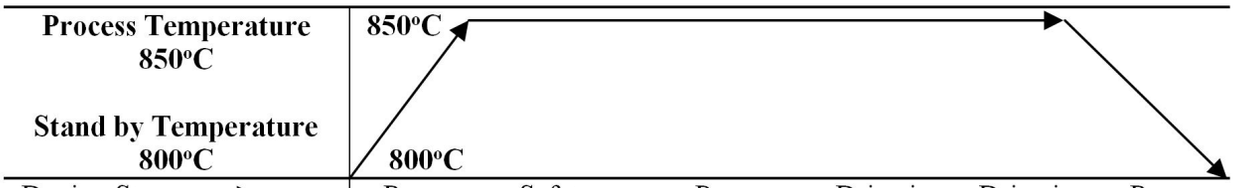

Doping Step → / Conditions ↓	Ramp up	Safety time	Pre-deposition	Drive in i	Drive in ii	Ramp down
N_2 flow rates (lpm)	5	5	5	5		5
O_2 flow rates	1	1	600 sccm	1	1	
$POCl_3$ flow rates			1200 sccm			
Time (min)	5	3	7	3	3	5

Table 1. A typical condition for phosphorus diffusion used in this study, using $POCl_3$ vapor as a source gas, here 'lpm' stands for liter per minutes.

2.4. Edge Isolation by Wet Chemical Etching

The edge isolation was carried out after screep printing of acid barrier paste as a mask, by the reactive ion etching [14-15]. However, it can also be performed by wet etching [16-17] with HF, HNO_3 and CH_3COOH acidic solution in the 1:3:1 volume ratio. Then the wafers were dipped into the acid solution for 1.5 – 2 minutes, after which the stack was rinsed in DI-W. Then the wafers were thoroughly rinsed with DI-W for five minutes and later spin dried to make it ready for silicon nitride film deposition.

2.5. Antireflection Coating and Front Surface Passivation

Light reflection as well as electronic defects at the front surface are undesirable, that needs to be minimized. The hydrogenated SiNx layer also acts as a high quality silicon surface passivator [18]. It has been observed that, more than 35% of the incident light gets reflected back from a bare silicon surface, and a significant amount of incident light reflects from the silicon surface even after surface texturing. For a single layer ARC, the wavelength (λ_0) at which the anti-reflection is most effective at normal incidence, can be expressed as: $\lambda_0 = 4\mu_1 d_1$, where μ_1 and d_1 are refractive index, and thickness of the ARC respectively. The reflectance R of the top surface of a solar cell is given by : $R = [(\mu_1^2 - \mu_o\mu_2) / (\mu_1^2 + \mu_0\mu_2)]^2$, where μ_o and μ_2 are the refractive indices of the medium above the ARC and that of the substrate below the ARC, respectively. For zero reflectance, i.e. R = 0, it gives: $\mu_1 = (\mu_o\mu_2)^{1/2}$. At λ = 550 nm, the desired thickness of silicon nitride film with μ_1 = 1.96 would be 700 Å, taking air (μ = 1) as ambient above the cells [19]. The thicknesses and refractive indices of the SiNx films prepared by PECVD under different gas flow ratios were characterized by Spectroscopic Ellipsometry.

The parameters for the SiNx depositions were: chamber pressure 0.6 Torr, deposition temperature 300°C, RF power density 0.08 W cm^{-2} at a 13.56 MHz frequency, silane (SiH_4) and ammonia (NH_3) source gases, deposition time 4 minutes, with deposition rate of 3 Å/s. The Si atom of SiNx mostly comes from silane source gas in RF PECVD process, following the reaction, $3\,SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$.

SiNx can also be deposited on Si surface through forming gas annealing at a higher temperature. Forming gas is a mixture of hydrogen (H_2) and nitrogen (N_2), that were obtained by dissociating ammonia (NH_3) at high temperature. In this case the Si atom of SiNx come from the surface atoms of Si wafer. However, due to higher process temperature, this method was avoided, as a higher process temperature may alter distribution of phosphorus atoms and hence the junction depth.

The recombination rate (U_s) at the surface, with surface recombination velocity (S), is related to excess concentration of minority carriers (Δn_s) at the surface. $U_s \equiv S\,\Delta\, n_{s.}$ Therefore, the recombination can be minimized by a reduction of minority carrier type at the surface. Using high-low junction n^+pp^+ structure the minority carriers at the surface can be reduced [20]. This technology, known as back surface field (BSF), is widely used at the rear surface of solar cells. Another method is the field effect passivation. The fixed charges in a passivation layer repel the minority carriers or the extremely large fixed charges bend the energy band, resulting in an inverting layer at the surface.

The effective lifetime of charge carrier can reflect total effect of bulk and surface recombination. For the p-type silicon wafer of thickness W and diffusion coefficient of electron D_n, having front and back surfaces equally passivated, the effective lifetime (τ_{eff}) can be expressed as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{W} \quad \text{for} \quad \frac{SW}{D_n} < \frac{1}{4} \quad \left(\text{Low recombination}\right) \tag{6}$$

and

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + D_n\left(\frac{\Pi}{W}\right)^2 \quad \text{for} \quad \frac{SW}{D_n} > 100 \quad \left(\text{High recombination}\right) \tag{7}$$

where τ_b is minority carrier lifetime at the back surface. By combining the two cases, the effective lifetime can be calculated by using above equations with about 5 % deviation from the exact solution [21]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \left[\frac{2S}{W} + D_n\left(\frac{\Pi}{W}\right)^2\right] \tag{8}$$

If the parameters, such as bulk lifetime of silicon (Π), wafer thickness, and diffusion co-efficient of electron are considered to be constant, the measure of effective lifetime gives the direct measure of S. As the S is an indicator of surface passivation, the measured τ_{eff} can also be used as an indicator of the quality of surface passivation in silicon substrate.

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2.6. Metallization

In order to reduce the production cost of the photovoltaic solar cell, metallization was realized by screen-printing of metal paste on the SiNx coating, followed by a co-firing. Another competing technology for solar cell production is buried-contact technology, that involves laser grooving and metal plating, which is a bit complex procedure, time consuming and may result in a significantly high number of faulty solar cells, because of small imperfection in metallizations, a kind of imperfection that does not make screen printed solar cells faulty.

Screen-printing (SP) is cost effective, robust, simple, inexpensive, and fast method of metallization of the solar cells [22-23]. It can also be easily automated with a high throughput (exceeding about 1,000 wafers per hour). This technique has been widely used for solar cell fabrication since the early 1970s.

For selective emitter formation at the back, etchant material was screen printed before screen printing the metal paste. During the co-firing process the necessary electronic connection of the cell layers with the electrodes were formed. We used the Ferro- 53-102 aluminum paste and Ferro-33-462 as Ag paste.

Baking of the screen printed wafers were carried out immediately after each printing step in a separate conveyor belt furnace at 150°C. A burn-out process removes the organic binders from the paste and it was carried out between 350 ~ 510°C.

The thickness of the Al over the entire back surface of the cell was maintained almost uniform with a variation of ± 2 μm. Wafer bowing is a problem with full Al printing at the back of the wafer, that was minimized to a level below 0.5 mm due to the use the low bow, lead free paste and a thicker wafer (300μm). Bowing happens mainly due to difference in the thermal expansion coefficients of Si and Al pastes (α_{Si} = 7.6 K^{-1}, α_{Al} = 23.8 K^{-1}) and can be avoided by the local back contact (LBC) approach. For the application of this LBC technique in industrial production, an addition step of Ag / Al printing in a pattern of two wide bus bars on the back surface was introduced in order to make back metal contact solderable during the module making process. Despite the simplicity and technical advantages of this process for making fully covered back metal contact and surface passivation through back surface field (BSF) in a single shot, the emerging trend of using thinner wafers to meet the challenges posed by depleting silicon feedstock may put this process at stake.

A problem of Aluminum ball formation was observed during the co-firing process, that was mostly eliminated by flowing sufficient oxygen during the co-firing and also by applying a rapid cooling approach at the end of co-firing.

Metallization is a very important step for device fabrication because it strongly affects performance of the solar cell on its short circuit current density (J_{sc}), open circuit voltage (V_{oc}), series resistance (R_s), shunt resistance (R_{sh}), and fill factor (FF). At the front surface the metallization creates electrical connection to thin n+ layer that is covered with SiNx. At the back surface it provides an electrical connection and at the same time it creates a p+ layer. A glass frit present in the Ag paste makes a superior metallization through SiNx film. However, optimization of the co-firing process is critical in obtaining desired metal contact. The peak tem-

perature and ramp-up rate during the co-firing process are crucial along with the belt speed that determines residual time of the wafers to various temperature zones. A cylindrical process zone has different local temperature setting and the belt carries the Si wafers at a certain speed. The grid pattern of the front electrode has a significant influence on R_s and FF, that demands optimization of co-firing process. With an increase in the sheet resistance (R_{sheet}) of the emitters, V_{oc} decreases, however J_{sc} increases, which may be because of the improvement of blue-response, more light entering the solar cell active region and the reduction of recombination in the front surface. At a faster co-firing condition BSF layers and Ohmic front contacts can preferably be established, because the R_{sheet} of emitters may remain nearly unchanged. We observed a V_{oc} of around 622mV and FF of 80.6% by Suns-V_{oc} measurement.

Suns-V_{oc} measurement is a method of estimating open circuit voltage from decay characteristics of photo generated charge carriers. This method is generally adopted when physical dimension of solar cell is different from its standard cell structure. Using the result, we obtain an optimized co-firing process.

Fig 1 shows important components of screen printing. The screen is made up of an interwoven mesh kept at a high tension, with an organic emulsion layer defining the printing pattern. Fig. 1(a) shows a microscopic image of the screen. Printing pattern of the front metal contact with optimized dimensions (finger width, finger spacing, busbar width, maximum defined finger length) was developed in the form of a computer- aided – design (CAD) as shown in Fig. 1(b). The screen printer is equipped with optical vision system for proper alignment. The co-firing was carried out in a conveyor belt furnace (Sierratherm).

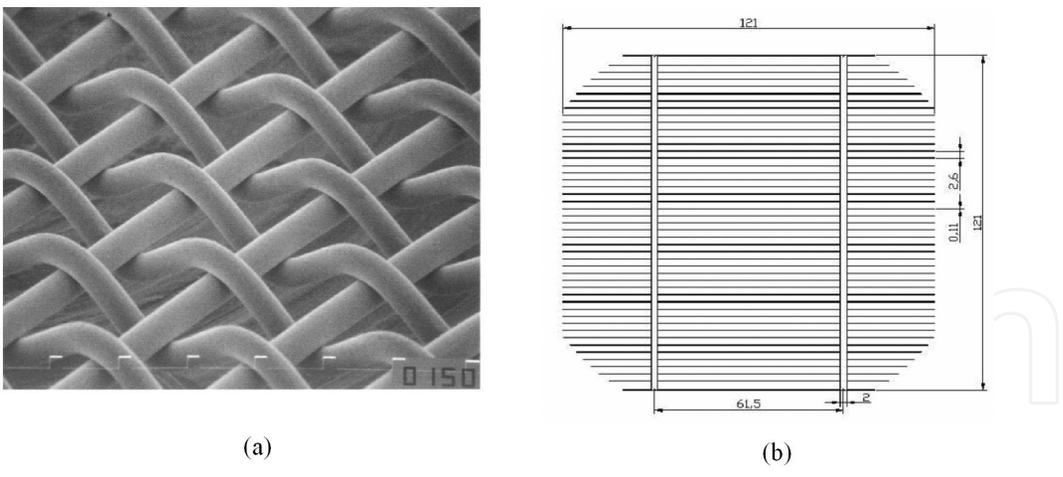

Figure 1. a) Microscopic image of the screen used in SP. (b) Design of the front metal printing pattern for the single c-Si wafer of size 125mm × 125mm (pseudo square).

2.6.1. Back Metallization by Screen printing

Rear surface of solar cells were screen printed with Aluminum paste (Ferro- 53-102). The thickness of the printed metal was maintained 20μm, with a variation of ±2μm. The average gain in mass of the wafer after back printing and drying was ~ 6 mg /cm^2.

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2.6.2. Co-firing of Screen Printed Pastes

Co-firing of printed metal paste was followed in three major steps, baking, burn- out, and sintering. Baking refers to the process of evaporating solvents of the pastes to avoid the gas bubbling and cracks formation during the high temperature treatment. The baking is carried out immediately after each metal printing step in a separate conveyor belt furnace at 150°C. Burn- out process removes the organic binders from the paste and it was carried out at 350-510°C.

The temperature profile for the co-firing cycle can be decided on the basis of the studies of Kim et. al [24]. With improper temperature and the belt speed settings of the co-firing, the metal electrodes can penetrate across the p-n junction, as schematically shown in Fig. 2, thus making the cell unusable.

The belt furnace used in this system was equipped with the facility to observe and adjust the actual front and back surface temperatures of the wafer by real time measurement, with two different thermocouples. As suggested in ref [24], we tested the co-firing with different temperatures of front and back surface. However, such a temperature difference may lead to bending of the wafer. So we prefer keeping the temperature of both the surfaces as equal. Proper Ohmic contact formation on the front and Al-Si alloying at back surface for proper BSF generation are the two significant accomplishments of this single shot method.

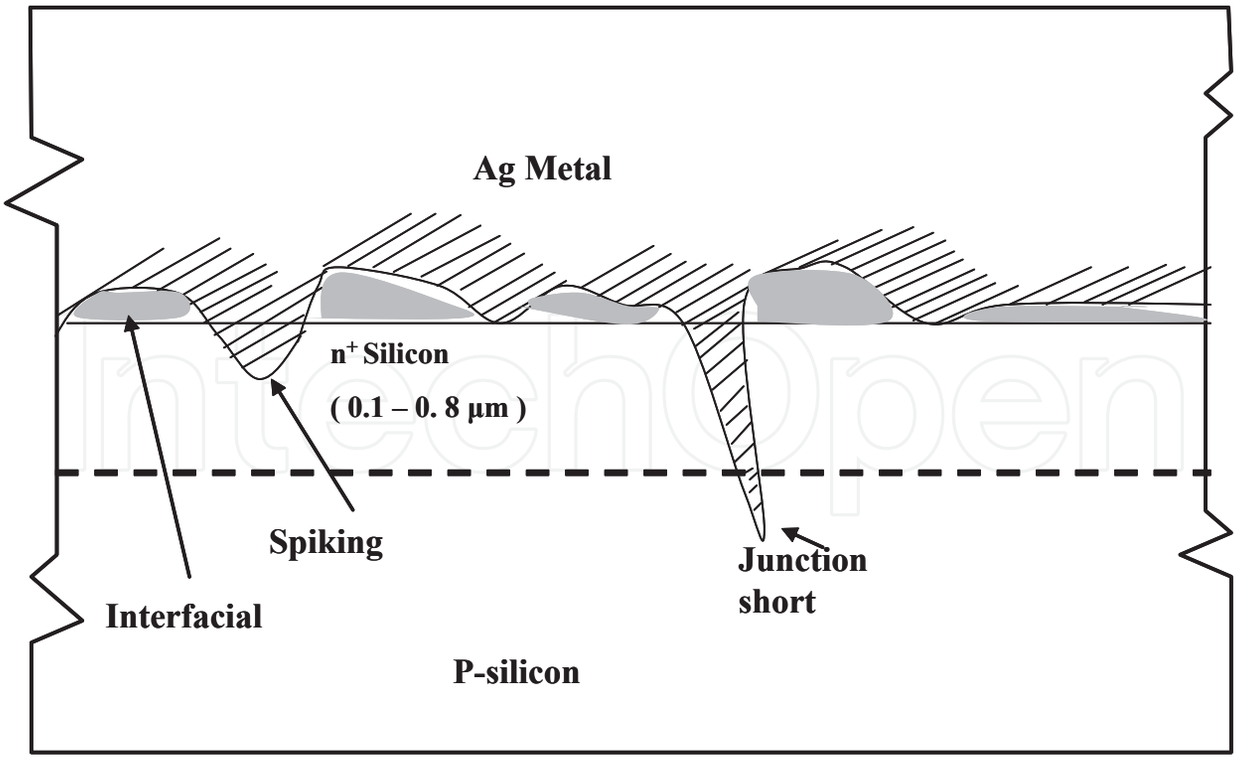

Figure 2. P-N junction of a typical solar cell with Ag metallization on front surface showing the possible cases of shunting through the p-n junction during co-firing as well as good sintering.

The co-firing was carried out in the condition of sufficient dry and filtered air flow into the furnace. It is one of the most sensitive steps of the solar cell fabrication. Any non-uniformity in surface cleaning, texturing, doping, or even ARC can have detrimental effect on the performance of the fabricated cells as well, especially in industrial process. If co-firing is done at a temperature below optimum temperature profile, it results in high series resistance and hence low FF due to poor Ohmic front contact and poor BSF, whereas over – co-firing at a higher temperature profile may result in junction shunting and degradation in surface and bulk passivation. Thus, finding an optimum co-firing temperature profile should be always the first priority in the industrial process.

An advantage of an LBSF compared to the standard full Al-BSF is the lower consumption of expensive printing pastes. In order to accomplish the local back contact in solar cells, many techniques have already been employed. It has been shown that the hybrid buried contact solar cell with photo lithographically defined rear contacts achieves an increase in V_{oc} by 30mV [25] as compared with a standard buried contact cell with conventional aluminum alloyed BSF, which may result in a high rear surface recombination velocity. Koschier et al. [26] also demonstrated a 30 to 40mV increase in open circuit voltage relative to conventional buried contact solar cells using the thyristor structure device on the rear which incorporates a grown p^+ layer in localized regions of the passivating oxide. However, both these rear contact schemes require the use of photolithography to remove regions of the oxide to expose the underlying surface for contact, which may not be suitable for large-scale commercial solar cell fabrication processes. Other techniques of creating small area contacts such as laser firing have been demonstrated to be feasible [27].

2.6.3. Study of rear surface passivation with SiNx film

Recombination of charge carriers at the rear surface in a solar cell can be suppressed by deposition of a silicon dioxide (SiO_2) layer at the back surface, grown in a high-temperature (≥900°C) oxidation process [28-29]. Additionally, the SiO_2/Al stack at the rear should act as a reflector for the near band gap photons, that leads to improved light trapping properties and hence the J_{sc} of the solar cell may improve as well. Thermally grown SiO_2 layers are manufactured using a time and energy intensive high temperature process, they may not be a good choice for mass production, although they possibly provide a good thermally stable passivation [30]. Hence, an alternative low temperature surface passivation became necessary for future industrial production of high efficiency Si solar cells, which should have properties comparable to the SiO_2 passivated solar cells.

One way of achieving this is deposition of SiNx layer by PECVD technique. It has been observed that this gives comparably low surface recombination velocity (SRVs) as compared to that with a thermal SiO_2 on low resistivity p-type silicon [31-32]. However, conventional studies have mentioned certain limitations of a SiNx layer on p-type substrates [33]. When it was applied to the rear of a PERC (Passivated Emitter and Rear Cell) solar cell, the short circuit current density (J_{sc}) reduced as compared to a SiO_2 passivated cell [34]. This effect has been attributed to the large density of the fixed positive charges in the SiNx layer, inducing an inversion layer in the c-Si near the SiNx layer. A capacitance-voltage (C-V) measurement

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of SiNx layer having variation of refractive index may demonstrate a part of improvement with Si-rich SiNx thin film. This may be because of field created by positive charges fixed at its surface. It is clear that a positive fixed charge is suitable for the n-type substrate, while a negative fixed charge is suitable for the p-type c-Si wafer substrate.

In this respect formation of local back contact is a promising technique, where a highly doped p-type local back contact can reduce the potential barrier that charge carriers may face before reaching the metal electrode.

Protection of the back surface of the Si-wafer may be achieved in two possible different ways, one is a complete coverage with Al back contact, and the other is with SiN_x anti reflection coating. The problem with full metal coverage with thinner Si wafers is the cracks and lattice defects formed during high temperature co-firing when there is high possibility of wafer bending. Thus partial coverage of the back surface with metal electrode and the rest covered by SiN_x ARC surface passivator is a better alternative.

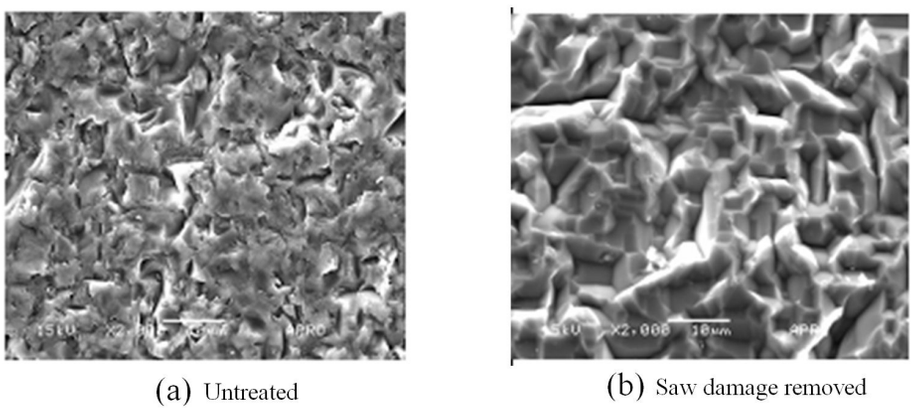

Figure 3. Comparison of SEM micrograph of the (a) saw damaged wafer surface, unclean and (b) saw damage removed clean surface of Cz-Si wafer.

3. Measurement Results for c-Si Solar Cells

3.1. Wafer Cleaning and Saw Damage Removal

The scanning electron microscopic (SEM) surface image of one of the cleaned and surface damage removed wafers is shown in Fig. 3. It shows image of untreated as well as wet chemical etched wafer surface where saw damages have been removed.

3.2. Surface Texturing

Since the concentration limit for anisotropic etching of surface texturing is 1.6 to 4 wt.%, the concentration of NaOH (wt. %) in the etchant solution was chosen as 2 wt.%. At a different etching time the resulting surface texture and specular reflection were different. For an etch-

ing/texturing time of 25, 30, 35, 40 mins, the average specular reflectivities were 17.2, 17.0, 16.1, 15.1%.

Fig. 4 (a), (b), (c) and (d) shows textured wafers with the four different texturing times and depict the increase in pyramid size with increase in etching time. The average heights of the pyramids on the surface textured for 25, 30, 35, and 40 min were estimated to be ~ 3, 5, 7, and 10 μm, respectively.

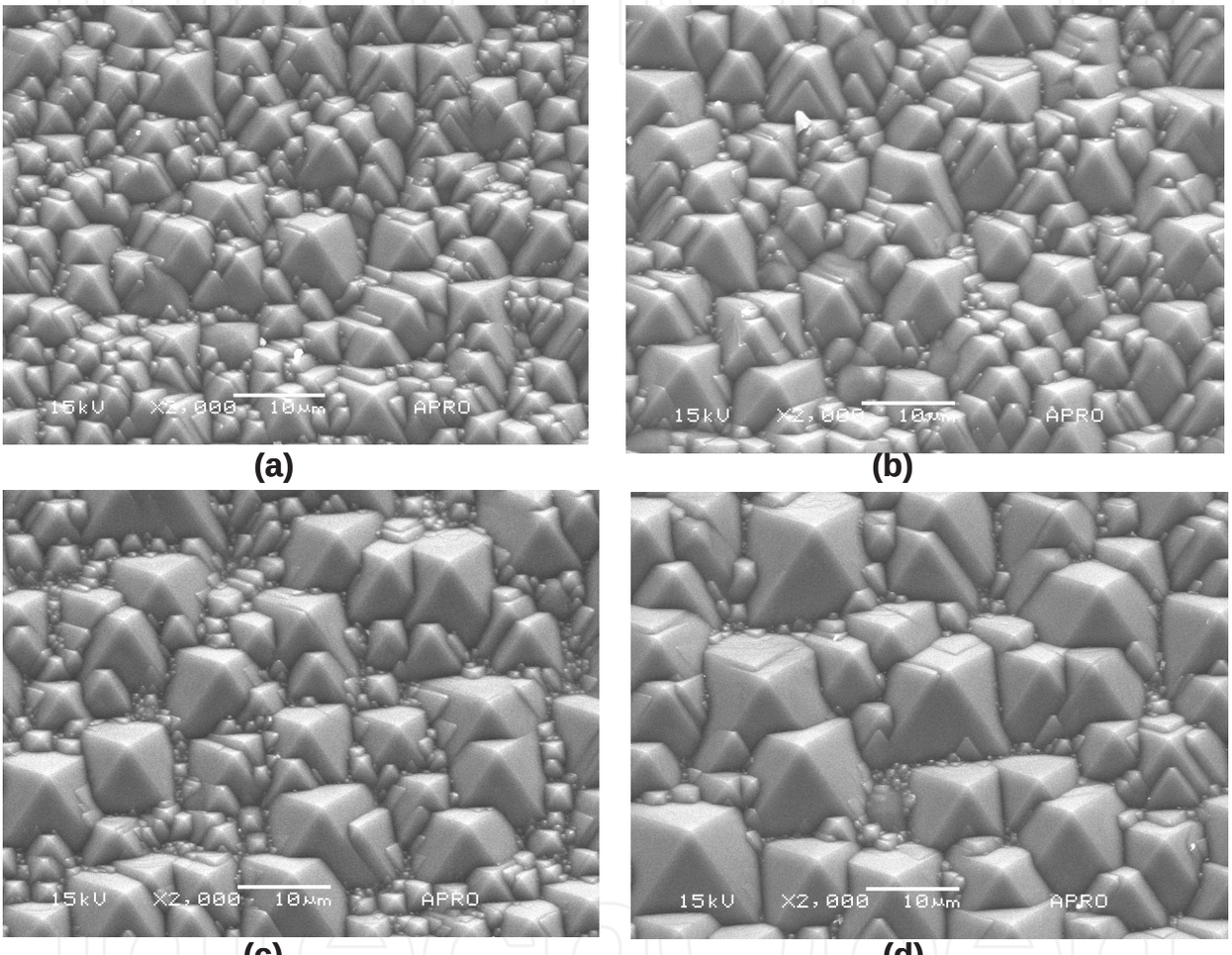

Figure 4. SEM micrographs of the silicon surface textured for (a) 25 min, (b) 30 min, (c) 35 min, and (d) 40 min in and solution containing NaOH (2 wt. %) in DI-W water and IPA (6 wt. %) at 82°C.

3.3. Phosphorus Diffusion for p-n Junction Formation

After the texturing, the emitter diffusion and PSG removal were carried out. Then the wafers were rinsed in DI-W and spin dryed. A secondary ion mass spectrometric (SIMS) depth profiling was carried out to measure the emitter junction depth. Fig. 5 shows depth profiling of P atoms observed by (SIMS) into the c-Si wafer. 5×10^{15} cm^{-3} seems to be the boron concentration of the p-type wafer, with junction depth of about 300 nm from the top surface.

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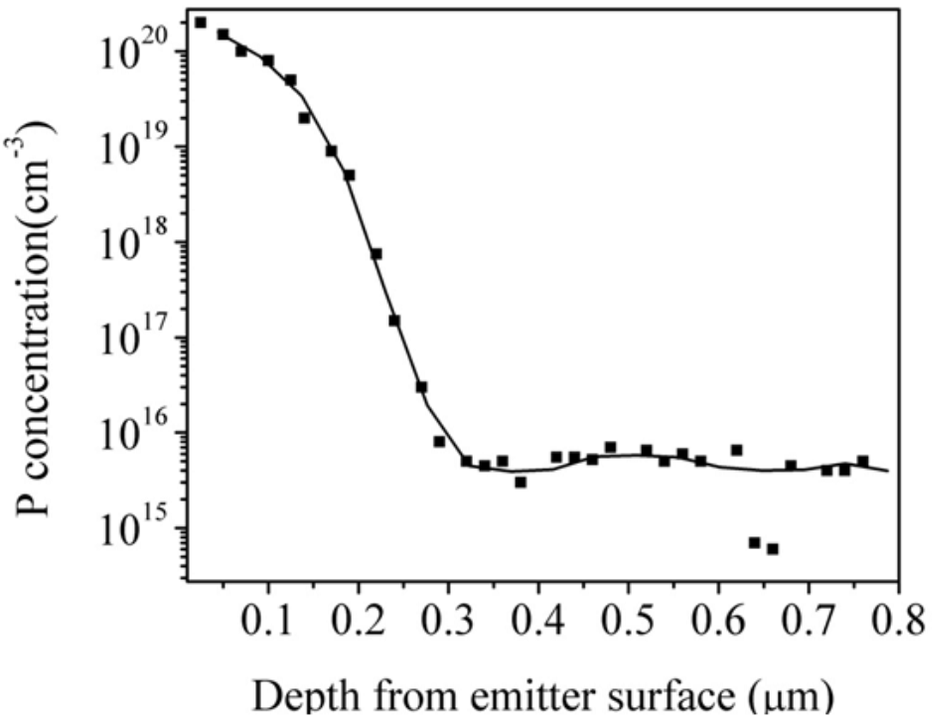

Figure 5. Variation of phosphorus (P) concentration with the distance from the emitter surface into the wafer, As observed by SIMS depth profiling.

The diffusion profile can be expressed as a complimentary error function.

3.4. Antireflection Coating and Front Surface Passivation

There is a trade off between good antireflective property and surface passivation. From high frequency capacitance-voltage (C–V) measurements with metal-insulator-semiconductor (MIS) structure as Al/SiN*x*:H /*p*-type Si, one can get the electrical properties of the SiNx film. It was observed that there was a distinct charge accumulation, depletion and inversion region in the MIS capacitor. The forward and reverse traces of the C–V curve exhibits anticlockwise hysteresis, which indicates the injection of holes into the silicon nitride film [35-36], which can also be associated with silicon dangling bonds (Si-N_3) [37]. The interface state density can be calculated using Terman's analysis [38] from the high frequency C–V measurements. Properties of deposited SiNx films are given in Table 2. The energy dependent trap densities (D_{it}) for as deposited SiNx films, and that fired at 600, 700, 800°C temperatures were 8.0 × 10^{11}, 1.4 × 10^{11}, 5 × 10^{10}, 1.1 × 10^{10} cm^2/eV respectively, for SiNx film of thickness 700 Å and refractive index 2.0. The effect of surface passivation on sheet resistance is shown in Table 3. It shows that at a higher O_2/$POCl_3$ flow rate the sheet resistance becomes lower. When the wafers were annealed at a temperature of 600°C, the D_{it} of the SiNx films with refractive indices 1.9, 2.0, 2.1, 2.2, 2.3 were 8.16 × 10^{10}, 1.40 × 10^{11}, 3.36 × 10^{11}, 5.00 × 10^{11}, 8.60 × 10^{11} cm^2/eV.

NH_3 Flow (sccm)	SiH_4 Flow (sccm)	Refractive index	Deposition rate (Å /s)
60	18	1.8	2.33
60	30	1.9	2.86
60	45	2.0	4.10
60	60	2.1	4.26
60	66	2.2	4.05
60	75	2.3	4.00

Table 2. Gas Composition in the plasma and the corresponding properties of the as- deposited films. Pressure 1 Torr, substrate temperature 450°C, thickness 80nm.

[O]	$[POCl_3]$	R_{sb} (Ω/sq)	R_{sa} (Ω/sq)
300	600	70.5	65.5
400	800	69	64.5
500	100	68.7	63.0
600	1200	65.5	62

Table 3. Comparison of emitter sheet resistance before and after the drive in step for the various different gas flow rates, where [O] is O_2 flow rate and $[POCl_3]$ is $POCl_3$ flow rate in sccm, R_{sb} is sheet resistance before passivation, R_{sa} is sheet resistance after passivation.

3.4.1. Carrier lifetime measurement

Carrier lifetime measurement can provide valuable information. We used a μ-PCD system of Semilab (WT-1000) in order to measure the carrier lifetime of the silicon wafers at various stages, with a measurement precision of ± 0.01 μs. A 940 nm wavelength laser pulse was used for generation of the photo carriers, and all the measurements were carried out in automatic parameter setting mode. The minority carrier effective lifetime of the bare wafers were measured first, thereafter (prior to metallization) the measurements of effective lifetime of silicon wafer were carried out.

3.4.2. Effect of different passivating layer on carrier lifetime

Different passivating layers such as silicon nitride (SiNx), silicon oxide (SiO_x), amorphous silicon (a-Si), microcrystalline silicon (μc-Si), oxidized aluminum nitride (AlON), and oxidized porous silicon (PS) were deposited on the surfaces of the wafers. Minority carrier lifetime was measured at least three different places of each wafer and mean of the results were taken. The results were then compared with the minority carrier effective lifetime of the bare wafer for further analysis.

We observed that the effective lifetime of each of the wafers increases by ~ 2 μs after cleaning and texturing. This improvement is attributed to the removal of contaminants and structural defects from the silicon surface after cleaning and saw damage removal. A significant

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improvement in lifetime, from ~ 6 μs to more than 10 μs, was observed after the phosphorus diffusion. This improvement reflects the increase in bulk as well as surface recombination lifetime during phosphorus diffusion. The thermal oxide passivation step after phosphorus diffusion causes further improvement in lifetime of about ~ 3 μs. This improvement can be attributed to the decrease of surface recombination velocity due to the passivation of surface by the thermally grown SiO_2 layer. The subsequent process of edge isolation by SF_6 plasma causes degradation in the lifetime by ~ 1 μs. Such a degradation is basically due to plasma induced damages, especially near the edges of the wafers that indicates the formation of recombination centers on the surface during the process. A sharp rise in lifetime by ~ 3 μs was observed after deposition of non-stoichiometric TiOx films [39-40]. It is likely that fixed positive charges in these films bend the semiconductor energy bands near the surface of the wafer, which improves the effective surface passivation [41]. A good surface passivation can be achieved by growing a thin thermal SiO_2 passivation layer over TiO_2 [39,42,43]. The variation in the minority carrier lifetime during the solar cell fabrication, indicates that the surface conditions play a vital role than the bulk of the Cz-Si wafers. During the solar cell fabrication and before metallization there might have been the improvement in the lifetime due to gettering of the impurities from the bulk during phosphorus doping. The SiNx films had a refractive index between 1.90 and 2.13 and a thickness of 65 nm after annealing in the 673-1173 K temperature range. The effective lifetime of the samples became maximum for the samples annealed at 773 K, while the lifetime of almost all samples, covered with as-grown film, showed a minimum value.

The out-diffusion of hydrogen from the Si-SiNx interface might cause degradation of lifetime of the samples if annealed above 773 K in vacuum. The maximum recorded effective lifetime for the sample passivated with SiNx with a refractive index of 1.94, annealed at 773 K was 55.21 μs whereas a minimum lifetime of 6.3 μs was found for the sample with as-deposited SiNx film with refractive index 1.9.

The minority carrier lifetime with different passivating films as AlON, Bare Si, Poly Si, μc-Si, SiOx, a-Si, SiNx were 9.6, 10.1, 21.5, 23.6, 43.4, 51.0, 55.2 μs respectively, where all the samples were annealed at 773 K in vacuum.

The comparison of surface passivation of the electronic grade Cz-Si wafers with the different passivating layers indicates that the SiNx film is superior to other films. In order to identify the appropriate properties and annealing condition of the SiNx films for solar cell application, the effective lifetimes of samples, coated with PECVD grown SiNx film, were measured after annealing at a pressure of ~ 10^5Pa for ~ 90sec and at temperatures, varying from 500 to 900°C in air ambience of a belt furnace. The minority carrier effective lifetime of the silicon wafers, after the surface passivation with SiNx films and annealed at 500, 600, 700, 800, 900°C results in the lifetime of 42, 43, 85, 115, 64μs respectively. The annealing temperature for optimized carrier lifetime was found to be the same (760°C) as the set temperature of the belt furnace at which c-Si solar cell was earlier optimized for co-firing to ensure good Ohmic contact on the front and back surfaces in conjunction with the proper back surface field (BSF) generation. Minority-carrier lifetime is a critical parameter for all solar cell designs. If the silicon wafers to be used for the fabrication of solar cell has a low minority carrier life-

time, therefore a short diffusion length, most of the minority carriers cannot be collected, and the solar cell will suffer from low conversion efficiency.

The results of this study indicate that the proper surface as well as bulk passivation in conjunction with gettering of defects during phosphorus diffusion can lead to a substantial gain in minority carrier effective lifetime of silicon wafers, provided the degradation of wafer surface condition during edge isolation is prevented.

3.5. Metallization

3.5.1. Effect of Co-firing Temperature on Solar Cell Performance

In order to optimize the co-firing we defined four different temperature zones in the furnace. We investigated each zone, changed stay time of the wafers in each zone, by varying the belt speed and the temperature of the zones. Emitters were formed with the sheet resistance in the range of 30 to 60Ω/sq. A uniform 80nm thick SiNx layer deposited on the front side served as an anti-reflection coating. Back and front contacts were screen printed on the wafers and baked. The back contacts were screen printed first, using Al paste, and then the wafers were dried at 150°C for 4min in a belt dryer. Then the front contacts were printed with Ag paste and the same post-printing treatment was carried out. Then the wafers were co-fired in a conventional belt-type furnace with four different temperature zones. For the maximization of the Suns-V_{oc} we varied the temperatures T1, T2, T3, and T4 of the four thermal zones. When an optimum temperature distribution was found, we investigated different belt speeds keeping the temperature unchanged. By measuring Suns-V_{oc}, we determine the effect of peak temperature change on the FF and V_{oc}. We measured the co-firing temperatures on the wafers directly in the belt-type furnace with a Datapaq 9000 system, which has a thin, sensitive thermo couple tip and a thermally insulated measuring system pack for recording the firing conditions of a wafer with a thermo couple tip on it. In the first set of experiment, without a front electrode, we varied the temperatures T1, T2, T3, and T4 in the four thermal zones and measured the Suns-V_{oc}.

In the second set of experiments, we examined the effect of varying only the belt speed 170, 140, 165 and 160 inch per minute (IPM) on the V_{oc} for the same sheet resistance. In this step, we used wafers of 2–4 μm texture, sheet resistance of 35 to 40 Ω/sq. and 80μm width of finger with 2.4mm spacing metallization.

In the third set of experiments, we investigated the variation in the V_{oc} with the changes in the sheet resistance, as obtained in different drive-in operations. In this step, we used wafers that have 2–4μm texture, sheet resistance of 30, 40, 50, and 60Ohm/sq and 80μm as width of finger with 2.2mm spacing of the metallization. The peak temperature was 759.5°C, the melting duration was 4.5s, and the belt speed was 170 IPM.

In the fourth set of experiment, we investigated firing conditions that determines sheet resistance, by varying belt speed, and temperature. We found a co-firing process window that resulted in a fill factor greater than 77%. For the metallization of the front side, we used Ferro 33-501 Ag paste with a peak temperature 700°C and a firing time <1–3s.

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In the fifth set of experiment, we examined the relationship between the number of grid lines to the series resistance, fill factor, and shading loss in a single-crystal, 5-inch (125mm X 125mm, 154.83cm^2) Czochralski-type solar cell. The grid model, as in ref [44], was used to optimize the grid line design in terms of resistance and shading loss.

In order to obtain higher V_{oc} by BSF layer, we observed that it is necessary to have the ramp-up rate higher than 70°C/s, that resulted in an average V_{oc} higher than 620mV [45], as shown in Table 4. At a higher ramp-up rate and proper belt speed setting made it possible to get a higher V_{oc} by reducing the deterioration caused by the effects of the thermal stress on the wafer. For further improvement in V_{oc}, a densely packed Al layer or uniformly formed BSF layer created by a high ramp-up rate would also be helpful.

However, as the heat increases, micro-cracks in a wafer or bowing of the wafer may occur, leading to an increase in leakage current. Large defects or poor features of a wafer increase the surface recombination and leakage current.

For sheet resistance of 40, 50, 60Ω/sq, the carrier lifetimes were 14, 14.9, 17.2μs and surface recombination velocities were 660, 480, 425cm/sec respectively. We observed that, as the emitter sheet resistance increases, the carrier lifetime increases with the decrease in surface recombination velocity. To a certain degree, the variation in sheet resistance is dependant upon the surface doping density, which is related to electron mobility and its lifetime in a silicon bulk [46].

Sample numbers →	**#1**	**#2**	**#3**	**#4**
Belt Speed (IPM)	170	140	165	160
Temp. Slope (°C/s)	70.82	64.13	69.15	72.8
Peak Temp. (°C)	756.5	759.5	765.0	753.0
Average V_{oc} (mV)	620.3	617.7	619.0	621.7
FF (%)	79.2	78.9	78.1	80.6

Table 4. High temperature firing specifications.

To investigate the effects of different drive-in operations, we examine the variation in V_{oc} and the J_{sc} according to the sheet resistance changes. As different drive-in operations for dopant diffusion can lead to changes in sheet resistance. In this step, we used wafers of 24-μm texture, sheet resistance of 30, 40, 50, or 60Ω/sq. and 80 μm width of finger with 2.2 mm spacing shows the V_{oc} as 621, 622, 623, 627mV and J_{sc} as 34.6, 34.9, 35.0, 35.3mA/cm^2 respectively. The peak temperature was 759.5°C, the melting duration was 4.5s, and the belt speed was 170 IPM.

As the emitter layer becomes thinner the sheet resistance increases, it becomes difficult to fire the electrode to a moderate depths (i.e., near the pn junction). So the higher sheet resistance means thinner emitter and it is more likely to lead to a short circuit of electrodes that penetrate through the emitter. With low sheet resistance (i.e., a heavy doping) by the over-

fired sites such a situation is less likely. Fig. 6 shows a safe operating zone for the range of belt speed (Fig. 6(a)) and firing temperature (Fig. 6(b)), it gets narrower as the sheet resistance increases. While the duration of firing was investigated, we found that the shorter the firing time, the more was the minority carriers lifetime. Thus shorter firing time results in increased number of minority carriers and as a result increased $V_{oc.}$ It is known that mobility is dependent on the effective minority carrier lifetime. We also investigated the relationship between the number of fingers and the series resistance, fill factor, and shading loss in a single-crystal, 5inch (125mm×125mm, 154.83cm^2) Czochralski-type solar cell. We used two different finger spacings 1.8mm and 2.4mm.

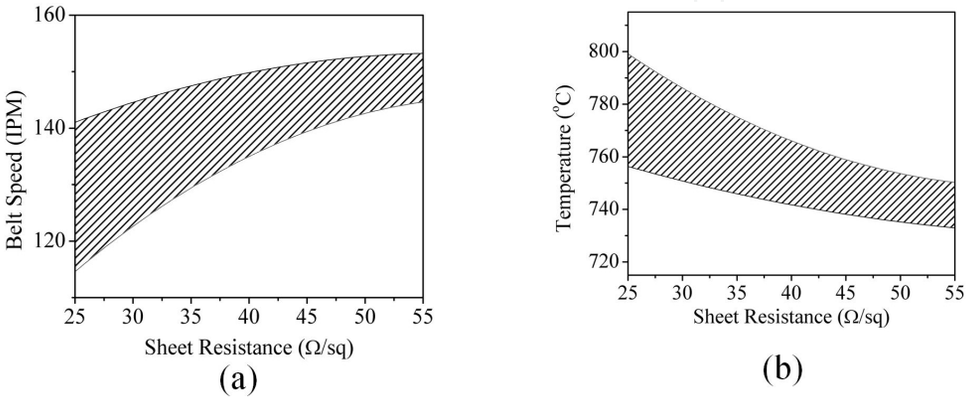

Figure 6. Firing process window from the firing conditions according to the variations of the sheet resistances, the (a) belt speeds and (b) the firing temperatures. Hatched area indicates the range (min.–max.) that has larger than 77% of the fill factor by the combination of variations of the sheet resistances (drive-in operations), the belt speeds and the firing temperatures.

The screen printed and metalized front side shading loss is relatively large, in the range of 8–10% [47]. A grid model suggested in [44] can be used to optimize the grid line design, considering resistance and shading loss. The finger width was as usual 80 μm in the case of the fired Ferro 33-501 Ag paste grid lines. Consequently, the number of grid lines compared to the original grid line design increased by 17. With the new grid line design, the finger spacing decreased from 2.4 to 1.8 mm. This led to a decrease in the total series resistance and an improvement in the fill factor. The design of the metal grid line was essentially a matter of finding the separation between the fingers that resulted in the best compromise between shading losses and resistive ones [48]. The contribution to the series resistance from the diffused sheet was 0.192Ω.cm^2 for 2.4mm spacing and 0.108Ω.cm^2 for 1.8mm spacing, so that emitter resistance (R_e) improved by 0.084Ω.cm^2. Each 1Ω.cm^2 in series resistance caused a decrease of about 0.041 in the fill factor (assuming a moderately high shunt resistance) [48], the total calculated improvement in fill factor due to the increase in emitter sheet resistance was 0.0078Ω. We also investigated the relation between the variations of R_{sheet} and spacing for the available range of more than 77% of the fill factor. As shown in Fig. 7, the narrower the spacing, the wider range of R_{sheet} can give a better solar cell. By shortening the spacing between the grid lines, the series resistance decreased and the FF increased, but the addition of extra fingers caused a 1% increase in shading loss as well as lowering the short circuit current. As a result of these drops, cell efficiency reduced from 17.18% to 16.92%.

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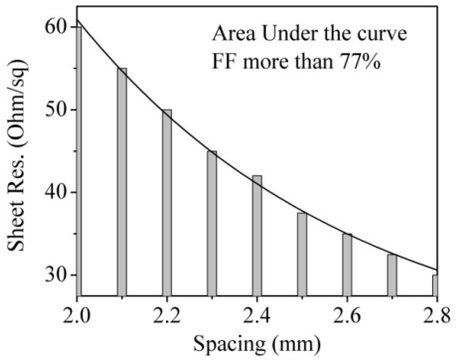

Figure 7. The relation between the sheet resistance with finger spacing for the available range of more than 77% of the fill factor.

3.5.2. Study of rear surface passivation with SiNx film

Cell Condition	Carrier Lifetime (μs)	Cell Condition	Carrier Lifetime (μs)
SiNx ARC		**PECVD ONO**	
As-deposited	100	As-deposited	110
FGA	125	FGA	70
Co-firing	180	Co-firing	165
Si rich SiNx		**SiON/Si-rich SiNx**	
As-deposited	205	As-deposited	120
FGA	320	FGA	225
Co-firing	11	Co-firing	20

Table 5. Temperature dependence of different passivating films. FGA – forming gas annealing, ONO – silicon -oxide - nitride -oxide.

For the fabrication of local back contact structure with little modification on conventional cell process, adaptation of rear passivating film on c-Si solar cell should address two issues which are

1. temperature dependence as shown in Table 5,
2. grid pattern on rear metallization.

In order to carry out a comparative investigation about the effectiveness of Al-BSF and dielectric passivation on rear surface, solar cells were fabricated with and without dielectric passivation in conjunction with screen printed Al grid pattern with different rear metal covered area. Comparative analysis show that the role of the rear surface passivation with SiNx film becomes dominant when the metal coverage area is below 45% of total surface area. But, as the metal coverage area goes above 45%, the quality of passivation degrades first

then starts improving due to the dominating effect of Al BSF over the passivation with SiNx. As the metal coverage area on the rear surface reaches as high as 85%, an improvement in infrared response with net improvement in I_{sc} by ~ 0.16 A has been observed. This indicates that there is dominance of Al-BSF passivation in comparison to the dielectric passivation on the cells fabricated with screen printed local back contact, especially when the rear metal coverage reaches 45% or more but when the metal coverage comes below 45%, the effect of the dielectric passivation becomes dominant.

All the results suggest that the passivation with dielectric film on the rear surface is a must for local back contact formation by screen printing of Al paste whereas the role of such dielectric passivation becomes significant for Al printed local back contact only if the metal covered area on the rear surface goes below 45%. These results indicate a suitable rear metal covered area for high efficiency thin c-Si solar cells with local back contact in conjunction with dielectric passivation with dielectric film of SiNx and were found to be in accordance with the results obtained by simulation in ref [28].

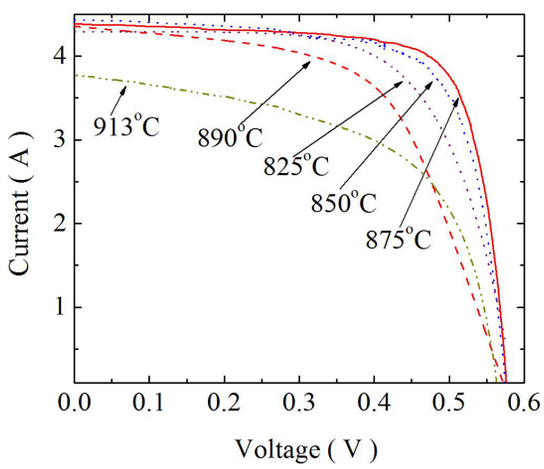

Figure 8. Comparison of the illuminated current-voltage (LIV) characteristics of the cells fabricated with local back contact through the opening in SiNx film on rear surface by varying the peak temperature of the co-firing profile, as indicated with the traces.

T_p (°C)	R_s (mΩ)	FF (%)	η (%)	V_{oc}(mV)	I_{sc} (Amp)
825	12	67	11.5	576.2	4.40
850	11	71	12.4	575.6	4.45
875	8	75	13.0	576.8	4.38
890	24	60	10.1	574.0	4.35
912	16	67	8.4	564.5	3.77

Table 6. Comparison of the performance parameters of the cells fabricated with local back contact through the opening window on SiNx film on rear surface by varying the peak temperature of the co-firing profile, where T_p is peak firing temperature.

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When the cells were co-fired keeping peak temperature below 875°C, the problem of Al bead formation was found to have reduced but the cells were found to have under-fired due to which the series resistance of the cells increased appreciably. The comparison of LIV characteristics of the cells with local back contact through the opening in SiNx film, fabricated by varying the peak co-firing temperature is shown in Fig. 8 and the comparative analysis of the performance parameters of the cells is shown in Table 6. The co-firing profile with peak temperature of 875°C was found to be the best for SiNx passivation layer in terms of performance parameters despite the formation of the Al beads on the rear surface when the cell was co-fired at this temperature.

The minimum R_s of 8 mΩ and maximum FF of 75% among the cells compared are the evidences of the improved front metal contact without over-heating of Ag finger lines in the case of the cell co-fired with a peak temperature 875°C. The bead formation could be minimized with the increased belt speed keeping peak temperature fixed at 875°C but that test could not be carried out in our system because of the limitation to increase the belt speed beyond 180 IPM.

4. Summary and Future Direction for Thin Silicon Wafer Processing

4.1. Summary

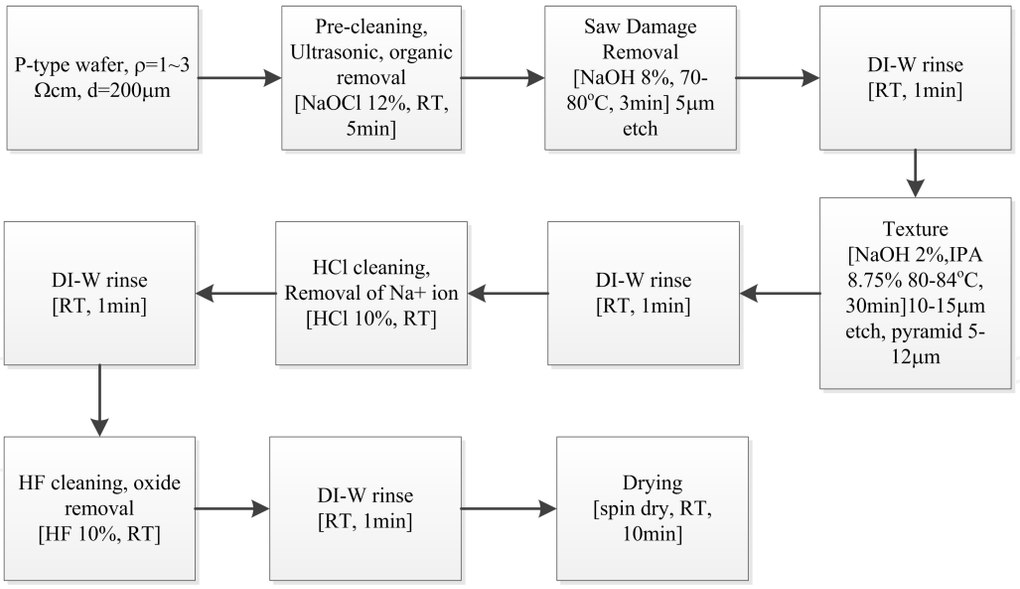

Figure 9. Process sequence of wafer cleaning, saw damage removal and surface texturing of c-Si wafer.

Wafer cleaning for saw damage removal is a fundamental step for c-Si solar cell fabrication. Texturing the top surface of the wafer reduces reflection loss of incident light, as well as increased effective surface area of the wafer for light trapping, light absorption, carrier collection inside the wafer. Surface passivation with silicon nitride layer increases carrier lifetime and further reduces reflectivity of the top surface as it also works as an anti-reflection coat-

ing. It also gives protection of the sensitive and thin top n+ layer from environmental degradation. Co-firing at two different temperatures for the top and the bottom surface of the wafer may be necessary as top surface needs lowed co-firing temperature than the bottom one. Because of the thin n+ layer at the top of the cell and thin silicon nitride layer, the Ag top contact may make electrical shorting through the n+/p interface, if co-firing is done at higher temperature. The Al/Ag paste that is used for back contact works for electrical contact as well as p+ doping of Si at the back surface. Al is a group III element in the periodic table so it works as a p-type dopant for Si. After the high temperature co-firing, the Si-Al alloy that is formed at the back of the cell acts as a p+ layer and creates strong back surface field so the photo generated holes are efficiently collected during light illumination.

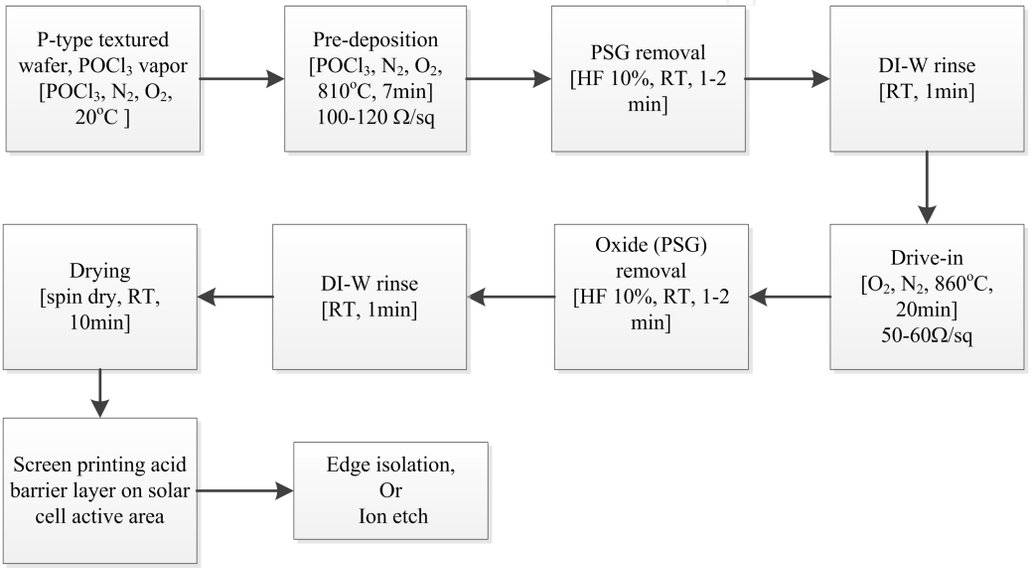

Figure 10. Process flow for doping or emitter diffusion of cleaned and textured wafer. The PSG removal can be carried out after the pre-deposition (as shown above), or it it can be done after the drive in operation. In the latter case the drive-in can be the third step (the PSG removal will be the fourth step), and all other steps remain in order. The emitter diffusion for this latter case has been depicted in Table 1.

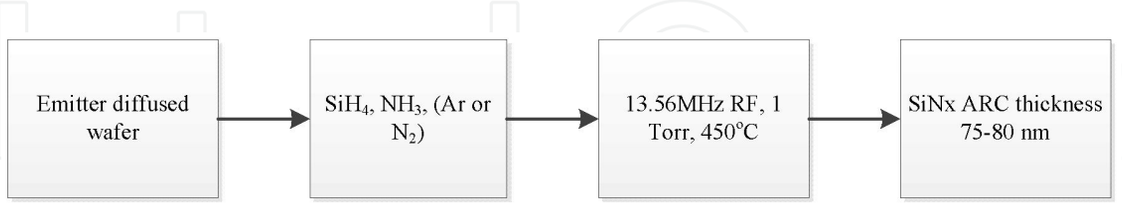

Figure 11. SiNx, ARC deposition on the wafer by RF PECVD.

Out of several approaches to improve the V_{oc} and FF, increasing the ramp-up rate of temperature and setting the belt speed along the heating furnace properly, makes it possible to get a higher V_{oc}. This increase in V_{oc} may be because of reduction in the deterioration due to the effect of thermal stress on the wafer. In presence of excess thermal stress small cracks in the wafer may develop, resulting in a high sheet resistance and low open circuit voltage. Thus optimizing the drive-in condition for low sheet resistance is necessary. The faster belt speed

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in the co-firing stage, results in higher ramp-up rate for temperature, that greatly enhances V_{oc}. By studying the results of our five sets of experiments, we determined certain approaches for improving the open circuit voltage and fill factor:

1. As the temperature ramp-up rate went higher, we could obtain better uniformity of the BSF layer.
2. A higher belt speed tends to reduce the overall leakage current of a wafer.
3. As the emitter sheet resistance increases, the open circuit voltage decreases with the decrease in dopant concentration in the emitter, although the short circuit current is increased, that is attributed to the improvement of the short wavelength response, more light entering the cell active region and to a reduction of recombination in the front surface.
4. The peak temperature of the wafer was optimized for the shorter the firing time. It results in increased minority carrier density, which in turn increases the open circuit voltage. We investigated the optimal firing conditions for different sheet resistance, temperature, and belt speed, and within the profile window of the firing process, we obtained a high V_{oc} (>620 mV) and fill factor (>77%) for a range of different sheet resistance emitters.
5. By narrowing the spacing between gridlines, the series resistance and the fill factor of the cell got enhanced.

However, the short circuit current falls because of shadow effect of the metal electrodes. In the case of low series resistance, we can expect to improve the fill factor, while the short circuit current decreased because of the shading loss.

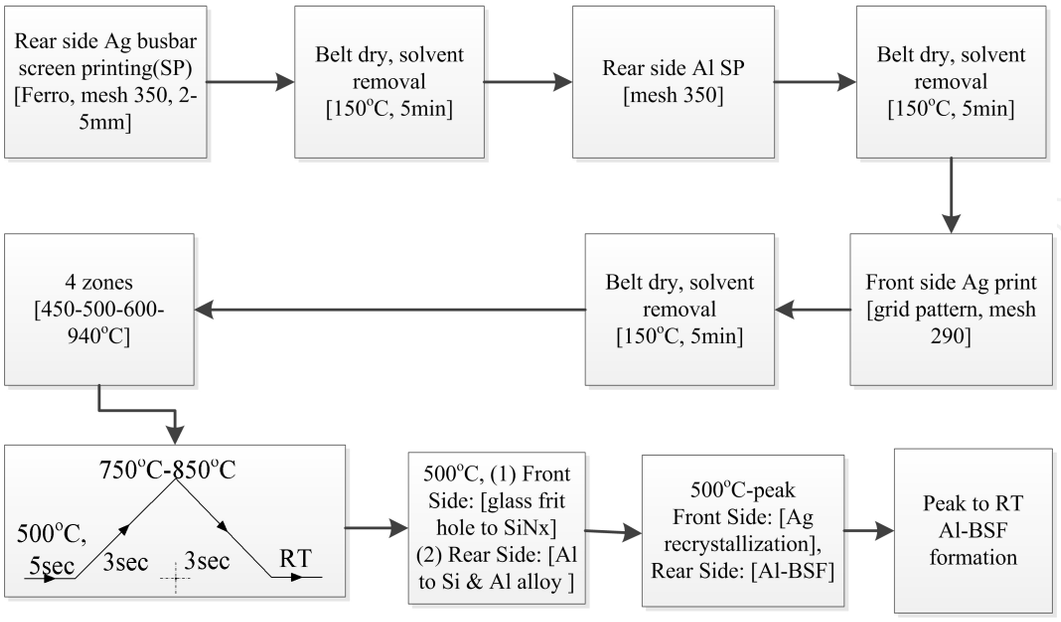

Figure 12. Process steps for metallization of the solar cell by screen printing (SP). In our system, the peak temperature was 759.5°C.

4.2. Future Direction for Thin Silicon Wafer Processing

Thin silicon wafer is more economical because it consumes less Si material, and results in more efficient solar cell because of higher built in field. Cost of silicon is one of the major expenses in c-Si solar cell production and thus with less consumption of semiconductor mass in the form of thinner wafer, the cost of production can be significantly reduced.

One problem that thin wafer may face is bowing during the co-firing process, and hence creation of additional structural defects. Due to unequal thermal expansion of Si and Al back electrode these defects may be created in the wafer. The LBC approach may be more suitable for such cells.

Resistance of screen printed front electrode provides additional element to the series resistance. Each electrode creates a shadow to the cell that reduces total number of electron-hole pair generation under constant illumination. Thus, although decreasing the spacing among the electrodes help reducing series resistance, yet shadow effect leads to reduced total number of electron-hole pair generation. For this, a finger with good conducting material and a high aspect ratio is preferable. Usually glass frit Ag/Al paste is used in the electrode design. If Ag/Al particles in the frit is bigger in size and less dense, and firing temperature profile is not best suited then an insulating layer between Si and Ag/Al electrode may form. This may be avoided by using Ag/Al nano-particles in the paste, with a higher number density of the particles.

Another method that has partly been adopted in commercial production is selective emitter design. In this method a local doping pattern is designed before phosphorus doping through diffusion chamber treatment. Ag electrodes at the front surface are fabricated over this so that a highly doped local semiconductor region is formed around the Ag-electrode after high temperature co-firing. In this way a barrier potential at metal semiconductor junction can be reduced. This electrode structure may bring the screen printed solar cell technology close to buried contact solar cell with one additional process step.

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