Chapter 6

Implementation of Schottky Barrier Diodes (SBD) in Standard CMOS Process for Biomedical Applications

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Additional information is available at the end of the chapter

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1. Introduction

Cost, size, lifetime and safety are important parameters when designing an RFID based biomedical system, especially if the receiver is an implanted device.

For size reduction and extended lifetime, the receiver can be implemented without batteries, thus characterizing a passive tag. Therefore, it is necessary an RF link to make the communication path between the base unit and the transponder. Through the link and a proper protocol, information can be exchanged and energy can be delivered to the implant for its activation. Fig. 1 shows a typical RFID topology applied to biomedical applications (Brandl et al, 2005).

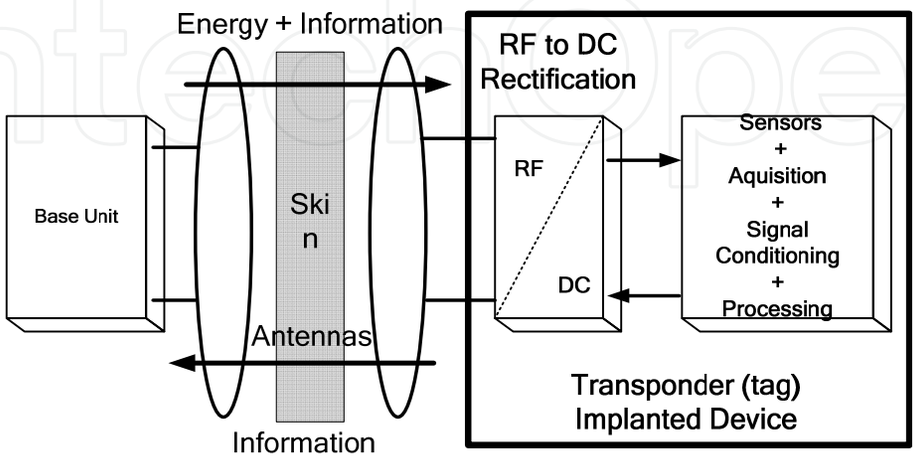


Figure 1. Typical RFID System.

As it can be observed, the energy is transmitted by a pair of coupled coils. For patient safety it is important to keep the induced electromagnetic fields at lower levels, to avoid tissues damages by raising the local temperature. The Specific Absorption Rate (SAR) represents direct measurements of the electric field (indirect measurement of the magnetic field) and induced current density over the human tissue at the implant location. The temperature variation over the time indicates the local heating factor. Both relations are given by (Pradier et al, 2005):

$$SAR = \frac{\sigma |E|^2}{\rho} \quad \left[W/Kg \right] \tag{1}$$

$$\frac{dT}{dt} = \frac{SAR}{c} \quad \left[{}^{0}C/s \right] \tag{2}$$

where σ, ρ and c represent the conductivity, the human tissue mass density and specific heat capacity, respectively, at the implant location. *E* is the incident electric field intensity (RMS). Based on equations (1) and (2), a safe value for the power transferred by the RF link is 10mW/cm^2.

Besides cost and size reduction, microelectronics also allows the implementation of the transponder circuits into a single die. The lowest prices can be achieved by using low cost standard CMOS technology.

Transponder front-end circuits include a rectifier to make the AC-DC conversion to provide unregulated power supply to the tag. In CMOS technology, NMOS and PMOS (more often than one of each type) transistors are used in different topologies to implement the rectifier circuit. These devices, however, have the disadvantage of presenting a turn on threshold voltage (Vth) that may require larger induced voltage in the receiver coil. Although the CMOS technology has been minimizing the transistors geometries, the Vth voltage does not scale down at the same rate. The use of a Schottky Barrier Diode – SBD is an alternative way to design the rectifier circuit in order to improve its efficiency. A more efficient rectifier will reduce the voltage drop between the tag input and the rest of the circuitry, thus reducing the power demand from the transmitter. For low currents levels, typically found in this kind of application, the SBD voltage drop can be lower than a CMOS Vth voltage.

The SBD is not readily implemented on a standard CMOS technology but after a few adjustments in the masking process, it can be implemented. In this work, a mask sequence is presented to implement SBDs in CMOS processes and a simple model for this device is discussed.

2. Conventional rectifier circuits

Basically, RFID systems can be divided into three major groups: active, semi-passive and passive tags. An active tag includes embedded batteries as their main energy source for autonomous operation. Semi-passive tags are also dependent on a battery for the start-up,

however the required energy for the communication link is provided by the reader. A passive tag, on the other hand, extracts the full power from the signal transmitted by the reader, thus there is no need of an on-board power supply. This autonomous capability of passive tags offers some interesting features such as low production cost, increased reliability and a longer maintenance-free lifetime. The last one is very important considering inherent surgical procedures related to an implanted device.

A passive tag requires a circuit block to obtain the power transmitted from the base unit (known as reader) by the RF signal. This kind of circuit is a RF-DC converter or, simply, rectifier circuit.

Mainly for passive tags, it is important to have a highly efficient RF to DC conversion (the RF energy received at the tag decreases rapidly as a function of distance from the reader) and it is also desired a stable power supply at the rectifier output.

The available power at the tag antenna (P_{AVAIL}) can be expressed by (Kotani and Takashi, 2009):

$$P_{AVAIL} = \left(\frac{\lambda}{4\pi d}\right)^2 P_{EIRP} G_{TAG} \tag{3}$$

where λ is the wavelength of the RF link, d is the distance between the base unit and the tag, P_{EIRP} is the effective isotropic radiation power of the base unit transmitter, and G_{TAG} is the tag antenna gain. The effective isotropic radiation power is determined by regulations, for instance, 4W for electronic product code (EPC) protocol in North America.

The tag antenna gain is manly determined by its area. Typically, G_{TAG} is about 1.64 for a $\lambda/2$ dipole type.

In this scenario, the performance of the rectifier circuit, evaluated in terms of power conversion efficiency (PCE) should be as large as possible. The PCE can be expressed as:

$$PCE_{rect} = \frac{P_{out}}{P_{in}} \tag{4}$$

where P_{out} is the output DC power circuit and P_{in} is the received RF input power.

By combining eq. (3) and (4), and considering the presence of impedance matching, it is possible to state the achievable power of an RFID tag:

$$P_{tag} = P_{EIRP} G_{TAG} PCE_{rect} \left(\frac{\lambda}{4\pi d}\right)^2 \tag{5}$$

By analysing eq. (5) it is clear that the PCE is the most interesting variable to manipulate as a way to obtain, for instance, an increase in the communication range d.

In a typical RF-to-DC rectifier, PCE is mainly degraded as a result of two distinct mechanisms: forward voltage drop in the switches (closed related to the finite on-resistance of this switches) and their leakage currents.

Although typical RF-to-DC implementations also exhibit parasitic elements that contribute to lower the rectifier efficiency, they play a second-order effect.

Rectifier circuits for RFID tags are usually Dickson based rectifiers and designed using CMOS transistors. It must be clear that RFID applications are cost and area sensitive and the tag circuitry is often implemented in CMOS technologies that offer a high level of integration and relative low cost.

The voltage drop of a diode-connected transistor is approximately the threshold voltage (V_{th}) of the MOS transistor. The literature presents few proposals to reduce the threshold voltage, known as "V_{th} cancelation". One of then, the external-V_{th}-cancelation (EVC), was proposed to for a semi-passive tag and depends on a gate bias voltage that is generated by a switched-capacitor circuit. Since the operation is switched, it requires an external power supply and clocking circuitry, and cannot be applied to passive-type RFIDs.

The internal-V_{th}-cancelation (IVC) was also proposed. In this case, gate bias voltage is generated internally from the output DC voltage by a bias generation circuit. This circuit works well under large input power conditions, but not otherwise since the gate bias voltages are generated by a voltage division mechanism. Regarding the efficiency, the IVC circuit dissipates an additional power due to the DC current, resulting in slightly degradation in PCE.

The self-V_{th}-cancelation (SVC) has the same topology of diode-connected CMOS rectifier circuit except that gates of the nMOS transistor and PMOS transistor are connected to the output and ground terminal, respectively. This connection boosts the gate source voltage of NMOS and PMOS transistors as much as possible, in other words, the threshold voltages are decreased by the same amount as the output DC voltage. The SVC provides better PCE than EVC and IVC implementations (Hashemi et al, 2012).

Fig. 2 and 3 shows examples of a conventional CMOS diode-connected rectifier and self-V_{th}-cancelation CMOS rectifier.

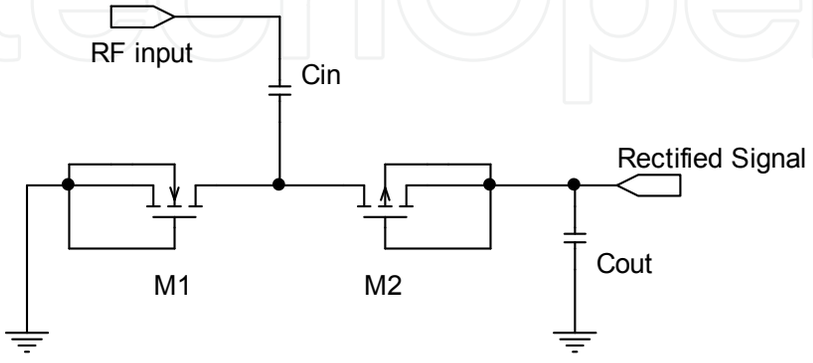


Figure 2. Conventional CMOS Type Rectifier Circuit.

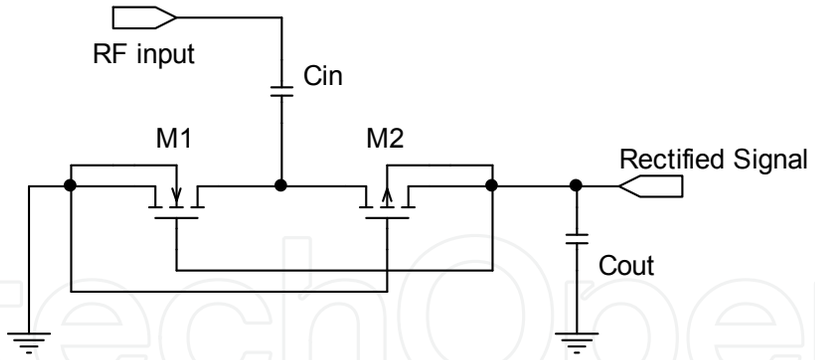


Figure 3. Self-V_{th}-Cancelation CMOS rectifier Circuit.

Another rectifier is the "four-transistor-cell" CMOS rectifier, which outperforms CMOS diode-based rectifiers, even when static V_{th} cancelation technique is used to reduce the turn-on voltage of the diodes. In this configuration, the on-resistance of the CMOS transistors is decreased by increasing gate-source voltage V_{GS} and reverse leakage is reduced by reversing the polarity of V_{DS} in the cross-coupled structures. Fig. 4 illustrates an example of "four-transistor-cell" rectifier.

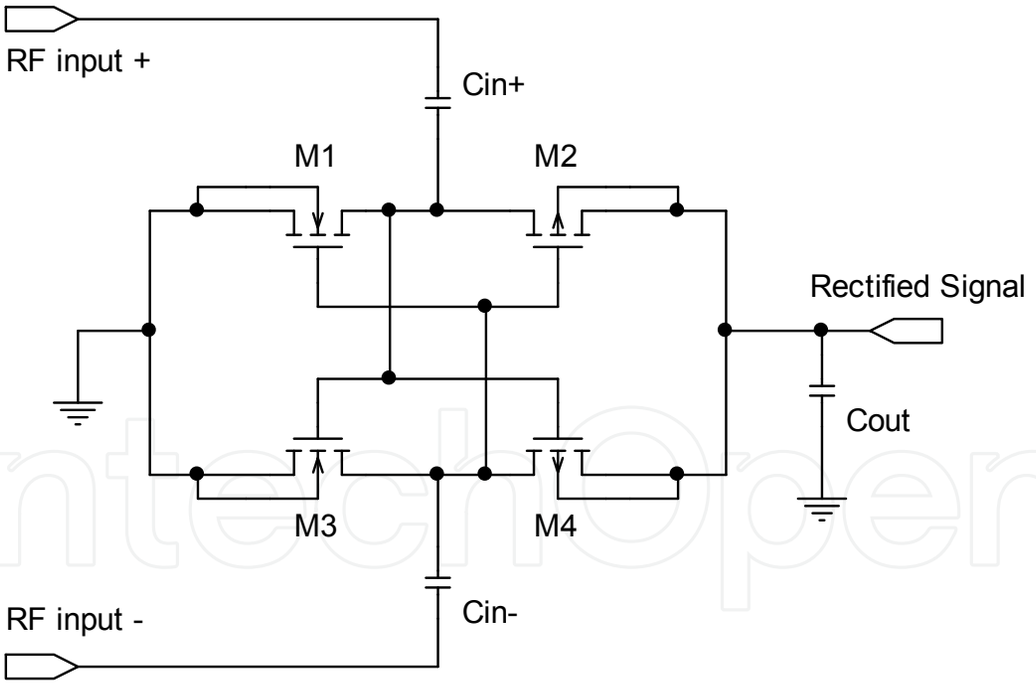


Figure 4. CMOS Four-Transistor-Cell Rectifier (Differential-Drive CMOS Rectifier).

The drawback of the four-transistor-cell topology is that it does not perform well when the received RF power is in the range of few μW. This problem is more pronounced when the tag is implemented in low-cost CMOS technologies, where the threshold voltage of NMOS and PMOS transistors lays in range o few hundred mV. There is the possibility that the transistors may not turn-on completely and the rectifier efficiency can be severely impaired.

The use of Schottky Barrier diodes in conventional Dickson rectifiers were considered as an attractive solution as a consequence of Schottky lower forward voltage drop and fast switching speed . Although, this kind of device is not readily supported in almost all CMOS technologies it is possible to be done with few mask flow changes. This chapter will show that procedure on a low-cost CMOS technology.

Fig. 5 shows the basic concept regarding a conventional Dickson rectifier with SBDs.

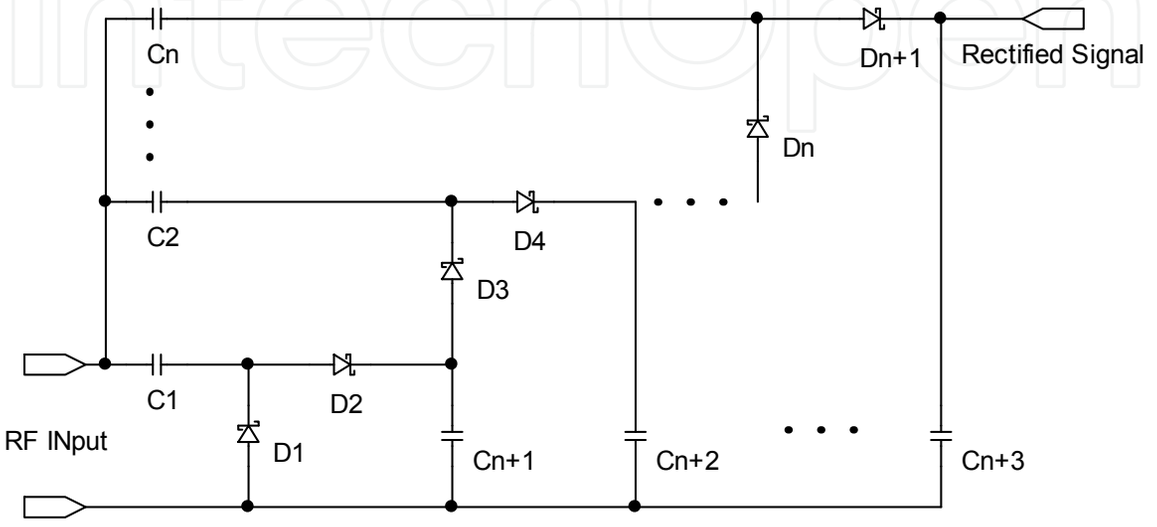


Figure 5. Basic Dickson Rectifier Circuit with SBD.

3. Silicon based Schottky Barrier Diode (SBD)

The Metal-Semiconductor contact (also called as Schottky Barrier Diode) has some features that allow its use in high frequency applications and systems that must operate at low voltage levels. These features are, basically, the low level of minority charge accumulation during commutation, which leads to high switching speeds and the low voltage drop between its terminals. Low turn on voltage, fast recovery time and low junction capacitance are advantages that SBD offer over other types of PN diodes. These are the main reasons that SBD are so popular in RF applications. Fig. 6 shows the energy band diagram for this kind of contact at thermal equilibrium. In this work, since we have used TSMC process, the metal is aluminium and the semiconductor is N-type, moderately doped, obtained by N Well diffusion (Janan et al, 2006), (Rainee and Philip, 2003) (Avenin, 1996).

As can be seen, there is a build in contact potential V_{bi} expressed by:

$$V_{bi} = \phi_{BN} - \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right) \tag{6}$$

where kT/q is the thermal voltage (25.9mV at T=300K), N_C is the effective state density (constant for a given temperature) in the conduction band, N_D is the donor doping level and ϕ_{BN} is maximum height of the potential barrier (Streetman, 1980).

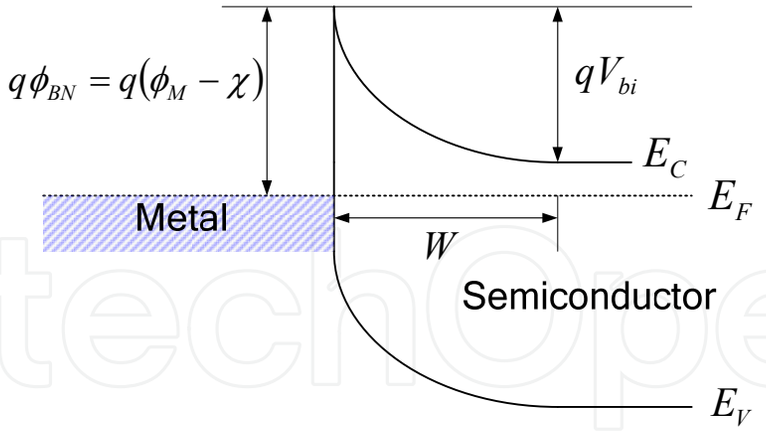


Figure 6. Energy Band Diagram for a Metal-Semiconductor Contact.

Eq. (6) shows that the built in voltage V_{bi} can be reduced if a moderate to low doping semiconductor is used. Considering ideal values for metal work function ($\phi_M \approx 4.28V$) and semiconductor electron affinity ($\chi \approx 4V$), the barrier ϕ_{BN} can be as low as 280mV. Considering, yet, eq. (6), the built in voltage V_{bi} can be further reduced by controlling the doping level N_D.

It must be necessary to evaluate the doping concentration N_D in order to use eq. (6) to obtain *Vbi*. For this procedure a C-V curve for a Metal-Insulator-Semiconductor (MIS capacitor)) structure is used. Fig 7 and Fig. 8 show a typical MIS capacitor (with N type semiconductor) and a C-V curve, respectively.

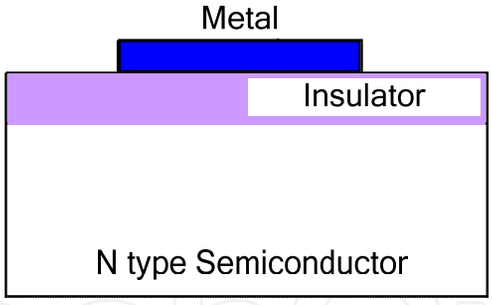


Figure 7. Metal-Insulator-Semiconductor (MIS) Capacitor.

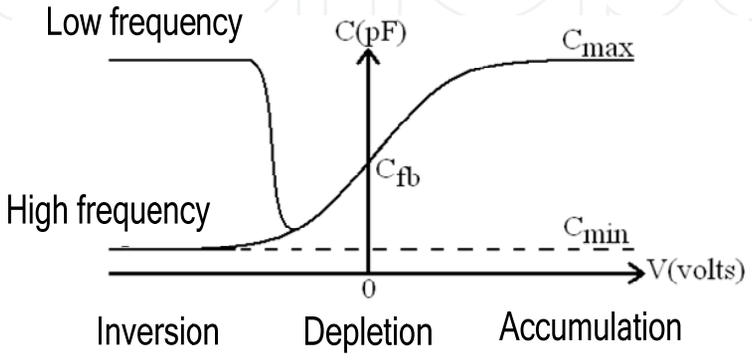


Figure 8. MIS C-V Curve.

The C-V curve can be obtained by simulating a PMOS transistor with TSMC model parameters as indicated in Fig. 9.

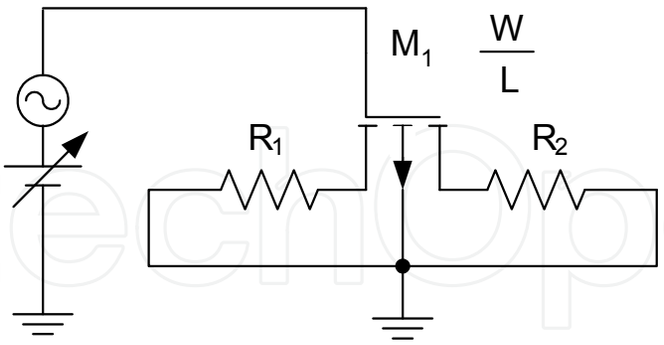


Figure 9. PMOS Transistor used to Plot C-V Curve.

In this simulation, resistors R1 and R2 are very large in order to restrict the action of PMOS in the channel area. The DC source is swept from negative to positive voltage values, to validate all regions of operation of the MOS capacitor formed by the gate, insulator and channel. The AC source can be set into low or high frequencies; therefore, it is possible to obtain the C-V curve behaviour as illustrated in Fig. 4.

The capacitor area (A) is determined by the geometric aspect W and L of the PMOS transistor.

The following equations are used to extract the doping concentration N_D in a recursive way:

$$W_D = \left(\frac{C_{max}}{C_{min}} - 1 \right) \frac{\varepsilon_0 \varepsilon_S A}{C_{max}} \tag{7}$$

$$N_D = \frac{4 \varepsilon_S \phi_F}{q W_D^2} \tag{8}$$

$$\phi_F = \frac{kT}{q} ln \left(\frac{N_D}{n_i} \right) \tag{9}$$

where W_D is the depth of depletion region formed in the contact, ε_0 and ε_S are the vacuum and silicon dielectric permittivity, respectively, A the contact area (considering a parallel plate capacitor).

The I-V characteristic of the Metal-Semiconductor structure is similar to a P^+N junction. In the forward bias mode (metal connected to positive voltage and semiconductor connected to ground), the device turns on at voltages as low as 0.28V. The Metal-Semiconductor structure offers large current density due to the smaller built-in potential as well as the nature of thermion-emission compared to P^+N diffusion. Also at Metal-Semiconductor interface there is the image-force-induced lowering phenomenon of the barrier energy for charge carrier emission, in the presence of an electric field. To understand this phenomenon, consider an electron, in vacuum and at a distance from a metal surface. A positive charge will be

induced on the metal at a distance -a from the surface resulting in an attractive force between them. This force is known as the force of the image and has associated with it an image potential energy which corresponds to the potential energy of an electron at a distance a from the metal. When an external field is applied, together these two energy components have the effect of lowering the Schottky barrier. Thus at high fields, the Schottky barrier is considerably lowered. According to the thermo-emission proposed by (Sze, 1981), the forward I-V characteristics can be represented by:

$$I_D = I_S exp\left(-\frac{q\phi_{BN}}{kT}\right)\left[exp\left(-\frac{q\phi_{BN}}{kT}\right)-1\right] \quad (10)$$

where I_S is the saturation current, ϕ_{BN} is the Schottky barrier height, q is unit charge, k is boltzmann constant and T is the absolute temperature. When the reverse bias is applied to the Schottky structure, the electrons are depleted at the semiconductor side. As the reverse voltage increases, breakdown similar to PN-junction can happen in the Metal-Semiconductor device. The reverse biased I-V curve of our Schottky diode exhibits "soft" breakdown characteristics, with breakdown voltage at approximately 5V.

4. SBD implementation in low-cost CMOS technologies

In the fabrication of Schottky Barrier Diodes there are two fundamentals arrangements of structures. It can be a conventional structure that is formed only by the overlap of the metal over semiconductor or in a finger configuration that optimize (decrease) the series resistance of the device. Guard rings are linked to these devices and overlap all the SBD structure to avoid latch-up and to separate the SBD from the others tag circuits that performs analog and/or digital functions.

This item aims to investigate the Schottky configuration with fingers for applications in high frequency in order to improve the efficiency of power conversion. It will be described the changes in the masking process of a low-cost CMOS technology, particularly, the 0.35μm channel length TSMC (Taiwan Semiconductor Manufacturing Company) process. The procedures outlined here can be applied to other similar technologies.

The layer pattern shown in Fig. 10 will be used in the process sequence.

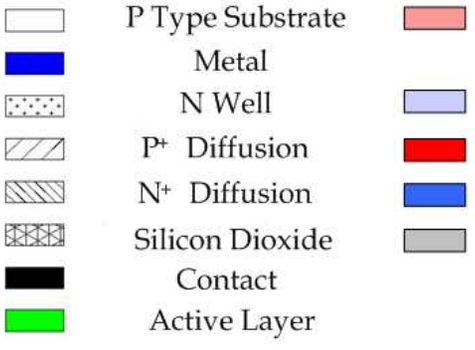


Figure 10. Layer Pattern.

It will be shown the development of a multifinger SBD, since it offers better electrical characteristics. Fig. 11 illustrates a simple view of a two fingers device.

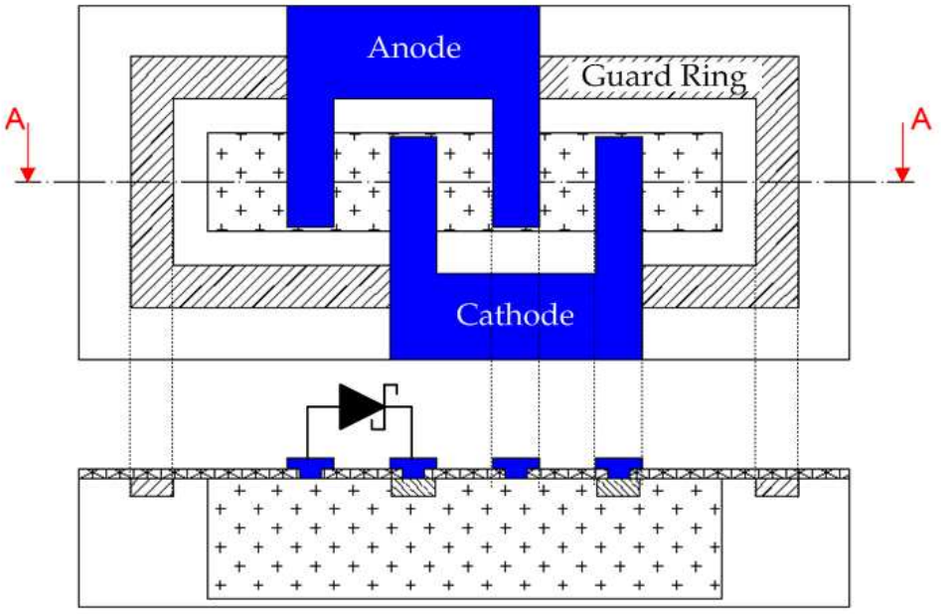


Figure 11. Two Finger SBD Structure.

Observe that the anode corresponds to the Metal-Semiconductor contact whereas the cathode corresponds to the ohmic contact. The SBD process in a standard CMOS is presented in the following figures. Fig. 12 (a) and (b) illustrates the P type silicon (substrate) and the oxide grown (actually silicon dioxide, SiO_2), respectively.

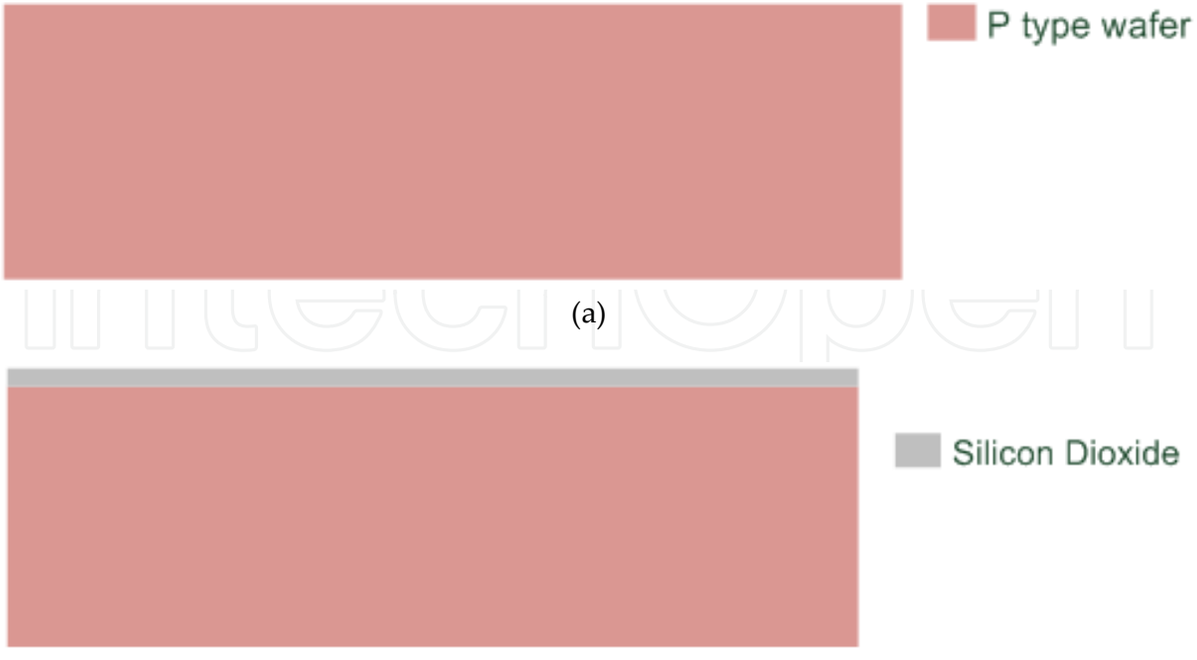
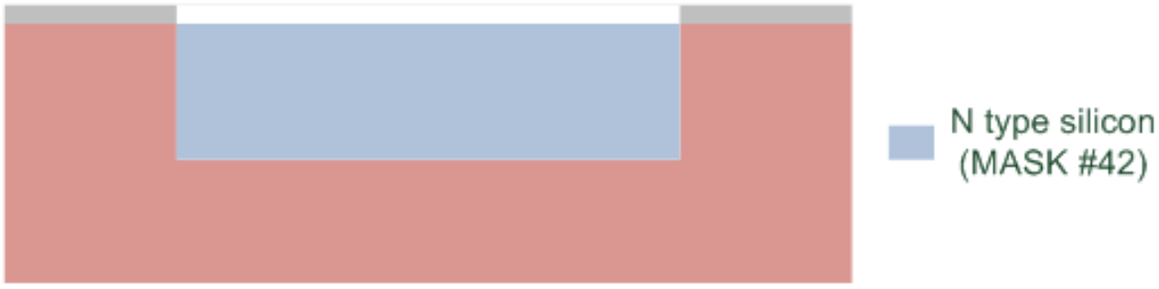
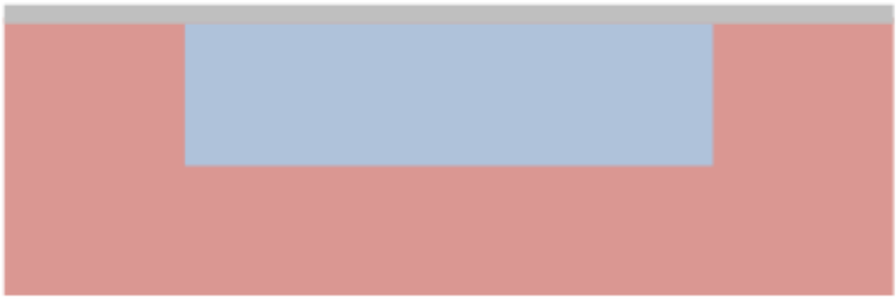


Figure 12. The P type wafer and the Oxide Grown.

After silicon oxide growth, an Nwell (#42) mask is used to make an N type well. The mask dimensions determine the diode finger maximum size. After this step, a new layer of silicon oxide is made. Figure 13 (a) and (b) shows those steps.



(a)



(b)

Figure 13. (a) N well in a P type wafer, (b) N well in a P type wafer after silicon oxide re-growth

The next step is the ACTIVE (#43) mask, responsible to determine the regions where P+ type materials are diffused. They correspond to the guard ring surrounding the SBD device, as shown in Fig. 14.

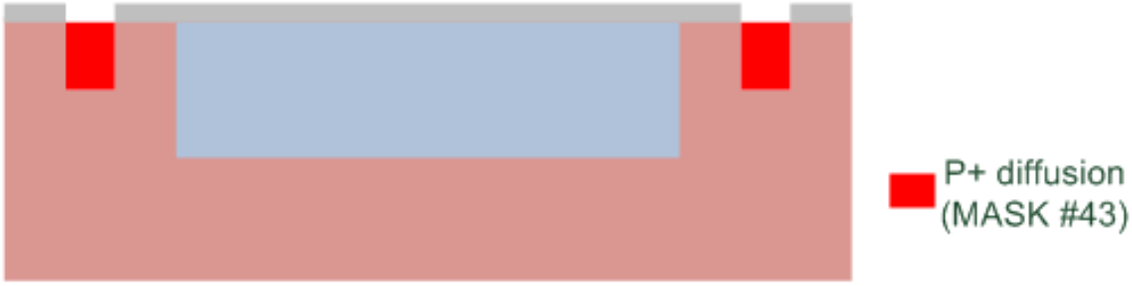


Figure 14. Guard ring get with P+ diffusion.

Next, the NPLUS (#45) mask is used for ohmic contact, i.e, N+ diffusion over an N type well. This contact will form the diode cathode. The number of contacts made at this stage is directly linked to the amount of diode fingers. In this step it is also open a hole in the oxide (via) over the N type well to form the diode anode (mask #48). Fig. 15 (a) and (b) show those steps.

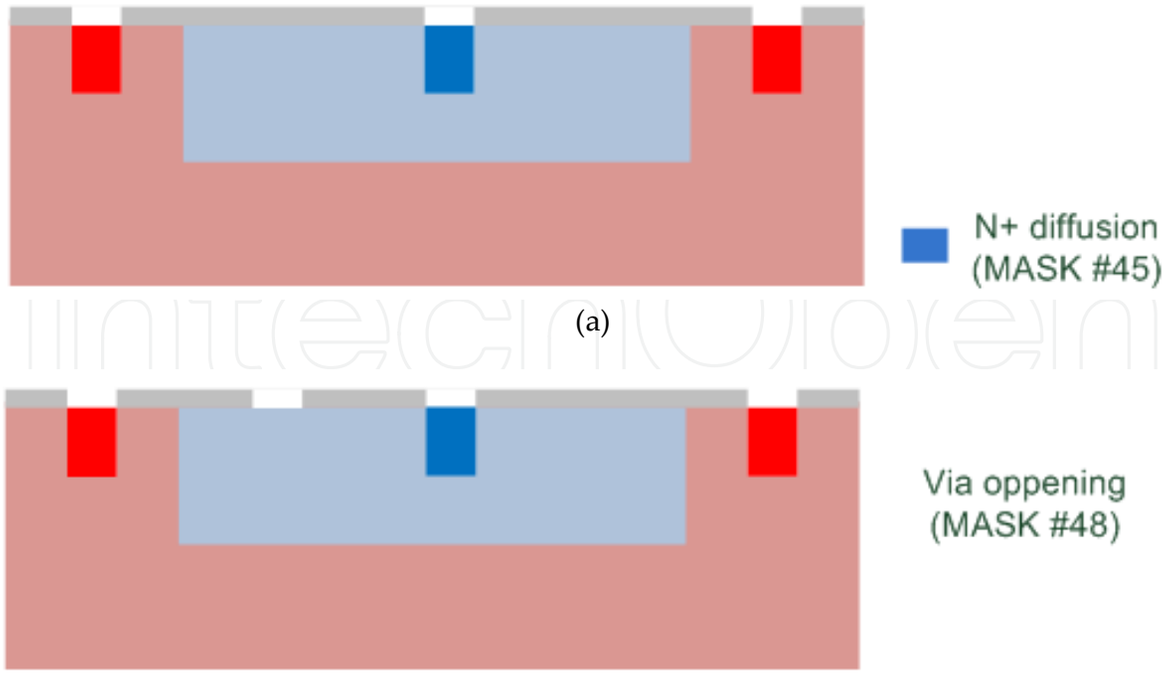


Figure 15. (a) Hole over N+ (cathode) and P+ (guard ring) diffusion. (b) Via over n type well to form diode anode.

It is necessary to deposit a conductor material in order to access the Schottky cathode, anode and guard ring. Mask METAL1 (#49) is used to define contact regions. That step is shown in Fig 16.

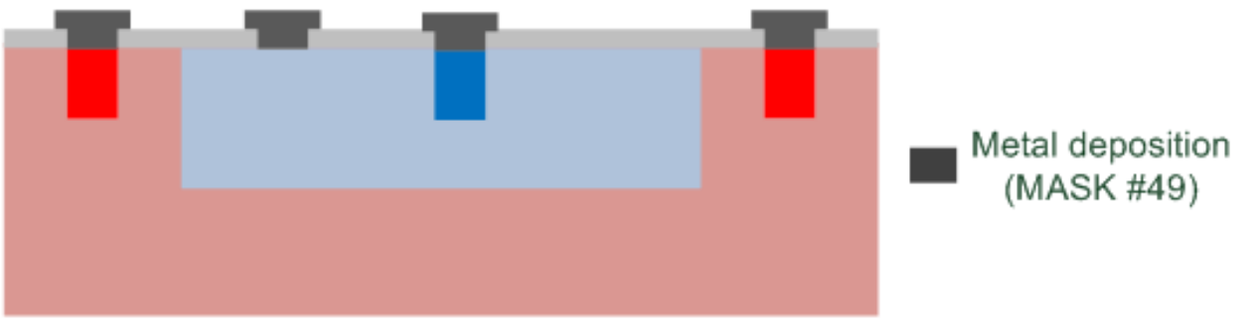


Figure 16. Metal definition for contacts in diode.

Finally, the VIA (#50) and METAL2 (#51) masks are used to access the metal layer that contacts the anode, cathode a guard ring. In summary, the following sequence of masks were used:

Mask NWELL (#42)

Mask ACTIVE (#43)

Mask NPLUS (#45)

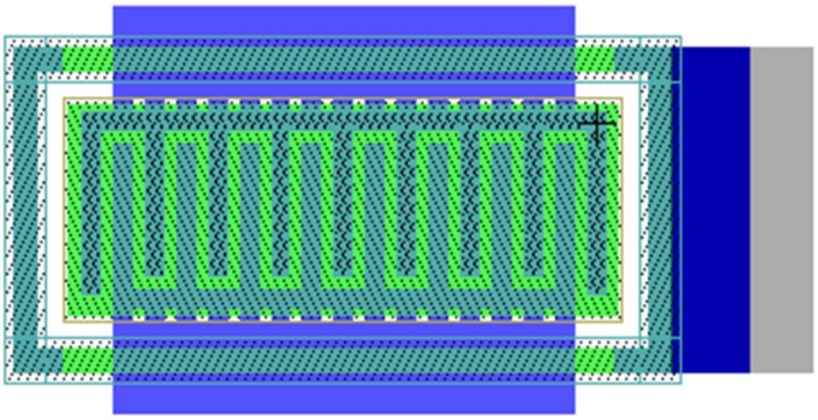
Mask CONTACT (#25)

Mask METAL1 (#49)

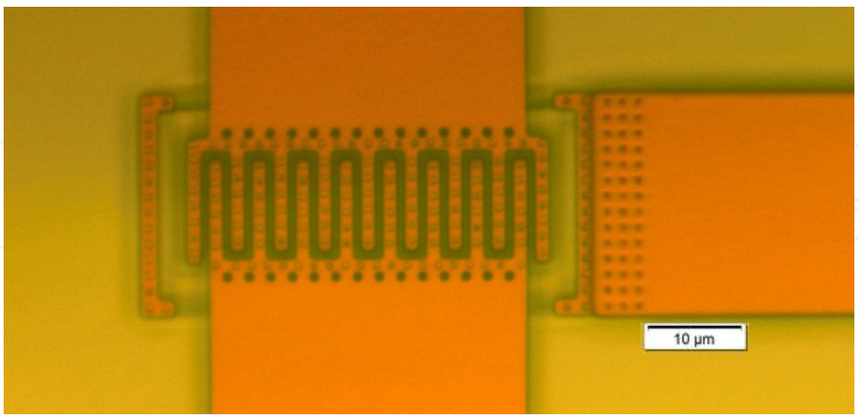
Mask VIA (#50)

Mask METAL2 (#51)

Fig. 17 (a) shows the final layout (similar to Fig. 7) and Figure 17 (b) shows the photo of a SBD.



(a)



(b)

Figure 17. (a) SBD layout and (b) SBD photo.

Each mask used to form the SBD is shown in Fig. 18. The mask sequence must be seen from bottom up.

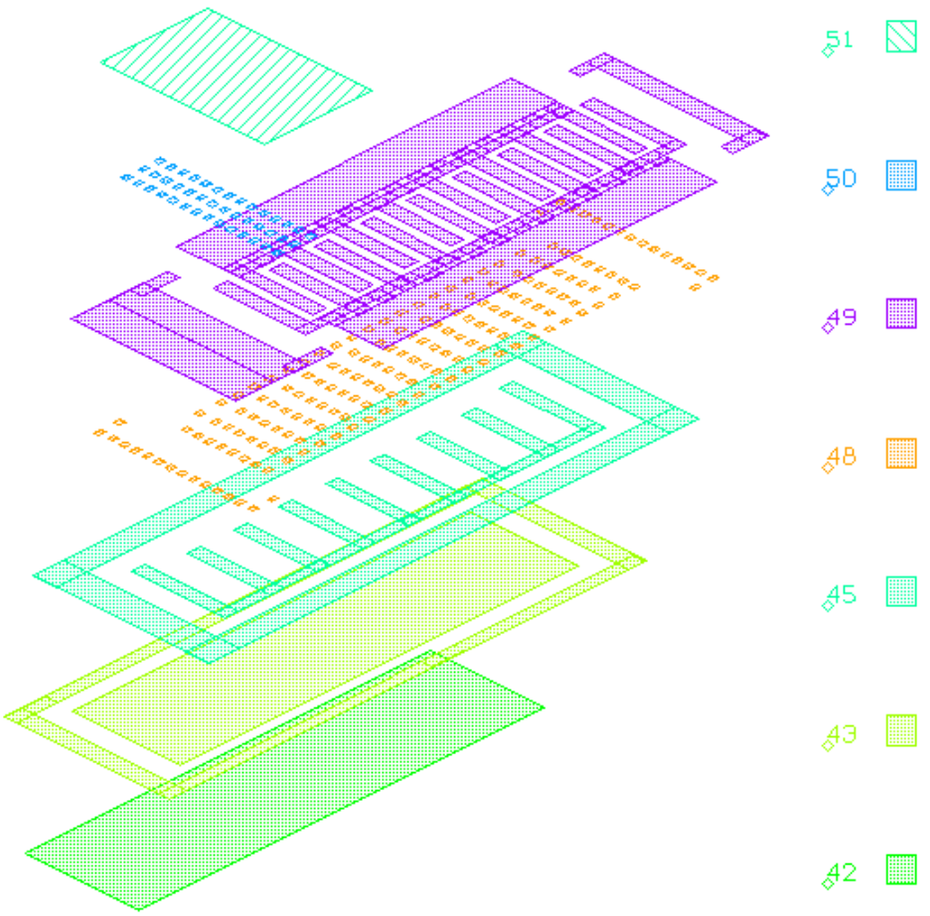


Figure 18. SBD masks in a Standard CMOS process

5. SBD Small-Signal Model

The most important difference between Schottky and PN structures is the lack of junction capacitance that significantly reduces the electrons recovery time. From the previous explanations, it is now possible to construct the equivalent small signal circuit model of the SBD, as shown in the Fig. 19.

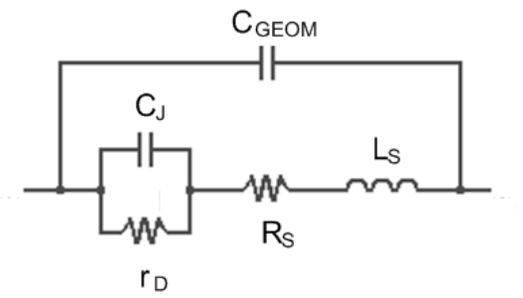


Figure 19. Small-signal SBD equivalent circuit.

In this equivalent circuit, capacitance (C_{GEOM}) arises from the fingers device geometry and exhibits the parasite capacitance between the two ports interdigitating fingers of Schottky diode. This capacitance can be found between 0.1 to 1pF.

Resistance r_d and a capacitance C_J are both from the depletion region, equated, respectively, by:

$$r_D = \frac{dV}{dI} \tag{11}$$

and

$$C_J = A\left[\frac{qN_D\varepsilon_s}{2\left(V_{bi}-V\right)}\right]^{1/2} \tag{12}$$

where q is the electric charge and the V is the voltage applied across the SBD.

Particularly, for a zero bias condition, i. e. V=0, equation (12) is stated as:

$$C_J(0) = A\left[\frac{qN_D\varepsilon_s}{2\left(\phi_B - V_t\right)}\right]^{1/2} \tag{13}$$

Resistor r_d is, in fact, an incremental value and can be extracted from the forward bias Schottky I-V curve in a region before the degradation imposed by series resistance R_S . As a high speed device, the Schottky diode presents a low diffusion capacitance in the forward bias condition too (Philippe, 2002).

It is important to notice the parameter A (junction area) present in the equations (12) and (13). This parameter corresponds to the anode fingers area inside the N well viewed from top, as depicted by Fig. 20.

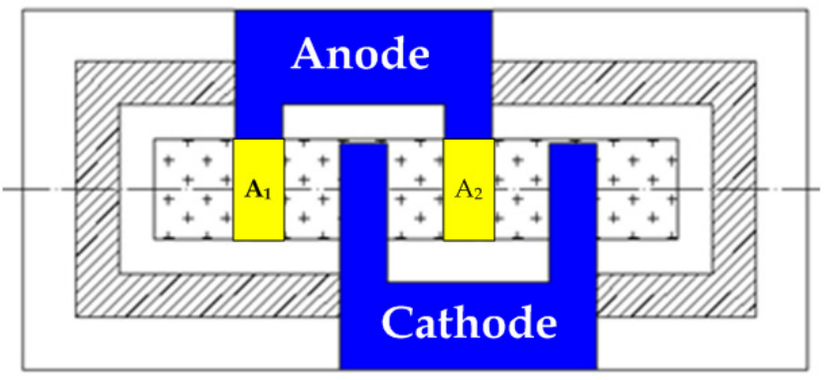


Figure 20. The Parameter A (area).

As can be seen A is the sum of all areas ($A_1+A_2+\ldots A_n$) corresponding to n anode fingers that are inside the N well. The cathode fingers area are not taken into account for junction capacitance as they are associated to ohmic contacts.

Finishing the model, the series resistance (R_s) represents the ohmic contacts and the neutral region of the semiconductor resistance. It is, typically, in the range tens of ohms (10 to 200Ω). Parasitic serial inductance (L_s) can be as low as 0.01nH and influences the device when operating at extremely high frequencies (GHz range). The SBD fabricated in standard CMOS process have the advantages such as low serial resistance and low parasite capacitance.

6. Measured results

The SBDs were diffused in three different versions; with 5 fingers, 10 fingers and 15 fingers. Fig. 21 shows the prototyped chip where it can be observed the various test layout patterns.

Table 1 shows the main calculated small-signal parameters from a set of DC measurements. The presented values are from an average of 40 samples. Those parameters can be used to optimize the final geometry of the SBD.

	r_D [Ω]	$C_J(0)$ [pF]
5 fingers	227	0.4
10 fingers	103	0.8
15 fingers	79	1.2

Table 1. SBD small-Signal parameters.

Fig. 22 shows the IV characteristic for the three diffused SBD. The curves represent an average value for 40 samples. For low level currents, as it is the case of implantable devices, the SBD turn-on voltage is in the range of 200 to 300mV. It is in accordance with eq. (3), considering typical values.

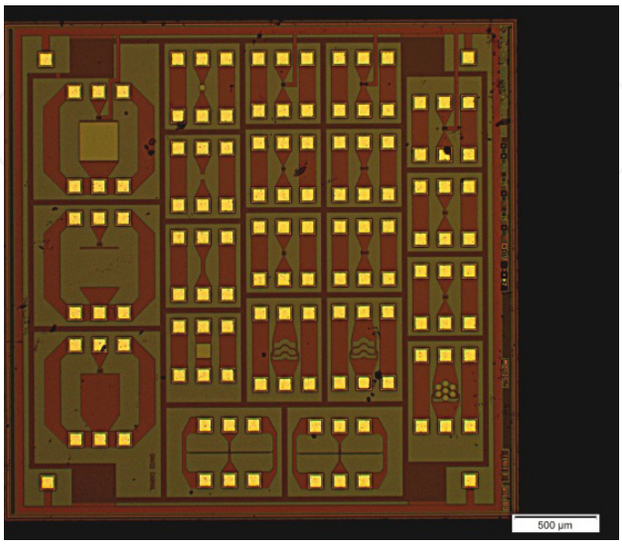


Figure 21. Prototyped chip .

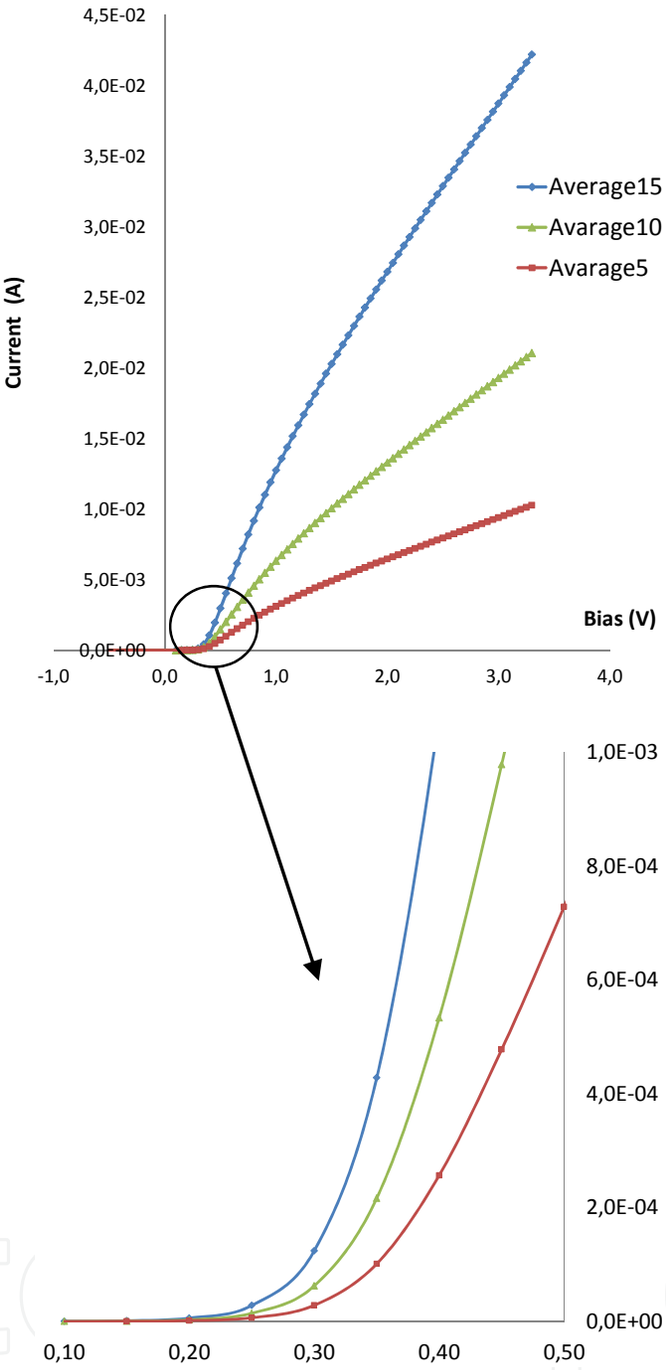


Figure 22. SBD IV characteristic.

The main goal at this point is to validate the fabrication process. As can be observed, it is possible to fabricate this kind of device in a standard CMOS technology, and it can be optimized through its geometric aspects.

Notice that this device is part of a more complex system. An improvement on AC-DC conversation efficiency can provide may allow the integration of the entire circuit, which can be even implanted. Nowadays, there are many important biomedical applications under research and development that depend on implanted systems, such as:

- A chip used to measure the glucose level.
- A chip to be used to evaluate the oxygen level.
- A chip to measure the concentration of creatine in the blood, which is used as the main indicator of renal function.
- A chip to indicate the presence of cancerous proteins in the blood.
- A chip used to store personal date and medical record, since blood type to patient history. In case of an emergency the chip can save lives since it reduces the time to obtain blood type, allergies, chronicle illnesses and provide all medical records.

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