Chapter 18

# A Low Noise Low Power OTA with Adjustable Gain PID Feedback Network for EEG SoC Arrays

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Additional information is available at the end of the chapter

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## 1. Introduction

Standard electroencephalogram (EEG) exams are subject to noises and interferences that may mask or corrupt signals and may cause a wrong medical evaluation. The noise from the environment is more relevant for discrete topologies, in which the components are placed far apart from other. That problem is more relevant on the neurological amplifiers, where the signals are in the range of tens of microvolts. Thus, the use of integrated circuits for the neurological signal amplification is essential to reduce that interference.

Additionally, cables used to connect the electrodes placed on the scalp and the amplifiers are also susceptible to interferences since they work as antennas, thus capturing all kind of environmental noises. Therefore the cables should be as short as possible, or even removed to be immune to the environmental interferences.

This chapter presents a circuit topology of a neurological amplifier to be placed directly on top of the electrodes. The proposed implementation offers better tradeoff among power x area x input referred noise than previously works [1] and offers a bandwidth even wider than necessary to accommodate EEG signals, thus providing a tool for further neurological studies.

Other works [2] present better noise efficiency factor (NEF) but at the expense of more complex source-degenerated current mirrors architecture, which makes them more susceptible to process variations.

The main circuit is comprised of a standard folded Cascode operational transconductance amplifier (OTA) and a fully integrated proportional, integral and derivative (PID) feedback network composed by a pMOS pseudo-resistor [3] and small integrated capacitors. The amplification can be adjustable over 5 different discrete values for better fitting the neural amplification to the analog to digital conversion (ADC) stage.

The amplifier topology was validated for ON 0.5 $\mu$m under the MOSIS program. Post layout simulations reveal the amplifier can provide a gain ranging from 34.32 dB to 43.63 dB, and the whole chip dissipates just 26 $\mu$W. The input referred noise is as low as other similar works [1] while requiring a smaller bias current. The circuit takes an area of just 0.134 mm$^2$.

## 2. EEG basic concepts and characteristics

EEG signals have particular characteristics that demand specific instruments to process them properly. The most important and specific characteristic of EEG signals is its small amplitude when measured by devices placed on the patient's scalp. According to the medical literature [4, 5], EEG signals' amplitude vary tipically from 5 to 10 $\mu$V to 500 $\mu$V within a bandwidth of about tens of miliHertz to 100 Hertz. They may present spikes of comparatively high amplitudes at very low frequencies, denoted local field potentials (LFP) that can achieve 1 V to 2 V [6].

Additionally, the EEG signals may suffer variations due to age, as shown in Table 1.

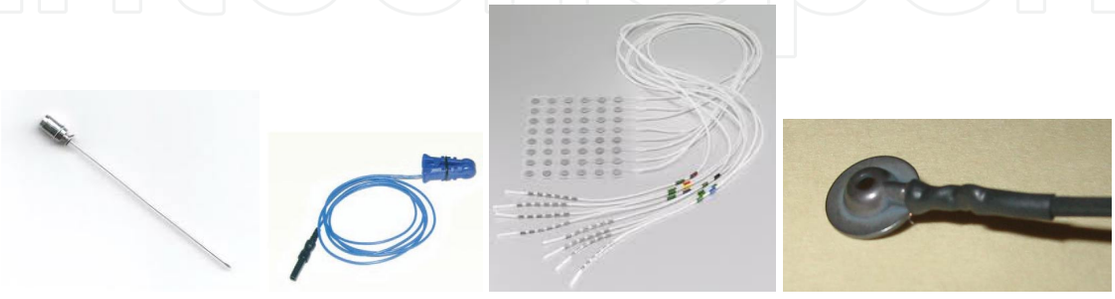
| **Rithm** | **DELTA** | **THETA** | **ALPHA** | **BETA** |
|---|---|---|---|---|
| Frequency Component | < 4 Hz | 4 to 7 Hz | 8 to 13 Hz | > 13 Hz |
| Amplitude | 100 $\mu$V | Child: 20 $\mu$V<br>Adult: 10 $\mu$V | Baby: 20 $\mu$V<br>Child: 75 $\mu$V<br>Adult: 50 $\mu$V | 10 to 20 $\mu$V |
| Main Scalp Area | Front | Temporal | Occipital<br>Pariental | Front |
| Human Condition | Deep Sleep | Sleepy | Relaxed<br>Closed Eyes | Relaxed<br>Openned Eyes |

**Table 1.** EEG Amplitudes Variations.

Those particularities suggest that the acquiring system should be able to provide adjustable gain, so that the physician could adjust the gain in order to obtain the best signal resolution.

Another important fact to consider is acquiring process itself. The acquiring devices may disturb and add others characteristics to the signal, that must be treated correctly by the measurement system, which is performed in this case by the EEG SoC array system.

For instance, the electrodes usually add 1 $V_{DC}$ to 2 $V_{DC}$ offset that must be eliminated. Figure 1 shows the most typical electrodes used on acquiring EEG signals.



(a) Niddle Electrode. (b) Ear Electrode. (c) Cortical Electrode. (d) Plate Dish Electrode.

**Figure 1.** Example of Electroencephalogram Electrodes.

Therefore the acquiring system must be capable of acquiring the data correctly, by taking into account the signal singularities and avoiding disturbing the measured signal.

The description of the measuring system and the design of the neural amplifier will be presented in the next sections.

## 3. System architecture

This chapter describes the design of a neural amplifier to be used as part of an EEG acquisition system, denoted by EEG system on chip (SoC) array.

As per EEG signal characteristics, it is necessary at least 22 acquisition elements to obtain enough data to properly perform an EEG neurological exam. Figure 2 shows the system architecture.

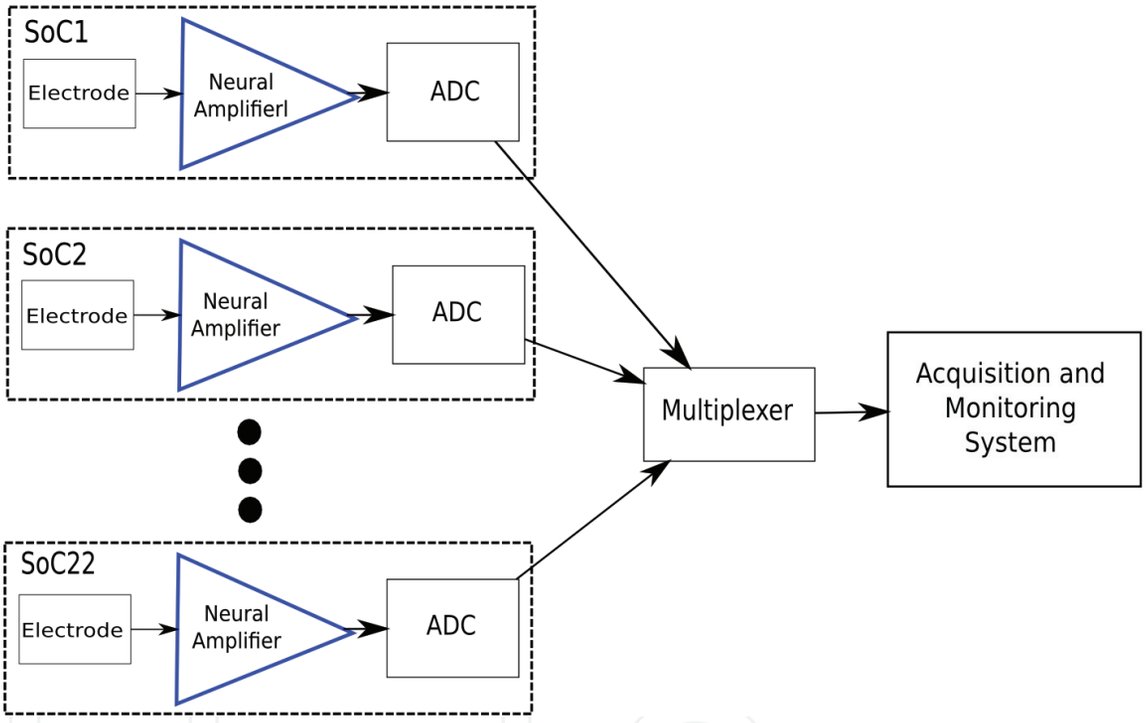



**Figure 2.** EEG Acquistion System Arquitecture.

Each acquiring element of the system is composed by an electrode, a neural amplifier (which is the focus of this work) and an analog to digital converter (ADC). If the amplification and AD conversion is placed on top of the electrode, the signal will be acquired, amplified and converted to digital almost at the same spot, and thus the previously related interferences may be deeply eliminated.

The digital converted signal from each electrode is multiplexed, serialized and then transmitted to the computer.

Figure 3 shows an example of physical implementation, where each small white spot on the blue cap represents an EEG SoC element. The output lines of the EEG SoC elements are input into a single element that multiplexes and transmits the data. The transmission can be performed by fiber optics, wire or even by any wireless procedure.

**Figure 3.** EEG Acquistion System Physical Structure.

## 4. Neural amplifier

The whole amplifier should provide low input referred noise and low power in order to meet the requirements of a neural amplifier for extended EEG applications. Figure 4 shows the basic circuit topology that will be detailed in the next sections.

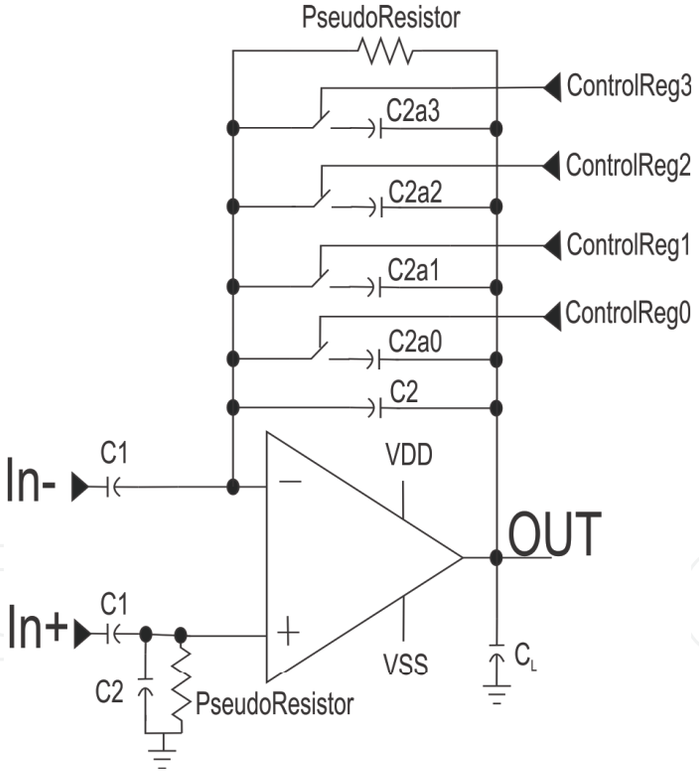



**Figure 4.** Proposed Neural Amplifier.

It also needs to provide an active band pass filter, allowing that signals in very low frequencies (hundreds of miliHertz) up to the proposed 1500 Hertz pass through while being amplified.

That is achieved with the PID feedback network, comprised by the OTA, decoupling capacitors, nMOS switches, pseudo-resistors and integration capacitors, that will be described on the next sections.

The achieved Neural Amplifier closed loop frequency response can be seen in Figure 5. Low and high-cut-off frequencies, as well as gains and input referred noise for each gain option are also compiled in Table 2.

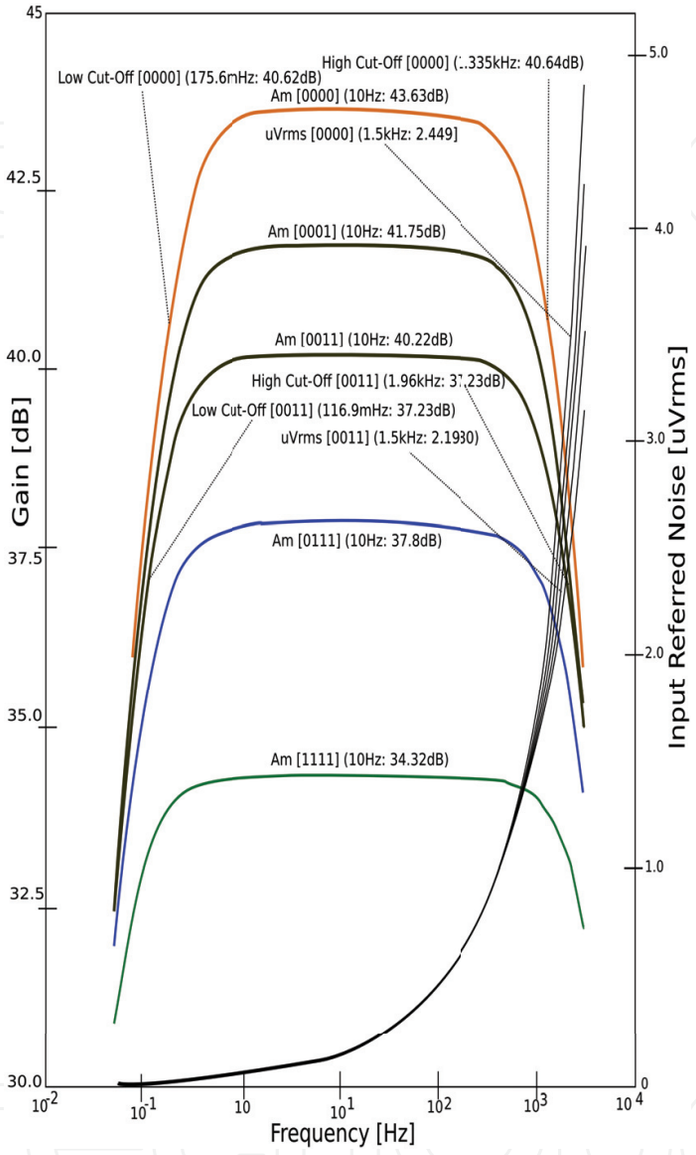



**Figure 5.** Neural Amplifier's Frequency Response.

| | Am (Designed) | Am (Simulated) | Low-CutOff | High-CutOff | Noise @ 1,5[kHz] |
|---|---|---|---|---|---|
| Register | [dB] | [dB] | [mHz] | [kHz] | [$\mu$Vrms] |
| 0000 | 43,52 | 43,63 | 175,6000 | 1,3350 | 2,4490 |
| 0001 | 41,94 | 41,75 | 150,7000 | 1,6435 | 2,2977 |
| 0011 | 40,00 | 40,22 | 116,9000 | 1,9600 | 2,1980 |
| 0111 | 37,50 | 37,80 | 88,2000 | 2,5643 | 2,0080 |
| 1111 | 33,98 | 34,32 | 55,5750 | 3,1000 | 1,9980 |

**Table 2.** Gains and Respective Input Referred Noise for Proposed Neural AMplifier.

### 4.1. PID feedback network with adjustable gain

The feedback network implements a band pass filter while controlling the gain, which can range approximately from 34.3 dB to 43.6 dB as shown in Figure 5. The variable gain is necessary to best fit the signal to the ADC stage, thus avoiding loss of resolution or signal saturation, while keeping the signal as reliable as possible. It also could mean an ADC of fewer bits, and consequently operating at lower frequencies, thus meaning even lower power dissipation. The inputs ControlReg come from digital registers that can be set by the software controlled by a physician, and the values are either $V_{DD}$ or $V_{SS}$ (in this case, $+1.8V$ or $-1.8V$, respectively).

The 4 ControlReg options allow 16 different gain combinations. However, due to capacitor integration concerns, to be presented in the next section, some combinations are not feasible. Therefore Table 2 presents only 5 different combination gains.

The highest gain is achieved with all ControlReg registers set as 0, in other words, just $C_2$ is connected to the network. The lower gain is implemented with all ControlReg registers set to 1, where $C_2$ and all integration capacitors $C_{2aX}$ are connected, as show in Table 2. Any other combination of ControlRegs implements a gain within the range of 43.52 dB to 33.98 dB.

The neural amplifier topology could be modified to reduce the number of gain steps by reducing the number of ControlReg lines, such as 2 or 3 lines.

The midband gain is given by (1):

$$A_M = \frac{C_1}{C_2 + \sum C_{2aX}} \tag{1}$$

where $C_{2aX}$ stands for each integration capacitor connected to the feedback network (controlled by its respective ControlReg switch, with X ranging from 0 to 3. $C_1$, $C_2$ and $C_{2aX}$ are shown in Figure 4.

The bandwidth, for $C_1$ and $C_L \gg C_2 + \sum C_{2aX}$ is given approximately by (2):

$$BW = \frac{g_m}{A_M.C_L} \tag{2}$$

where $g_m$ is the OTA transconductance, $A_M$ is the midband gain, BW is the bandwidth and $C_L$ is the load capacitance [1].

#### *4.1.1. Integration capacitors*

Integration capacitors $C_2$, $C_{2a0}$, $C_{2a1}$, $C_{2a2}$ and $C_{2a3}$ were taken as 139, 34.8, 34.8, 69.5 and 139 fF, respectively. They were implemented using a matched capacitor matrix [7], as shown in Figure 6, to decrease process variations that could disturb the gain and bandwidth, since it is essential to keep them as accurately as possible. Each individual capacitor provides 34.76 fF. They have equal wide and length dimensions, of 6.6 $\mu$m. By connecting groups of capacitors, it is possible to obtain multiple values.

Capacitor $C_1$ was sized 18 pF and $C_L$ is equal to 15 pF, and the received the same layout care as the integration capacitors. A guard ring made of dummy capacitors surrounds the matrix of capacitors to protect it against incoming noises.

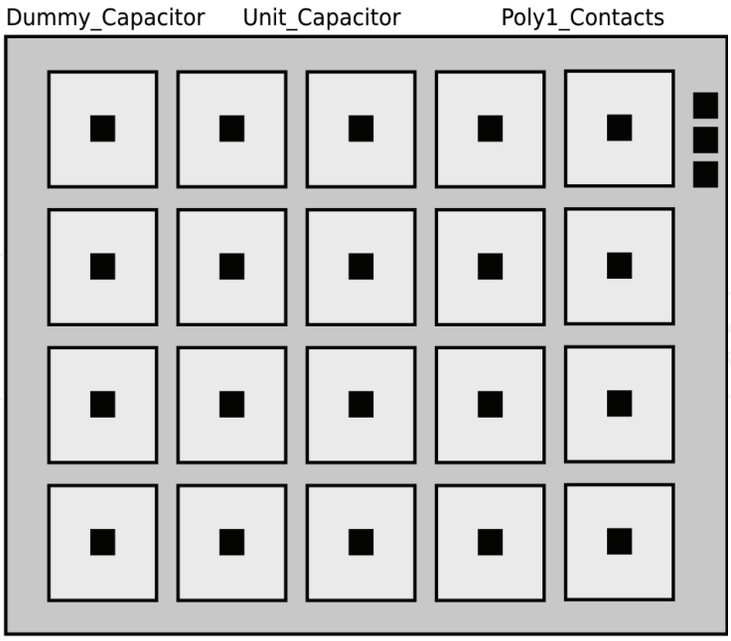



**Figure 6.** Matrix of Matched Capacitors for Integration Capacitors Layout.

*4.1.2. pMOS pseudo-resistor*

The pseudo-resistor presented in Figure 4 is actually composed of 6 diode connected pMOS transistors, as shown in Figure 7. In this topology each transistor was sized 4 $\mu$m x 4 $\mu$m. As described in [3], under positive $V_{GS}$, the parasitic source-well-drain pnp bipolar junction transistor (BJT) is activated, making the devices to act as junction BJT diode, thus providing the resistivity behavior indicated in Figure 8. It can be observed that for $V_{GS}$ close to 0 V the resistance decreases. It is not interesting to our application, since the low-frequency cutoff given by (3) increases for lower values of resistance.

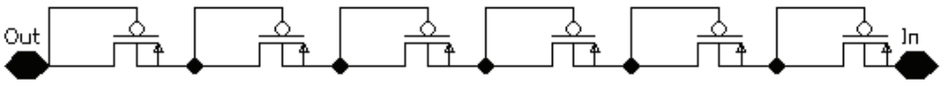



**Figure 7.** pMOS Pseudoresistor Implementation.

$$W_L = \frac{1}{2.R_{PseudoResistor}.C_2} \tag{3}$$

The cutoff should be as close to zero as possible but at the same time, it should block the DC signals, so that the offset generated by electrodes can be eliminated in order to avoid biasing problems on the OTA differential pair. Therefore the OTA was designed to provide approximately 90 mV of systematic offset to achieve the low cutoff frequency required by the EEG applications, hence keeping capacitance $C_2$ low. It reduces the need of large area to build large integration capacitances, since the pseudo-resistor provides resistance on the order of $10^9$ Ohms for this range of $V_{GS}$. It was chosen the dimension of 4 $\mu$m x 4 $\mu$m for the capacitors to avoid any short channel effects on the feedback network, which could cause unexpected behaviors.

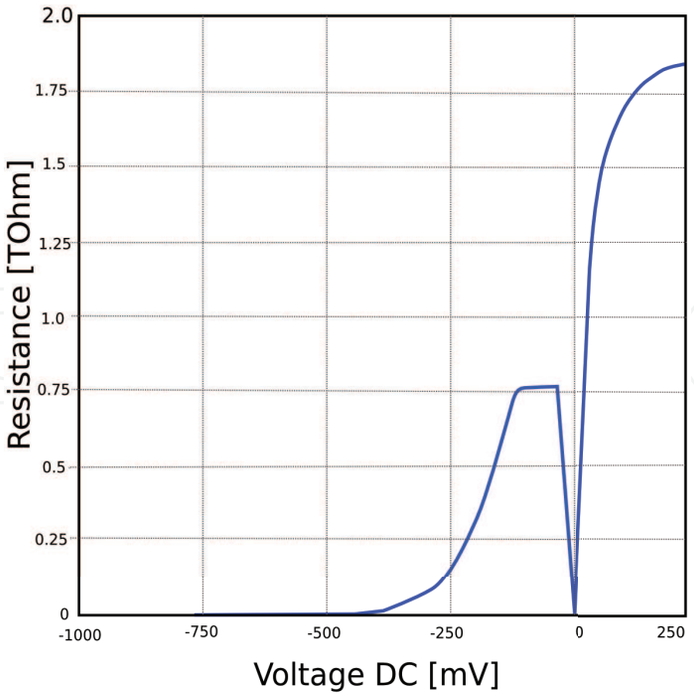



**Figure 8.** PseudoResistor Resistance Behavior.

*4.1.3. Parasitic insensitive nMOS switch*

In order to switch the integrator capacitors of the PID network it was used a topology of nMOS transmission switches [8], as shown in Figure 9. That topology is essential since it substantially minimizes the effects of parasitic on the switching transistors.

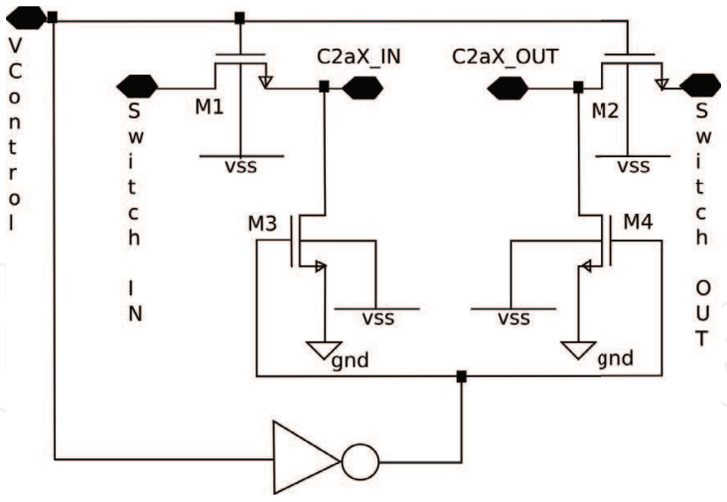



**Figure 9.** nMOS Transmission Switch.

The circuit works switching the integrator capacitor placed between $C_{2aX-IN}$ and $C_{2aX-OUT}$, as indicated in Figure 9. The switched capacitors correspond to each capacitor $C_{2a0}$ to $C_{2a3}$ in Figure 4. As the control register goes high ($V_{DD}$) the signal $V_{Control}$ biases directly transistors $M_1$ and $M_2$, and the switching capacitor is placed on the OTA feedback network while transistors $M_3$ and $M_4$ are kept off. Whenever the control register assumes low level ($V_{SS}$), $M_1$ and $M_2$ are turned off and $M_3$ and $M_4$ are turned on, taking potential GND to the sources

of $M_1$ and $M_2$, thus decreasing the effects of parasitic when the feedback branch is not on. All transistors were sized 4 $\mu$m x 2 $\mu$m.

Figure 10 shows the schematic of the OTA used for the neural signal amplification that can be used in a wide range of applications [1].

## 4.2. OTA design

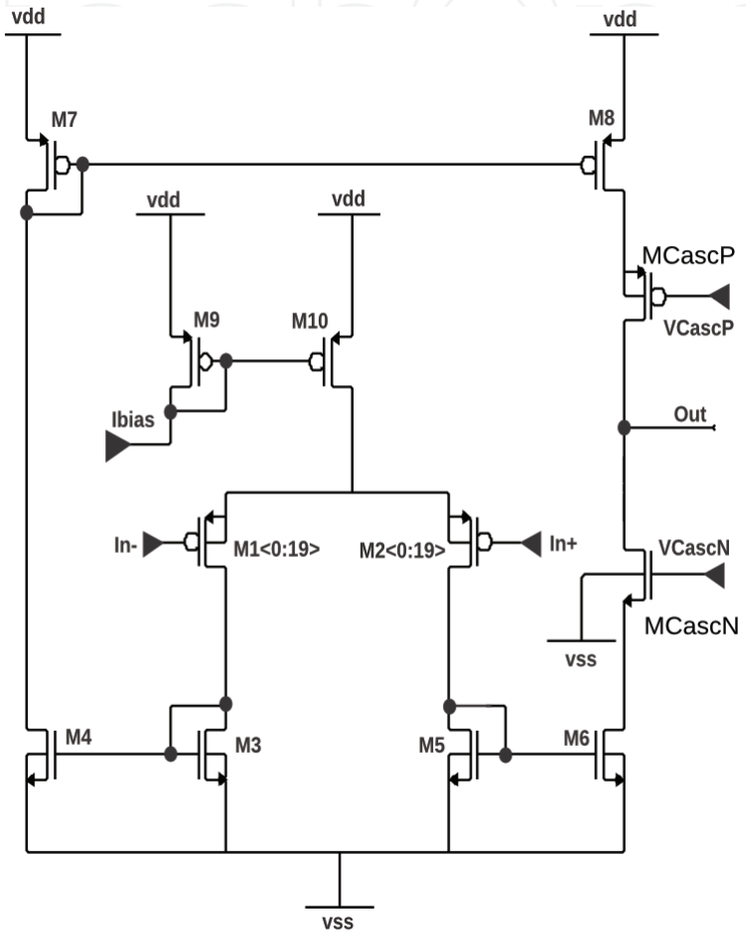



**Figure 10.** OTA Design.

The bias current IBias was set to 3 $\mu$A, so that $M_1$ to $M_8$ drain currents are 1.5 $\mu$A and total bias drained current is 6 $\mu$A.

It was calculated the region of operation for each transistor by calculating the moderate inversion characteristic current IS [9] using equation (4):

$$I_S = \frac{2.\mu.C_{OX}.{U_T}^2}{\kappa}.\frac{W}{L} \tag{4}$$

where $U_T$ is the thermal voltage $\frac{kT}{q}$, and $\kappa$ is the subthreshold gate coupling coefficient which is equivalent to 1/n where n denotes the reciprocal of the change in surface potential $\psi_{sa}$ for a change in gate-to-body voltage $V_{GB}$ [1, 9, 10].

Next it was calculated the inversion coefficient, which is given by the transistor drain current divided by moderate inversion characteristic current [1], as (5):

$$IC = \frac{I_D}{I_S} \tag{5}$$

An IC $>$ 10 means the device operates in strong inversion. In case IC $<$ 0.1, it operates in weak inversion. Any IC between those limits means the device is operating in moderate inversion.

In this work, the transconductance $g_m$ of those devices operating in weak and moderate inversion have been modeled by using the EKV model [11], as given by (6):

$$g_m = \frac{\kappa.I_D}{U_T}.\left(\frac{2}{1+\sqrt{1+4.IC}}\right) \tag{6}$$

The strong inversion device modeling is given by (7):

$$g_m = \sqrt{2.I_D.\mu.C_{OX}.\frac{W}{L}} \tag{7}$$

Table 3 summarizes the main data of each device, including its operation region. Devices grouped in the same row in Table 3 have the same size and hence the same region of operation, and same transconductance $g_m$. For simplicity their $g_m$ will be generalized to the first index device (i.e. $g_{m3}$ equals to $g_{m4}$, $g_{m5}$ and $g_{m6}$).

| Devices | $V_{GS}$ [V] | $V_{overdrive}$[V] | IC | W/L | $I_D$ [uA] |
|---|---|---|---|---|---|
| $M_1$, $M_2$ | 0,9033 | 0,0160 | 0,053 | 900 / 2 | 1,500 |
| $M_3$, $M_4$, $M_5$, $M_6$ | 1,3293 | 0,4702 | 43,387 | 10 / 40 | 1,500 |
| $M_7$, $M_8$ | 1,5788 | 0,7197 | 99,008 | 6 / 25 | 1,500 |
| $M_9$, $M_{10}$ | 1,6015 | 0,7142 | 105,609 | 9 / 20 | 3,000 |
| $M_{cascN}$ | 0,9948 | 0,1357 | 3,616 | 12 / 4 | 1,500 |
| $M_{cascP}$ | 1,2945 | 0,4072 | 34,323 | 4.5 / 6.5 | 1,500 |

**Table 3.** OTA's Design Calculated Values

As shown by [1], the input referred thermal noise power for that adopted OTA topology is given by (8):

$$\overline{v^2_{ni,thermal}} = \left[\frac{16.k.T}{3.g_{m1}}.\left(1+2.\frac{g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right)\right].\Delta f[V^2] \tag{8}$$

It can be observed that in order to minimize the noise, it is necessary to increase $g_{m1}$ and decrease $g_{m3}$ and $g_{m7}$. By proper sizing the differential pair, as shown in Figure 10, it can be guaranteed weak inversion operation. It sets high $g_{m1}$ whereas $g_{m3}$ and $g_{m7}$ are placed into strong inversion, which decreases their $g_m$. Several simulations were conducted to minimize this ratio in order to minimize noise, while keeping the stability of the OTA. By considering the transistors geometry designed and a load capacitance $C_L$ of 15 pF, the OTA provided a 63 degrees phase margin, as shown in Figure 11.

In order to decrease the flicker noise 1/f, which is always a constraint for low frequency applications, it was used a differential pair composed of pMOS transistors, which provide typically, one to two magnitude orders lower than in nMOS devices [9, 12]. The flicker noise

is inversely proportional to gate area, so the devices were made as large as possible while keeping it reasonable. The amplifier input referred noise can be related to the OTA input referred-noise [1] by (9):

$$\overline{v^2_{ni,amp}} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right).\overline{v^2_{ni}}[V^2] \tag{9}$$

where $C_1$ and $C_2$ are indicated in Figure 4 and again $C_2$ means the sum of integration capacitors connected to the PID feedback network.

Since $C_{in}$ contributes to a capacitive divider that attenuates the input signal, any increase in $C_{in}$ also increases the input referred noise of the whole amplifier.

*4.2.1. Stability criterion*

As described in the previous section, the design of the OTA prioritizes the minimum amount of noise generated by increasing the transconductance of the differential pair (denoted by $g_{m1}$) whereas decreasing the transconductance of the current mirrors devices (denoted by $g_{m3}$ and $g_{m7}$). However it can not be done indefinitely due to the risk of losing stability.

For the OTA architecture, the stability criterion is defined as:

$$\frac{g_{m1}}{C_L} \ll \frac{g_{m3}}{C_3} and \frac{g_{m7}}{C_7} \tag{10}$$

where $C_3$ means the capacitance seen by the gate of $M_3$, $C_7$ means the capacitance seen by the gate of $M_7$, $C_L$ is the load capacitance, $\frac{g_{m1}}{C_L}$ denotes the main pole and $\frac{g_{m3}}{C_3}$ and $\frac{g_{m7}}{C_7}$ are secundary poles.

As seen in Figure 11, the OTA was designed to have about 63 degrees of phase margin, ensuring system stability.

### 4.3. Noise Efficiency Factor - NEF

The NEF is one of the most important benchmark for this kind of application. The noise should be minimized while keeping a low power consumption budget. The NEF [11] is given by (11):

$$NEF = V_{ni,rms} \cdot \sqrt{\frac{2.I_{Total}}{\pi.U_T.4kT.BW}} \tag{11}$$

where $V_{ni,rms}$ is the input-referred noise rms voltage, $I_{Total}$ is the total consumed current and BW is the bandwidth, in Hertz.

For better understanding the NEF, it is made a comparison with a bipolar transistor, which is considered not having flicker noise. The NEF of a bipolar transistor is said to be equal 1. All real circuits, although, have a NEF higher than 1.

By replacing (11) for (8), which express the thermal noise for the OTA topology, integrating for the entire bandwidth BW, and assuming $g_{m3}$ e $g_{m7} \ll g_{m1}$ (totally reasonable), then by looking at Table 3, (11) becomes:

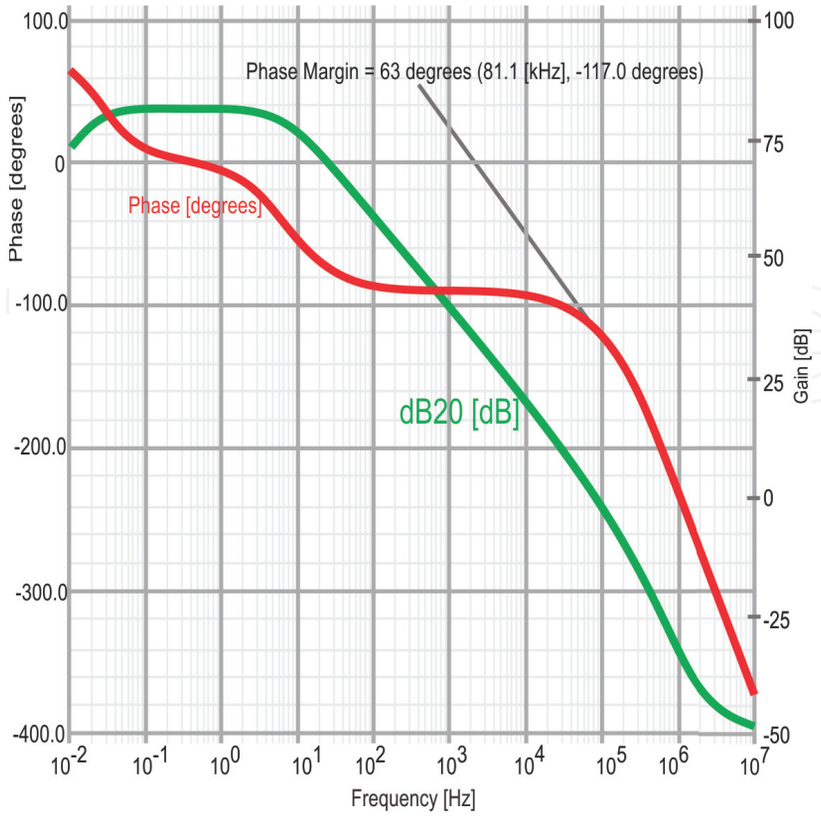



**Figure 11.** OTA Bode Diagram.

$$NEF = \sqrt{\frac{4.I_{Total}}{3.U_T.g_{m1}}} = \sqrt{\frac{16}{3.U_T}.\frac{I_{D1}}{g_{m1}}} \tag{12}$$

where $I_{D1}$ is the drain current through $M_1$ or $M_2$, which is easy to see that it is $\frac{1}{4}$ of $I_{Total}$.

Therefore, it can be concluded that for minimizing NEF, the relative transconductance $g_m$ of the pMOS transistor of the differential pair must be increased. Hence, those devices were sized in such a way to guarantee the operation in saturation - weak inversion since, in that region of operation, the relative transconductance reaches its maximum value of $\frac{\kappa}{U_T}$, as in [1].

Using a more accurate model of thermal noise for the saturation - weak inversion region of operation, as presented in [9], the NEF becomes:

$$NEF = \sqrt{\frac{4}{\kappa.U_T}.\frac{I_{D1}}{g_{m1}}} \tag{13}$$

Finally, assuming a value of $\kappa$ of approximately 0.7, which was calculated for this technology, the NEF can be reduced to (14):

$$NEF = \sqrt{\frac{4}{\kappa^2}} \approx 2,9 \tag{14}$$

That value of 2.9 can be considered the theoretical limit of NEF for the design using ON 0.5 $\mu$m technology.

## 5. Proposed layouts

Figure 12 shows a proposed layout for the OTA. The differential pair devices are designed as 20 parallel devices each one, helping to decrease even more the noise. They are shown at the bottom part. Current mirrors and Cascode devices are placed on the top.

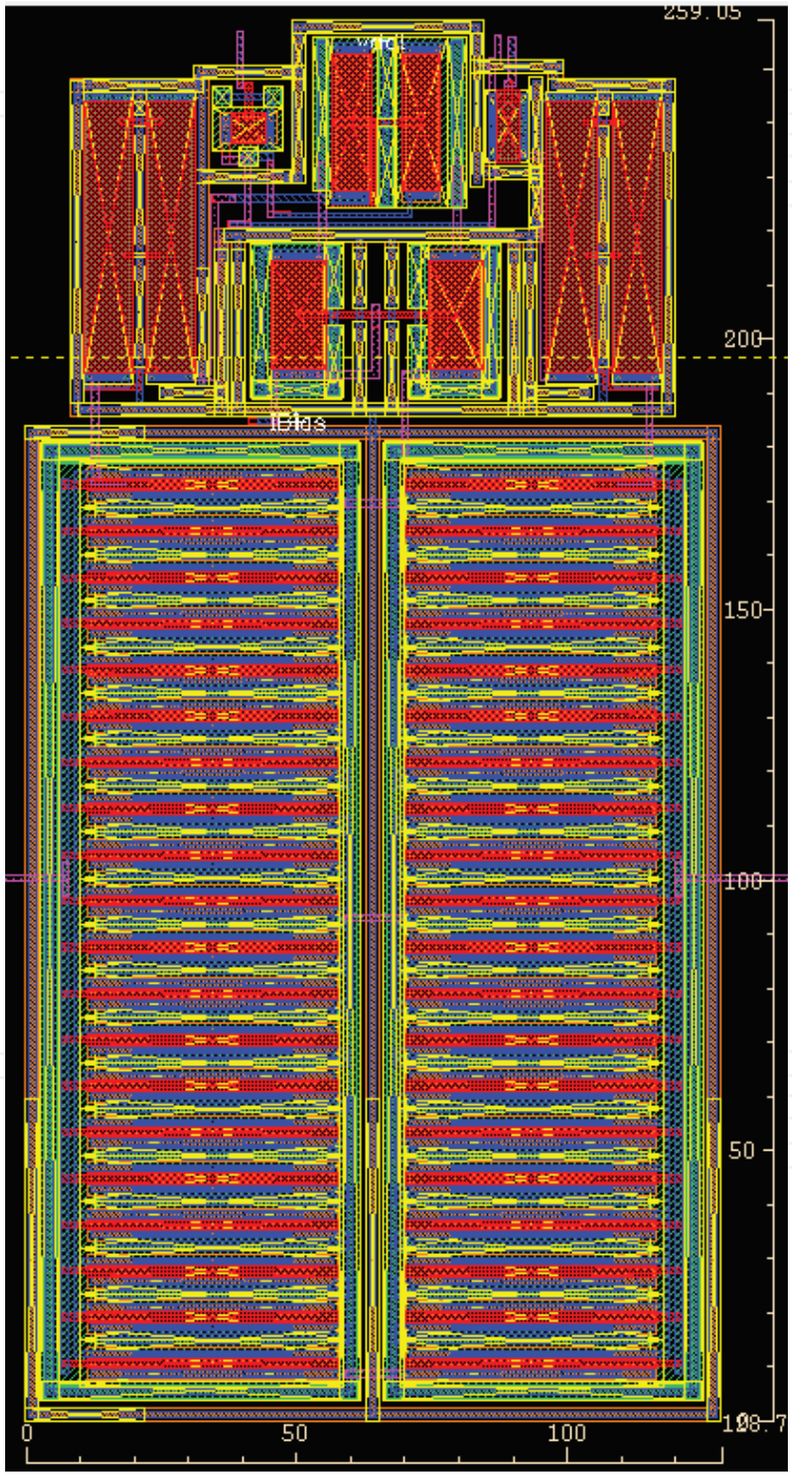



**Figure 12.** OTA Proposed Layout.

Figure 13 shows the proposed implementation of the entire neural amplifier. Decoupling capacitors $C_1$ are implemented aside of the differential pair inputs. All active areas were shielded with a grounded Metal 3 layer. Capacitors $C_2$, pseudo-resistors and nMOS switches are implemented at the top part.

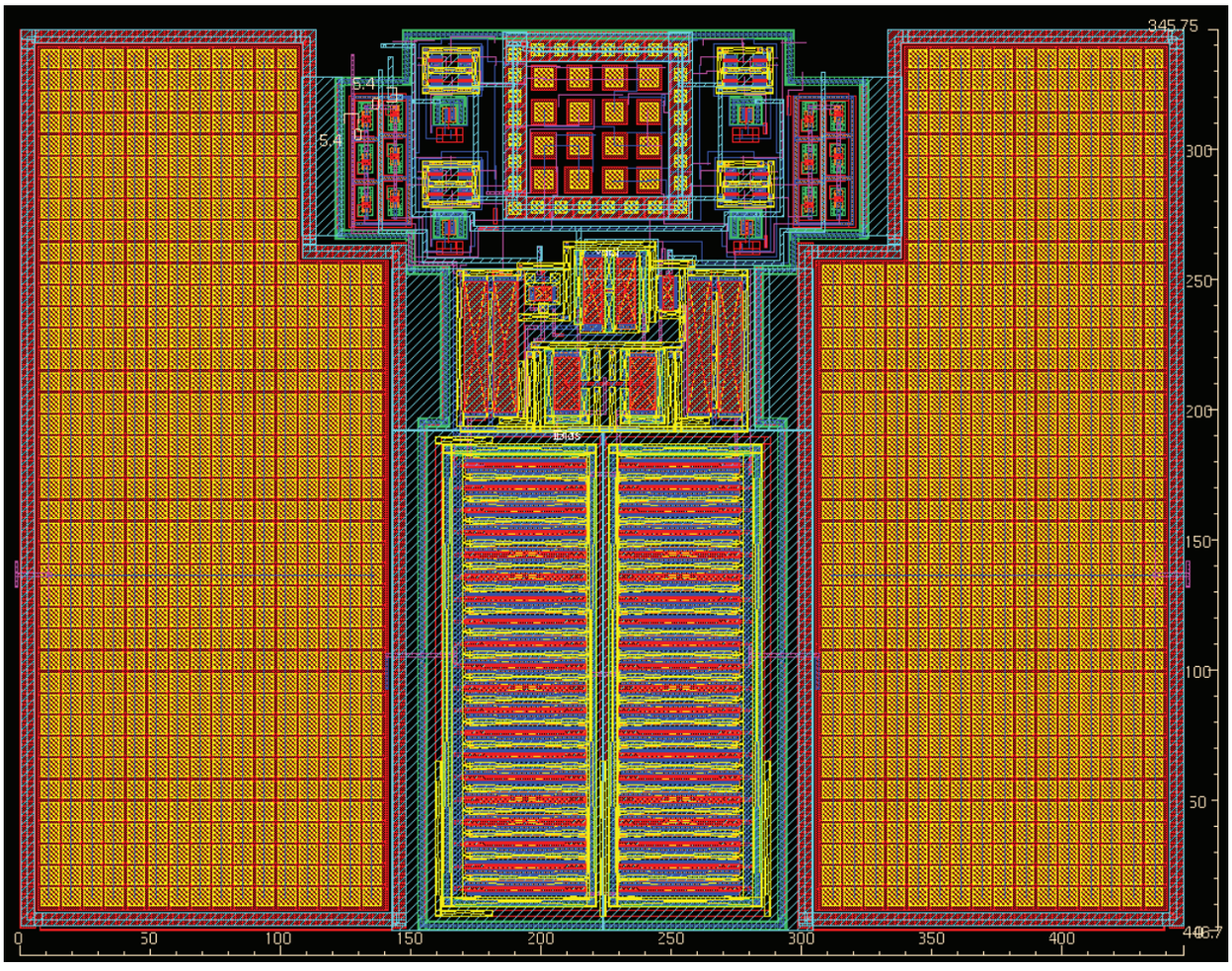



**Figure 13.** Neural Amplifier Proposed Layout.

## 6. Future research

By going through the proccess of designing this neural amplifier, it was realized the need of, basically:

- The neural amplifier must be fabricated and validated;
- Other technologies and diffusion characteristics could be used to evaluate any noise increase;
- Add the sample & hold circuit as well as an ADC;
- Integrate all elements on chip (neural amplifier, sample & hold and ADC);
- Conduct the analysis of disturbances in the analog signal due to noises generated by the digital converter.

## 7. Conclusion

This chapter described the implementation of a neural amplifier in ON 0.5 $\mu$m technology. It consumes only 26 $\mu$W on an $\pm$ 1.8 V power supply. It is comprised of a fully integrated PID feedback network formed by pMOS pseudo-resistors, nom-sensitive nMOS switches and a matrix of matched integration capacitors, capable of amplifying neurological signals on a 1.5 kHz bandwidth.

It also offers the option of choosing the gain among five different discrete values, varying from 43.52 dB to 33.98 db, as described on Table 2. The option of gain controlling is essential. It could mean lesser bits on the ADC converter, so that it could work under lower frequency and consequently dissipating lower power.

The input signal can vary from few $\mu$Vpp to approximately 10 mVpp with total harmonic distortion (THD) lower than 1%, and therefore the amplitude range is much wider than necessary for EEG signals.

The neural amplifier can be part of a fully integrated system on chip (SoC) for a full EEG measurement device, capable of measuring signals in higher frequencies than in standard EEG signals bandwidth. This complete system, an EEG SoC Multichannel Array would also contemplate a sample and hold structure, an ADC converter and a multiplexer for gathering and transmitting the data.

This chapter also presented a compilation of the benchmarks obtained for the neural amplifier, presented in Table 4 along with a comparison to the main references. Since the references, as

| | | **This Work** | **[1]** | |
|---|---|---|---|---|
| | **Technology** | **ON 0.5 $\mu$m** | **Standard 1.5 $\mu$m** | |
| | **Unity [ ]** | **Simulated** | **Simulated** | **Measured** |
| Power Supply Voltage | $\pm$ V | 1,8 | 2,5 | 2,5 |
| Biasing Current | $\mu A$ | 6 | 16 | 16 |
| Gain | dB | 40,22 | 40 | 39,5 |
| Low Cutoff Frequency (40 [dB]) | mHz | 116,9 | 130 | 25 |
| High Cutoff Frequency (40 [dB]) | kHz | 1,96 | 7,5 | 7,2 |
| Input Referred Noise | $\mu V_{rms}$ | 2,1980 | 2,1 | 2,2 |
| NEF | [ ] | 4,55 | 3,8 | 4 |
| THD ($<$ 12.8 mVpp) | % | $<$ 1 | - | 1 |
| Dynamic Range (1% THD) | dB | - | - | 69 |
| CMRR $\leq$ 5[kHz] ($>$ than) | dB | 86,32 | 42 | 83 |
| Slew Rate Rise/Fall | $\frac{V}{ms}$ | 100 / 200 | - | - |
| Settling Time Rise/Fall | [$\mu$s] | 60 / 15 | - | - |
| PSRR $\leq$ 5[kHz] ($>$ than) | dB | 75,12 | 42 | 85 |
| CrossTalk | dB | - | - | -64 |
| Area | $mm^2$ | 0,134 | 0,16 | 0,16 |
| Power | $\mu W$ | 26 | 80 | 80 |
| Phase Margin | $^o$ | 63 | 52 | - |

**Table 4.** Results and Comparison

in [1] did not offer gain control, all benchmarks were calculated taking the 40 dB gain as reference, in order to present similar circumstances.

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