Chapter 14

Low-Voltage, Low-Power V_t Independent Voltage Reference for Bio-Implants

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Additional information is available at the end of the chapter

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1. Introduction

Microelectronics has become a powerful tool of electronic systems for biomedical applications. In recent years, integrated circuits are being fabricated with large densities and endowed with intelligence. The reliability of these systems has been increasing and the costs have been reducing. The interaction between medicine and technology, as it is the case of microelectronics and biosensor materials, allows the development of diagnosing devices capable of monitoring pathogens and diseases. The design of sensors, signal conditioners and processing units aim to place the whole system in the patient or, even more desirable, implanted, where it becomes a Lab-on-Chip and/or a Point-of-Care device (Colomer-Farrarons et al., 2009). Once an implanted device becomes part of a biological data acquisition system, it must meet important constraints, such as reduced size, low power consumption and the possibility of being powered by an RF link, thus operating as a passive RFID tag (Landt. J, 2005).

The low power restriction is extremely important to the patient safety in order to avoid local heating and consequently possible tissue damage. It also limits the power of RF transmitter that can, as well, induce dangerous electromagnetic fields – EMF (large current density in the body tissue surrounding the implant). The EMF risks can be extended to the implanted device itself such as malfunction (undesirable lack of action, erroneous action and hazardous action) and even, permanent damage.

The focus of this chapter is to discuss the implementation of a CMOS voltage reference and the boundary conditions, including the use of a low cost CMOS process (0.35 TSMC for instance), low-voltage low-power operation and simple circuit topology.

2. Typical implanted device as a smart biological sensor

A typical CMOS front-end architecture for an in-vivo Biomedical Implanted Device – BID is shown in Figure 1. The system consists, basically, of the sensitive biological element, the transducer or detector element and its associate electronics and signal processing, and the RF link to establish a communication with the external unit. The combination of the implanted device, the local wireless link and a communication network results in a Wireless Biosensor Network (WBSN) (Guennoun, et al., 2008).

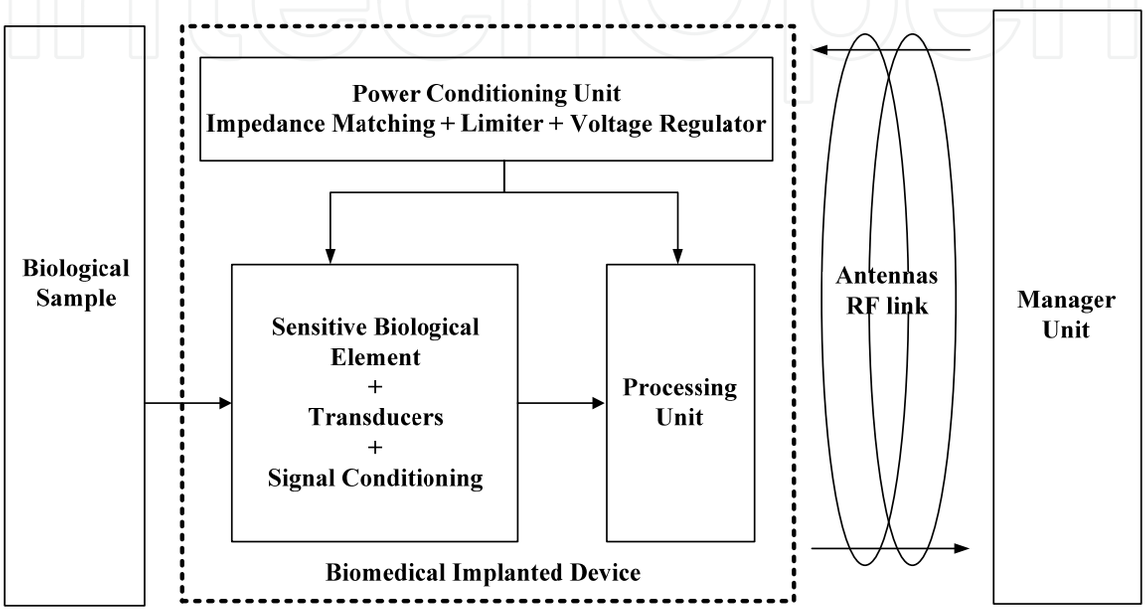

Figure 1. Typical Implanted Biomedical Device acting as a RFID Tag.

Linear systems based on semiconductor devices demand a stable power supply voltage for proper operation. Fluctuations on the input line voltage, load current and temperature variations may cause the circuit to deviate from its optimum operation bias point and even loose its linearity. Therefore, the power supply topology must assure minimum impacts on the linearity under those variations (Crepaldi et al., 2010). The impact of temperature variations in implantable devices is minimized once the body temperature is kept stable at approximately 37°C by an efficient biological feedback system (Mackowiak et al., 1992). Even in the presence of a disease or during a surgery proceeding, the body temperature suffers from just a few Celsius degrees variation.

As can be seen on Figure 1, a Voltage Regulator is part of the power conditioning unit. It is responsible to provide a stable voltage to the sensors/transducers and their associated electronics.

The classic topologies designed to provide stable power supply voltage are the linear and the switched voltage regulators. Switched regulators present a complex topology, mainly due to its control systems, and generally require more power consumption and larger silicon area than linear ones. Additionally they generate more noise at the regulated output due to its inerently switching operation (Rincon-Mora & Allen, 1998).

The low-dropout (LDO) voltage regulator is one of the most popular power converter used in power management and it is extremelly suitable for implanted systems. This kind of regulator requires a voltage reference circuit with a good Process-Voltage-Temperature (PVT) tolerance, generally achieved by Bandgap references. There are alternative circuits capable of obtaining low-voltage and high-accuracy, nevertheless some of those approaches may require components not readily available in CMOS technology and may require additional fabrications steps. Bandgap references based on weak inversion operation are a promising trend in biomedical applications (Roknsharifi et al., 2001; Magnelli et al., 2011). Since the reference is intended to be used in an implanted device, the temperature range is narrow and therefore it is not taken into account. The reference voltage Power Supply Rejection Ratio (PSRR) and process dependence are the main concerns.

3. Voltage reference

Figure 2 shows the voltage reference suitable for umplented devices. Transistors M_1 and M_2 form the composite structure (Ferreira & Pimenta, 2006). This kind of arragement represents the key feature for low-voltage operation, and along with low current operation (in the range of nA), the circuit provides low power operation. The voltage reference is obtained at M_2 drain and it corresponds to its V_{DS} voltage. The current I_D is be fixed at tenths of nA in order to reduce the total power consumption, as stated. Also, it is desirable to have the power supply reduced to a minimum, respecting, however, the corner process.

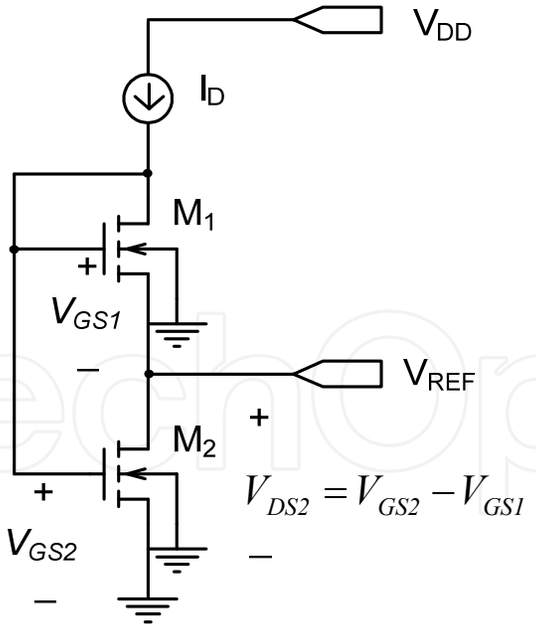

Figure 2. Voltage Reference Basic Topology.

If the MOS transistors are biased in the sub-threshold region, the drain current is given by equation (1). This current is based on the channel diffusion current referred to voltage source. It is a consensus formulation among EKV, ACM and BSIM3v3 models. I_S is the weak inversion characteristic current, T is the absolute temperature, n is the slope factor in weak

inversion (typically 1.3), k is the Boltzmann constant, (W/L) is the transitor geometric aspect ratio, V_{TH} is the threshold voltage and q is the charge of the electron.

$$I_{DS} = I_S\left(\frac{W}{L}\right)exp\left(\frac{V_{GS}-V_{TH}}{\frac{nkT}{q}}\right)\left[1-exp\left(-\frac{V_{DS}}{\frac{kT}{q}}\right)\right] \tag{1}$$

Considering transistor M_2 operating in the saturation region, equation (1) can be simplified for V_{DS} values that are larger than the thermal equivalent voltage (kT/q). At body temperature, approximately 310K, (kT/q) can be set to 26.7mV, so for an 80mV at V_{DS} (3 times larger) the (1-exp) term in equation (1) can be neglected and the drain current is expressed as:

$$I_{DS} = I_S\left(\frac{W}{L}\right)exp\left(\frac{V_{GS}-V_{TH}}{\frac{nkT}{q}}\right); \quad V_{DS} \geq 3\frac{kT}{q} \approx 80mV@T = 310K \tag{2}$$

The current I_S is the same for transistors M_1 and M_2 since it is a function of process parameters. V_{REF} is obtained by considering that M_1 and M_2 drain currents (I_{DS}) are also equal.

$$\frac{I_{DS}(M1)}{I_{DS}(M2)} = \frac{I_S\left(\frac{W}{L}\right)_{M1}exp\left(\frac{V_{GS1}-V_{TH1}}{\frac{nkT}{q}}\right)}{I_S\left(\frac{W}{L}\right)_{M2}exp\left(\frac{V_{GS2}-V_{TH2}}{\frac{nkT}{q}}\right)} = 1 \tag{3}$$

By inspection of Figure 2 it is possible to establish a relationship between the drain source voltage of M2 and the gate voltages of M1 and M2, given as:

$$V_{DS2} = V_{GS2} - V_{GS1} \tag{4}$$

By substituting (4) into (3), V_{DS2} is given as:

$$V_{DS2} = \frac{nkT}{q}ln\left[\frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{M2}}\right] - V_{TH1} + V_{TH2} \tag{5}$$

Transistor M_2 has a nominal threshold voltage (V_{TH0}) but M_1 suffer from body effect and, consequently, its threshold voltage should be adjusted by:

$$V_{TH1} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \tag{6}$$

where γ is the body factor coefficient and $2\Phi_F$ (≈600mV) is the Fermi potential. Notice that V_{SB} (bulk-source potential) is equal to M_2 drain source voltage or, in other words, it is equal to V_{REF}. The following approximation (Burington, 1973). can be used, if $(V_{REF})^2 << (2\Phi_F)^2$.

$$\begin{aligned} \sqrt{a+x} &= \sqrt{a} + \frac{x}{2\sqrt{a}}; \quad a^2 >> x^2 \\ \sqrt{2\Phi_F + V_{REF}} &= \sqrt{2\Phi_F} + \frac{V_{REF}}{2\sqrt{2\Phi_F}}; \quad {V_{REF}}^2 << (2\Phi_F)^2 \end{aligned} \tag{7}$$

By combining (5), (6) and (7), the reference voltage is given as:

$$V_{REF} = \frac{n\frac{kT}{q} ln\left[\frac{\left(W/L\right)_{M1}}{\left(W/L\right)_{M2}}\right]}{1 + \frac{\gamma}{2\sqrt{2\Phi_F}}} \tag{8}$$

Considering that (Tsividis, 1999):

$$1 + \frac{\gamma}{2\sqrt{2\Phi_F}} = n \tag{9}$$

The resulting equation for the reference voltage is:

$$V_{REF} = \frac{kT}{q} ln\left[\frac{\left(W/L\right)_{M1}}{\left(W/L\right)_{M2}}\right] \tag{10}$$

As can be observed, the reference voltage does not depend on MOS transistors threshold voltages and its value is adjusted by the geometric aspect ratio between the M1 and M2. The threshold voltage is largely affected by process variations (corners). For instance, in TSMC 0.35μm technology, the 3σ deviation from typical conditions can be as large as 20%.

Furthermore, the operation in the subthreshold region (or weak inversion) provides promotes an additional feature for the circuit, which is the low-voltage and low-power topology (Bero & Nyathi, 2006; Nomani et al., 2010; Ueno et al., 2006).

3.1. V_{REF} range values

The minimum V_{REF} value is determined by the approximation that leads to eq. (2). The maximum value is determined by the approximation that leads to eq. (7) and Table I shows the relative error at different values of V_{REF}.

V_{REF} [mV]	$\sqrt{2\Phi_F + V_{REF}}$	$\sqrt{2\Phi_F} + \frac{V_{REF}}{2\sqrt{2\Phi_F}}$	Relative Error (%)
80	0.825	0.826	0.196
100	0.837	0.839	0.297
120	0.849	0.852	0.416
140	0.860	0.865	0.550
160	0.872	0.878	0.699

Table 1. V_{REF} Relative Error for eq. (7) approximation.

For this project, it is adopted 100mV for V_{REF}. This value is larger than 3(kT/q) and represents an error of less than 0.5%, as stated in Table I. Besides, it is an "exact" value to be used in the voltage regulator to obtain other reference values.

3.2. V_{REF} temperature impact

Although the proposed circuit is intended to be used in a temperature controlled environment, a temperature analysis is performed, and it shows a linear behavior. Although it is an important result, the implanted biomedical system could use any calibration method to compensate the process corners deviations. The temperature behavior of V_{REF} can be found from eq. (11) at the different temperatures T_0 and T.

$$\frac{V_{REF}(T)}{V_{REF}(T_0)} = \frac{\frac{kT}{q} ln\left[\frac{\left(W/L\right)_{M2}}{\left(W/L\right)_{M1}}\right]}{\frac{kT_0}{q} ln\left[\frac{\left(W/L\right)_{M2}}{\left(W/L\right)_{M1}}\right]} = \frac{T}{T_0} \tag{11}$$

It can be inferred from eq. 11 that the drain-source voltage of M1 presents a PTAT (Proportional to Absolute Temperature) behavior. Fig. 3 shows the simulation of circuit from Fig. 1 over the 35°C to 42°C temperature range, for a 500mV power supply voltage. That temperature range corresponds to limits between surgical procedures (lowered body temperature) or any pathology (fever). The simulation includes the three corners; typical, slow and fast. Additional circuitry, as shown in Fig. 1 (Processing Unit), can be added to provide an analog to digital conversion, where the gain and offset errors can be minimized.

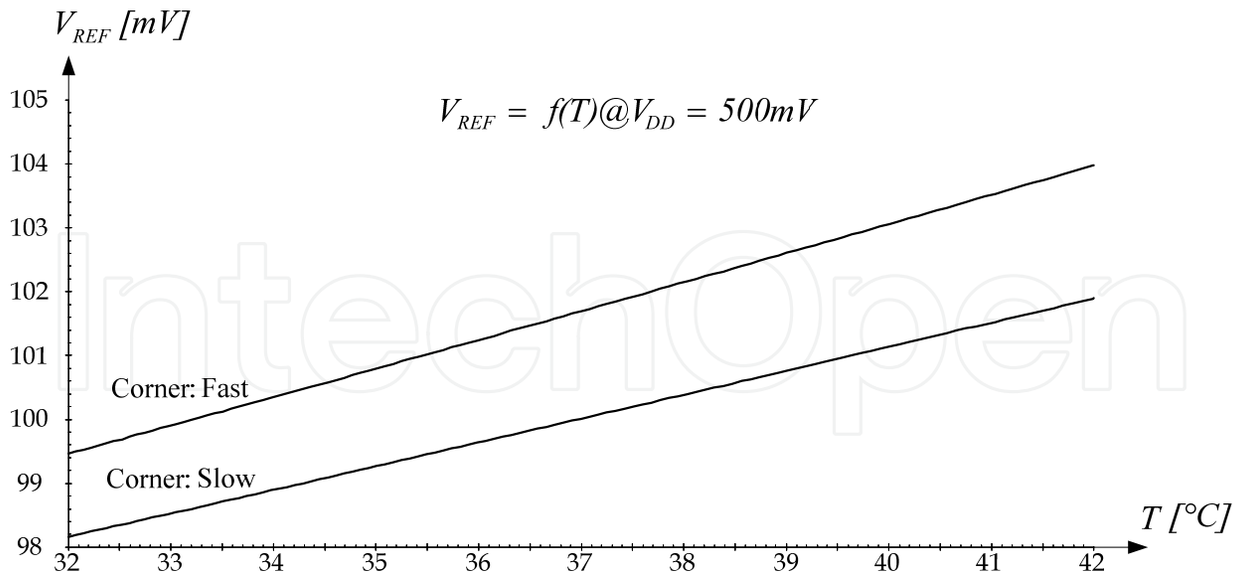

Figure 3. Simulation of V_{REF} voltage @ V_{DD}=0.5V for a clinical temperature range including the fast and slow process corners.

Including this temperature impact, the voltage reference can be stated as having a nominal value of 100mV (typical) with a worst case dispersion of +4% (fast corner) and -1,8% (slow corner). The respective temperature coefficients are 0.35mV/°C (slow corner) and 0.45mV/°C (fast corner).

4. The voltage reference circuit implemented with composite transistors

Fig. 4 shows the circuit used to generate the current I_D. Transistor M5 is biased by the voltage reference, which it is assumed to be constant, and its drain current (I_{REF}) is mirrored by M3-M4. The overall circuit implementation is done by using composite transistors as depicted in Fig. 5. The current I_D is fixed at approximately 15nA. As can be observed, there is a feedback loop M2-M5 that does improve the PSRR of the circuit, as it will be demonstrated by simulation. The use of composite transistors is fundamental to reduce the mismatch between the mirrored currents.

As it is the case of self-biased circuits, it is necessary a startup circuit. It is implemented through transistor M_{START}, and capacitors C_{START1} and C_{START2}. On power up, an impulsive current will flow and the circuit will be lead to the desired operation point condition. All the transistors aspect ratios are optimized by a set of interactive simulations aiming the target values I_D=15nA and V_{REF}=100mV, for the typical process parameters.

Transistor M6 is included in the feedback loop to improve the power supply rejection ratio (PSSR) at higher frequencies, as it acts a low pass filter.

Mostly transistors aspect ratios are also refined by interactive simulations. Transistor M2 aspect ratio is assumed to be 50/1 where the channel length of 1μm is adopted to be approximately 3 times the minimum size of 0.35 TSMC process to reduce the short channel effects.

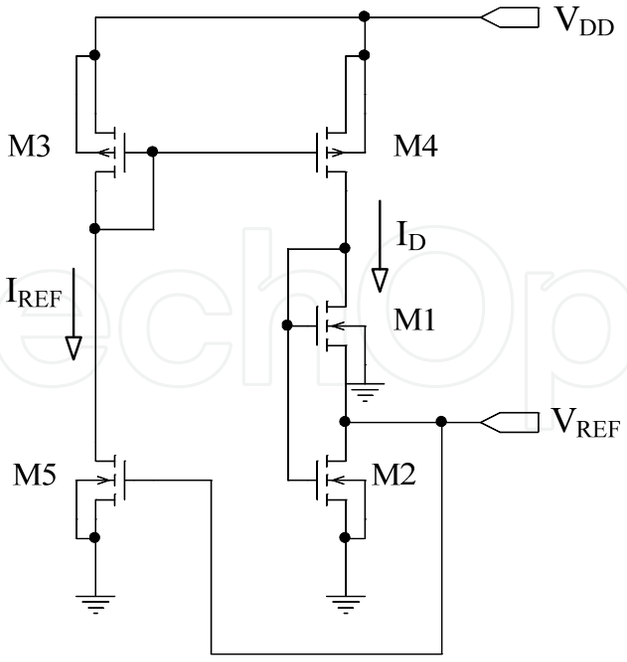

Figure 4. ID current generation by mirroring concept.

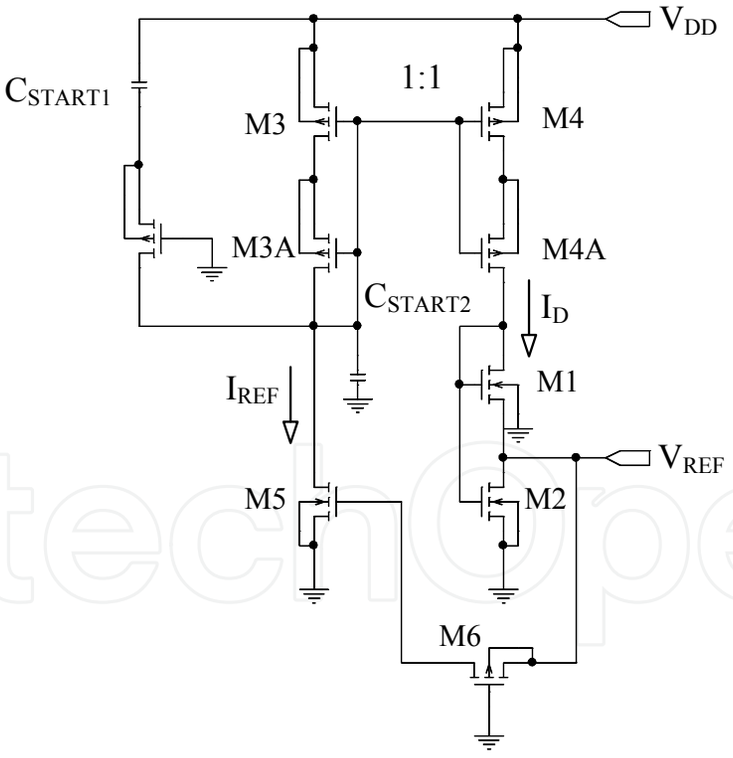

Figure 5. Proposed Reference circuit.

5. Simulation results

This section presents a set of electrical simulations that validate the main concepts of the voltage reference.

5.1. Minimum power supply

As stated early, it is important to keep the whole system operating in the low power condition. Fig. 6 shows the simulation used to investigate the minimum power supply that maintains the circuit proper function. The temperature was kept constant at 37ºC. The three curves are result of typical, slow, and fast PMOS and NMOS parameters of 0.35 TSMC process.

As it can be observed, the supply voltage can be as low as 500mV. Table 2 lists the reference voltage values for some supply voltages and the relative deviation from the nominal (typical) value. The 500mV power supply indicates a worst case deviation of 1.69% at the process corners. This simulation shows an important result since it is in accordance with equation (10), thus indicating an independence of the voltage reference regarding the process corners. Additionally, the use of transistors operating in weak inversion allows power supply voltage reduction to values that characterize low voltage operation.

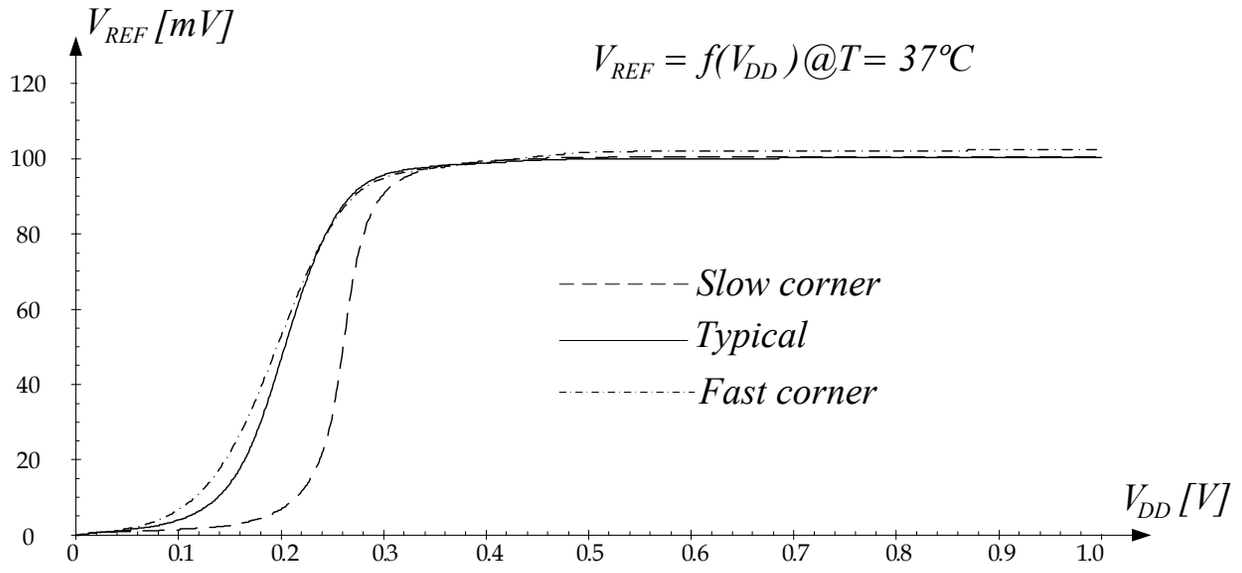

Figure 6. Simulation to Evaluate the Minimum Power Supply Voltage.

	V_{REF} @ T=37ºC (mV)			
V_{DD} [V]	Slow	Typical	Fast	Deviation (worst case)
0.5	100.31	99.99	101.68	+1.69%
0.6	100.38	100.09	102.04	+1.95%
0.7	100.39	100.11	102.10	+1.99%
0.8	100.40	100.13	102.15	+2.01%

Table 2. V_{REF} as a Function of V_{DD} for typical values and process corners.

5.2. Matching between I_{REF} and I_D

The PMOS composite pairs improve the matching between currents I_{REF} and I_D. The simulation results on Fig. 7 show the relative error (ER in %) between currents I_{REF} and I_D for

the typical and corners process. At a 500mV supply voltage, the worst case is approximately 0.155%. The current matching between I_{REF} and I_D is achieved by the PMOS current mirror due to the higher impedance of the composite structure. This output impedance, for both PMOS pairs, can be stated as:

$$r_O(M3A) = ng_m(M3A)r_O(M3A)r_O(M3) \tag{12}$$

Another point of interest is the fact that the matching between the currents is significant (lower dispersion) from 500mV of power supply, confirming the use of this minimum value.

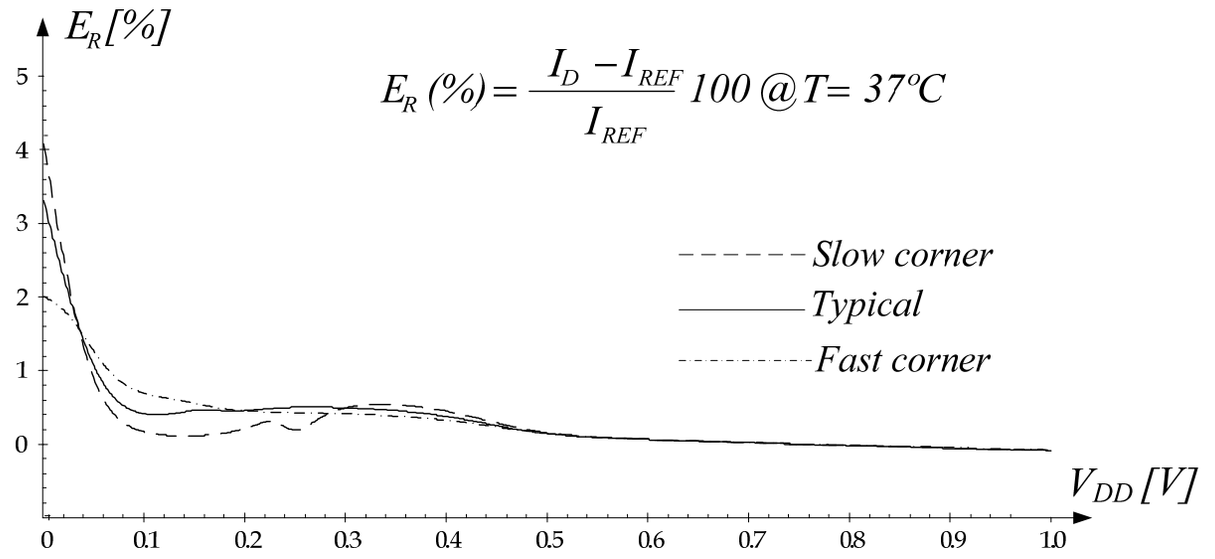

Figure 7. Simulation to Evaluate Mismatch Between I_{REF} and I_D.

5.3. Geometric aspect ratio for transistors M1 and M2

Eq. (10) presents the geometric aspect ratios of transistors M1 and M2, $(W/L)_1$ and $(W/L)_2$, respectively. Therefore, it is possible to evaluate this ideal relationship to achieve the desired target value for the reference voltage. As mentioned previously, it was adopted the minimum channel length L as 1μm to minimize short channel effects.

Consequently it is also necessary to adopt a geometric aspect ratio of transistor M2. The $(W/L)_2$ relationship must be large enough to maintain the I_D current along all the process corners. A simulation of M2 shows that a 50/1 geometric aspect is enough. Therefore, a simulation process is used to investigate the ideal W/L relationship for M1. Fig. 8 shows the simulation of equation (10) considering the V_{REF} as a function of geometric aspect ratios $(W/L)_1$ and $(W/L)_2$. Table 3 resumes the values for the 100mV target value.

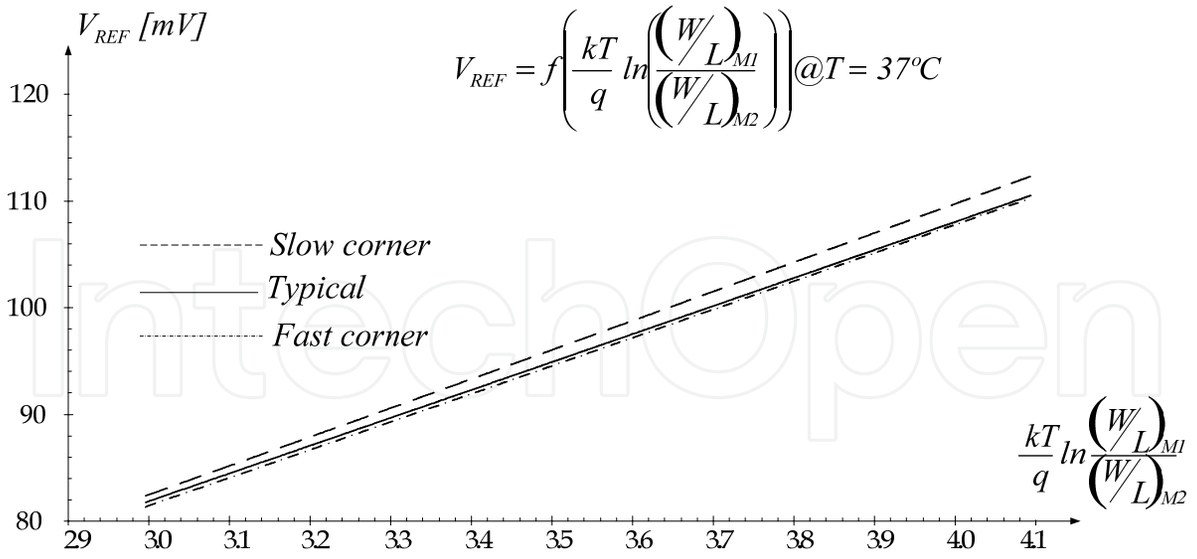

Figure 8. Simulation used to Evaluate the Geometric Aspect Ratio of Transistor M1

V_{REF}=100mV@ T=37ºC and $(W/L)_{M2}$=50/1			
	Slow	Typical	Fast
$\ln\left[\frac{(W/L)_{M1}}{(W/L)_{M2}}\right]$	3.6951	3.7069	3.6448
$(W/L)_{M1}$ [μm]	2012.5	2036.4	1913.7
Equation (10) considering (kT/q)=26.73mV@T=37ºC			
$\ln\left[\frac{(W/L)_{M1}}{(W/L)_{M2}}\right]$ =3.7453 and $(W/L)_{M1}$ =2107 [μm]			

Table 3. Simulated and Calculated Geometric Aspect Ratio for Transistor M1.

It was adopted, in this work, $(W/L)_1$ =2036/1 as the typical value. Although there is a dispersion of about 9% between the calculated and simulated (W/L) values for the worst case corner (fast), the impact on the reference voltage is minimized by the logarithmic dependence.

5.4. Monte Carlo analysis

A set of 5000 runs were performed to evaluate the statistical parameters related to V_{REF}. Figs. 9 and Fig. 10 show the simulation result for the reference voltage V_{REF} and the total power dissipation P_D. Table 4 presents the main values.

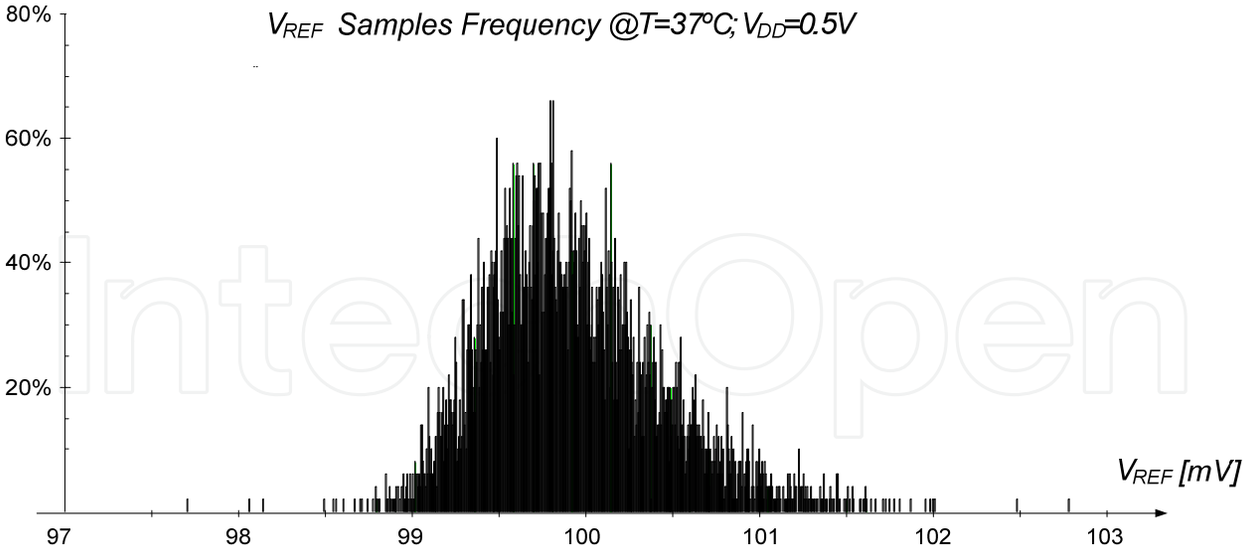

Figure 9. Monte Carlo Analysis – V_{REF} percentage samples.

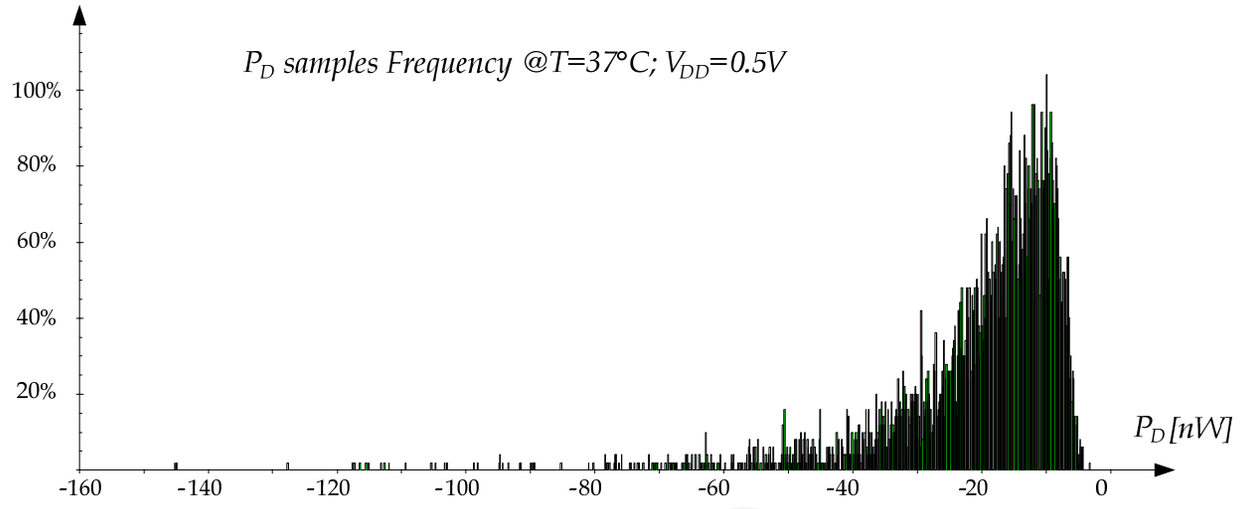

Figure 10. Monte Carlo Analysis – P_D percentage samples.

	V_{REF}[mV]	P_D [nW]
Mean	99.9	16.9
σ	0.503	14.6
3σ	1.512	43.9

Table 4. Monte Carlo Analysis @ V_{DD}=500mV and T=37°C.

Table 4 shows that the V_{REF} can be expressed as 99.9±1.512mV (±1.5%) for a 3σ dispersion. This is an important result considering that the process inherently dispersion on Vt is approximately ±20% (3σ). A total power dissipation in the range of tenths of nW characterizes a low-power operation. The minus signal in the simulation results is due to the simulation algorithm.

5.5. Start-Up circuit

As it is the case of a self-polarized circuit, it is necessary a start-up approach to move the circuit operation to the desired condition. In other words, the start-up circuit must lead the main circuit to the desired operating point. This is realized by introducing the additional components MSTART, CSTART1 and CSTART2. Fig. 11 shows the simulation of MSTART current and CSTART1 voltage as a response to a voltage ramp applied to VDD. As the current vanishes to zero, CSTART1 charges toward VDD and the power dissipated in MSTART tends to zero. The fast and small impulsive current IDS(MSTART) is sufficient to start the whole reference circuit.

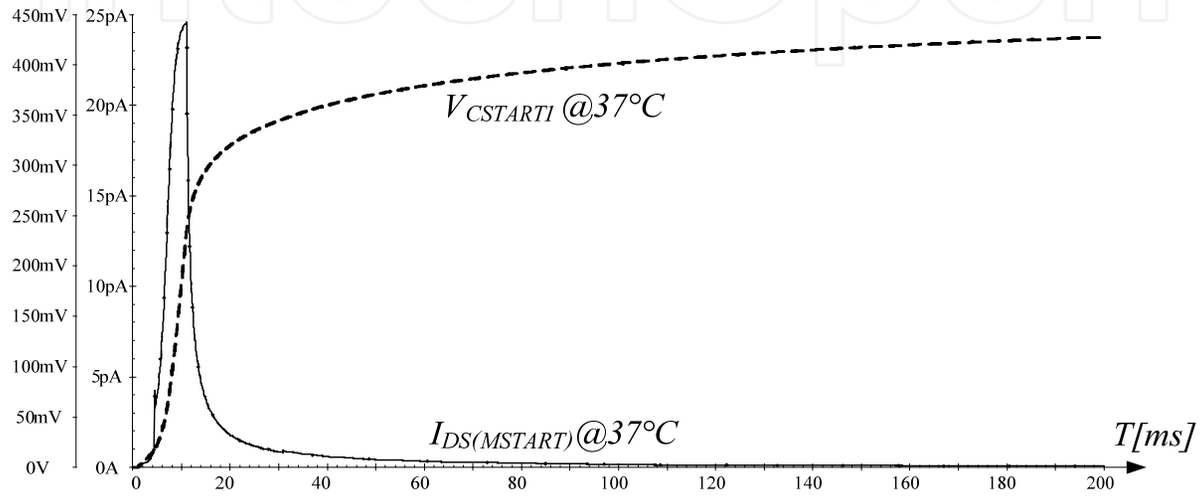

Figure 11. Current though MSTART and CSTART1 voltage.

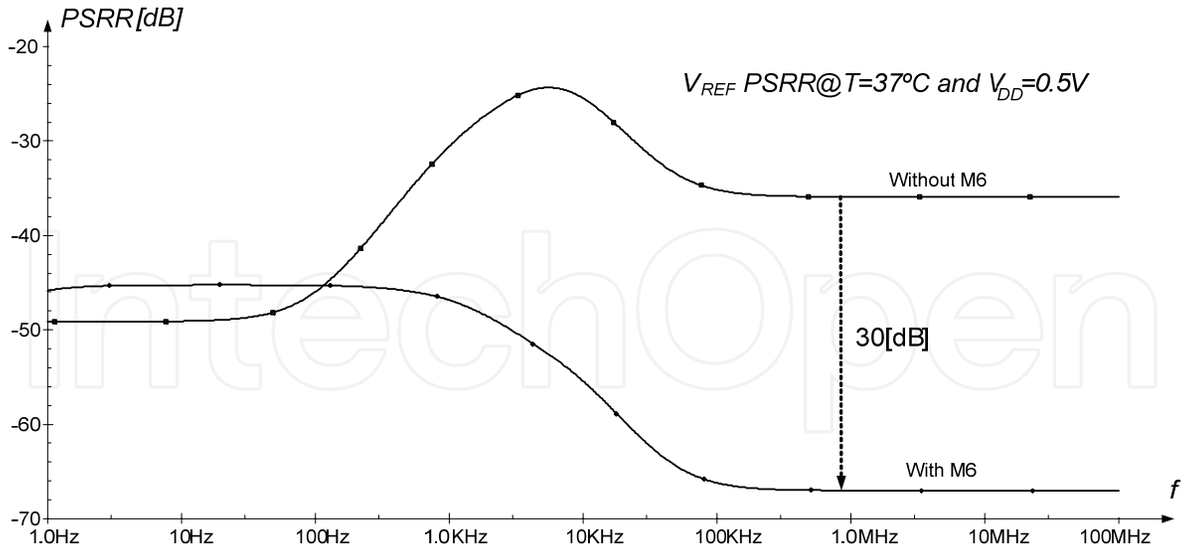

Figure 12. PSRR simulation with and without transistor M6.

5.6. Power Supply Rejection Ratio (PSRR)

The voltage reference must exhibit a high PSRR, especially at high frequencies since the implanted device will be activated by a Radio Frequency link. The PMOS transistor placed

between M2 and M5 acts as a low-pass filter. Fig. 12 shows the PSRR simulation. As it can be observed from the PSRR simulation presented in Fig 12, the PSRR can be 65dB in the MHz frequency range.

6. Layout

The proposed circuit was implemented in standard 0.35μm TSMC CMOS process through MOSIS educational program. Table 5 shows the aspect ratios of the all transistors. In this table the factor M represents a multiplier; i. e. the respective transistor is, actually, a parallel association. For instance, transistor M4A is a parallel association of 3 identical transistors with a geometric aspect ratio of 1000/2.

Transistor	W/L [μm]	M
M1	50/1	1
M2	2036/1	1
M3	150/2	1
M3A	1000/2	3
M4	150/2	1
M4A	1000/2	3
M5	2500/1	5
M6	2500/120	1

Table 5. All Transistors Geometric Aspect Ratio.

The capacitors are poly-insulator-poly – PIP structures and the layouts of the NMOS and PMOS transistors were implemented using multifinger common centroid configuration. Besides better matching, this layout technique is less sensitive to process variation (Hastings, 2001; Qiang et al., 2011). The source-bulk connection of the PMOS transistors is possible since the TSMC is an n-well process, and therefore all the PMOS transistors are fabricated in different wells.

Mainly for the design of analog integrated circuits, the layout of two matched components is realized in such a way that they can be divided into identical sections, placed symmetrically in a matrix array.

The common centroid layout using matched components arranged in a matrix array, in identical and symmetrical sections, is essential to reduce or even eliminate the systematic mismatching. The distances between the centroids components are null and so are the mismatching caused by mechanical and temperature stress. For instance, in order to improve the differential pair match in operational amplifiers, these transistors are placed in a cross coupled array. Fig. 13 (a) shows two matched devices, each composed of two segments arranged in an array of two rows and two columns (cross-coupled pair). Resistors are rarely laid out as cross-coupled pairs because the resulting arrays usually have unwieldy aspect ratios. If the matched devices are large enough to segment into more than two pieces, then the cross-coupled pair can be further subdivided as show Fig. 13 (b).

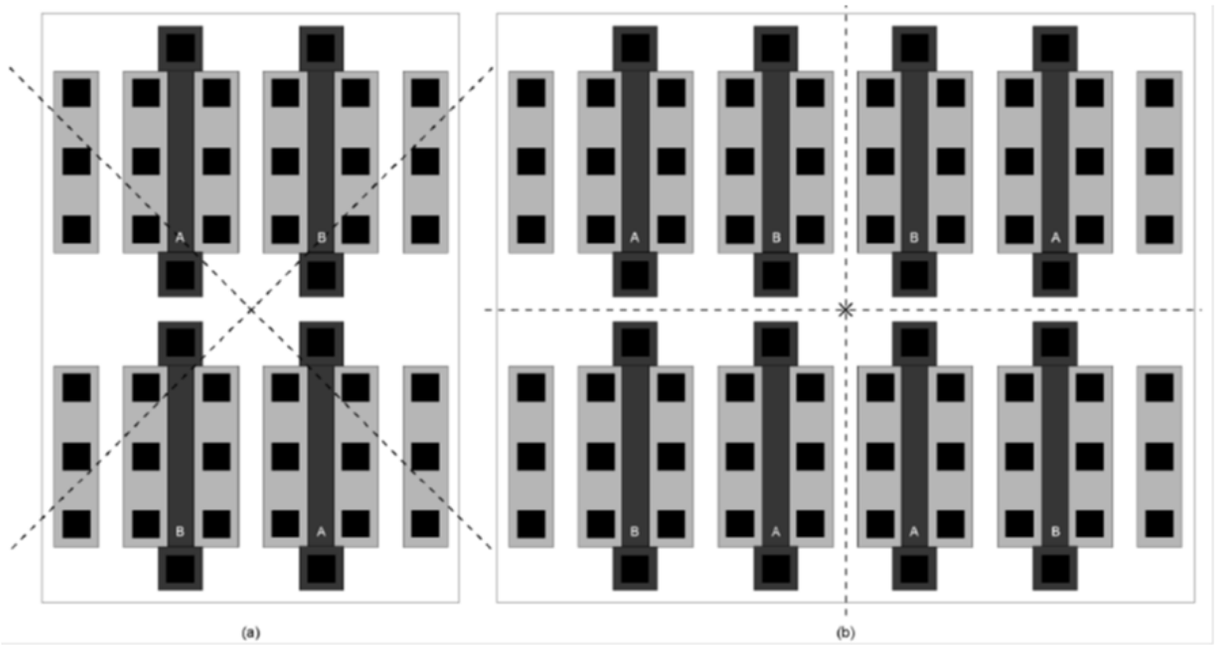

Figure 13. Examples of two dimensional common-centroid arrays.

It is recommended that matched components are fabricated near each other, minimizing the mechanical stress. The mechanical stress difference between two matched components is proportional to the abrasive gradient and their distance. For calculations purposes, the location of the component is determined as the average contribution of each section of the component. The resultant location is called centroid of the component. It is important that any symmetric axis crosses the centroid of the device or component

To design components with a centroid layout some rules must be observed:

1. *Coincidence*: The matched devices centroids must be superimposed or as close as possible;
2. *Symmetry*: The component matrix must be symmetrical along the X and Y axes. Ideally, the symmetry must be a consequence of the placement positions of the components and not for the symmetry of each component individually;
3. *Dispersion*: The matrix must exhibit the greatest dispersion level, i.e., each component must be placed with high symmetry along the matrix;
4. *Compression*: The matrix should be as compact as possible, ideally close to a square shape.

A better matching between integrated components reflects in the overall performance of the designed circuit or system. Depending on the matching accuracy, it is possible to consider the following cases:

1. *Minimum*: In the range of ± 1% (representing 6 to 7 bits of resolution). Used for general components in an analog circuit. For instance, current mirrors and biasing circuits;
2. *Moderate*: In the range of ± 0.1% (representing 9 to 10 bits of resolution). Used in bandgap references, operational amplifiers and input stage of voltage comparators. This range is the most appropriate for analog designs.

3. *Severe*: In the range of ± 0.01% (representing 13 to 14 bits of resolution). Used in high precision analog to digital converters (ADCs) and digital to analog converters (DACs). Analog designs using capacitors relations reach this resolution easier than those that use resistors relations.

In the case of a MOS transistor, the process and electrical parameters that have must be taken into account into matching purposes are listed in Table 6.

Process Parameters	Electrical Parameters
Flat band voltage	Drain current
Mobility	Gate-Source voltage
Substrate Dopant Concentration	Transconductance
Chanel length variation	Output resistance
Chanel width variation	
Short channel effect	
Narrow channel effect	
Gate oxide thickness	
Source/Drain sheet resistance	

Table 6. Process and Electrical Parameters for Component Matching.

7. Conclusions

This chapter presented a low-voltage low-power voltage reference for biomedical applications in which the operating temperature is kept almost constant. Besides a simple topology, the proposed circuit has the advantage of low power dissipation, thus avoiding patient tissue damages. The topology offers a low dependence on process corners and high PSRR. Simulation results point to a reference voltage of 100mV with ±1.5% dispersion (3σ) considering typical and corners parameters. The maximum total dissipated power is about 60.8nW (max) and the PSRR is better than 45dB for a frequency range between 1Hz and 100MHz.

Table 7 shows a comparison of this work with other previously reported in the literature.

	This Work	(Lukaszewicz et.al, 2011)	(Li et al., 2007)
Technology	CMOS 0.35µm	CMOS 65nm	CMOS 0.5µm
V_{DD} [V]	0.5	2.6 – 3.63	4 - 6
I_D [µA]	0.12	47	-
V_{REF} [mV]	100	-	-
I_{REF} [µA]	-	6.45	1.612
Area [mm²]	0.43	-	0.026
PSRR [dB]	65@10MHz	103@10MHz	45
Process Sensitivity [%]	±1.5	±3	±5.2

Table 7. Comparison with previous work.

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