Chapter 12

Silicon Carbide Power MESFET

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Additional information is available at the end of the chapter

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1. Introduction

The wide band gap materials, such as silicon carbide (SiC) [1-3] and gallium nitride (GaN) [4-6], are the third generation semiconductor materials, which had been developed after the Silicon (Si) and gallium arsenide (GaAs) materials. Especially, the SiC material is very well-suited for the high voltage, high power and high temperature applications due to its superior material properties. Silicon carbide has been known investigated since 1907 after Captain H. J. Round demonstrated yellow and blue emission by application bias between a metal needle and SiC crystal. The potential of using SiC in semiconductor electronics was already recognized about a half of century ago. The most remarkable SiC properties include the wide band gap, very large avalanche breakdown field, high thermal conductivity, high maximum operating temperature and chemical inertness and radiation hardness.

Therefore the microwave power devices based on 4H-SiC have received increasing attention. The MESFETs (Metal Semiconductor Field Effect Transistor) is a hot research topic [7-10].

For the SiC power MESFETs, the breakdown voltage is a very important parameter that allows the power devices to achieve a specific power density and power conversion. Prior research has proposed many techniques to improve the breakdown voltage [11-15]. The conventional termination techniques include of the Field Plate structure in the source or drain electrode [16], RESURF (Reduced Surface field) technology [17], floating metal rings [18-19], p-epi guard rings [20], etc [21-23]. In order to optimize the surface electric field and improve the breakdown voltage, the new technologies had been proposed, which includes of the REBULF (REduced BULk Field) [24] and complete 3D RESURF [15]. For the new power devices based on the silicon materials, the trade-off relationship had been broken between the breakdown voltage and specific on resistance by the complete 3D RESURF [15]. The high breakdown voltage had been obtained on the ultra thin epitaxial layer with the REBULF technology [24]. It can be sure that these new technologies can be transplanted directly to the SiC power MESFETs. So, sever-

al new SiC power MESFETs had been designed to optimize the characteristic of the breakdown voltage, specific on resistance, frequency and transconductance.

2. Operation principle for the 4H-SiC Power MESFETs

For the *n*-channel MESFETs, which including normally-on (depletion mode) and normally-off (enhancement mode) devices, as are shown in Fig.1, an *n*-type channel connects the drain and source regions with the n^+ type doping. The depletion layer under the metal-semiconductor contact determines the current flow across the channel between the source and drain electrodes. The thickness of the channel conductivity is modulated by the gate bias-dependent depletion region.

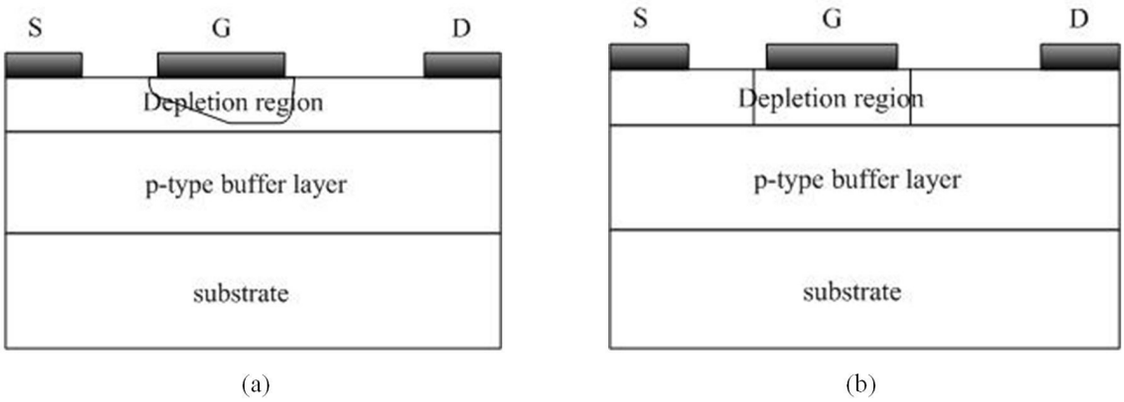

Figure 1. Normally-on (a) and normally-off (b) MESFETs at zero gate bias.

The channel of normally-off MESFETs is totally depleted by the gate build-in potential even at zero gate bias, and its threshold voltage is positive. In contrast, the normally-on MESFETs have a finite cross-section of conducting channel at zero gate bias and the negative threshold voltage.

The basic operation principle will be discussed in this section for the 4H-SiC power MESFETs.

For the normally-on MESFETs, usually, the source is grounded, and the gate and drain are biased negatively and positively, respectively. A schematic diagram of the depletion region under the gate of MESFETs for a finite drain-to-source voltage is shown in Fig. 2. On this condition, the electrons will flow from the source to the drain and a current flow (I_{ds}) occurs in the channel. When the negative gate bias is changed, or an altering-current (AC) voltage signal is superposed on the direct- current (DC) gate bias, the thickness of the depletion layer or the width of the conducting channel, which determining the resistance of the channel, will be modulated, and thus the current flow in the channel is regulated. So, the MESFETs is actually a voltage-controlled electric device by the means that the gate bias modulates the conducting channel resistance, and thus controls the current flow in the channel.

For the *p*-channel normally-on MESFETs, the gate is biased positively, so as to ensure that the gate is reverse biased. Note that it is the electrons for the *n*-channel MESFETs, but the

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holes for the *p*-channel MESFETs that transport as the carriers in the channel. However, whether in the *n*-channel or *p*-channel MESFETs, the unique majority carriers undertake transporting the current. So, the MESFETs is an unipolar device.

3. New 4H-SiC Power MESFETs

In this section several new structures for the 4H-SiC power MESFETs are provided in which the surface electric field and breakdown characteristics are optimized.

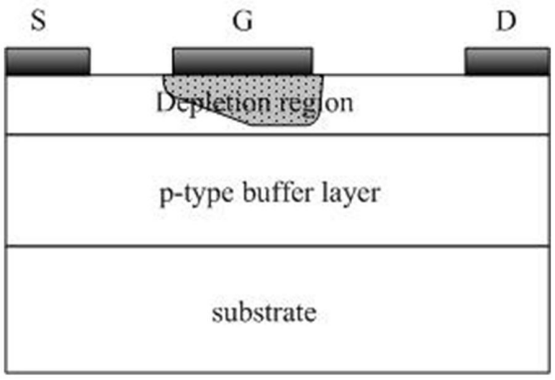

Figure 2. Depletion region in MESFETs with positive drain bias.

3.1. Field-Plated 4H-SiC MESFETs structure

Fig. 3 is the schematic diagram of the 4H-SiC MESFETs with the field-plate [25], which is the same as the channel-recessed device except the Si_3N_4 layer on top of the surface. The gate length (L_g) is 0.5 μm, and the space of gate-source (L_{gs}) and gate-drain (L_{gd}) are 0.5 μm and 1.0 μm, respectively. The thickness of Si_3N_4 is 100 nm.

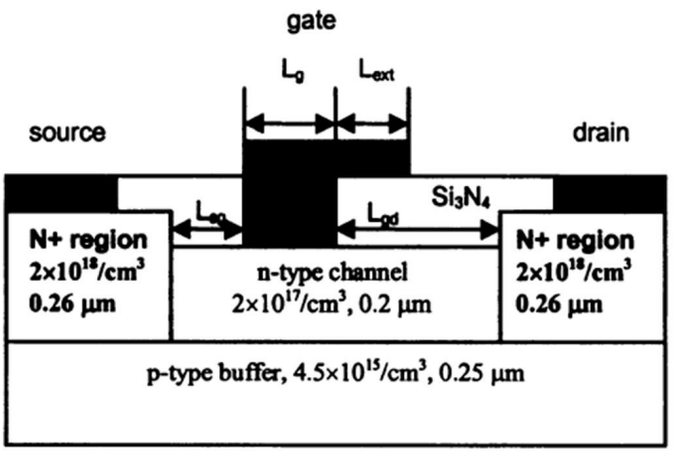

Figure 3. Field-plate SiC MESFETS structure.

Fig.4 shows that the breakdown voltage is dependent on the extension length of the field-plate toward the drain side L_{ext} and show a peak at L_{ext}=0.35 μm. The breakdown voltage of 240-250V is obtained at L_{ext}=0.35 μm, which is 100 V higher than that of the conventional structure without the field-plate. This is because that the gate leakage current is decreased due to the surface field peak significantly lowered at the gate corner while raised at the drain corner, as is shown in Fig.5.

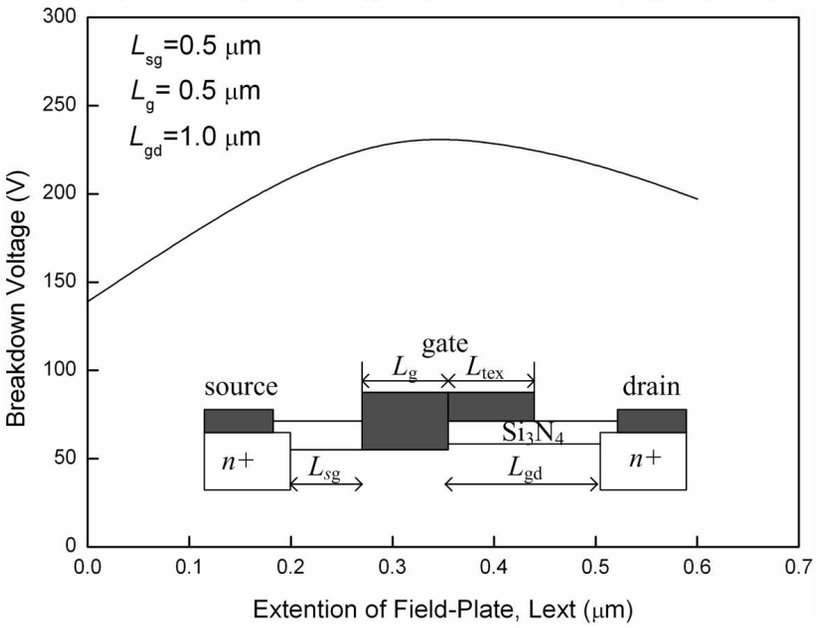

Figure 4. Breakdown voltage versus the extension length of the field-plate toward the drain side L_{ext}.

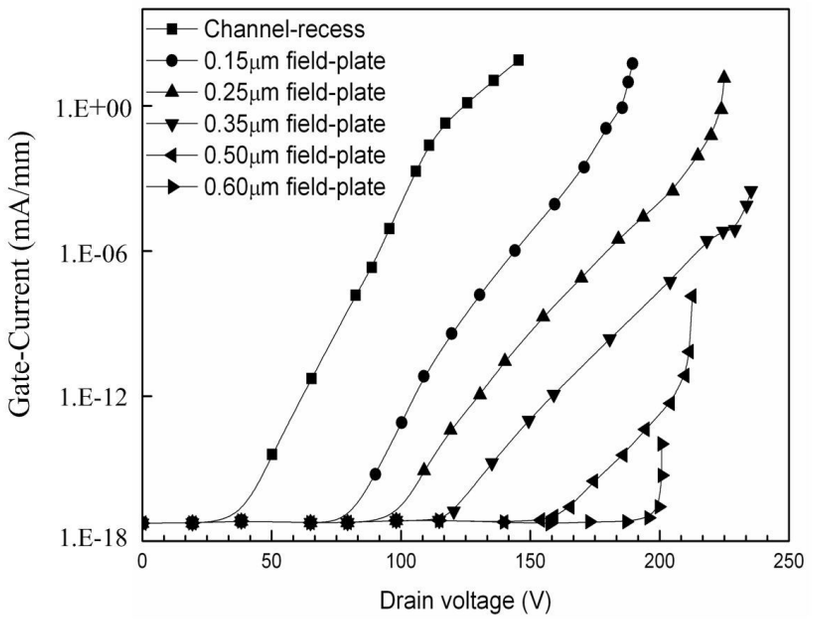

Figure 5. Behavior of the gate leakage current versus the drain voltage as a function of L_{ext}.

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3.2. Double-recessed 4H-SiC MESFETs structure with recessed source/drain drift region

Fig. 6 shows the schematic cross-section of the 4H-SiC MESFETs [26]. Fig. 6a and 6b show the improved DR and conventional DR structures, respectively. Compared with the conventional DR structure, additional source/drain drift region recess will be formed for the improved DR structure.

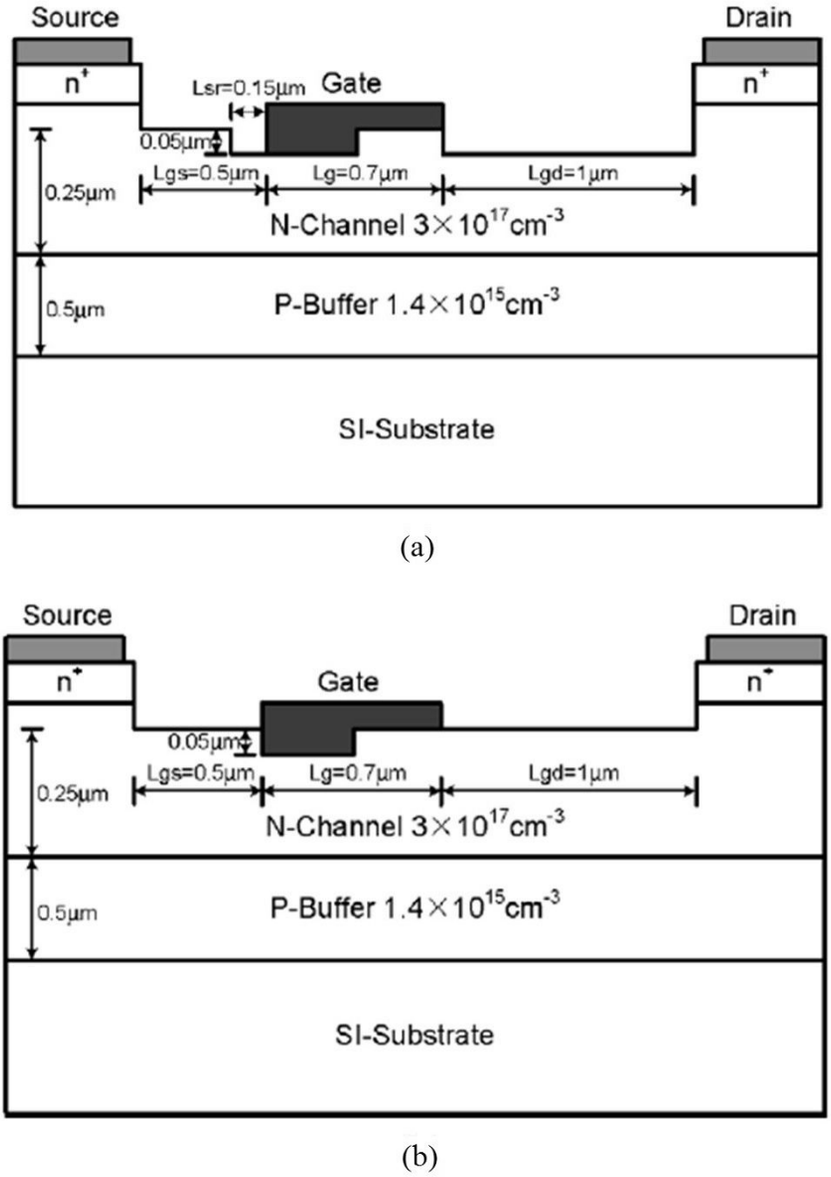

Figure 6. Schematic cross-section of the 4H-SiC MESFETs structures (a) Improved DR structure (b) double-recessed (DR) structure.

It can be seen from Fig.7 that the breakdown voltage (V_b) of the improved DR structure is increased compared to that of the conventional DR structure. A further investigation shows that the breakdown happened at gate corner near drain electrode due to the electric field

crowding at that corner for these two structures. Actually, the maximum electrical field at gate corner near drain of the improved DR structure is reduced, compared with that of the conventional DR structure. Therefore, it clearly shows that the increase of breakdown voltage is attributed to reduced electric field crowding at gate corner near the drain due to thin channel thickness between the gate and drain electrodes with recessed drain drift region.

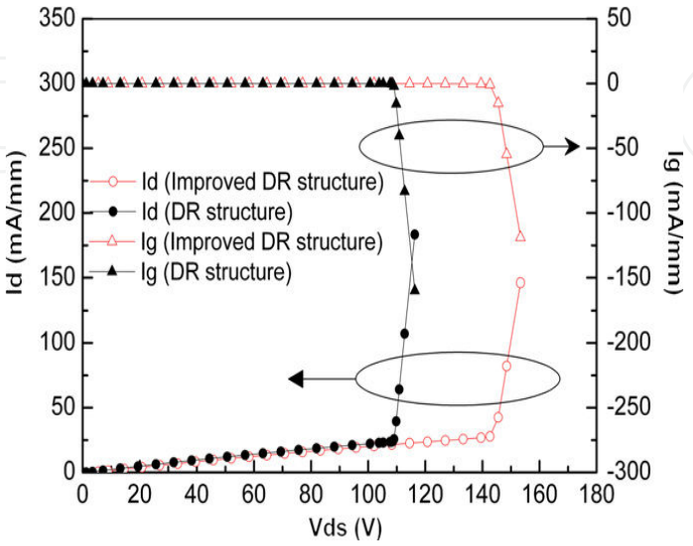

Figure 7. Simulated three-terminal breakdown characteristics.

3.3. Buffer-Gate 4H-SiC MESFETs structure

Fig. 8 is the schematic diagram of the structure of the Buffer-Gate SiC MESFETs structure [27]. Compared with the conventional 4H-SiC MESFETs, a low doped gate-buffer layer is introduced between the gate and channel layer.

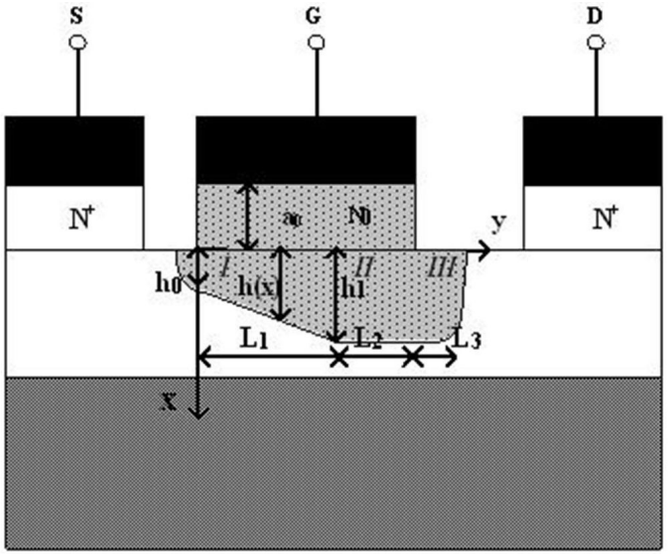

Figure 8. The schematic diagram of the buffer-gate structure.

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In Buffer-Gate 4H-SiC MESFETs, the gate length and width are 0.7 μm and 332 μm. Meanwhile, the thickness and doping concentration are 0.26 μm and 1.7×10^{17} cm^{-3} for the channel layer, and 0.2 μm and 1×10^{14} cm^{-3} for the gate-buffer layer between the gate and channel.

Fig. 9 shows the dependence of the current in the channel on the gate-buffer layer. It reveals that the thicker the gate-buffer layer is, the larger the drain current is. This is because the channel width is increased owing to the decrease of the thickness of the depletion layer in the channel when the gate-buffer layer doping concentration and thickness are increased. It is also shown in Fig. 9 that when the gate-buffer layer is increased sufficiently, the drain current increases slowly because the thickness of the depleted layer in the channel layer decreases, and thus the width of the conduction channel increases more and more slowly with increasing the thickness of the gate-buffer layer.

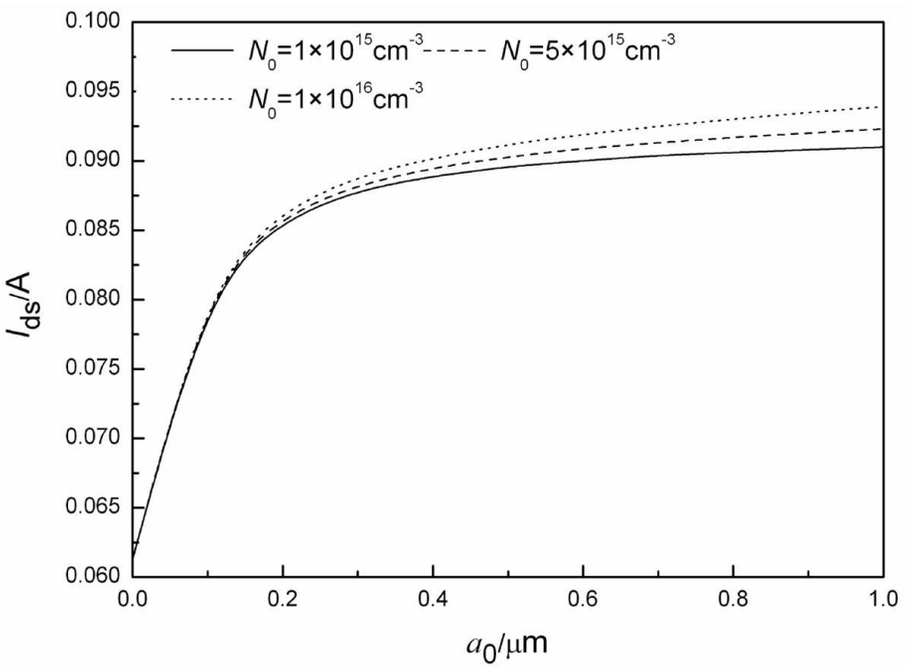

Figure 9. The dependence of the drain current on the gate-buffer layer for N_0=1×10^{15}cm^{-3}(solid line), N_0=5×10^{15}cm^{-3}(dash line) and N_0=1×10^{16}cm^{-3}(dot line). V_{gs}=0 V, V_{ds}=5 V.

Fig.10(a). is the breakdown characteristics for the two structures. It can be seen that the breakdown voltage (V_b) is significantly increased, compared with that of the conventional structure. In fact, the breakdown happens at the gate corner near to the drain side due to the electric field crowding here for both two structures. However, the electric field peak is significantly lowered at the gate corner, i.e., the surface electric field is more uniform, owing to the inserted lower doped gate-buffer layer when compared with that of the conventional 4H-SiC MESFETs. Fig.10 (b) plots the corresponding electric field distribution. The reason for the suppression of the electric field at the gate corner is similar to that for the weakened surface electric field caused by lightly doped drain (LDD) in the MOSFETs [28].

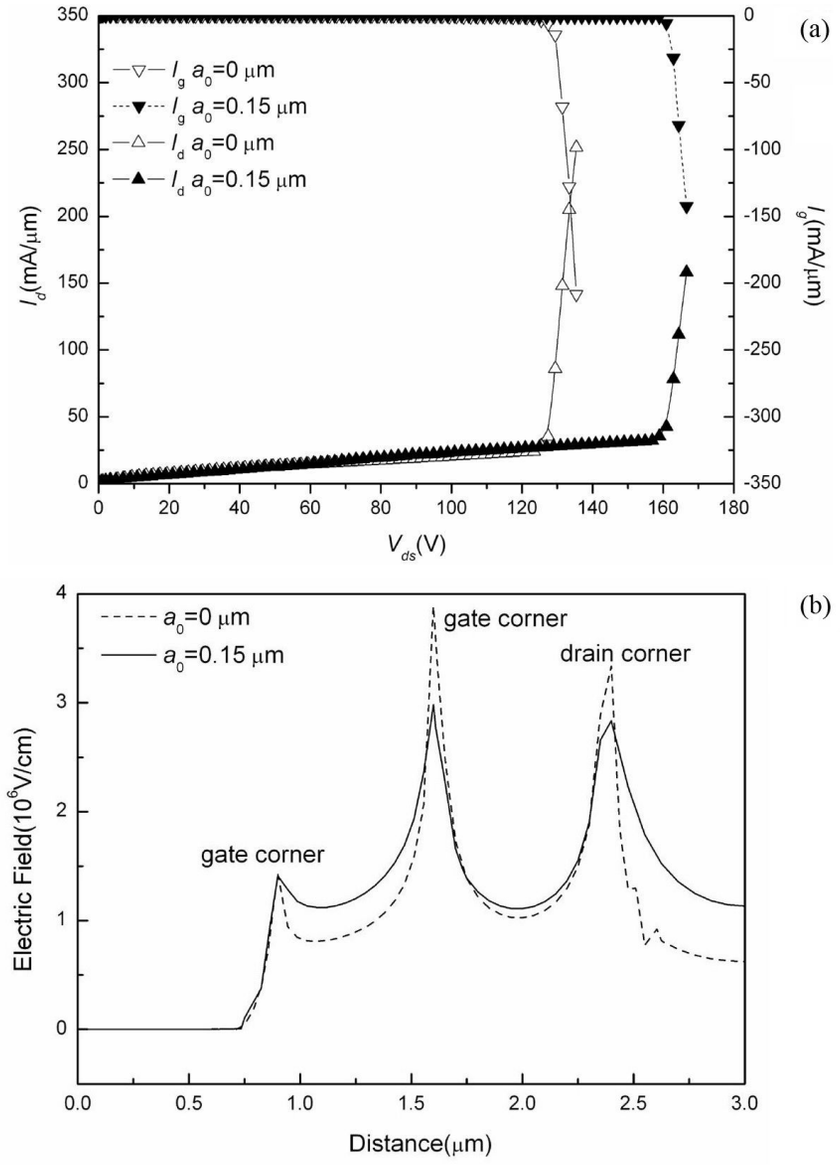

Figure 10. (a) The simulated breakdown characteristics for a_0=0 μm (open) and a_0=0.15 μm (filled), (b) The distribution of the surface electric field for a_0=0 μm (dash) and a_0=0.15 μm (solid).

3.4. Gate-drain surface epitaxial layer MESFETs structure (GDSE)

The schematic diagram of the GDSE structure is shown in Fig.11 [29]. Compared with the conventional 4H-SiC MESFETs, a low doped p-type surface epitaxial layer is introduced between the gate and drain when its doping concentration is lower than that of the channel layer by two orders. Firstly, there appears a build-in potential in the p-n junction between the p-type epitaxial layer and n-type channel layer or n^+ cap layer, which reduces the electric field peak at the gate corner. Thus it improves the electric field distribution. Secondly, the most part of the depletion layer in the p-n junction lies in the p-type epitaxial layer due to its doping concentration much lower than that of the n-type channel layer. Therefore, the gate-drain p-type epitaxial layer has little bad effect on the current density.

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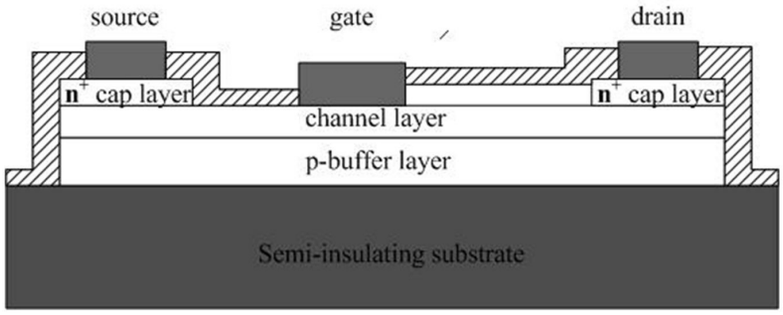

Figure 11. The schematic diagram of the MESFETs with gate-drain surface epi-layer.

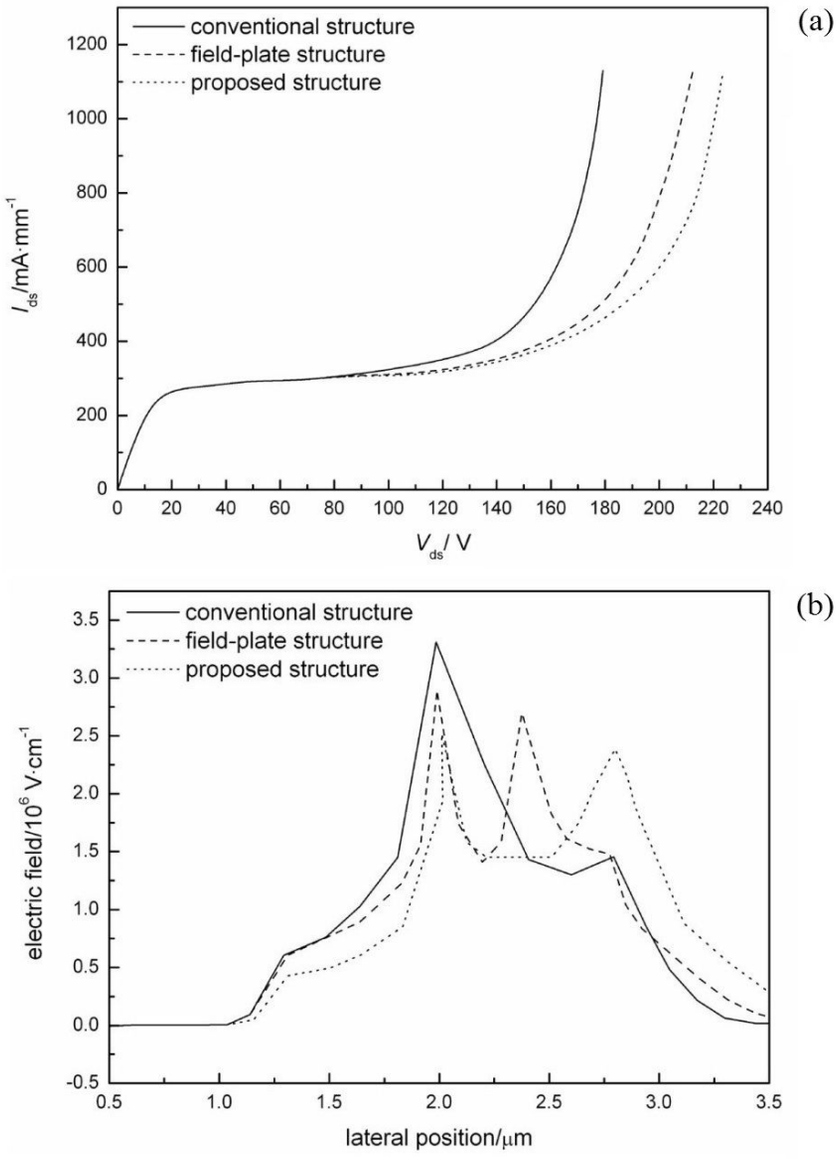

Figure 12. Comparison of the surface electric field (a) and the breakdown voltage (b) for the conventional, Field-plated, and the GDSE structure.

The breakdown characteristics and surface electric field distribution are shown in Fig.11. Fig.12 (a) shows that the breakdown voltage of the GDSE structure is the largest one for the three structures. The reason for the breakdown increased is that the electric field peak is significantly lowered at the gate corner, i.e., the surface electric field is more uniform, owing to the inserted lower doped p-type epitaxial layer when compared with that of the other two SiC MESFETs, as is shown in Fig.12 (b).

4. New 4H-SiC Power MESFETs Modeling

In most cases, the constant mobility is adopted for simplicity to develop the analytical models of the MESFETs which describes device operation. However, the constant mobility approximation is not adequate to describe the electron transport in the low field region and leads to an inaccurate estimation of the drain current and device characteristics of the 4H-SiC MESFETs. In this section, the improved analytical model for the conventional 4H-SiC MESFETs is provided which adopts the field-dependent mobility of the electrons, and takes into account the ungated high field region between the gate and drain which is usually omitted [30].

For the 4H-SiC material, the dependence of the mobility of the electron on the electric field can be described by Caughey–Thomas model [31].

$$\mu(E)=\frac{\mu_0}{\left[1+\left(\frac{\mu_0 E}{\upsilon_s}\right)^{\beta}\right]^{1/\beta}} \tag{1}$$

where μ_0 is the low field mobility, υ_s the saturation velocity, E the electric field strength and β a curvature parameter of the order of 1 describing the saturation tendency. For SiC material, the measured value of β is 1.2 in the experiment [32]. For simplicity, β=1 is a reasonably good approximation [33].

Fig. 13 is the schematic diagram of the 4H-SiC MESFETs. The depletion layer thickness $h(x)$ under the gate, x away from the source is obtained by solving the one dimensional (1-D) Poisson's equation.

$$h(x)=\left(\frac{2\varepsilon\left[V(x)+V_G+V_{bi}\right]}{qN_D}\right)^{\frac{1}{2}} \tag{2}$$

where N_D is the uniformly doping concentration of the channel layer, and ε the dielectric constant. $V(x)$ is the potential difference between the source and the point x away from the source, V_G the gate bias, and V_{bi} the build-in voltage.

When the drain voltage is low, the electric field in the channel is less than the saturation field E_s, and only region ◎ exists. Based on integrating over the channel length L, the channel current is obtained

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$$I_C(V_G, V_D) = I_P \frac{[3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3)]}{1 + Z(u_d^2 - u_0^2)} \tag{3}$$

where u_0 (u_d) is the depletion layer width h_0 (h_d) at the source (drain) end of the channel normalized to the epi-layer channel layer thickness a. I_P, Z and V_P are constants expressed by

$$I_p = \frac{q^2 N_D^2 a^3 \mu_0 W}{6\varepsilon L}, \; V_p = \frac{qN_D a^2}{2\varepsilon}, \; Z = \frac{qN_D a^2 \mu_0}{2\varepsilon L \, v_s} \tag{4}$$

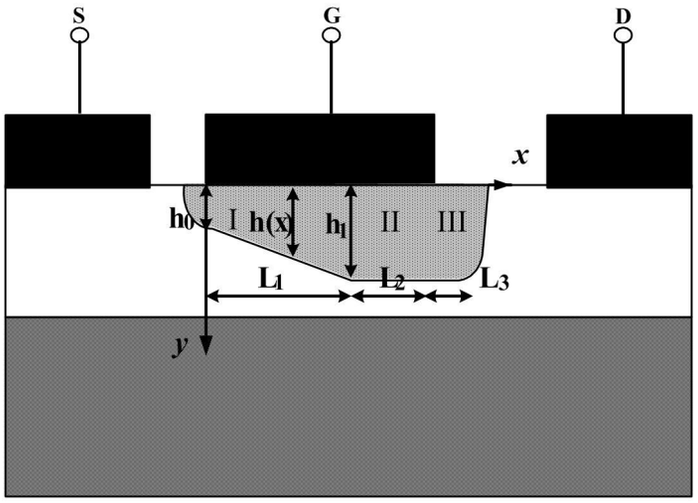

Figure 13. The schematic diagram of the 4H-SiC MESFETs.

With the drain bias increasing gradually, the lateral electric field increases and the electron velocity rises toward its saturation value. At enough high drain bias, the channel is in saturation regime, and can be divided into three regions which are shown in Fig. 13. In region ◎ with its length of L_1 and nearer to the source under the gate, the electric field is low and the electron velocity is less than the saturation velocity (v_s). The saturation region below the gate and the saturation region between the gate and the drain are labeled as regions ◎ and ◎, respectively. The saturation channel current is

$$I_{csat} = qN_D W a \gamma v_s (1 - u_1) \tag{5}$$

where u_1 is the normalized depletion layer thickness at the point where the electron reaches the saturation velocity, γ=0.99.

$$u_1(V_G, V_D) = \frac{h_1}{a} = \frac{1}{a}\sqrt{\frac{\varepsilon}{qN_D}[V(L_1) + V_G + V_{bi}]} = \sqrt{\frac{[V(L_1) + V_G + V_{bi}]}{V_P}} \tag{6}$$

where h_1 is the depletion layer thickness at the point where the electron reaches the saturation velocity, $V(L_1)$ is the potential difference between the source and the point at $x=L_1$, where the saturation velocity $v(L_1)=\gamma v_s$.

To obtain the saturation current in the channel, there requires other equations involving u_1 or L_1, which can be obtained by solving 2-D Poisson's equation.

The potential drop across regions◎and ◎ achieved by solving the 2-D Poisson's equation is

$$V(L_1+L_3)-V(L_1)=\left(\frac{2au_1}{\pi}+\frac{L_3}{3}\right)E_s\sinh\left(\frac{\pi L_2}{2au_1}\right)\exp\left(\frac{-\pi L_3}{2au_1}\right)+\frac{E_s L_3}{3}\left(2\exp\left(\frac{\pi L_2}{2au_1}\right)+1\right) \tag{7}$$

The equation involving L_3 is

$$L_3^2\left[\frac{qN_D au_1}{\varepsilon}-E_s\exp\left(\frac{\pi L_2}{2au_1}\right)+E_s\sinh\left(\frac{\pi L_2}{2au_1}\right)\right]=(au1)^2E_s\left[\exp\left(\frac{\pi L_2}{2au_1}\right)-1-\sinh\left(\frac{\pi L_2}{2au_1}\right)\exp\left(\frac{-\pi L_3}{2au_1}\right)\right] \tag{8}$$

where
$V(L_1+L_3)=V_D-I_C R_D$.

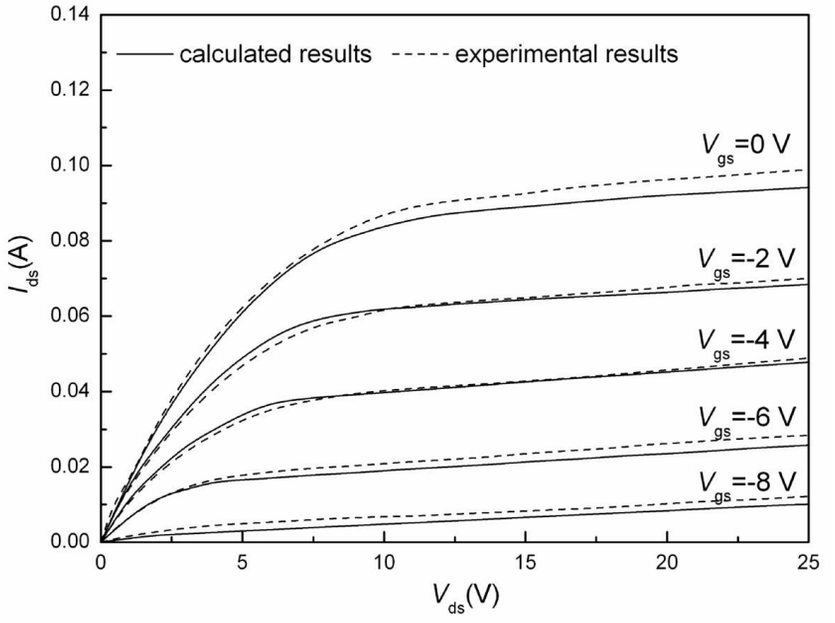

Figure 14. Calculated and experimental *I-V* characteristics, at V_{gs}=0,-2,-4,-6,-8 V.

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From the analysis above, the drain current can be achieved when the structure parameters (L, W, a, a_0, N_D, N_0) and bias voltage (V_D, V_G) are given.

Using the obtained model, the *I-V* characteristics are calculated, as is shown in Fig.14. It can be seen that the *I–V* characteristics calculated using the obtained model are in agreement with the experimental data, which verifies the validity of the model.

Adopting the same approach, Yang et al developed analytical models for the new Buffer-Gate MESFETs [27]. The analytical models describing the direct-current (DC) and alternating current (AC) characteristics are as follows:

Under low drain voltage, the channel current is

$$I_C(V_G, V_D) = I_P \frac{[3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3)] - 3a_0/a \cdot [(u_d^2 - u_0^2) - 2(u_d - u_0)]}{1 + Z(u_d^2 - u_0^2) + Z \cdot 2a_0/a \cdot (u_d - u_0)} \tag{9}$$

At high drain bias, the channel is in saturation mode, the saturation channel current is I_{csat}.

$$I_{csat} = qN_D Wa\gamma v_s(1 - u_1) \tag{10}$$

where u_1 is the depletion layer thickness normalized to the epilayer channel layer thickness a at the point where the electron reaches the saturation velocity and given by equation (11)

$$u_1(V_G, V_D) = \frac{h_1}{a} = \sqrt{(1 - \frac{N_0}{N_D})\frac{a_0^2}{a^2} + \frac{(V(L_1) + V_G + V_{bi})}{V_p}} - \frac{a_0}{a} \tag{11}$$

where h_1 is the depletion layer thickness at the point where the electron reaches the saturation velocity, $V(L_1)$ is the potential difference between the source and the point at $x=L_1$, where the saturation velocity $v(L_1)=\gamma v_s$.

To evaluate the high frequency performance conveniently, it is important to describe the small signal parameters analytically.

From Eq.(9), the device's drain conductance for the linear region can be derived which is given in equation (12)

$$g_{dl} = \frac{3I_P \cdot (u_d + a_0/a)}{m_d V_P} \cdot \frac{\left[(1 - u_d) - Z(u_d - a_0/a)(u_d^2 - u_0^2) + 2/3 \cdot Z(u_d^3 - u_0^3) - 2Z \cdot a_0/a \cdot u_d \cdot (u_d - u_0)\right]}{\left[1 + Z(u_d^2 - u_0^2) + 2Z \cdot a_0/a \cdot (u_d - u_0)\right]^2} \tag{12}$$

where

$m_d = u_d + a_0/a$.

Similarly, the transconductance for the linear region is equation (13)

$$g_{ml}=\frac{3I_P\cdot(u_d+a_0/a)}{m_dV_P}\cdot\frac{\left[(1-u_d)-Z(u_d-a_0/a)(u_d^{\,2}-u_0^{\,2})+2/3\cdot Z(u_d^{\,3}-u_0^{\,3})-2Z\cdot a_0/a\cdot u_d\cdot(u_d-u_0)\right]}{\left[1+Z(u_d^{\,2}-u_0^{\,2})+2Z\cdot a_0/a\cdot(u_d-u_0)\right]^2}$$
$$-\frac{3I_P\cdot(u_0+a_0/a)}{m_0V_P}\cdot\frac{\left[(1-u_0)-Z(u_0-a_0/a)(u_d^{\,2}-u_0^{\,2})+2/3\cdot Z(u_d^{\,3}-u_0^{\,3})-2Z\cdot a_0/a\cdot u_0\cdot(u_d-u_0)\right]}{\left[1+Z(u_d^{\,2}-u_0^{\,2})+2Z\cdot a_0/a\cdot(u_d-u_0)\right]^2} \tag{13}$$

where

$m_0=u_0+a_0/a.$

From Eq.(10), the drain conductance for the saturation region is obtained expressed by Eq.(14)

$$g_{ds}=-\frac{3\gamma I_P}{2Zm_{L_1}V_P}f \tag{14}$$

where

$$f^{-1}=1+\frac{1}{2m_{L_1}V_P}\left[\frac{2E_Sa}{\pi}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)}-\frac{E_Sa(L-L_1)}{(au_1+a_0)}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)}\right]-$$
$$\frac{E_SLZ}{2m_{L_1}V_P}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)}\times m_{L_1}=u_1+a_0/a.$$
$$\left\{\left[\frac{2u_1(1-\gamma)}{\gamma}+\frac{(u_1^{\,2}-u_0^{\,2})-2/3(u_1^{\,3}-u_0^{\,3})}{\gamma(1-u_1)^2}\right]-\frac{a_0}{\gamma a}\left[\frac{(u_1^{\,2}-u_0^{\,2})-(u_1-u_0)}{(1-u_1)^2}-2(1-\gamma)\right]\right\}$$

The expression of transconductance for the saturation region is equation (15)

$$g_{ms}=-\frac{3\gamma I_P}{2Zm_{L_1}V_P}(k+1) \tag{15}$$

where

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$$h = -\frac{1}{2m_{L_1}V_P}\left[\frac{2E_S a}{\pi}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)} - \frac{E_S a(L-L_1)}{(au_1+a_0)}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)}\right] + \frac{E_S LZ}{2m_{L_1}V_P}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} \times \left\{\left[\frac{2u_1(1-\gamma)}{\lambda} + \frac{(u_1^2-u_0^2)-2/3(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right] - \frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\right\} \cdot - \frac{u_0 E_S LZ}{m_0 V_P}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)}\left[\frac{1-u_0}{\gamma(1-u_1)} - 1\right]\left(1+\frac{a_0}{au_0}\right)$$

To find the gate-source capacitance, the magnitude of the charge in the depletion layer under the gate is needed. It can be derived from the potential distribution in the depletion layer which is obtained by solving the 2-D Poisson's equation.

The expression of the gate-source capacitance is equation (16)

$$C_{gs} = C_{gs1} + C_{gs2} + C_{gs3} \tag{16}$$

where

$$C_{gs1} = \frac{4\varepsilon WL\ V_P I_P}{aID}\left\{\begin{array}{l}\frac{-g_m}{I_D}\left[(1-\frac{a_0}{a})(u_1^3-u_0^3) - \frac{3}{4}(u_1^4-u_0^4) + \frac{3a_0}{a}(u_1^2-u_0^2)\right] \\ + \frac{3u_1}{2m_{L_1}V_P}(u_1+\frac{a_0}{a})(1-u_1-\frac{ZI_D}{3I_P})(k+1) - \frac{3u_0}{2m_0 V_P}(u_0+\frac{a_0}{a})(1-u_0-\frac{ZI_D}{3I_P})\end{array}\right\}$$

$$C_{gs2} = \frac{2\varepsilon WLZu_1}{a}\left\{\frac{g}{2Zm_{L_1}u_1}(k+1) + \frac{u_0}{m_0}\left[\frac{u_1-u_0}{\gamma(1-u_1)} + \frac{1-\gamma}{\gamma}\right]\left(1+\frac{a_0}{au_0}\right)\right\}$$

$$C_{gs3} = -\varepsilon E_S Wa\left\{\begin{array}{l}\frac{k+1}{2m_{L_1}V_P}\left\{\begin{array}{l}1-\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} - \frac{\pi(1-u_1)}{2(au_1+a_0)}\sinh \\ \frac{\pi(L-L_1)}{2(au_1+a_0)}\left[\frac{a(L-L_1)}{au_1+a_0} - \frac{L\cdot g - L + L_1}{u_1}\right]\end{array}\right\} \\ + \frac{\pi u_0 LZ(1-u_1)}{2m_0 V_P(au_1+a_0)}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)}\left(\frac{1-u_0}{\gamma(1-u_1)} - 1\right)\left(1+\frac{a_0}{au_0}\right)\end{array}\right\}$$

$$g = 1 - \frac{L_1}{L} - Zu_1\left\{\begin{array}{l}\left[\frac{2u_1(1-\gamma)}{\gamma} + \frac{(u_1^2-u_0^2)-2/3(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right] - \\ \frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\end{array}\right\} \cdot$$

Using their model, Yang et al calculate the *I-V* characteristics and DC small signal characteristics of the proposed 4H-SiC MESFETs with a gate-buffer layer of 0.2 μm. The results are shown in Fig.15 to Fig.18.

Fig.15 shows the *I-V* characteristics of the proposed 4H-SiC MESFETs. For a specified gate bias, the drain currents achieved in their proposed device are larger than that in the conventional one. For instance, the maximum saturation drain current is 0.18 A, which is larger than 0.1 A in the conventional structure. Since the total depletion layer is composed of the completely depleted gate-buffer layer and the depletion layer in the channel layer, the part in the channel layer shrinks when there exists a gate-buffer layer, compared to the conventional structure, as shown in Fig. 8. As a result, the effective channel width is increased and a larger current occurs in the Buffer-Gate MESFETs than in the conventional structure.

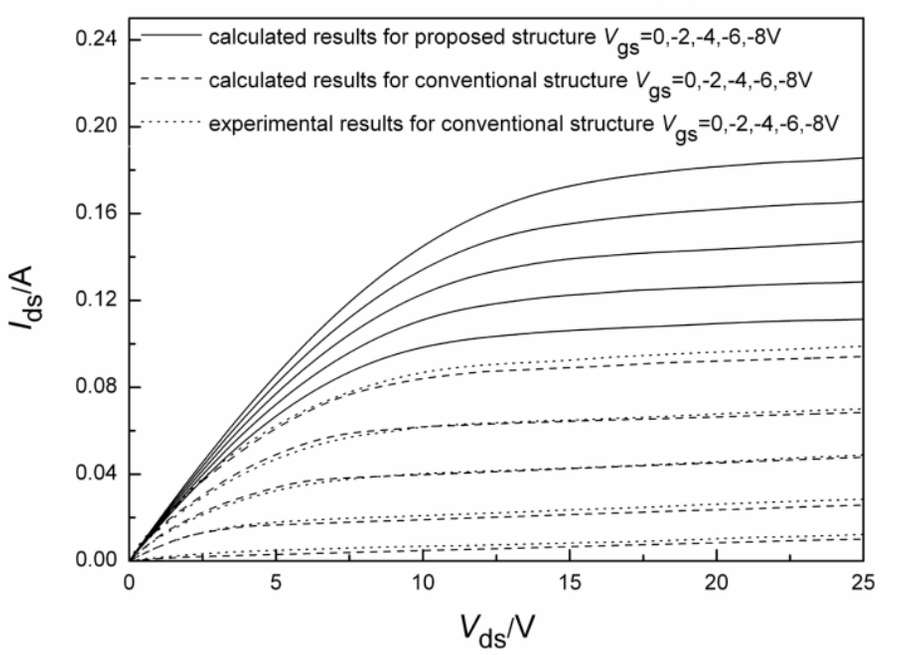

Figure 15. Calculated and experimental *I-V* characteristics, for the conventional and buffer-gate structures, V_{gs}=0,-2,-4,-6,-8 V.

Fig. 16, 17 and 18 show the effect of the gate-buffer layer thickness on the small signal parameters. The transconductance, gate-source capacitance and channel resistance are decreased, while the drain conductance is increased with the inserted *lower doped* gate-buffer layer thickness (completely depleted) because the total depletion layer thickness under the gate is increased but the part in the channel is decreased, as are depicted in Fig.16 and Fig. 17. The cutoff frequency (f_T) is increased with the gate-buffer layer thickness slowly because the decrease of the transconductance is overcome by the decrease of the gate-source capacitance. Since the decrease of the channel resistance is more dominant than the increase of the drain conductance with the gate buffer layer thickness, the maximum oscillation frequency (f_{max}) is increased more rapidly than the cutoff frequency. The results show that f_T and f_{max} are significantly improved, compared with those of the conventional structure. Therefore, the buffer-gate structure has better frequency performance than that of the similar device based on the conventional structure.

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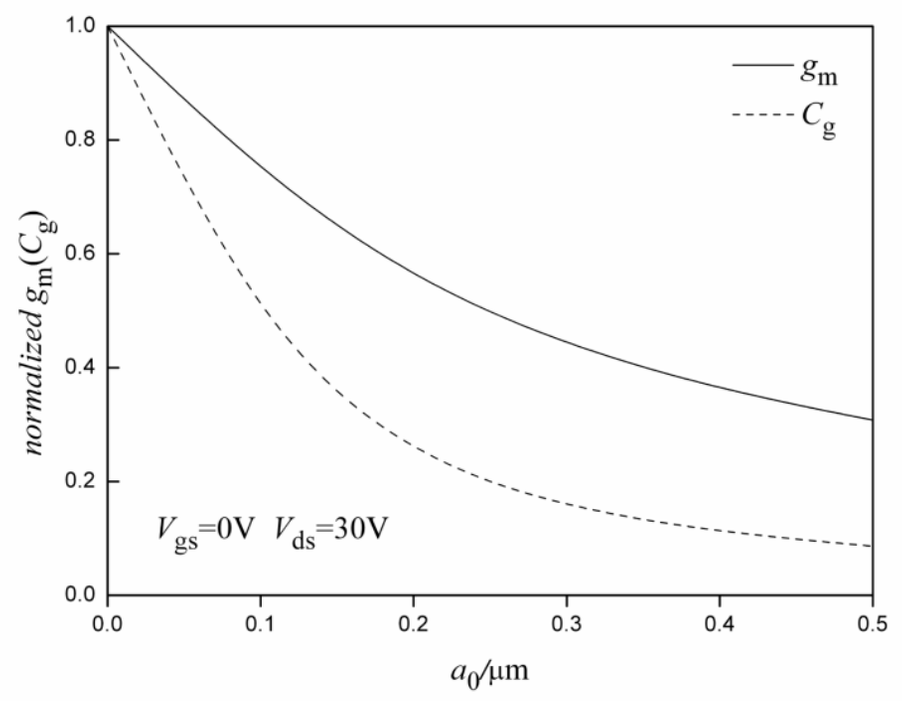

Figure 16. Dependence of transconductance g_m and gate-source capacitance C_{gs} on the gate buffer layer thickness, V_{gs}=0 V, V_{ds}=30 V.

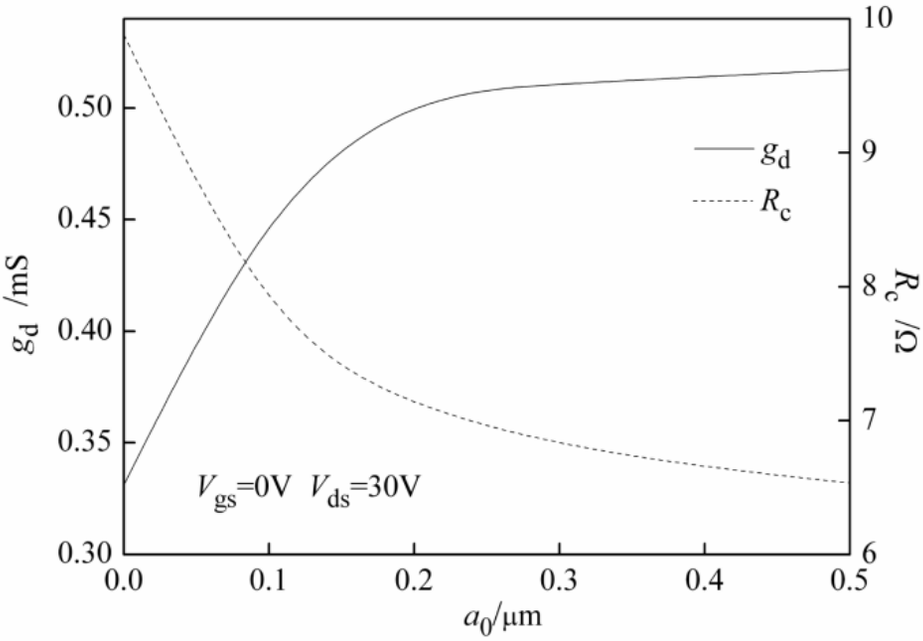

Figure 17. Dependence of drain conductance g_d and channel resistance R_c on the gate buffer layer thickness, V_{gs}=0 V, V_{ds}=30 V.

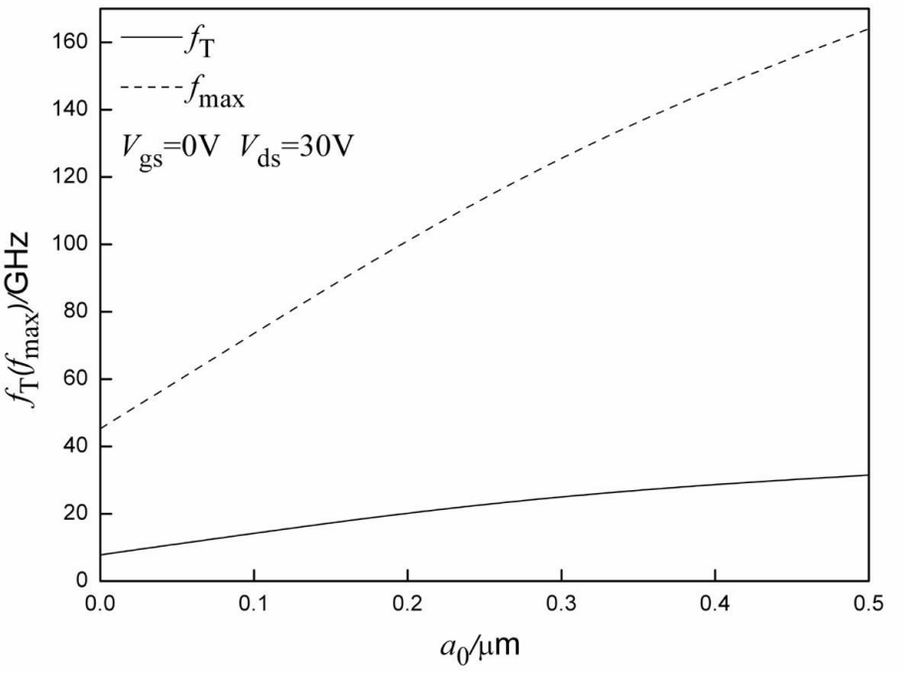

Figure 18. Dependence of cutoff frequency f_T and maximum oscillation frequency f_{max} on the gate buffer layer thickness, V_{gs}=0 V, V_{ds}=30 V.

Notes

In this chapter, the significant results, which are obtained recently, are reviewed for the 4H-SiC MESFETs (Metal Semiconductor Field Effect Transistor). First, the basic operation principle for the 4H-SiC power MESFETs is briefly reported. Then, several new 4H-SiC power MESFETs structures are discussed, focusing on the surface electric field, breakdown voltage and frequency characteristics. Finally, the models with the electric field-dependent mobility are also reported for the conventional and buffer gate SiC MESFETs.

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