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Josephson Junctions for Present and Next Generation Voltage Metrology

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1. Introduction

Josephson array voltage standards are the most complex superconducting integrated circuits in actual use, and represent the first and the most outstanding achievement in quantum metrology.

However some issues must still be improved for a more extended exploitation of these devices in basic metrology and in advanced precision instrumentation for applications ranging from aerospace, to defense and others.

This is mainly true when the extension of DC voltage references based on Josephson effect to AC or to the generation of programmable voltages is considered, since the circuits of these arrays are usually more complex, requiring an higher number of junctions.

In this chapter we present the most developed and the most advanced solutions studied sofar to satisfy this problem, which require to achieve the best integration and the lowest power dissipation, while preserving the basic issue of the highest noise immunity of the voltages produced by the arrays.

These characteristics should be met through the most suitable selection of some Josephson junctions parameters such as the maximum critical current density, the characteristic voltage, the junction size and the degree of hysteresis of the current voltage characteristic.

A nontrivial role is also played by the thermal stability of some of these parameters.

In order to obtain the best performances, and therefore to optimize the characteristics outlined above, we will examine different types of Josephson junctions, discussing the advantages and disadvantages of each type and showing possible research directions to choose the most suited fabrication materials and processes, considering also the possibility of using cryocoolers.

The contents of the chapter are the following:

In a first section, Josephson effect and Josephson junctions, some basic physical concepts are reviewed

In the second section, Josephson Voltage Standards: from DC to AC, the application of the quantum effect to Voltage metrology is outlined, emphasizing the specificity of the extension to AC respect to the traditional DC standard

The main focus of section 3, Current junction technologies and fabrication issues, is on the different type of Josephson junctions employed so far in circuits for programmable and AC voltage standard, with details on the link between fabrication technology and device performances.

In a last section, Special issues for next generation standard and possible solutions the present and future applications of these standards to measurement are mentioned, with main stress on the routes to overcome present limitations to these challenges

2. Josephson effect and Josephson junctions

Modern voltage metrology is based on the Josephson effect which is a macroscopic quantum effect of inherent fundamental precision occurring in a weak link between two superconductors.

The essential properties of superconductive material are that the resistance to a continuous electrical current becomes zero and a magnetic field cannot penetrate inside, up to a critical value, which is characteristic of each material. Superconductivity is therefore described by the conditions electrical resistance $R=0$ and magnetic induction $B=0$. The superconductive, non dissipative state, is characterized by an advantageous energetic condition respect to the normal state, since in some materials below a critical temperature T_c and a critical applied magnetic field H_c, all the electrons condensate at the same energy, which is separated by the Fermi level from a gap Δ, in the range of about 1 mV.

This energetically favorable superconductive state establishes a long range order extending through the material, where the charge carriers, the Cooper pairs, flow without dissipation. The Cooper pairs are a particle which has twice the electric charge of the electron and a virtual radius corresponding to the coherence length of the superconductor, of the order of tenths of micrometer. They are formed at low temperature by the mutual attraction occurring between two electrons exchanging virtual phonons related with vibrations of the lattice [1].
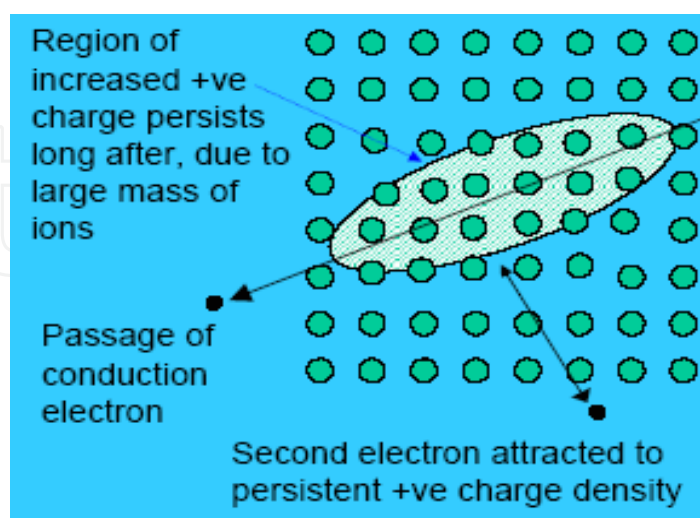

Fig. 1. Picture of the Cooper pair binding mechanism inside the atomic lattice.

Concerning the Josephson effect, it was firstly theoretically predicted and observed for tunnel junctions with two superconductive electrodes separated by a very thin insulating

barrier (of the order of nm) [2]. In this first model, for a Josephson junction realized as a weak link between two superconductors, a quasiparticle inside the barrier, in order to penetrate in one of the superconductors must get an energy greater than the superconductor energy gap, which is not possible by direct charge transfer.

But another process may occur: in the so called Andreev reflection [3] an electron impinging at the interface of the weak link with the superconductor, is converted into an hole moving in the opposite direction, thus creating a Cooper pair. Similarly, at the other side of the weak link, the reflection process annihilates a Cooper pair from the other superconductor. The result is the tunneling of the Cooper pairs through the barrier of the weak link. Nowadays, it was generalized to a variety of junctions, the most accepted interpretation is based on the Andreev reflection process.

This tunneling is not dissipative up to a critical value of current I_c, whose amplitude is determined by the geometry of the junction, the materials and the operating temperature. Below this value the current depends only from the phase difference φ of the two wave functions describing the superconductive electrodes of the junction.
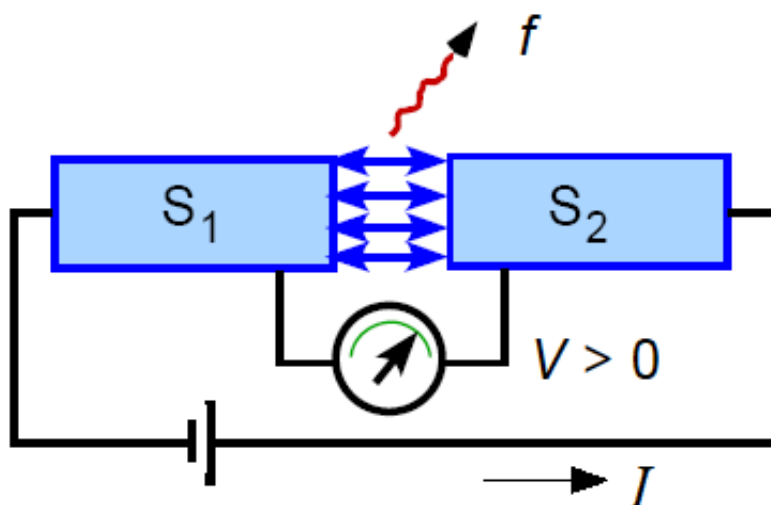

Fig. 2. Josephson junction general scheme. When a voltage drop V appears between the two superconductive electrodes an oscillating signal of frequency f is emitted by the junction.

The first Josephson equation, called DC Josephson effect then states:

$$I = I_c \sin\varphi \tag{1}$$

When the biasing current I is $> I_c$, a voltage V appears across the junction and this voltage generates on its own an oscillating current, whose frequency f is related to the voltage from the second Josephson equation.

$$V = (h/2e) \times f \tag{2}$$

The last relation is at the basis of the modern Voltage metrology. The quantity $h/2e$ is called Φ_0, and represents the unity flux quanta.

As stated, equation 2) is independent from any device characteristic or any operating condition, and does not have any drift in time.

In the practical experiment, the Josephson frequency, which is in the THz range, is modulated by a microwave signal, producing voltage steps at fixed, constant interval n $(h/2e) \times f$, with n integer 1, 2,.. These steps, called Shapiro steps, are used as reference voltage in the measurements, and their amplitude in current depends on the power of the microwave signal coupled to the junction, according with good approximation to the relatioship: (3) These steps, which are what is used as reference voltage in the measurement, are called Shapiro steps, and their amplitude depends on the power of the microwave signal coupled to the junction.

$$I_s = I_c \sum_{n=0}^{\infty} (-1)^n J_n \left(V_1 \Big/ \Phi_0 f_1 \right) \sin \left[\varphi_0 + \frac{2\pi}{\Phi_0} V_0 t - 2\pi n f_1 t \right] \qquad (3)$$

where: I_s step current width, I_c critical current, I_s step current width, V_0 (V_1) dc (ac) voltage bias, f_1 ac bias frequency, and J_n Bessel function of order n.

Experiments where the voltage provided by two different Josephson devices radiated by different microwave signals was detected through a Superconductive Quantum Interference Device, SQUID, the present most sensitive flux and current detector (resolution of the order of. $\varphi_0 = 2.068 \times 10^{-15}$ Wb), showed no difference also in measurement repeated along the time, at the level of 10^{-16}.

The device realizing the relations 1) and 2), the Josephson junction, can be obtained in different ways, according to what mentioned above. In particular, for the application to Voltage standard, after first point contact junctions, which were not reproducible, and generated voltages around 1 mV, thin film junctions have been used, exploiting the development of microelectronics processes.

The motion equation of the Josephson junction, describing the current flow is the electrical equivalent of the mechanical pendulum, and gives the total current in the junction as sum of three terms

$$I = I_c \sin\varphi + VR + C \, dV/dt, \qquad (4)$$

where R and C are equivalent resistance and capacitance of the junction

Defining the parameter $\beta c = (2\pi I c R^2 C) / \varphi_0$ as the damping factor of the junction in analogy with the pendulum, the current voltage, I V characteristic of a Josephson junction can be single valued for $\beta c < 1$, and the junction is called non-hysteretic or overdamped, or multiple valued, for $\beta c > 1$, and the junction is called hysteretic or underdamped.

Correspondingly, the response to a microwave signal produce two type of staircase, as will be reported in the next section.

3. Voltage standards: From DC to AC

A DC voltage V applied to a Josephson junction equals exactly the rate of single flux quanta $f\Phi_0$, transferred along the junction: $V = \Phi_0 f$. If the flux transfer is phase-locked to an external oscillator with the highly stabilised frequency f, the transfer rate is kept constant over a certain range of current through the junction: this leads to constant voltage steps in the DC characteristic at $V_n = n\Phi_0 f$. Due to the nonlinearity of the DC charcteristic, this occurs not only at the fundamental frequency f but also at the higher harmonics (n = 2, 3, 4,....). For a

drive frequency of 70 GHz, the fundamental voltage step amounts to about 135 μV. As the frequency can be stabilised to a very high degree, such a voltage step is a perfect voltage reference with a reproducibility of up to a few parts in 10^{10}.

Josephson junctions used nowadays in DC voltage standard applications are based on hysteretic SIS junctions with zero crossing steps i.e. voltage steps whose current range spans positive and negative values, including the condition of zero DC bias. The choice of this technique dates back to the first attempts in series-connecting the thousands of junctions needed to reach output levels of 1 V and above, as required in metrological applications. The voltage steps are generated in the sub-gap part of the DC characteristi and all voltage steps between the maximum output voltages, e.g. -10 V and +10 V are biased by the same current. Exploitation of the zero crossing steps, fist suggested by Levinsen [4] eventually allowed to overcome many technological difficulties and made it possible to realize arrays with reproducible overlapping steps.
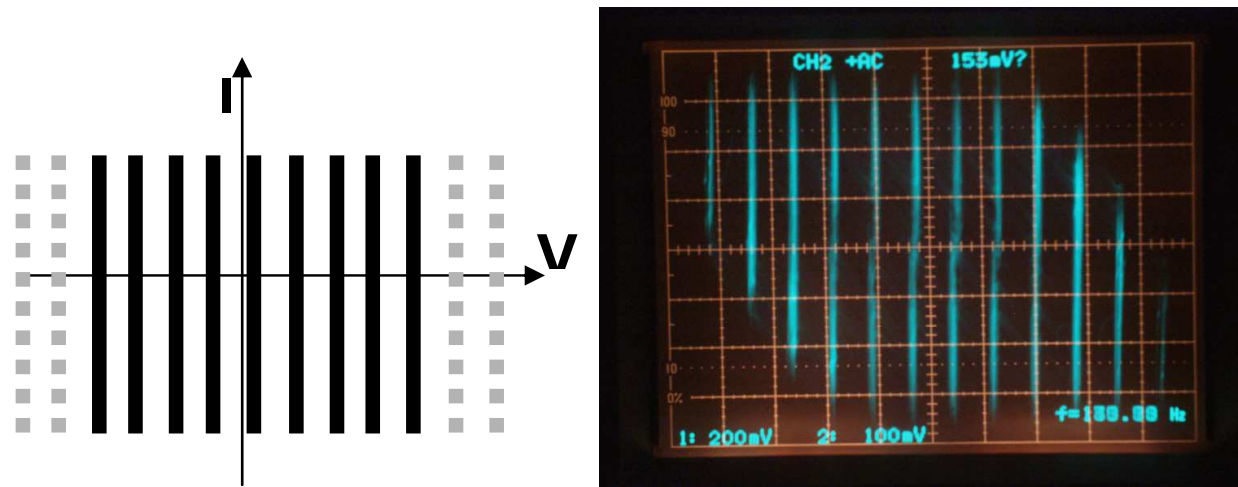

Fig. 3. Operating principle of programmable Josephson arrays (right) and IV characteristics (left) of the INRiM 10 V standard observed at the oscilloscope.
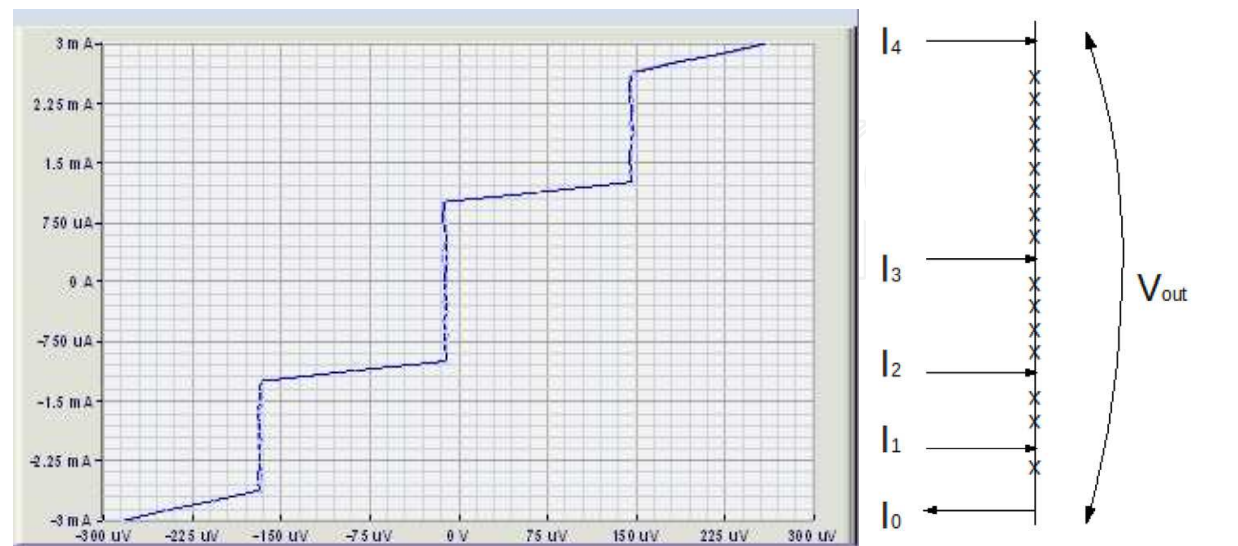

Fig. 4. Operating principle of programmable Josephson arrays. By controlling the bias currents I_1 - I_4 it is possible to change the output voltage V_{out}.

To increase the output reference voltage to practical values, large series arrays of strongly under-damped Josephson tunnel junctions of the SIS-type (Superconductor-Insulator-Superconductor) – in this case Nb-Al_2O_3-Nb – with hysteretic DC characteristic were developed. On the one hand, this allows to make use of higher harmonics steps up to n = 6 on a average per junction and generate 10 V output voltages with the relatively low number of 12000 to 14000 junctions. The availability of 10 V standards with quantum accuracy has led to dramatic improvements in DC voltage metrology, and it is now possible in primary DC voltage calibrations at 10 V to attain relative uncertainties as low as 10^{-11}.

More recently, the interest in voltage standard research has moved to the investigation of techniques for extending the application of Josephson arrays to AC quantum standards and to standards for arbitrary time-varying signals. To this aim, junctions with non hysteretic behavior were suggested to allow changing the output voltage through control of the bias current. The substantial difference, from the application viewpoint, in using non hysteretic junctions, is that their IV curve (voltage *vs.* current relationship) under irradiation is a one to one staircase, thus the output voltage is univocally defined by the current feed through the bias circuit. This is not the case for hysteretic junctions used in DC standards, were steps are overlapping and all share approximately the same interval of currents.

In so-called programmable standards, the junctions bias currents are used to activate/deactivate array sections. Such arrays are typically subdivided in sub-circuits with series connected junctions generating voltages following a power of two sequence. Combining the sections it is then possible to source binary programmed voltages in a way that is very similar to the technique used in electronic digital to analog converters [5]. In order to replace best AC standards, the uttermost accuracy has to be reached and many efforts have been devoted in realizing arrays with performances suited to the tight requirements set by modern primary metrology. Many approaches to junction fabrication have been developed, and several different technologies have proven successful in providing voltages up to 10 V, with good metrological properties. Programmable Josephson arrays are so far the most successful attempt to extend metrological applications of Josephson standards beyond dc. Programmable arrays operating at 1 V have been effectively used for several applications: as traveling standards for international comparisons [6], for generating precisely varying voltages in a watt balance [7], as quantum impedance and power standards [8]. Moreover, only programmable standards can presently provide output voltages up and above 1 V, and even exceeding 10 V [9].

Nonetheless, this technique suffer from some limitations, the most severe is due to the time for step switching, where junctions are not operating in a quantized state. During these transients, the array voltage is not precisely known and the uncertainty of the generated signal increases with the fraction of period spent in the transients. Since the minimum transient time is constrained by technological limitations, programmable arrays can fulfill primary metrology uncertainties only for signals with frequencies up to few hundreds Hz [10].

To overcome limitations of programmable standards, arrays operating with a pulsed, square wave, rf signal have been developed. Using short pulses instead of a sinusoidal rf signal

makes it possible to effectively modulate the signal period while keeping junctions phase locked over a wide range of frequencies [11],[12],[13]. Fundamental accuracy follows from the control of the flux quanta transferred through the junctions by the pulsed signal. The output voltage is then exactly calculable in terms of fundamental constants if the number of the flux quanta per unit time, i.e. the pulse repetition rate is known [14]. Pulsed standards allow to synthesize arbitrary waveforms with quantum accuracy based on the sigma-delta technique for digital to analog conversion developed for semiconductor electronics and very high spectral purity [15]. Both operation and fabrication of pulsed standards set very challenging problems. Due to the complexity of pulse waveform, the apparatuses for generation of precisely frequency controlled pulses are sophisticated and expensive, and the design of rf transmission lines is extremely difficult because of the harmonic richness of the signal. In addition, it is extremely difficult to generate a bipolar output with a frequency modulated Josephson array, and very complex AC biasing techniques, involving a sine wave and a pulsed signal, both synchronized, must be used for real AC operation [16]. Generation of the pulse train for proper junction operation requires top-end instrumentation and unavoidably limits the signal fundamental frequency to values much lower than those obtainable with continuous wave sources. Power distribution to array junctions is also of concern, since the usual microwave techniques developed for nearly monochromatic signals are not directly applicable to broadband pulses. Adoption of lumped circuit methodologies seems at present the most viable solution, though highly demanding on the fabrication side. In order to have negligible effects on circuit behavior, the propagation time of rf signal along the array must be smaller than the signal period, i.e. the array dimensions must be smaller than the signal wavelength λ. To guarantee reliable operation, $\lambda/8$ is typically considered the maximum value acceptable for array dimensions. Despite all these difficulties, arrays with as many as 10000 junctions have been successfully fabricated, and synthesized voltage signals up to 275 mV rms have been generated with quantum accuracy and extreme spectral purity [17].

Type of Voltage standard	Development status	Performances limitation and typical linewidths	Open questions	Future expected impact
DC voltage standard	1 and 10 V with part in 10^{10} accuracy, used world wide	10 μm		Present status: standard calibration tool
Programmable voltage standard	1V available, 10 V few samples, first applications	AC voltages < 3 KHz 5 μm	To reduce the influence of transients	World wide use for improved AC metrology
Pulse driven voltage standard	275 mV, pure spectra, first applications	1 μm and less	Increase output voltage to 1 and 10 V	World wide use for improved AC metrology

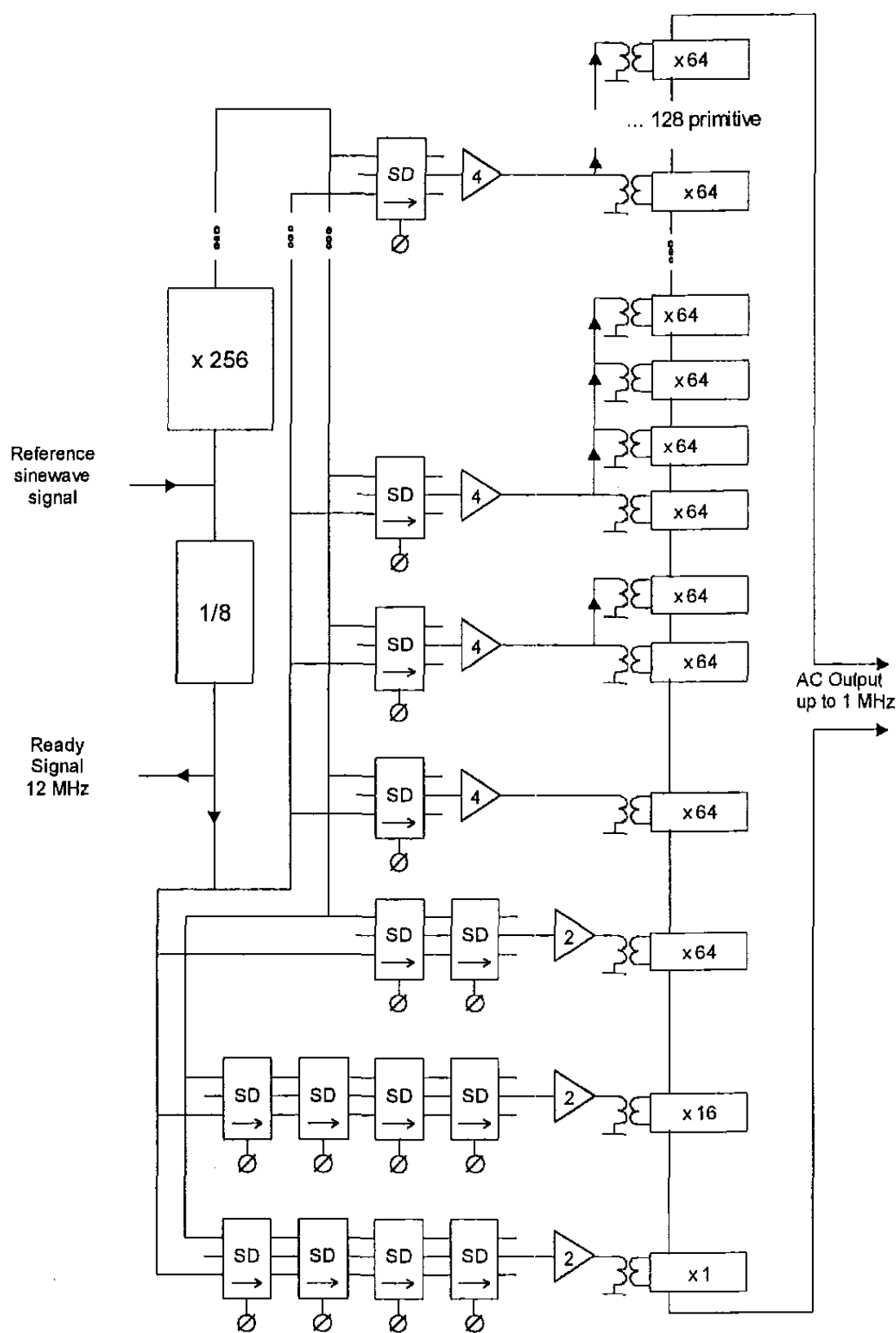Table 1. Comparison of different type of voltage standard.

Fig. 5. Simplified schematic of a Digital to Analog converter realized with RSFQ technology (from [20]).

A new technique has been recently proposed to overcome some of the difficulties encountered with programmable and pulsed standards. The method, named Pulse Power Modulation (PPM), is based on a controlled activation/deactivation of the driving rf signal, to simultaneously set every junction in the array into either one of two states: zero voltage in absence of rf signal and a quantum defined step voltage upon rf application. Waveform synthesis can then be realized by Pulse Width Modulation of the array voltage [18]. The requirements in junction technology for PPM are different form those set by programmable and pulsed standards, since for proper operation an IV curve where the interval of currents of the relevant steps partially overlaps the critical current is needed. Such a behavior can be obtained if a precise control over junction hysteresis is feasible in the fabrication stage, to provide an intermediate degree of hysteresis, between those of the fully hysteretic SIS for DC and the non hysteretic SNS.

Although limited in space, this overview wouldn't be complete without mentioning RSFQ as an alternative technique to synthesize arbitrary and AC signals with quantum voltage accuracy. RSFQ has been, and still remains, a very active field of research for quantum digital electronics applications [19], yet developments for voltage standards have always been left out of the mainstream of research interests in Metrology. One of the main reasons for that is most likely to be found in the completely different approach, know-how and experiences involved by RSFQ, with respect to the common background of voltage metrologist. In RSFQ standards, accurate voltage signals are generated by controlling flux quantized by a Josephson junction. Flux quanta generation is "triggered" by a pulse sequence, thus can be precisely timed, in analogy with the "phase lock" process exploited in array standards [20]. RSFQ approach is potentially advantageous in that the complex and expensive microwave apparatus needed for ordinary standards is avoided, the drive signal being generated by the superconductive circuit itself. The only requirement for RSFQ circuits is an external accurate frequency reference, typically operating in the MHz range. The simplification in instrumentation must be traded off with a much higher complexity of superconductive circuit, namely an increased number of junctions, additional elements like inductors, and fabrication of junctions with different parameters in the same device. The basic element in RSFQ is the Josephson transmission line, a string of Josephson junctions connected by inductors where the pulse can propagate, like in transmission lines, and even amplified [21]. A basic Digital to Analog converter suitable for voltage standard will include at least some voltage multiplier stages, to increase the output signal to practical values. Coupling between Josephson transmission lines and voltage multipliers is obtained by capacitive coupling [22], but magnetic coupling through transformer-like circuits has proven to be more effective [23]. Nowadays DAC for Metrology are fairly more complex devices, with many digital blocks performing various specialized functions, and correspondingly high power consumption. Successful operation, of a 10-bit RSFQ DAC capable of generating up to 20 mV has recently been reported [24].

4. Current junction technologies and fabrication issues

The fabrication of arrays for AC generation and waveform synthesis is a difficult, challenging task, and many different technologies have been proposed and tested, yet the choice of material and fabrication techniques still represents an open question. Independent

of the technique adopted for signal generation, a relevant problem is posed by the high number of junctions needed to reach practical voltages, since junctions for AC typically operate on the first step and the drive frequency is limited for technical and economical reasons [25]. A high noise immunity, low power dissipation, reduced dimensions are also essential properties in metrological applications and in view of spreading quantum standards to a wider range of users.

The chip dimensions are set by the area and the number of junctions, both essential parameters for technology, because a reduced area along with a high number of junctions make it difficult to guarantee the uniformity of their electrical properties, which is essential to observe decent collective steps.

These requirements can be translated into well-defined specifications on junction parameters.

First, the critical current I_c, which sets an upper limit on the amplitude of the quantized steps, should be large enough for steps with suitable width and noise immunity, yet a too high value increases dissipation in junctions. The area of the junction must be small, to reduce array dimensions, but avoiding the excessive difficulties in fabrication imposed by deep submicron patterning, today still hard to achieve for high integration superconductive circuits. It follows that an optimal range exist for critical current density. Presently, values ranging from few kA to tens of thousands kA/cm² appear to be the best choice.

The characteristic voltage, V_c determines the microwave optimal drive frequency f_d, from the relation $\Omega = f_d / f_c$, where f_c is $V_c \times (2e/h)$ and thus the step voltage (i.e. the voltage resolution of the array) and the number of junctions needed to achieve the maximum requested voltage output. To obtain the maximum step amplitude, Ω must be ≈ 1 [26]. In order to use commercial microwave instrumentation and reduce as much as possible the number of junctions, achieving the maximum possible voltage output, drive frequencies close to 70 Ghz are used, and V_c around 150 µV are needed. Of course even larger values, which on the other hand are absolutely advantageous for speed applications, can be used. But in voltage standard application this causes a sensible reduction of the step width.

Moreover, the characteristic voltage defines also the highest speed of RSFQ circuits, since this is proportional to $\tau_{car} = 1/f_c$. In this case, the highest V_c, the higher the speed.

On the contrary, where we focus on the best possible voltage resolution of the standard, junctions with reduced V_c should be used.

In this chapter we discuss extensively niobium and niobium nitride based junctions, considering high T_c junctions in the section devoted to the use at temperatures above 4.2 K. A challenging problem to be solved in the next future for voltage metrology and superconductive electronics applications, is operation in cryocoolers at a temperature greater than 4.2 K. Indeed, in order to make the Josephson quantum standards available to a widespread market, rather than limited only to the National Laboratories, as well as affordable for private companies needing an accurate voltage reference, refrigeration systems cheaper and more compact than those nowadays used for niobium junctions are required. Moreover, as it will be discussed in a next section, the use of a cryocooler would allow a reduction of the measuring leads between the Josephson device and the measuring system, reducing the indetermination associated to the transition between voltage levels.

Considering the electrode configuration, non-hysteretic IV characteristic can be obtained by three main classes of junctions:

- hysteretic SIS with external shunt
- metallic barrier SNS
- double barrier SINIS.

The first class, directly derived from the most developed and optimized process of superconductive electronics, namely Nb/AlOx/Nb junctions and which is still the predominant technology for RSFQ circuits, suffers from the disadvantage of a configuration requiring an external resistor or a more complex circuitry. This, with the severe limitation to I_c from chaotic instabilities [27] limits the use of these junctions in voltage standard circuits. In spite of this a programmable array based on shunted Nb based SIS, where a reactive shunting was realized for blocks of several junctions, proved suitable operation at 1 V level [28].

In any case we will not consider junctions of this type in the following, where a detailed analysis limited to the last two classes will be carried out.

4.1 Programmable voltage standards

Programmable voltage standards (PJAVS) are made with series-connected subarrays, whose size follows a power of two sequence. Through control of the bias current of each section, the series voltage is set by the code represented by on/off status of array bias lines. To switch subarrays, junctions that can generate a current-controlled, univocally defined voltage, i.e. junctions with a single valued (non-hysteretic) IV curve must be used. To provide signal to noise ratios adequate to metrological applications, critical currents at the mA level are at least required. On the other side, due to the fact that only the first Shapiro step of junctions is used, to achieve voltages of 1 and 10 V, V_c even in excess of 100 μV are sought to reduce number of junctions.

As known, the amplitude of the n = 1 quantized Shapiro step normalized to the critical current attains its maximum when the microwave drive frequency and the junction characteristic frequency are nearly equal. This corresponds also to a condition of minimal power dissipation [26]. This leads to optimal V_c of 100-200 μV.

SINIS junctions achieve the shunting of the capacitance of a SIS junction, by using two, very thin oxide layers, separated by a metallic barrier. They are typically made of Nb/Al/AlOx/Al/AlOx/Al/Nb and have been extensively studied both theoretically and experimentally [29-34]. The best results on these junctions for superconductive electronics applications and especially for programmable voltage standard have been obtained by the PTB group, who realized complete successful circuits for programmable potentiometer at 1 and 10 V level with 7000 and 70.000 junctions respectively. These SINIS junctions feature $J_c \leq$ 1kA/cm, V_c as high as more than 250 μV at 4.2 K with junction size 100-1000 μm². SINIS junctions with various values of Al thickness and AlOx barrier transparency have been reported, but, even if they feature J_c and V_c higher than those given above, their IV characteristic was rather anomalous showing an high residual hysteresis at 4.2 K, and were hardly reproducible.

In general a problem for the SINIS junctions is due to the high transparency of the two insulating barriers, with the necessity to realize very smooth planarization of the underlying films, since the probability of defects such as pinholes is increased. The fabrication process, requiring that the two barriers and the three thin aluminum layers been highly homogenous, has set a limitation to the fabrication of really high number of junctions, as in arrays for programmable voltages at 10 V and more [35].

In SNS junctions the damping of the IV characteristic for non-hysteretic behavior is obtained by using a normal metal as barrier. SNS have high values of J_c, but typically the metals used have very low resistivities. Nb/PdAu/Nb junctions have been the first developed type of SNS junctions for this application by NIST group, and have produced stable voltage outputs at 1 V as binary arrays for programmable potentiometers, being also used in circuits for pulse driven AC synthesis [14],[15]. They feature values in the range of 100 kA/cm2 and V_c between 5 and 30 µV with typical size of few µm2, even if J_c values would support also submicron dimensions. The values of V_c limit their use to drive frequencies of few GHz and circuits have about 30.000 junctions for 1 V.

Impressive results have been obtained with NbN/TiN/NbN junctions, developed by the Tsukuba group, since very large arrays, with more than 300.000 series connected junctions have been succesfully tested in a 8 and 11 bit DAC circuits with quantized steps at 10 V at 10 K [36],[37]. Features of these junctions are J_c about 10 to 10 A/cm and V_c 10-20 µV at 10 K with areas of few square micrometer. 20 V output has been also achieved, by series connecting two arrays of different chips, minimizing interconnecting dissipation [9].

Materials have been also proposed as normal metal barrier which are at the metallic insulator transition. In such a way it was possible to tune the barrier resistivity and the characteristic voltage of the junctions [38],[39]. Among the experimental results we mention Nb/TaOx/Nb, NbN/TaN/NbN and Nb/Nb$_x$Si/Nb junctions. Nb/TaOx/Nb junctions fabricated at IEN-INRiM, showed resistivities varying different order of magnitudes depending on the bias voltage of the cathode during the sputtering deposition of the TaOx film [40]. The junctions have however a marked aging, featuring a reduction of at values less than 10 A/cm. Also NbN/TaN/NbN junctions studied in [41] have not yet been suitable for large circuits production. These junctions featured very high Vc, up to more than 0.5 mV at 4.2 K with J_c 10^4-10^5 A/cm2, but required a difficult tuning of fabrication parameters and also the temperature dependence of these parameters was critical.

In this category, Nb/NbxSi$_{1-x}$/Nb junctions represent the most successful attempt so far. Although previously studied by Barrera and Beasley in the '80 [42], the most promising results have been achieved in the last years by the NIST researchers, which experimented these junctions in arrays at 1 V level [43]. These authors achieved a transition from a conductive to an highly resistive phase by varying the sputter deposition power of the two elements. J_c varying from 10 to 10 kA/cm2 and V_c from few µV to 150 µV and more at 4.2 K have been obtained. The stabilization of the barrier stoichiometry, critical aspect of this type of junctions, can be achieved by a thermal annealing after the deposition of the trilayer. Depending on the Nb content and the barrier thickness, also the temperature stability of these junctions can be optimized, see in a next section [44].

4.2 Pulsed standards for waveform synthesis

The series of pulses used for waveform synthesis has a very rich harmonic content and requires proper optimization of the microwave behavior in circuits for rf signal distribution. Most of the techniques adopted for analysis and design of circuits with distributed parameters assumes operation with narrow band signals, thus cannot be directly applied for pulse transmission. The most reliable solution to guarantee pulse operation is to reduce array dimensions allowing lumped analysis of circuit. To that aim array length must be shorter than $\lambda/8$, where λ is the wavelength of the microwave signal. This constraint sets strong requirements on junctions technology, in particular on junction size.

Therefore the main stream for the realization of these devices is a) submicrometric junction technology development or/and b) vertical multistacking of junctions

In order to realize the array configuration described, materials resulting in improved steepness of the etch profile are preferred, especially when multistacks of junctions are employed.

SINIS junctions, initially developed for programmable voltage standards and previously described, have also been tried for AC synthesis, notwithstanding their limitations [33].

However, as mentioned above, the first, and presently the best results in pulse driven standards had been attained with Nb/PdAu/Nb junctions, which, due to their high current density allow to strongly reduce their dimensions [14].

Nb/HfTi/Nb junctions have been experimented by PTB team with successful results in the realization of large submicrometric circuits for AC synthesis which have recently reached quantized voltages from 2000 series junctions. These junctions feature about 80 kA/cm for HfTi 20 nm thick and of 15 μV in junctions 0.2 μm×0.2 μm [33].

Other type of SNS junctions with similar low characteristic voltage, such as Nb/Ti/Nb junctions developed by Jena team and Nb/Al/Nb junctions studied at INRiM have not been resulted in large circuits yet [45]. Ti barrier junctions feature of 10^4 -10^5 A/cm^2 and from 10 μV up to 100 μV Vc, while for Al film 100 nm thick, also higher values of and similar or lower values for were obtained. In both case the junction size was in the micrometer and submicrometer range.

Nb/MoSi/Nb junctions also studied and experimented by NIST team, have been used to realize multistacked junctions for lumped arrays for AC synthesis [46]. They feature critical current density between 10^4 and 10^5 A/cm^2, depending on barrier thickness, while characteristic voltage is typically few tens of μV in junctions of few μm^2.

4.3 Power control standards

Power control standards set some peculiar requisites on junction technologies, their operation being based on the overlapping of the range of currents of the steps and critical current. To fulfill these requirements, a tight control of junction hysteresis is needed.

Referring in particular to [47], where the parameters which must be fulfilled by the junctions to obtain the overlapping of the n=0 and n= 1 step are discussed, it is pointed that the mentioned overlapping is obtained in a stable way when f > (1.5-2) f_c [48]. In particular the authors suggest the employ of edge type junctions with *Vc* as high as 1 mV.

However, in principle, no constraint on V_c is needed, while the need of a sufficient, but not exceedingly high overlapping of the two steps is the only fundamental aspect.

4.4 Application to RSFQ

The application of superconductive technology to RSFQ requires a high level of reliability, suitable for the development and testing of very complex circuits, with thousands of junctions implementing many different functional blocks. The best established technology, well mastered by many foundries, is based on SIS junctions, usually made of a Nb/AlOx/Nb, with an externally shunt resistor [49]. The minimum junction area that can be fabricated with this technology is 12 um2, and the whole process involves as many as 12 mask steps. Impressive results have been obtained with the standard Nb/AlOx/Nb technology: in [50] the operation of a RSFQ quantum DAC with 6000 Josephson junctions, subdivided in several functional blocks, is reported. SINIS junctions have proven to be suitable for RSFQ, and some fundamental circuits based on this technology were successfully operated [51]. More recently, owing to the wide range of tunability of their electrical parameters, co-sputtered Niobium-silicide barrier junctions appear interesting for a wide range of applications in digital electronics and well suited to RSFQ [52]. Even more complex circuits, comprehending RSFQ electronics as a pattern generator of pulses, followed by semiconductor amplifier and a Josephson junction series array as a quantizer are studied, and realization of preliminary building blocks is in progress.
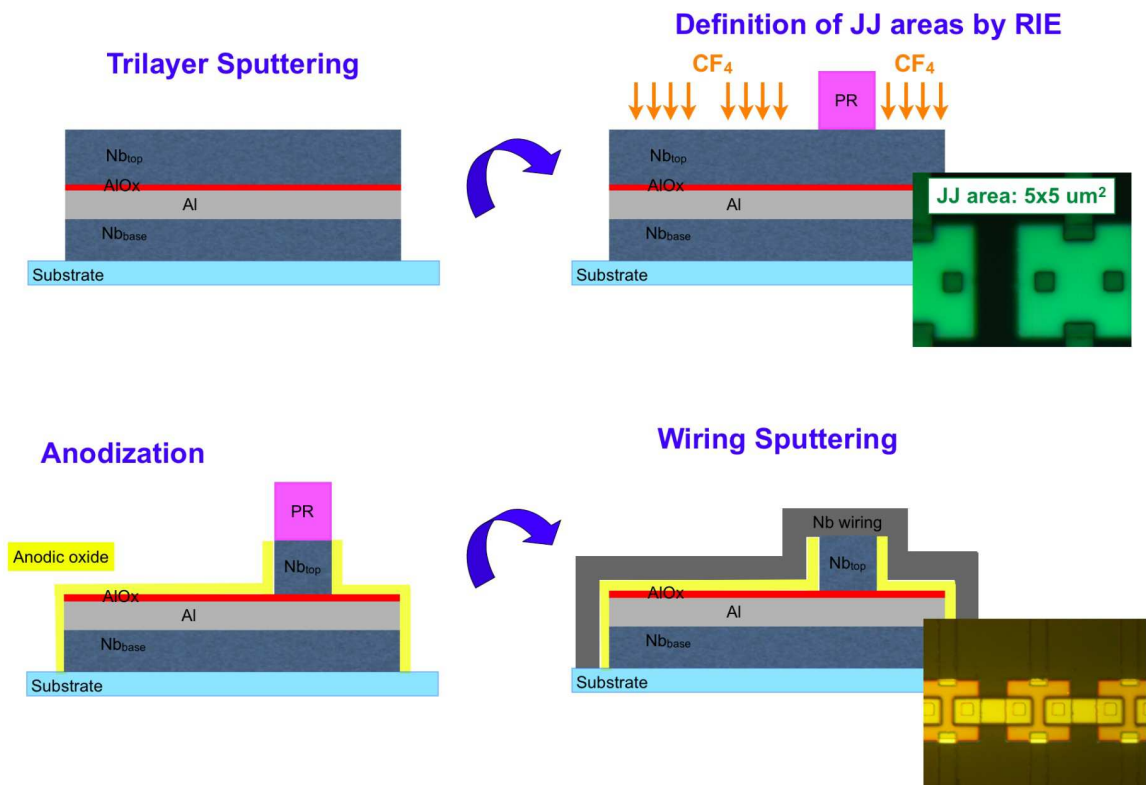

Fig. 6. Example of fabrication process sequence of a Josephson junctions array. The process is started with the trilayer deposition, by sputtering, followed by the area patterning, by photolithographic process and reactive ion etching, and the insulation of the electrodes by liquid anodization. The deposition of contact layers concludes the process.

4.5 An example of a multifunctional junction: Nb/Al-AlOx/Nb overdamped SNIS junctions

SNIS Josephson devices of the Nb/Al-AlOx/Nb type do belong to the family of internally shunted junctions, exhibiting important similarities, but demonstrating additional advantages comparing with other types of self-shunted junctions, namely an extended range of electrical parameters and an advanced temperature stability of transport characteristics.

The main difference respect to the structure of the basic Nb/AlOx/Nb SIS junctions is the thickness of the aluminum film which is increased at tens of nm, up to about 100 nm, and the augmented transparency of the AlOx [53],[54].

An essential feature of SNIS is that, at 4.2 K a transition from the hysteretic to the non-hysteretic state can be induced, when the aluminum thickness is in the above mentioned range, by changing the AlOx exposure dose. Conversely, once chosen Al thickness and AlOx exposure values, this transition is observed as function of the junction temperature in measurements below 4.2 K (see Figure 7) [63].
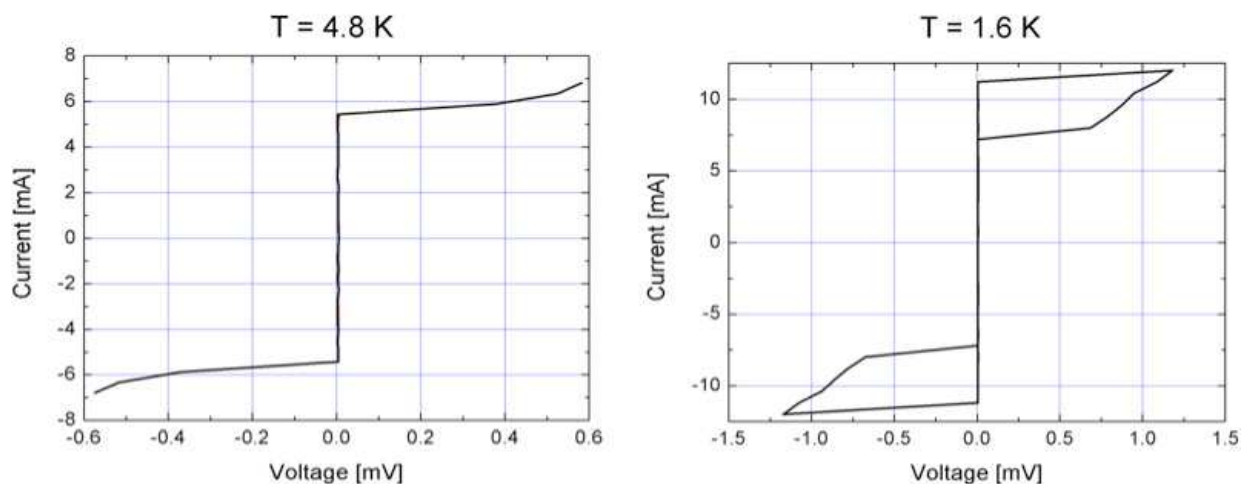

Fig. 7. Transition from non-hysteretic to hysteretic behavior for a SNIS junction, obtained by changing the operating temperature.

Critical current densities J_c of the SNIS junctions are sufficiently high (also 2 mA/μm2, along with characteristic voltage values V_c up to several hundred microvolts at 4.2 K. In particular, junctions with Al-layer thickness ranged from 40 to 120 nm and exposure doses of AlOx between 160 and 250 Pa·s showed J_c from 0.01 to 1 mA/μm2 and V_c from 0.1 to 0.7 mV at 4.2 K. The dependence of J_c on E_{ox} within the indicated interval of E_{ox} is almost linear in the log-log scale, as for other types of Josephson devices with oxide barriers, while the characteristic voltages are more dependent on d_{Al}.

The specific normal conductance of these devices ranges from 0.3 108 Ohm-1cm-2 to 0.7 108 Ohm-1cm-2 and, hence, is of the same order of magnitude as that in high-current-density single-barrier Josephson junctions and double-barrier SINIS heterostructures [54].

As indicated in the literature, the main explanation of the self-shunting phenomenon in high specific-conductance devices both SIS and in SINIS structures, consists in the enhanced subgap conductivity. The same result has been verified in SNIS junctions where the subgap

resistance R_{sg} at 4.2 K and very low voltages is of the order of 0.3 Ohm which is higher but comparable with the normal-state junction resistance R_N.

The main contribution to this subgap enhancement may be related to Andreev reflection processes in the interlayer. Really, since the Al film thickness in SNIS junctions is comparable with the electron mean free path, the transparency of the weak link between the Nb electrodes is dominated by that of the insulating layer. Its average resistance nearly coincides with that in high-specific-conductance Nb-AlOx-Nb junctions where appearance of multiple Andreev reflections was revealed by analyzing comparatively high subgap 'leakage' currents in Nb-AlOx-Nb junctions. Hence, the explanation of the phenomenon suggested for these structures and based on the existence of a universal distribution of transparencies in dirty disordered tunnel barriers [55],[56] in the interlayer. Really, since the Al film thickness in SNIS junctions is comparable with the electron mean free path, the transparency of the weak link between the Nb electrodes is dominated by that of the insulating layer, Its average resistance nearly coincides with that in high-specific-conductance Nb-AlOx-Nb junctions where appearance of multiple Andreev reflections was revealed by analyzing comparatively high subgap 'leakage' currents in Nb-AlOx-Nb junctions . Hence, the explanation of the phenomenon suggested for these structures and based on the existence of a universal distribution of transparencies in dirty disordered tunnel barriers is appropriate to these devices as well. They do not arise from trivial pinholes because after suppressing the Josephson effect, usually no leakage supercurrents were observed.

5. Special issues for next generation standard and possible solutions

5.1 About the extended use of Josephson Voltage standard in AC measurement

The use of Josephson junctions arrays for AC measurement, while has already set up reference standards of AC voltages in defined ranges of amplitude and frequency, as described in section 2, represents also the first step of new quantum based electrical metrology and instrumentation, of which the quantum voltmeters represent an example.

A first application to AC measurement has been realized by using a programmable array to generate the AC voltage to be compared, at some frequencies, with the DC voltage of a thermal converter, through a suitable balance bridge. In such a way the determination of this standard is also linked to the e and h fundamental constant A comparison between the traditional technique and the one employing PJVS has demonstrated and the accuracy for AC voltages up to 100 Hz can be better than one part in 10^7.

Further improvement are expected concerning AC equivalent of the resistance: it is in fact possible to realize quantum impedance bridges, by using two separate sections of an array, or even two different arrays each separately radiated by a microwave signal, with a known and measurable phase difference. A two terminal pair impedance bridge has achieved an accuracy of one part in 10^8 in a frequency range from 25 Hz to 10 KHz, limited mainly by contact resistance changes at the bridge terminals [57]. Further progress is expected when a four terminal connection to the resistances can be provided..

Also quantum sampling of waveforms is made possible, by realization of Josephson DAC with quantum accuracy, and using them with a proper electronics which enclose in the same circuit conventional and quantum based DAC.

A further employ, presently already in progress, is the realization of standards for Johnson noise thermometry, where arrays of a small number of Josephson junctions are used to generate random white noise voltages. For this application, while the amplitude is not important, the device should extend the frequency range of quantum standard as much as possible [58].

All these aspects have been the subject of specific research projects of Euromet, named ProVolt, JAWS, Binary Josephson Array Power Standard, JOSY and future proposals of next calls.

But, considering the use of Josephson junctions for Voltage standard, the content of this chapter, what are the main goals for the next generation devices?

As mentioned above, see figure 7, both amplitude and frequency of the AC voltage must be pushed to higher values.

It should of course be observed that for people working in the AC field the value of importance is the rms voltage, while typically the output from the values mentioned for some of the mentioned devices is the maximum output DC value.
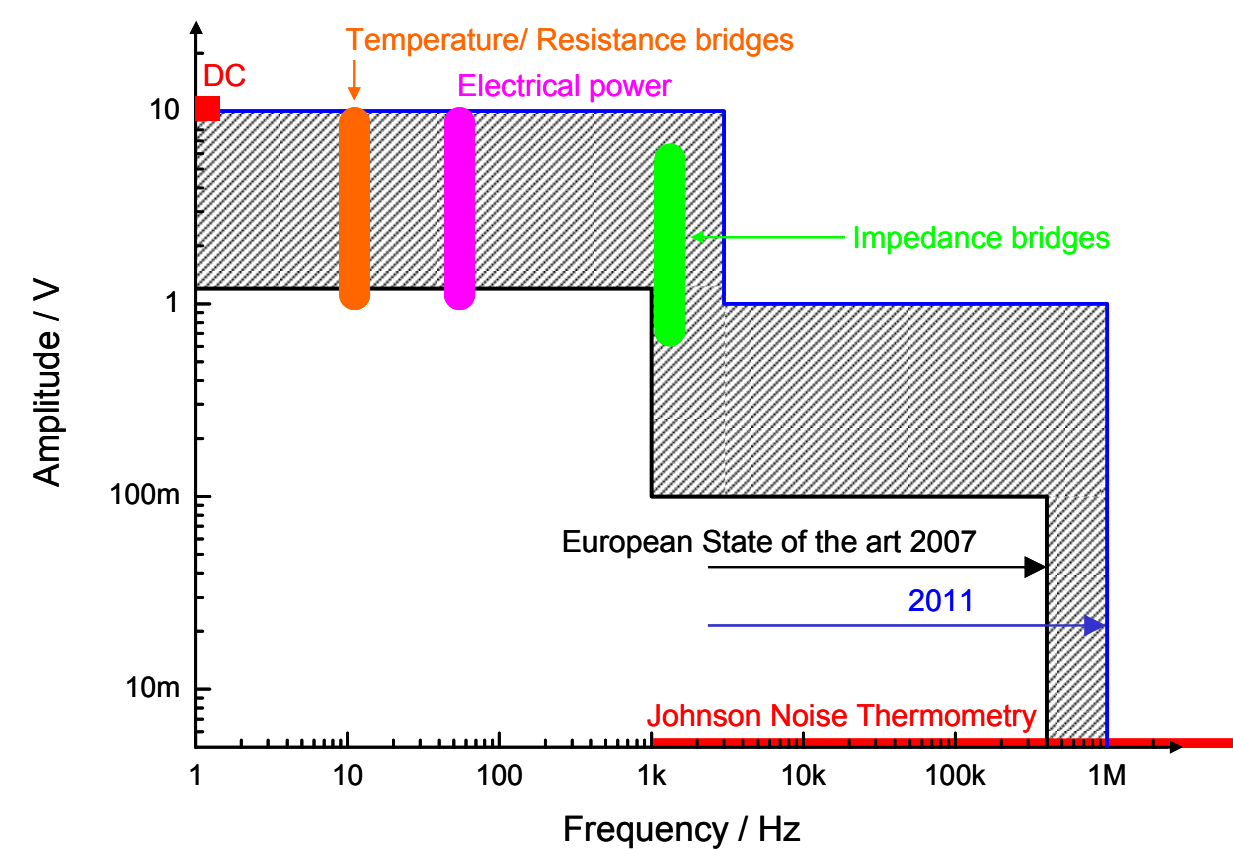

Fig. 8. Josephson programmable and pulse driven AC Voltage standard impact on measurement of AC voltages for some applications. The amplitude and the frequency extension for the time period from 2007 to 2011 is indicated. (from IMERA TP 4 Josy project extended summary).

To increase the output voltage of the arrays is a serious challenge since nowadays to have more than 10^6 Josephson junctions on the same chip with tolerable spread of parameters (5-10%), is beyond the state of art of superconductive technology, As reported in a previous section, 250.000 junctions in plane or 330.000 in vertical stacks of three junctions [17], are the best result sofar.

So, waiting for a technology which can overcome this limit a different approach must be presently searched, reducing as much as possible the number N of junctions and their dimensions for a given voltage output, while keeping the desired voltage resolution.

Another relevant issue is in the possibility of operation at temperatures higher than 4.2 K, in view of the substitution of expensive liquid helium refrigeration systems with the compact cryocoolers which can lead the diffusion of voltage standards to the private companies.

This is a challenge of great importance for superconductive circuits and voltage standards apparently not to be solved in a short period by high T_c junctions. At present, large arrays fabricated with higher critical temperature superconductors, like YBCO or the more recent MgB_2, are not yet available, since the technology of these junctions do not allow to achieve the required integration level [59]. One big problem of these junctions is the stability in time and with thermal cycling.

The most interesting results sofar have been achieved with YBCO bicrystal shunted junctions, where quantized steps have been measured near 77 K above 100 mV [60].

Concerning niobium and niobium nitride based junctions, only NbN/TiN/NbN have demonstrated operation at these temperatures, achieving a sound result such as a 11 bit DAC with 10 V output at 10 K, which were also risen at 20 V, by using two separate chip connected in series [9].

However, they are sensitive to temperature changes, requiring a stabilization of the cryocooler at 0.1 K level, have a strong demand on dissipated power and require a top-level, costly, fabrication process.

The need of the temperature stability means that small temperature variations should cause only small current changes and can be of interest for applications where a simplified refrigerator is used such as RSFQ and also voltage standard applications [19]. For example, conventional SIS junctions exhibit an excellently stable temperature range from 0 to nearly 0.6 T_c but a very strong *Ic-vs-T* dependence above.

A possible solution for both the above mentioned issues is to use high characteristic voltage junctions.

As reported in section 3, this is not trivial, since intrinsically overdamped junctions have V_c below 100 µV at 4.2 K.

However two different technologies have been recently proposed able to produce V_c as high as 0.5 mV and more at such temperature: $Nb/Nb_xSi_{1-x}/Nb$ SNS and Nb/Al-AlOx/Nb SNIS junctions

In the following results using SNIS are reported.

5.2 Advantages of using junctions with high characteristic voltage: a) Use of higher order steps to optimize Vmax/N

A specific feature of SNIS junctions is the possibility of achieving high values of both I_c and V_c, see section 3.5, with current density J_c up to 0.5 mA/μm2 and V_c up to 0.7 mV at 4.2 K.

It is then possible to fabricate junctions with dimensions in the range of 1 μm2, with critical currents in the mA range, which ensures that adequate amplitudes of the Shapiro steps are obtained in circuits with reduced dimensions.

Concerning the step amplitude, as reported in section 3.1, the optimal value for the Shapiro steps in overdamped junctions is obtained when $f_{drive} \approx f_c = 2e/h\ V_c$, which gives values of about 0.15 mV for f_{drive} = 70 GHz. The choice of $f_{drive} = f_c$ is regarded as the best operating condition for Josephson binary arrays since it ensures the minimal demand of microwave power for equal and maximized 0 and ±1 step amplitude. In fact for many applications the step n = 0 is needed to establish zero output voltage. However, steps corresponding to higher order harmonics are enhanced for f_c multiple of f_{drive} [61]. This allows to measure voltages twice, three and also four times higher for a given number of junctions and for instance, a binary-divided arrays consisting of 8192 SNIS Josephson junction has given output voltages of 1.25, 2.5, 3.75 and 5 V [62].

Of course an increased power dissipation is required to work on higher order steps, proportional to the square of the bias current of the step, especially if the maximum amplitude of the step is searched.

In figure 9 the amplitude of the Bessel functions of order 1 to 3, to which are proportional to the corresponding steps, is plotted vs. the argument of these function, which, according to Shapiro calculations, is related to the voltage of the microwave signal of frequency f_{drive}
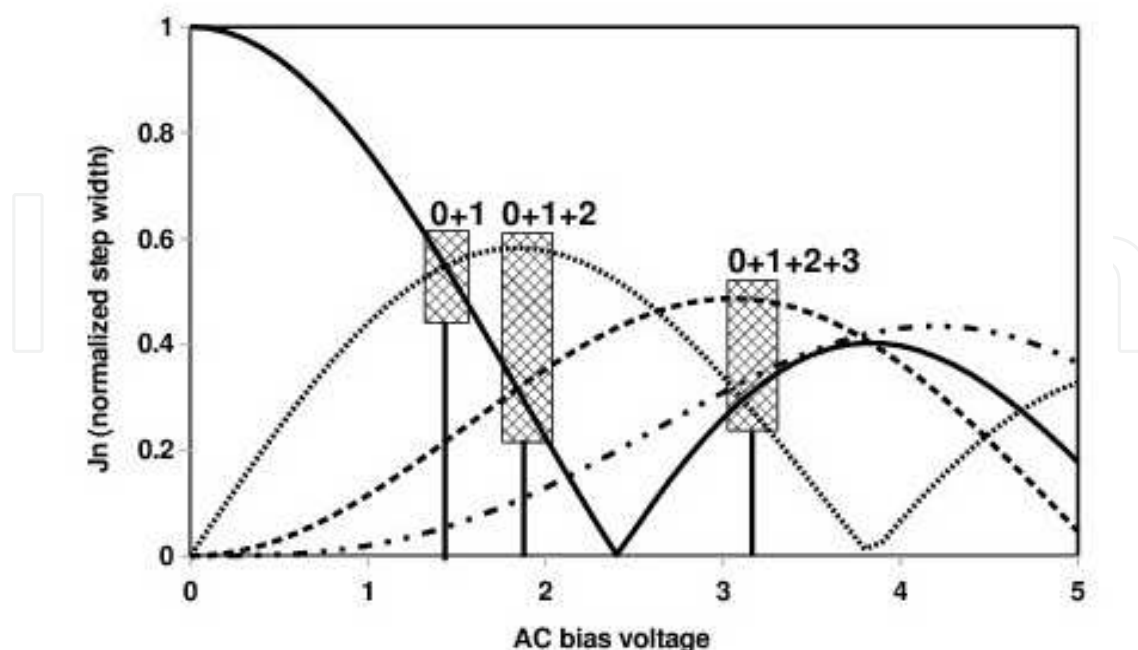

Fig. 9. Step amplitude behavior for n=0–3, see eq. 4. Conditions for optimal 0 and 1, 0, 1 and 2 and also 0, 1, 2 and 3 are indicated.

And it must be remembered that, when higher order steps are used, the voltage resolution of the device is correspondingly reduced, since now vmin. = f_{drive} × n.

Therefore it must be evaluated what is the target to be fulfilled: if maximum voltage output, circuit dimensions, power dissipation or resolution. In correspondence different type of standard can be fabricated.

An optimal solution seems achieved when using arrays made of junctions with characteristic voltage in the range between f_{drive} < f_c < $2f_{drive}$, where it is possible to have both first and second step enhanced.

From figure 9 the condition where the steps n=0, 1 and 2 are all optimized requires a low increment of the microwave voltage, with respect to that for optimized steps n=0 and n=1.

Experimentally, for a radiation frequency of 70 GHz, an RF power of about 40 mW, measured at the input flange of the waveguide cryoprobe for equal 1st and 2nd step (cf. Figure 10), is slightly higher of 20-25 mW for the case of n=0 and n=1. The V_c of this array was 0.3 mV. The step amplitudes, measured with oscilloscope and with sub-microvolt techniques confirm flatness at metrological level (Figure 9 inset), while the RF power is slightly higher of 20-25 mW for the case of n=0 and n=1. The V_c of this array was 0.3 mV. The step amplitudes, measured with oscilloscope and with sub-microvolt techniques confirm flatness at metrological level (Figure 10).
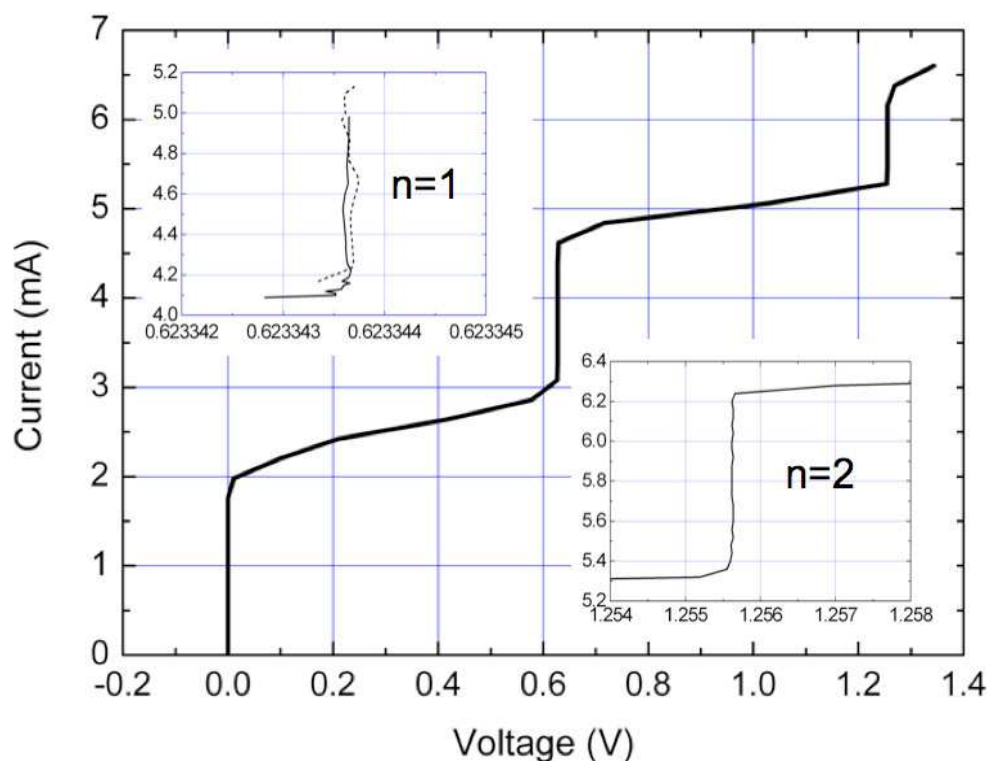

Fig. 10. Part of a binary-divided array consisting of 4096 SNIS junctions irradiated by 73 GHz microwaves. The microwave power, 40 mW at the input flange, has been optimized to have equal and wide (1 mA) 1st and 2nd steps. The insets show high resolution measurements of steps profiles. The n=1 step was traced with a precision DVM (dashed) and by array comparison (continuous).

The precision measurement have been carried out using different approach: i) the array voltage has been measured with a Digital Voltage Multimeter, DVM, using multi averaging to reduce noise, ii) the voltage of one half of the array was measured vs. the voltage of the other half, biased on the same step, iii) the voltage of the programmable array was compared with the 10 V DC voltage standard, biased at the appropriate voltage level. Depending on the method, the resolution ranged between 1μV and 10 nV.

Being $V = Nn \, (h/2e) \, f_{drive}$, where N is the number of series connected junctions and n is the step order, this results in the possibility of using an array where half the number of junctions provide the same voltage output, with the same resolution, by realizing a suitable biasing electronics for 1st, and 2nd and 0 step.

As a consequence, the chip size can be reduced of a factor 2 respect to the size of the present type of programmable voltage standard .

5.3 Advantages of high characteristic voltage: b) Operation of voltage references above 4.2 K

The high value of V_c at 4.2 K is also a tool for operation of the arrays above 4.2 K, since the scaling of the electrical parameters with temperature, still allows to use them at higher temperatures.

However a further requirement to the junctions is set by the temperature stability of the electrical parameters, especially above 4.2 K. For a superconductive junctions in fact several non-equilibrium phenomena arise when the operating temperature approaches T_c

The stability of V_c mainly depends from the critical current dependence on temperature, since the junction resistance is almost constant in that temperature range for the majority of metallic and insulating barriers. In particular an evaluation of the temperature stability can be made considering the temperature derivative of the current, normalized to the value at $T = 0$, vs. the incremental temperature, normalized to Tc: $d(I_c(T) \, / \, I_c(0)) \, / \, d(T \, / \, T_c)$

In figure 11 the relation is plotted for different type of Josephson junctions.

For hysteretic SIS junctions, whose temperature behavior is described according to the Ambegaokar and Baratoff theory, curve AB, a strong change is observed especially above 4.2. On the contrary for SNS junction, described by a Kulik and Omelianchuk formulation, curve KO, a less pronounced dependence can be observed, but it must not be ignored that in the majority of case these junctions have quite low Vc values already at 4.2 K [63].

In the figure are also shown three calculated curves for SNIS junctions, where by changing the N/S relative thickness in the Nb/Al first electrode, through the parameter of the parameter γ_{eff}, the temperature dependence can be properly tailored.

In particular, the dotted curve, corresponding to a thickness of the aluminum film about 100 nm, shows a a very small change from 0.7 T/Tc.

Thus, it is possible to engineer the temperature stability of 4-layered structure by increasing the thickness of the different layers and changing, as a result, the shape of supercurrent-vs-temperature characteristics [64].

Experiments on single junctions and small array of 10 junctions demonstrated the operation up to temperatures near junction Tc [65].
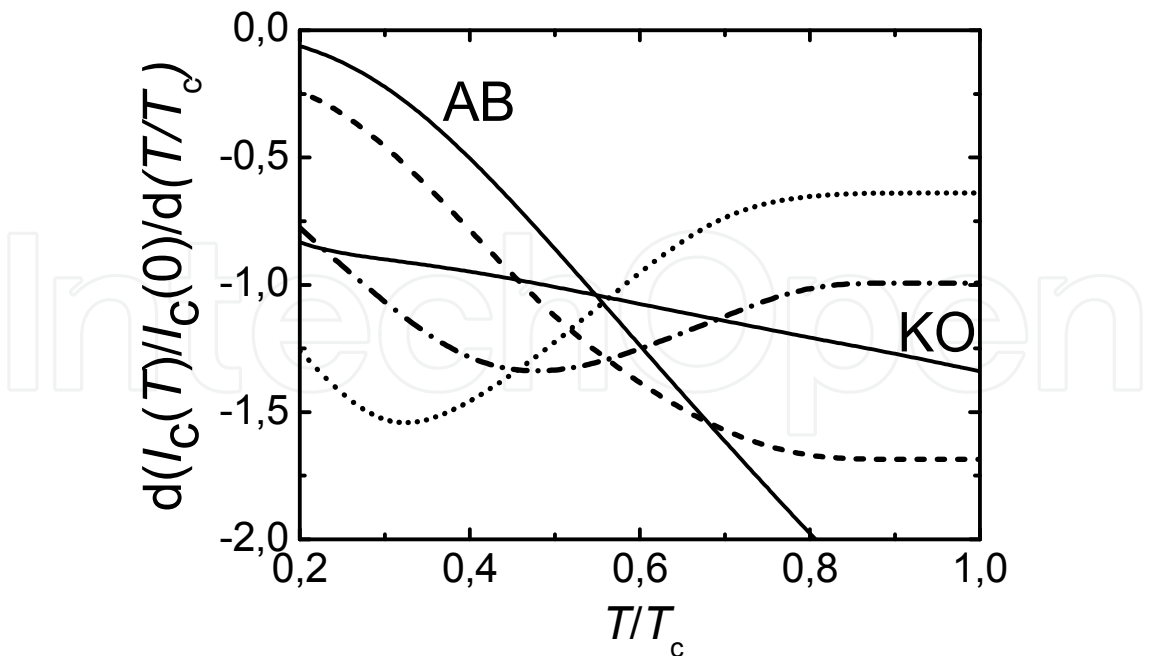
Fig. 11. Normalized temperature derivative of the critical supercurrent calculated for conventional SIS (the AB curve) and SNS (the curve KO) junctions and the SNIS devices with γ_{eff} = 2, 10, and 20 (dashed, dashed-dotted, and dotted lines respectively).
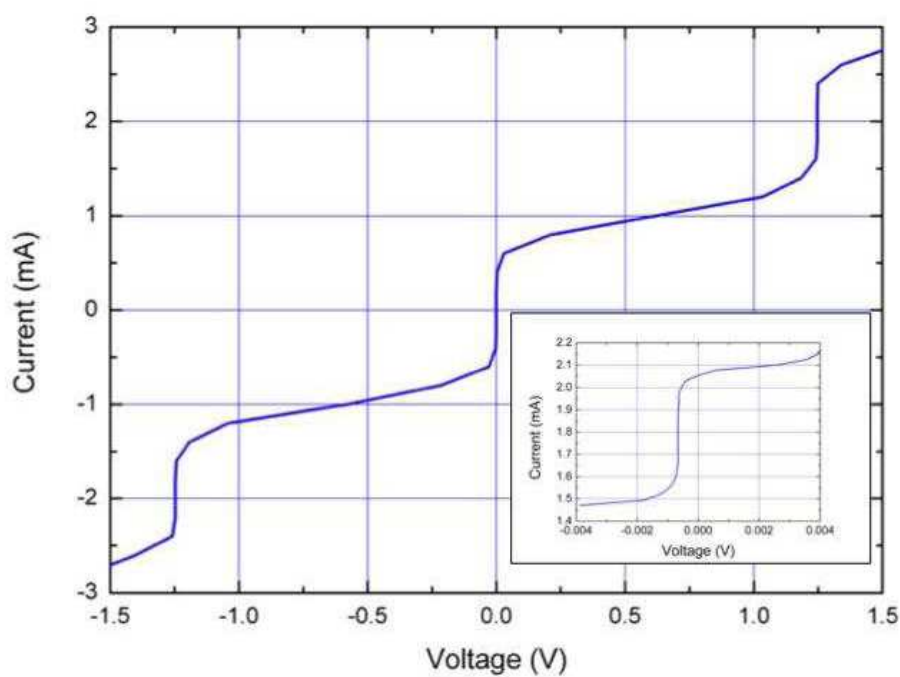

Fig. 12. Voltage step at 1.25 V measured at T = 6.3 K on a binary-divided array of 8192 JJ. The inset shows detail of the quantized step, 0.25 mA wide.

Of course when using more complex circuits, as the programmable arrays described above, non-uniformities in the fabrication and in the distribution of the microwave signal reduce the maximum temperature, especially if the device is operated in gas.

Figure 12 show steps at 1.25 V, 0.25 mA of a binary array, measured at T = 6.3 K Wider steps, 0.5 to 1 mA, have been measured up to 7.2 K on subsections of the arrays.

It is expected that the results will be improved by improving fabrication homogeneity, microwave signal coupling and using a cryocooler setup.

6. Conclusions

The extension of DC Josephson Voltage standard to AC has led to the development of different type of circuits, according to the specific application, which have been analyzed in section 2.

In section 3 a comparison of different types of overdamped junctions developed for the large circuits needed by the AC extension of Josephson voltage standard has shown advantages and disadvantages of a certain electrode configuration or material. In order to achieve the desired noise immunity of the quantized voltage levels, the junctions must maximize both Jc and Vc this last issue being also useful for applications where the highest speed of the Josephson circuits is expected. And these issues must be attained using a tolerable degree of technological effort, also in terms of allowable integration. In fact, in order to have a widespread development in the world laboratories for these circuits, neither the number of junctions should be increased nor the size reduced beyond a certain limit. All together, these issues are not solved by any of the junctions reported in this analysis, even if some of the described technologies had achieved sound results.

In section 4 future developments of these circuits have been considered with attention to the problems to be solved.

Waiting for a further development of superconductive junction technology integration, and the use of high temperature materials, the employ of high characteristic voltage junctions is presented as a possible route for extending the performances and applications of Josephson voltage standard not only in fundamental metrology but also for laboratory instrumentation.

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