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Silicon Oxide Films Containing Amorphous or Crystalline Silicon Nanodots for Device Applications

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1. Introduction

The impressive recent growth of the portable systems market (mobile PC, MP3 audio player, digital camera, mobile phones, hybrid hard disks, etc.), has increased the interest of the semiconductor industry on non-volatile memory (NVM) technologies. The demand for mobility applications is the main reason for the fast development of NVM technologies and products. Therefore lower power consumption, lower system costs, ever higher capacity and system performance are required. The conventional floating-gate memories satisfy these needs at present but the scaling of these memories is becoming increasingly difficult primarily because reliability problems limiting the bottom (tunnel) oxide to a thickness of around 10 nm.

The application of discrete storage nodes in conventional non-volatile memory has been considered as one of the key items for ensuring a better reliability of the non-volatile memory and to increase scaling. The basic idea is to replace the floating gate (FG) of NVMs by many discrete trapping centers. The most important effect of the localized trapping is the fact that a single leakage path due to a defect (intrinsic or created during the operation by the applied write/erase electric field) in the oxide can only discharge a few storage nodes. In the devices with discrete storage nodes, the storage medium consists either of natural traps, normally in a nitride layer (Eitan et al., 2000; Minami et al., 1994), or of semiconductor nanocrystals (Tiwari et al., 1995).

Two kinds of semiconductor structures containing nanocrystals are studied recently for non-volatile memory purposes. Ones of them are metal-insulator-semiconductor (MIS) structures containing semiconductor nanocrystals in the insulator layer. In such structures nanocrystals serve as charge storage media replacing the floating gate in conventional memory field effect transistors (FETs) (Horváth&Basa, 2009; Lombardo et al., 2004; Steimle et al., 2007; Tiwari et al., 1995). The other ones are the phase-change memory structures (which are not subject of consideration in this chapter), where the channel layer itself is

switched between nanocrystalline and amorphous state with high and low conductivity, respectively (Hudgens&Johnson, 2004).

Since MIS structures containing semiconductor nanocrystals are less vulnerable to charge loss through isolated defects in the bottom oxide they provide opportunity for reduction of the size of the memory device and for operation at lower voltages compared to continuous floating gate flash devices. They use processes of direct charge tunnelling to the nanocrystals, Fowler-Nordheim tunnelling or channel hot electron (CHE) injection. The result is capturing of one or a few electrons in a potential well with well defined spatial position (Tsoukalas et al., 2005). The captured electron controls the current through a conducting channel situated close to the position of the captured electron and thus the nanocrystal plays the role of a floating gate. The electron stays in the nanocrystal for a certain time, which determines the duration of the "memory" effect in the device (i.e. the retention time).

At room temperature the memory effect, i.e. the charge capture in nanocrystals, manifests itself as a well defined shift of the capacitance-voltage (C-V) dependence of MIS structure (as a result of its charging or discharging) and as a change of the threshold voltage, called memory window, of the transistors fabricated with the same gate dielectric. The reduced density of states in the NCs restricts the states available for electrons and holes to tunnel to. Besides the Coulomb blockade effect arises from a larger electrostatic energy associated with placing a charged particle onto a rather small capacitance. Due to the both effects less charged carriers are used in the operation of the device that results in low-power operation without sacrificing speed. In addition, because the charge loss through lateral paths is suppressed the constraints on electrical contact isolation can be relaxed which permits thinner oxides and therefore lower voltage/power operation. An important advantage of the NVMs containing NCs is that they have shown a superior endurance at increased temperatures than the standard polysilicon floating gate NVMs and those using charge storage in natural traps. More detailed information on the principles of operation and non-volatile memories containing semiconductor or metal nanoparticles in various matrices can be found in a number of recent reviews [see for example (Horváth&Basa, 2009; Steimle et al., 2007; Tsoukalas et al., 2005).

The attention in this chapter is addressed to properties of memory structures in which the standard floating gate is replaced by crystalline or amorphous silicon nanoparticles (NPs), as storage nodes, separated by silicon oxide. The insulator of such MIS structure normally consists of three layers (Dimitrakis et al., 2005; Tiwari et al., 1996; Tsoi et al., 2005): (i) ultra thin tunnel SiO_2 layer grown on the crystalline Si wafer followed by (ii) composite layer of Si nanocrystals (NCs) in a SiO_2 matrix (nc-Si- SiO_2) and (iii) control SiO_2 layer, which insulates the NCs from the control gate. The middle nc-Si-SiO_2 layer has been mostly prepared by ion implantation of Si in thermal SiO_2 and subsequent annealing at high temperature ($\geq 900\ ^0C$) (Normand et al., 2004 and references therein; Carreras et al., 2005; Ng et al., 2006a), by applying some chemical vapor deposition (CVD) technique for Si nanocrystals fabrication and subsequent CVD deposition of silicon dioxide (Lombardo et al., 2004; Oda et al., 2005; Rao et al., 2004), by deposition of a ultra thin amorphous Si layer and a subsequent oxidation of this layer at a high temperature (Kouvatsos et al., 2003; Tsoi et al., 2005) or by thermal evaporation of SiO powder under selected oxygen pressure (Lu et al., 2005, 2006).

The principal materials science aspects of the fabrication of two dimentional arrays of Si nanocrystals in thin SiO_2 layers and at tunable distances from the interface with the Si substrate have been considered in Ref. (Claverie et al., 2006). Below we mention only few

interesting points in this respect. The effect of annealing temperature and gas ambient on the properties of nc-Si-SiO_2 has been studied in Ref. (Ioannou-Sougleridis et al., 2003). It has been ascertained that the samples annealed at 900 ^oC show significant memory effect which is a result of electron or hole capture in defect states with approximately same density for both types of carriers (~ $2x10^{12}$ cm^{-2}). The hydrogen annealing has shown that the main part of the defect states in these samples is due to unsaturated bonds at the nc-Si/SiO_2 interface. In the samples annealed at 1100 ^oC, the charge capturing does not depend substantially on the hydrogen annealing, which is explained assuming much lower concentration of defect states (~ $2.5x10^{11}$ cm^{-2}). In another study (Yu et al., 2003) dependence of the charge effect on the thickness of the nc-Si-SiO_2 layer is reported. Depth profiling of the charging effect of the nc-Si has revealed (Liu et al., 2006) that the charging effect decreases with the increase of nc-Si concentration and vanishes when a densely stacked nanocrystal layer is formed. The phenomenon is attributed to charge diffusion among the nanocrystals.

The impact of programming mechanisms Fowler-Nordheim/Fowler-Nordheim or channel hot electron/Fowler-Nordheim on the Performance and Reliability of NVM devices based on Si anocrystals has been explored at both room temperature and 85 ^0C in Ref. (Ng et al., 2006b). It has been shown that the channel hot electron programming has a larger memory window, a better endurance, and a longer retention time as compared to Fowler-Nordheim programming. Moreover, the channel hot electron programming yields less stress-induced leakage current than the Fowler-Nordheim programming, suggesting that it produces less damage to the gate oxide and the oxide/Si interface.

It has been demonstrated that the application of low-energy ion beam implantation has resulted in preparation of very promising NVMs with Si nanocrystals (Horváth&Basa, 2009; Tsoukalas et al., 2005) since it allows (Normand et al., 1998) to avoid wide distribution of NCs through the oxide layer and to obtain NCs at a specific location into the host matrix. It has been demonstrated that memory cells fabricated following a procedure including implantation with 1 keV silicon ions to a dose of 2×10^{16} cm^{-2} and subsequent annealing at 950 ^0C for 30 min in N_2 + 1.5% O_2 (Normand et al., 2003; Tsoukalas et al., 2005) displayed more than 10^6 write/erase ± 9 V/10 ms cycles without observation of gate degradation. The long time extrapolation of the data retention characteristics at two different temperatures, 25 and 85 ^0C, after + 9 V/− 9 V 10 ms pulses has shown that those Si NC memory device could achieve 10 years data retention at 85 ^0C. The memory transistors produced displayed about 2 V memory window for the write/erase pulses of ± 9 V, 10 ms.

Low-energy implantation (at 2 keV) has also been applied (Ng et al., 2006a) for preparation of MIS structures in which the tunneling oxide thickness was 3 nm or 7 nm for realization of direct or Fowler-Nordheim tunneling during the charging process. For direct tunneling a memory window width of about 1 V was obtained using charging pulses of ± 12 V, 1 μs. For Fowler-Nordheim tunneling the memory window width was about 0.5 V using charging pulses of ± 12 V, 1 ms. Thus, it has been shown that devices with a thicker tunnel layer required longer charging pulses, and they degraded faster, as well, but the extrapolated for 10 years memory window width at 85 ^0C was about 0.3 V for both type of structures.

Successful preparation of Si nanocrystals for memory applications has been also realized by chemical vapour deposition. Devices for non-volatile purposes were produced using 3.8-5.0 nm thick tunnel oxide (Rao et al., 2004) and a threshold voltage shift of ~ 1.5 V has

been obtained by voltage pulses of 14 V, 100 μs or 12 V, 1 ms. Retention characteristics have also been very good, but the memory window shifted slightly with increasing number of write/erase cycles.

Recently tunnel barrier engineering has been suggested (Jung&Cho, 2008) as a promising way for tunnel oxide scaling. It uses multiple dielectric stacks to enhance field-sensitivity and thus to allow for shorter writing/erasing times and/or lower operating voltages than single SiO_2 tunnel oxide without altering the ten-year data retention constraint. Experiments on memory structures containing one-three Si NC layers prepared by evaporation of SiO powder and layer by layer growth (Lu et al., 2005, 2006) have shown that in structures with two or three NC layers two or three different saturation voltages were obtained with increasing bias related to charge injection to and capture at the first, second, or third NC layer (Lu et al., 2005). Charge captured in the first layer yielded a memory window width of about 2.5 V, charge captured in the second NC layer yielded an additional flat-band voltage shift of about 2.5 V, while charge captured in the third layer yielded an additional shift of about 1.5 V. It has been observed that the multilayer storage in memory structures prepared by different deposition methods yielded very good retention, as well (Han et al., 2007; Lu et al., 2005; Nassiopoulou et al., 2009).

For decades the radiation effects have been a serious problem for electronics used in defense and space systems and therefore the study of the radiation effects on metal-oxide-semiconductor (MOS) based devices, including MOS capacitors, has been an active research area over the past decades. An advantage of the nanocrystalline NVMs is their higher tolerance to radiation ionization which can result in memory applications in avionics, nuclear power stations, nuclear waste disposal sites, military, medicine etc. (Gerardi et al., 2011). Besides, MOS structures and transistors with nanocrystals are developed for dosimeter purposes.

Generally MOS structures pose high spatial resolution and their production is compatible with the technology used in the microelectronic industry. Two types MOS transistors are used for detecting of ionizing radiation: radiation-sensing field effect transistor (RADFET) (Buehler et al., 1993; Holmes-Siedle&Adams, 1986; Hughes et al., 1988; Price et al., 2004; Ramani et al., 1997; Stanic et al., 2005) and floating gate transistors (Edgecock et al., 2009; Kassabov et al., 1991; McNulty et al., 2006; Scheick et al., 1998, 1999; Tarr et al., 1998, 2004). Normally the RADFET is a p-channel MOS transistor whose SiO_2 gate is grown at specific conditions and its thickness is around 1 μm (Sarrabayrouse, 1991). A part of the charge carriers generated by the ionizing radiation is trapped in the oxide and the integrated irradiation dose is detected as a change in the transistor threshold voltage. To ensure good sensitivity of these dosimeters an electric field is normally applied on the control gated during irradiation. The radiation induces changes are irreversible and therefore RADFET dosimeters are for a single use only. At the floating gate dosimeter before irradiation the floating gate is charged by electron injection from the control gate (Kassabov et al., 1991; Tarr et al., 1998) or substrate (Martin et al., 2001) and this creates an electrical field in the oxide layer. Therefore no application of external electric field is necessary during irradiation which makes their application more convenient. In addition, the radiation induces changes which are reversible and multiple usage of those dosimeters is possible. Recently, experiments have been performed (Aktag et al., 2010) on introduction of Ge nanocrystals in the oxide layer of floating gate dosimeters. It has been

observed that the presence of nanocrystals improves the radiation resistance of detectors but decreases their sensitivity.

In this chapter a review is made of the most important results obtained during the last five years by the authors and their collaborators in the field of development of metal-insulator-silicon structures with dielectric film containing amorphous or crystalline silicon nanoparticles, which are suitable for non-volatile memory and radiation applications. **In the introductory part** a brief review of the results of other research groups on MIS structures containing Si nanoparticles for non-volatile memory and detector applications has been made. **The next second part** gives information about the preparation of SiO_x films of different compositions and the annealing conditions used for the growth of amorphous (na-Si) and crystalline (nc-Si) silicon nanoparticles. Infrared absorption and Rutherford backscattering data give information on the oxygen content, while X-ray Diffraction and Reflectivity, X-ray Photoelectron Spectroscopy, Transmission Electron Microscopy, Atomic Force Microscopy, Infra Red Transmission and, Raman Scattering spectroscopy and Spectroscopic Ellipsometry data give information about the effect of furnace annealing on the properties of the SiO_x films. **In the third part** newly developed techniques for preparation of MIS structures containing amorphous and crystalline Si nanoparticles suitable for non-volatile memory application are described. The fabricated MIS structures are characterized by high frequency (100 kHz and 1 MHz) capacitance/conductance-voltage (C/G-V) measurements at applied dc voltage varying within a voltage range ± 15 V. **The last fourth part** presents recent data on preparation of MIS structures containing Si nanocrystals and their response to γ-radiation.

2. Preparation of SiO_x films and growth of amorphous and crystalline Si nanoparticles

It is well known that the film preparation and processing are very important for the performance of the MIS structures and devices with nanocrystals. They determine the film composition, which in the case of Si NP growth by SiO_x film annealing is of critical importance for the nanocrystal size, the filling of the oxides matrix with NCs (NC filling factor), the quality of the interface with the Si substrate, etc. Therefore this part of the chapter describes results from a thorough characterization of the SiO_x films. This information is important since these films are an essential part of the two(multi)layer insulator in the MIS structures described in Parts 3 and 4; they are the layers that contain Si NPs.

2.1 Preparation of SiO_x films

SiO_x layers with an initial composition of $x = 1.1$ and 1.3 and thickness of ~ 15 nm were prepared by thermal evaporation of SiO at a vacuum of 1×10^{-3} Pa on n- or p-type (100) c-Si (4 - 6 and 1 Ω×cm, respectively) substrates maintained at room temperature. The SiO evaporation was carried out from a tantalum crucible provided with a molybdenum cylindrical screen and thus evaporation in a quasi-closed volume takes place (Nesheva et al., 2003). The film thickness and deposition rate were monitored by a quartz microbalance system. Before the films deposition the silicon wafers were cleaned chemically using a standard procedure for the microelectronics industry. For Raman scattering, infra red and optical transmission measurements SiO_x films with same compositions but with thickness of

0.2 and 1 μm were deposited on c-Si and quartz substrates. The film composition has been determined by means of Rutherford Back Scattering (Nesheva et al., 2003).

All as-deposited layers were annealed at 250 ^{0}C for 30 min in an Ar atmosphere to keep them stable at room conditions. In order to grow Si nanoparticles an additional annealing at 700 ^{0}C in Ar or 1000 ^{0}C in N_2 atmosphere for 60 min was carried out.

2.2 Si nanoparticle growth, oxygen matrix densification, interface quality

The films annealed at high temperatures as well as control ones (annealed at 250 ^{0}C) were characterized by Transmission Electron Microscopy (TEM), Raman Spectroscopy, X-ray Diffraction (XRD) and Reflectivity (XRR), X-ray Photoelectron Spectroscopy (XPS) and Atomic Force Microscopy (AFM). Lattice-resolution TEM was carried out at 200 kV with a JEOL 2100 with a point-to-point resolution of 0.22 nm in the TEM mode. XRD/XRR measurements were performed using Philips X´pert Diffractometer (Cu Kα source), XPS analysis by Kratos Axis Ultra spectrometer (Al Kα (1486.6 eV) X-ray source), Raman spectra using Witec α-SNOM and AFM micrographs were taken by Asylum Research Microscope in tapping mode. Cross-sectional TEM (XTEM) samples were also prepared by gluing film-to-film two Si wafers and then cutting vertical sections which were first mechanically thinned to a thickness of 25 μm. Final thinning to electron transparency was accomplished by ion milling at very low angles (15° - 10°) from both cross-sectional sides. Optical and infra red transmission measurements were also carried out by means of Cary 5E, Perkin-Elmer Spectrum One FTIR and Bruker Vertex 70 spectrophotometers, respectively.

Raman scattering spectra of SiO_x films with thickness of 1 μm deposited on quartz substrates and annealed at 700 ^{0}C and 1000 ^{0}C for 60 min are shown in Fig.1. A broad band centered at ~ 470 cm^{-1} is observed in the spectrum of the film annealed at 700 ^{0}C. It is typical for amorphous silicon (Iqbal&Veprek, 1982; Nesheva et al., 2002) and its observation can be

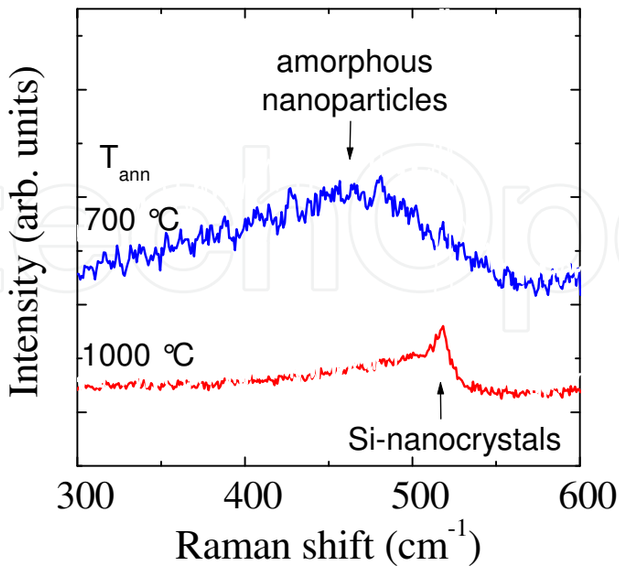


Fig. 1. Raman scattering spectra of SiO_x films (1 μm thick) deposited on quartz substrates and annealed at 700 ^{0}C or 1000 ^{0}C.

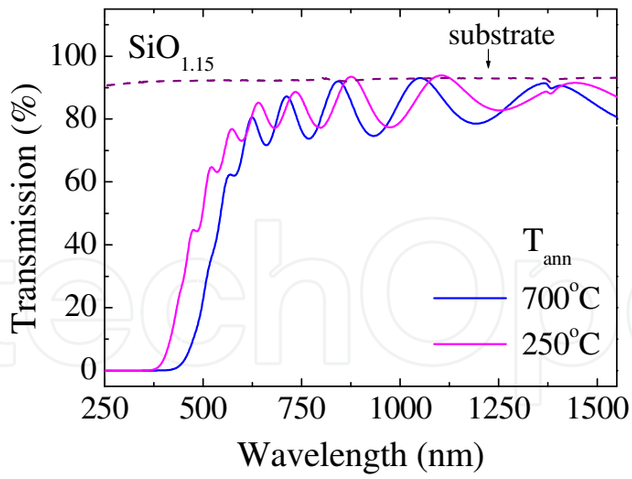


Fig. 2. Optical transmission spectra of two $SiO_{1.15}$ layers annealed at 250 and 700 ^{0}C. A red shift is observed upon annealing at 700 ^{0}C.

related to existence of pure amorphous silicon phase in these films. Such band is not seen in the spectrum of the film on quartz substrate annealed at 1000 ^{0}C, which confirms that the band at 470 cm^{-1} is related to a-Si phase rather than to light scattering from the SiO_x matrix or SiO_2 substrate. An asymmetric band peaked at ~ 518 cm^{-1} is observed in the spectrum of the film annealed at 1000 ^{0}C, which cannot originate from the quartz substrate and its appearance is an evidence for the existence of Si nanocrystals (Iqbal&Veprek, 1982).

The existence of pure silicon phase in the films annealed at 700 ^{0}C has also been confirmed by optical transmission measurements carried out on SiO_x layers on quartz substrates. Figure 2 shows optical transmission spectra of a sample with $x = 1.15$ measured before and after annealing at 700 ^{0}C. It is seen that the annealing causes a "red" shift of the spectrum. Since the increase of the oxygen content in the matrix should result in a "blue" shift, the observed "red" shift is an indication that absorption in a pure silicon phase takes place. A value of 2.64 eV has been obtained for the optical band gap of the amorphous Si particles grown upon annealing of samples with $x = 1.15$ at 700 ^{0}C and a value of 2.1 nm has been estimated for the average diameter of the largest amorphous Si NPs in our films (Nesheva et al., 2008).

Figures 3 (a) and (b) show XTEM micrographs of a control (250 ^{0}C) and an annealed at 1000 ^{0}C sample with $x = 1.3$ and thickness of 15 nm. Figure 3 (a) exhibits an amorphous structure and a nearly atomically flat interface, while Figure 3 (b) exhibits randomly oriented nanocrystals with a diameter of ~ 4-5 nm and an increase of the roughness of the c-Si wafer/dielectric interface. The NCs are positioned closer to the c-Si wafer than to the top SiO_x surface and are separated from the c-Si/SiO_x interface by an amorphous region with thickness ≥ 3 nm. The thicknesses of the SiO_x layers determined are of 16.2 nm and 13.8 nm for the control and annealed sample, respectively. While the thickness of the control film is close to the one set during the deposition, film densification of about 15% has been concluded in result of the annealing at 1000 ^{0}C for 60 min.

The XRD results of control and 1000 ^{0}C annealed samples obtained in the 2Θ/Ω scans show (Fig. 4) only two peaks at 33^o and 68^o corresponding to diffraction from the crystalline Si

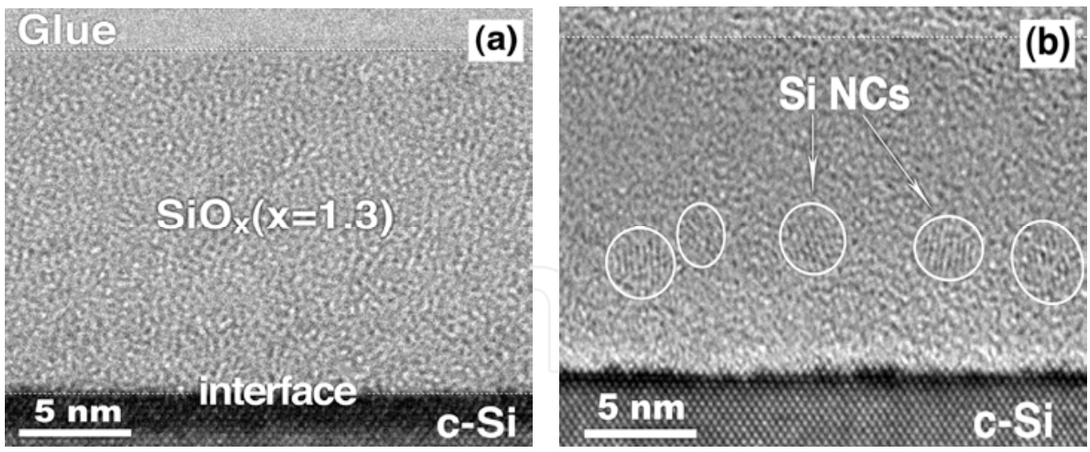


Fig. 3. Cross-sectional (XTEM) micrographs of a control sample (a) and an annealed at 1000 ^{0}C sample with nanocrystals in a dielectric matrix and rougher interface (b).

(100) substrate. No contribution due to the nanocrystals is observed because of the random NCs orientation, as revealed by TEM. The XRR spectra of a control and annealed at 700 and 1000 ^{0}C samples are shown in Fig. 5. The well defined interference fringes in the spectrum of the control sample (curve 1) imply an excellent interface between the dielectric and the c-Si wafer. With the increase of the annealing temperature from 700 ^{0}C to 1000 ^{0}C the amplitude of the interference fringes decreases (curves 2 and 3) indicating an increase of the interface roughness. The obtained results are in good agreement with the XTEM ones. The XRR technique was also applied to determine the thicknesses of the SiO_x layers. Values of 16.8 nm for the control and 16.9 and 14.8 nm for the annealed at 700 ^{0}C and 1000 ^{0}C layers, respectively, have been obtained. The errors in the thicknesses of the control and 1000 ^{0}C annealed samples are 3.7 and 7.2 %, respectively. Again, the sample annealed at 1000 ^{0}C show a small decrease of the initial thickness while the thickness of the film annealed at 700 ^{0}C is practically constant. This observation can be understood if assuming that at 700 ^{0}C the disorder of the substoichiometric SiO_x matrix is still rather high.

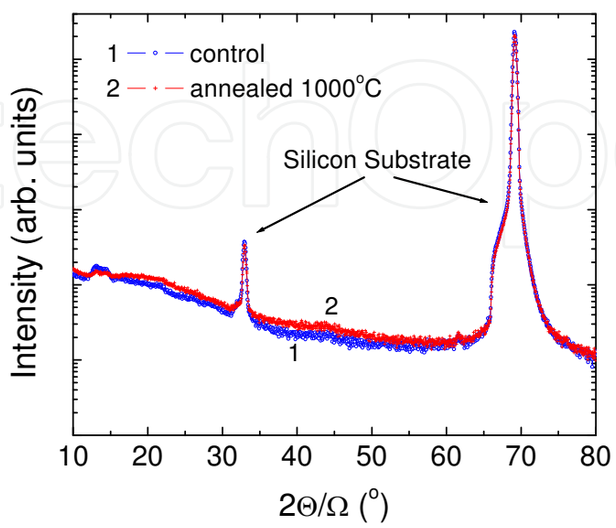


Fig. 4. 2Θ/Ω scans of a control (1) and annealed at 1000 ^{0}C for 60 min (2) samples.

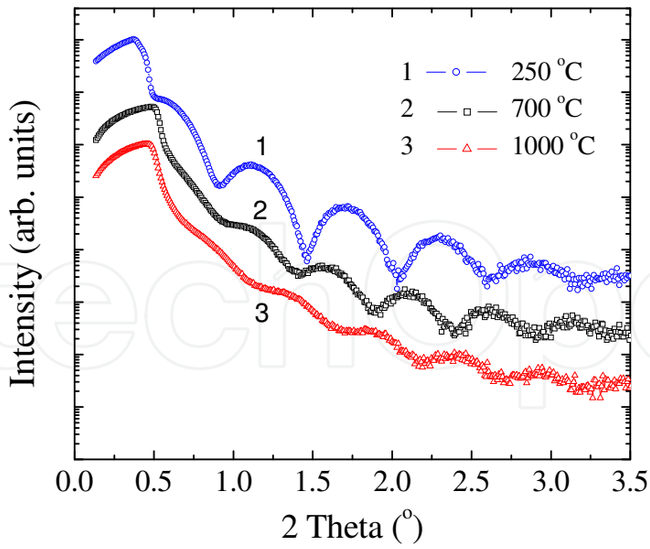


Fig. 5. XRR spectra of a control (1) and annealed at 700 (2) and 1000 ^{0}C (3) samples.

XPS was used to obtain further information about the structure and chemical composition of the 15 nm films. In Figs 6 and 7 spectra of the Si 2p core level of control and annealed layers with expected $x = 1.3$ at incidence angles of 30^o and 90^o, respectively, are presented. The Gaussian fitting curves are also shown. The main peak in the spectrum of the control sample at both angles (Figs. 6 (a) and 7 (a)) is positioned at 102.4 eV and corresponds to a SiO_x film with $x = 1.35$ (Alfonsetti et al., 1993), a value that is close to the composition set by the deposition conditions. After deconvolution three Gaussians peaked at 103.6, 102.4 and 100.1 eV were resolved. The peaks at 103.6 and 102.4 eV are attributed to Si-O bonds in pure SiO_2 and in Si_2O_3 compounds, respectively, while the shoulder at lower binding energy could be superposition of signals resulting from Si-O bonds in Si_2O suboxide and Si-Si bonds in silicon, having binding energies close to each other, 100.7 eV and 99.8 eV, respectively (Alfonsetti et al., 1993). In all spectra of the annealed films (Figs. 6 (b), (c), 7 (b), (c)) a well defined peak positioned at 103.8 eV corresponding to stoichiometric SiO_2 is present. This finding seems to be in disagreement with our previous results about the matrix composition after 700 ^{0}C annealing obtained by IR spectroscopy (Donchev et al., Nesheva et al., 2003, 2008) but the IR measurements were carried out on thicker films (~ 0.2 μm) and give information about the volume properties of the films. The XPS signal originates from a region with thickness ≤ 10 nm and one can conclude that most likely the Si nanoscrystals close to the top surface get transformed into SiO_2 to a thickness of ~ 5–6 nm, due to native oxide formation after exposure to air, as confirmed by XTEM (Fig. 3 (b)). However, there is a substantial difference in the amplitude of the peak corresponding to pure Si phase (the doublet Si 2p 3/2, Si 2p 1/2 with binding energies of 99.4 and 99.9 eV) in the spectra of the layer annealed at 1000 ^{0}C when measured at 30^o and 90^o (Figs. 6 (c), 7 (c)). At angle of incidence of 30^o the chemical composition of the first ~ 3 nm below the film surface is determined, while in the case of normal incidence the obtained information is for thicker region (~ 10 nm). The observed difference in the Si peak amplitude can be understood keeping in mind that the nanocrystals have a diameter of ~ 4-5 nm, they are positioned closer to the c-Si/dielectric interface and the top 6 - 7 nm of the SiO_x film are depleted of NCs (Fig. 3 (b)).

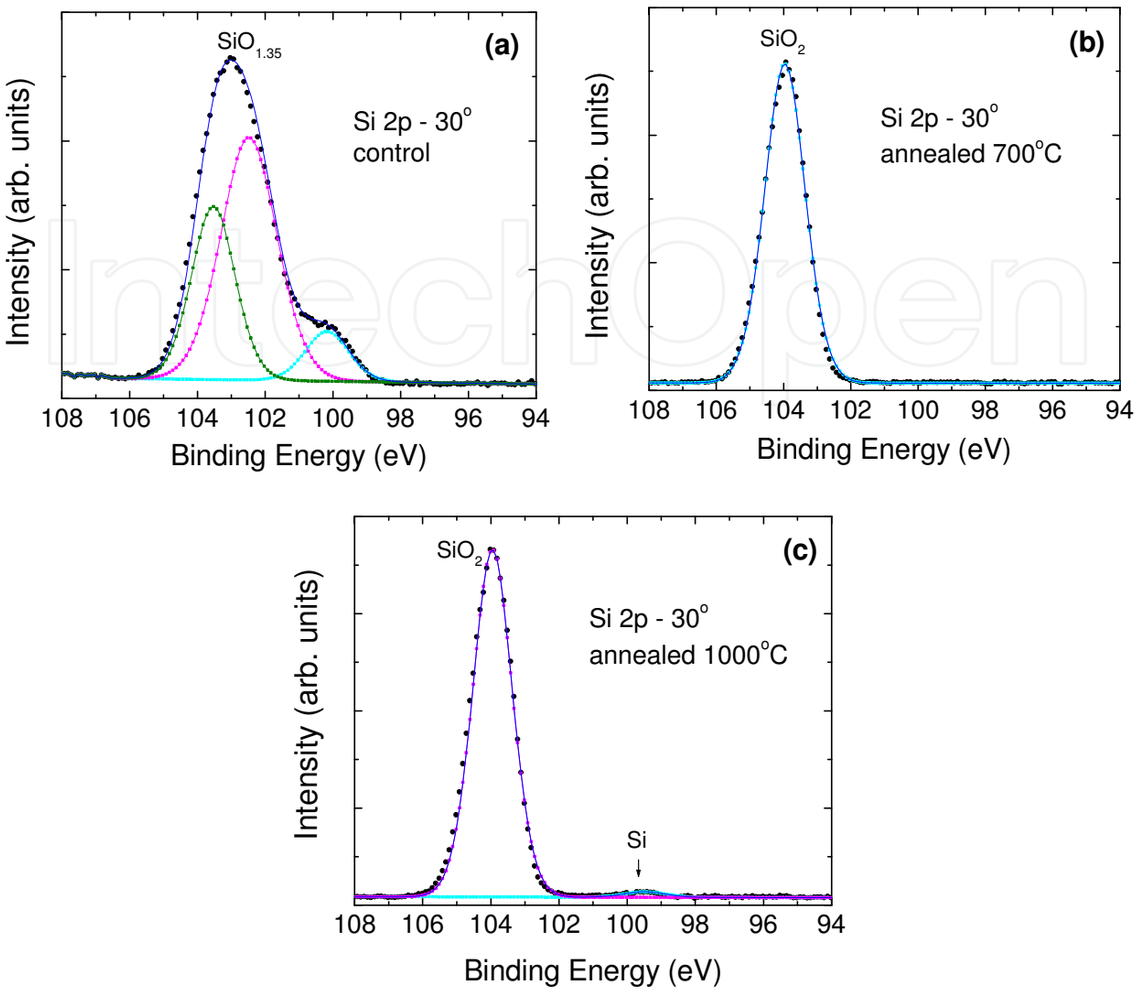


Fig. 6. Si 2p core level spectra of a control (a) and annealed at 700 ^{0}C (b) and 1000 ^{0}C (c) layers measured at 30^o angle of incidence.

In the case of a-Si nanoparticles formed by annealing at 700 ^{0}C the same trend in the spectra measured at 30^o and 90^o is observed. Because of the smaller diameter of the a-Si NPs (~ 2 nm) and probably the same or similar to the nanocrystal spatial distribution the contribution of the Si phase in the XPS spectra is zero (Fig. 5 (b)) or very small at 90^o angle of incidence (Fig. 6 (b)).

The AFM images in Fig. 8 (a)-(c) show the surface morphology of 15 nm SiO_x (x = 1.3) films annealed at 250 ^{0}C, 700 ^{0}C and 1000 ^{0}C, respectively. The scan area was set to 200 × 200 nm and the root mean square roughness (RMS) obtained has a value of 0.164 nm for the control sample (a), 0.258 nm for the 700 ^{0}C (b) and 0.129 nm for the 1000 ^{0}C (c) annealed samples, respectively. The AFM measurements revealed that the 700 ^{0}C annealing leads to an increase of the surface roughness which could be due to incomplete phase separation, while the increase of the annealing temperature to 1000 ^{0}C causes a decrease of the surface roughness and obtaining of smoother films. These results are consistent with the XRR data for the thickness variation after annealing at 700 ^{0}C and 1000 ^{0}C.

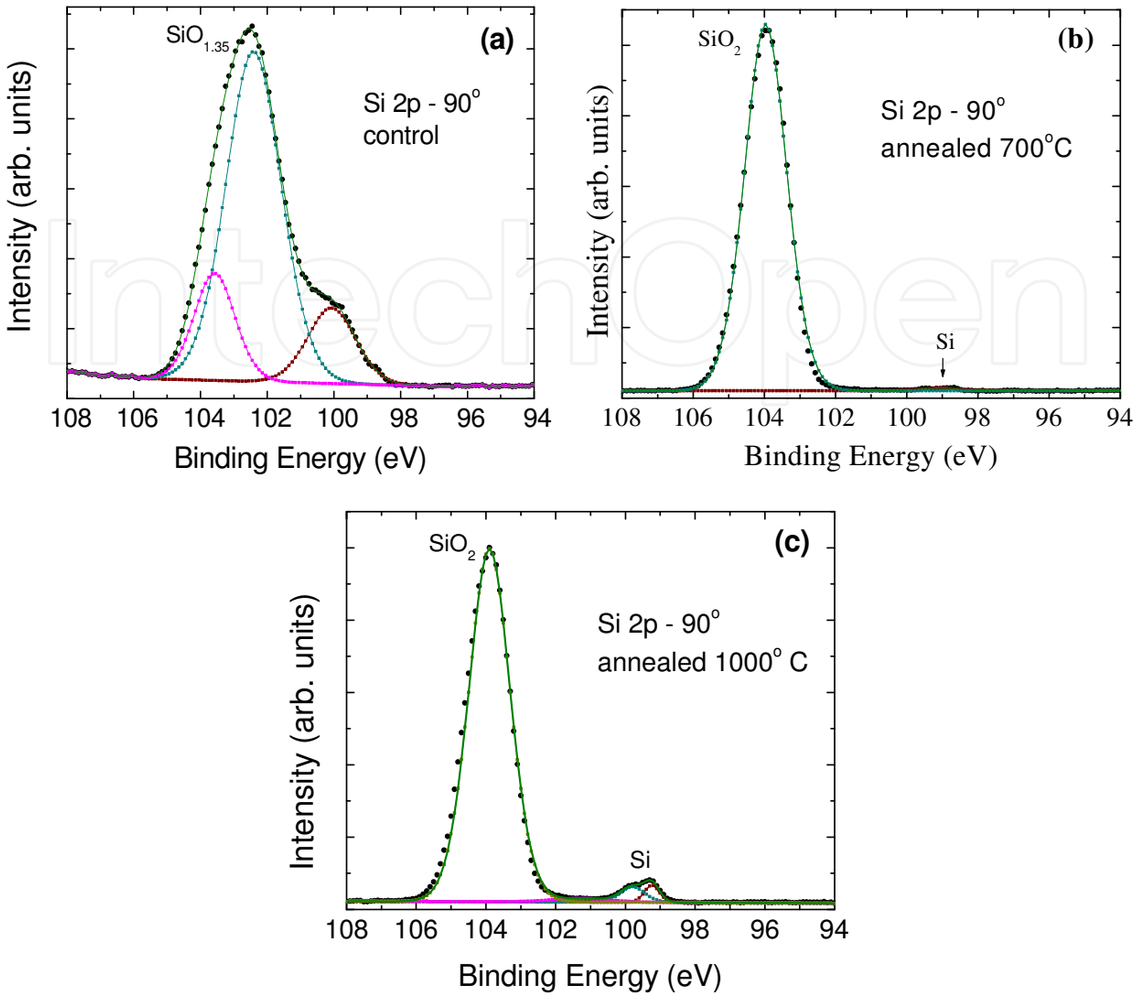


Fig. 7. Si 2p core level spectra of a control (a) and annealed at 700 ^{0}C (b) and 1000 ^{0}C (c) layers measured at 90^o angle of incidence.

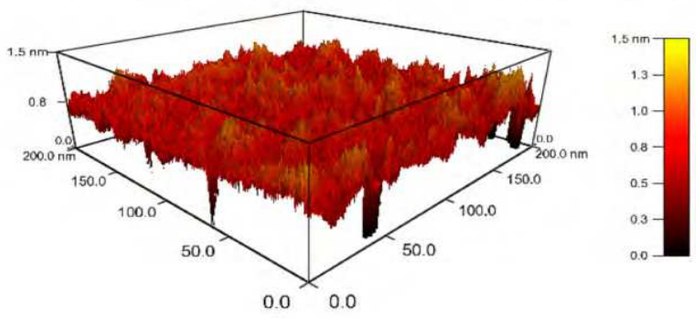
The np-Si-SiO_x layers are composite materials in which the increase of the volume fraction f of the filler (amorphous or crystalline Si NPs) decreases the distance between the nanoparticles and at a certain concentration contact between some adjacent particles may occur and two- or three-dimensional networks of semiconductor nanoparticles may be formed. As mentioned above, network formation is undesired in the case of NVM devices with NPs and therefore the knowledge of f is important.

Assuming that there is no loss of oxygen atoms upon film annealing, the following relation between f and the atomic densities of the initial layer ρ_{SiOx} and pure silicon phase ρ_{Si} has been found (Nesheva et al., 2008):

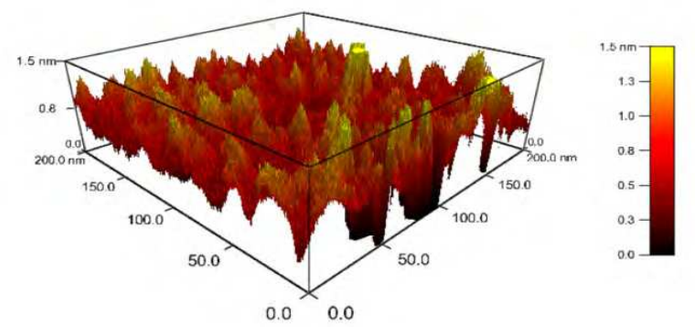
$$f = (\rho_{SiOx} / \rho_{Si})\ (x + 1)^{-1}[1 - (x/y)] \quad (1)$$

where x is the initial oxygen content and y is the oxygen content in the matrix of the annealed layers. Approximate values of f have been obtained using this relation in which the x and y values were determined from the IR transmission data (Donchev et al., in press). It

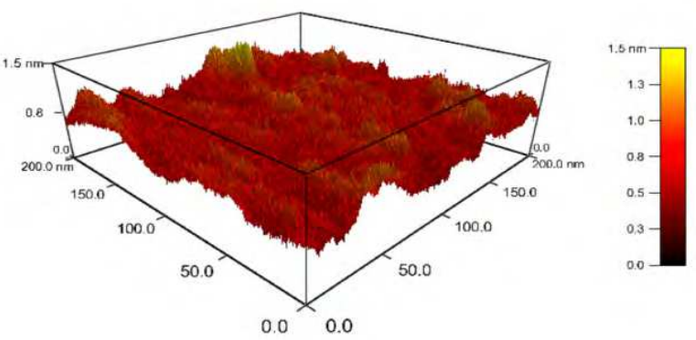
has been obtained that the filling factor changes with the initial oxygen content and for films annealed at 700 ^{0}C and 1000 ^{0}C it varies between 0.05 and 0.2 and 0.07 and 0.28, respectively, when x decreases from 1.7 down to 1.15. The investigation of the carrier transport mechanism in 1 μm thick films have not shown network formation in high temperature annealed films. In the films annealed at 700 ^{0}C_containing a-Si NPs, Poole–Frenkel transport mechanism has been observed while tunneling has been dominating in the films annealed at 1000 ^{0}C (Nesheva et al., 2008).



(a)



(b)



(c)

Fig. 8. AFM images of a control (a) and annealed at 700 ^{0}C (b) and 1000 ^{0}C (c) SiO_x films.

3. MOS structures containing amorphous or crystalline Si nanoparticles for non-volatile memory applications

3.1 Experimental details

The experimental structures used in memory effect study (Nedev et al., 2008a, 2008b; Nesheva et al., 2007) were fabricated by deposition of a SiO_x ($x = 1.15$) layer with a thickness of ~ 15 nm on top of p- or n-type (100) crystalline silicon with resistivity of 1 and 4 - 6 Ω×cm, respectively, followed by radio frequency (r.f.) sputtering of a control silicon dioxide layer with a thickness of ~ 40 nm. Before the film deposition the silicon wafer was cleaned chemically following a standard for the microelectronics procedure. In order to form amorphous or crystalline silicon nanoparticles (with size ~ 5 nm), the structures were annealed for 60 min at 700 ^{0}C in Ar or 1000 ^{0}C in N_2, respectively. The annealing process was used not only for growing of silicon nanoparticles but also to form simultaneously a tunnel SiO_2 close to the interface with the silicon wafer free from nanoparticles (see Fig. 3 (b)). After the annealing Al metallization was carried out through a mask and MOS capacitors with area of ~ 2×10^{-3} cm^2 were formed. Aluminum was also used as a back contact to the crystalline silicon.

The MOS structures were characterized electrically by capacitance/conductance–voltage (C/G-V) measurements using Agilent E4980A Precision LCR Meter controlled by Agilent B1500A Semiconductor Device Analyzer. The polarity of the applied voltage given below concerns the top Al electrode.

3.2 Charge storage

The C-V characteristics of MOS structures with as-deposited SiO_x-SiO_2 gate dielectric have not displayed strong shift in the positive or negative direction, corresponding to charging from the c-Si substrate, when the gate voltage was swept in various ranges. Another important feature of the as-deposited structures is that they lose the trapped charge for several minutes.

Figures 9 (a) and (b) show high frequency C-V hysteresis curves of two annealed samples with amorphous and crystalline silicon nanoparticles, respectively, measured in the range ±11 V (curves 2) and ±15 V (curves 3). In all measurements ± scanning means that the gate bias was first swept from positive to negative voltage and then in the reverse direction. The first measurement on each MOS capacitor (initial curve) was carried out in a narrow enough range (see Fig. 9) in order to avoid charging of the structures. From the capacitance in accumulation a value of about 56 nm for the insulator effective thickness was obtained. This value is in good agreement with the total expected thickness of the deposited layers set by the deposition conditions, i.e. the sum of the SiO_x film thickness (~ 15 nm) and the thickness of the sputtered SiO_2 (~ 40 nm).

For both types of samples the application of a positive voltage shifts the C-V curves to the right, which corresponds to a negative charge trapped in the oxide close to the crystalline silicon wafer, and vice versa a negative bias shifts the curves in the opposite direction. As seen from Fig. 9 (a), (b) the shifted curves are parallel to the initial ones, which indicates uniform distribution of the trapped charge. Therefore one can expect that the charging is mainly due to capturing of electrons/holes in nanoparticles and not in traps in the dielectric,

which could have varying spatial and energetic distributions. The value of the clockwise hysteresis is about 4.3 and 9 V (a) and 5.5 and 9.8 V (b) for ±11 V and ±15 V scanning ranges. The maximum average electric field across the gate dielectric, which corresponds to these scanning ranges, is about 2.0 MV/cm and 2.7 MV/cm, respectively. It is interesting that the C-V characteristics of the a-Si NP structure are much steeper, which indicates lower defect density at the c-Si wafer/silicon oxide interface.

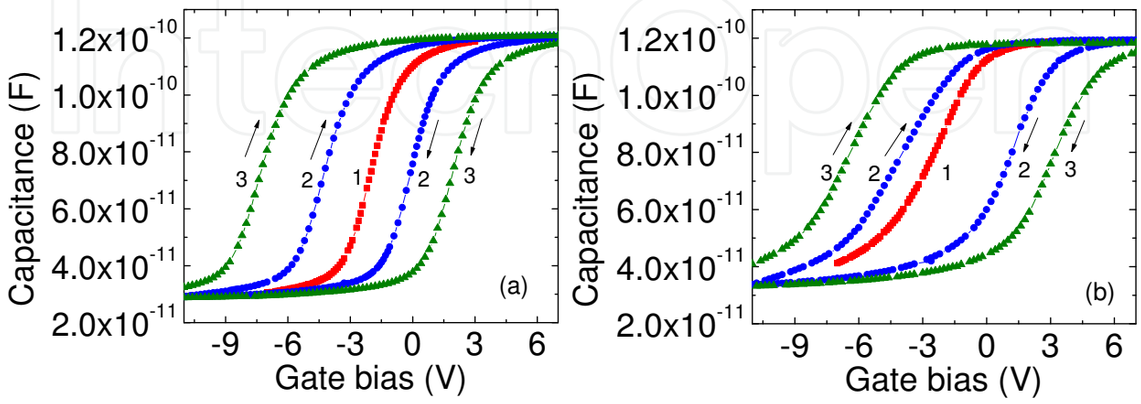


Fig. 9. C-V dependencies measured in the ranges ±11 V (curves 2) and ±15 V (curves 3) at 1 MHz of samples with (a) amorphous (b) crystalline silicon nanoparticles. The initial curve 1 was measured in the range +3 V, -7 V for both (a) and (b) samples.

Figures 10 (a) and (b) show the equivalent parallel conductance G vs. gate bias for the two types of samples. The measurements of G and C were carried out simultaneously in the same voltage scan. The observed shape of the equivalent parallel conductance, with a peak in weak inversion, corresponds to energy loss due to carrier generation and recombination through interface states (Nicollian&Brews, 2002). It is seen that the curves of structures with a-Si NPs are narrower than those of structures with Si NCs. Also the peak of the parallel

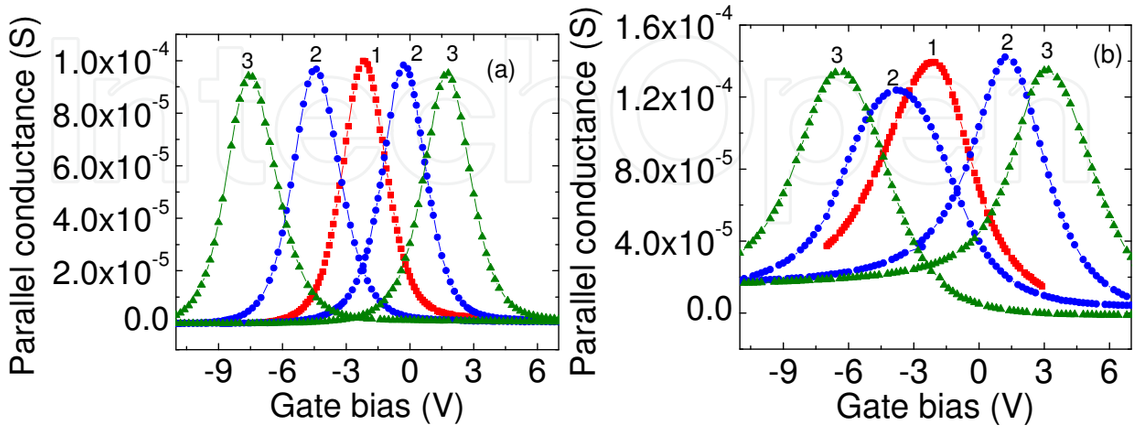


Fig. 10. Equivalent parallel conductance measured at 1 MHz of samples with (a) amorphous and (b) crystalline silicon nanoparticles. The scanning ranges are the same as for the C-V measurements in Fig. 9.

conductance has smaller value (with about 40 %) for the a-Si NP sample. These results confirm the above conclusion that the structures with a-Si NPs have a better SiO_2/c-Si interface than those with Si NCs and are in agreement with the XTEM data (Curiel et al., 2010a, 2010b) where epitaxial overgrowth and increased interface roughness have been found after annealing at 1000 ^{0}C (Fig. 3 (b)).

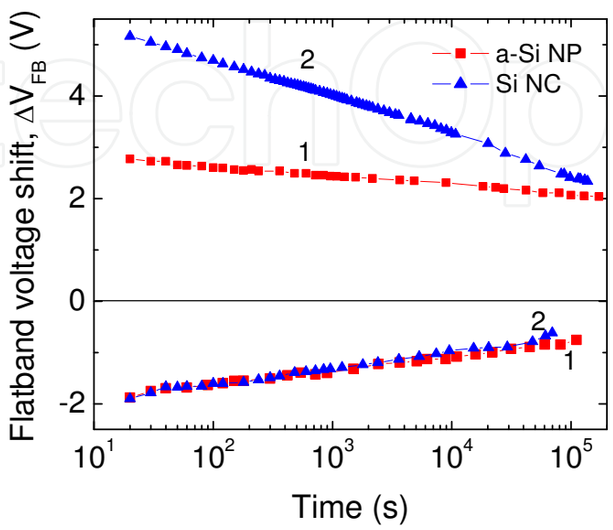


Fig. 11. Retention characteristics of structures with a-Si NPs (curves 1) and nanocrystals (curves 2) after charging structures negatively with voltage ramp sweep up to +12 V or positively with ramp sweep to -12 V.

The retention characteristics of structures with a-Si NPs and Si NCs were obtained by measuring the time-dependent variation of the flatband voltage (Fig. 11), which is proportional to the area density of the trapped charge (Sze, 1981). In both types of structures the charge loss follows approximately a logarithmic law. An essential advantage of the a-Si nanoparticle structures compared to the NC ones is the much slower discharging process observed, especially of trapped electrons. For example, 48 hours after charging with +12 V the MOS structures containing a-Si NPs still have 75% of the initial charge, while the structures with nanocrystals retain about 43%.

4. Radiation dosimeter based on metal-oxide-semiconductor structures with silicon nanocrystals

Figure 12 shows schematically a cross-section of the MOS structures used in dosimetry measurements. An essential difference between the dosimetry structures and the ones used in the memory studies is that an additional SiO_2 layer, 3.9 nm thick, was grown thermally before the deposition of the SiO_x film. The oxidation process was carried out in dry O_2 atmosphere at 850 ^{0}C. Except for the thermal oxidation and the greater thickness of the control oxide, which for dosimeters was 60 nm, the fabrication process was identical with the one used for fabrication of the memory study samples.

The principle of operation of the proposed dosimeter is based on generation of electron-hole pairs in the SiO_2 when the structure is exposed to ionizing radiation and separation of the

generated carriers by local internal electric field created around each preliminary charged nanocrystal. For example if the NCs are negatively charged the holes generated in the SiO_2 are swept towards the nanocrystals, where they recombine with a part of the trapped electrons and reduce the net charge, while the generated electrons are swept towards the gate electrode. The discharge of the nanocrystals causes change of the MOS structure flatband voltage, which can be used to measure the absorbed dose.

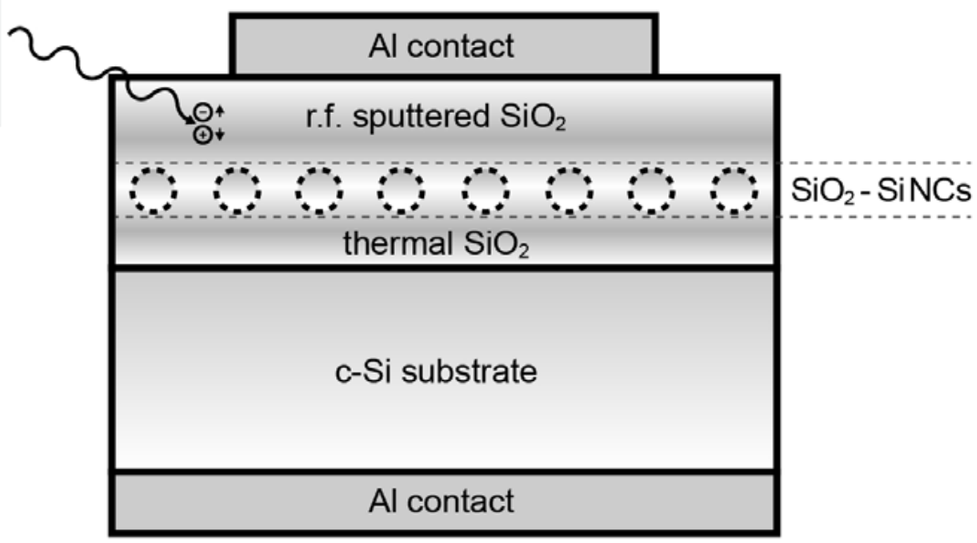


Fig. 12. Schematic cross-section of a MOS structure with three-layer gate dielectric: thermal SiO_2/SiO_2 – Si NC/sputtered SiO_2.

In order to set an initial flatband voltage ΔV_{FB0} prior to irradiation each dosimeter was charged by applying voltage pulses to the control gate with positive or negative polarity and with various amplitudes and durations. The positive pulses charge Si nanocrystals with electrons injected from the crystalline silicon wafer, while the negative ones charge NCs with holes. Figure 13 shows the initial as well as shifted C-V curves obtained after charging a structure with six sequential 10 V/5 s pulses. Each pulse causes parallel shift in the positive direction changing the flatband voltage with ~ 0.14 V; thus after the last pulse a shift of ΔV_{FB0} = 0.83 V was obtained. The shifts in the positive direction correspond to a gradual increase of the negative charge in the gate dielectric. The characteristic after each charging pulse was measured in both directions in a narrow interval (0 – 2 V), in order to avoid change in the charge state of the nanocrystals; no hysteresis has been obtained.

Because of the thermal oxide, which makes the total SiO_2 thickness between the nanocrystals and the c-Si wafer greater than 7 nm and the thicker control oxide (60 nm) the structures used in dosimetry experiments showed much longer retention time than the memory ones (Nedev et al., 2011). Two weeks after charging the capacitors they showed an average relative change of the flatband voltage due to discharging at ambient conditions of ~ 2 %.

Charged samples were subjected to various integral gamma irradiation doses from 3 to 200 Gy which were accumulated in steps at a dose rate of 37 Gy/h. The γ-irradiation was carried out in air of 75 to 80% humidity by means of a 38 000 Ci ^{60}Co source with an average energy E_γ = 1.25 MeV.

Fig. 14 shows changes of the flatband voltage versus absorbed dose for two capacitors having an initial flatband voltage shift of $\Delta V_{FB0} = 0.8$ and 0.67 V. The two curves have similar shape within an initial interval, 0 - 100 Gy, in which approximately linear dependence between ΔV_{FB} and the dose is observed. The obtained sensitivities for the linear region are $S \sim 2.1$ and 2.3 mV/Gy, respectively, and no correlation between ΔV_{FB0} and S was found (Nedev et al., 2011). The reduced sensitivity at doses higher than 100 Gy can be related to discharging of nanocrystals and decrease of the oxide internal electric field.

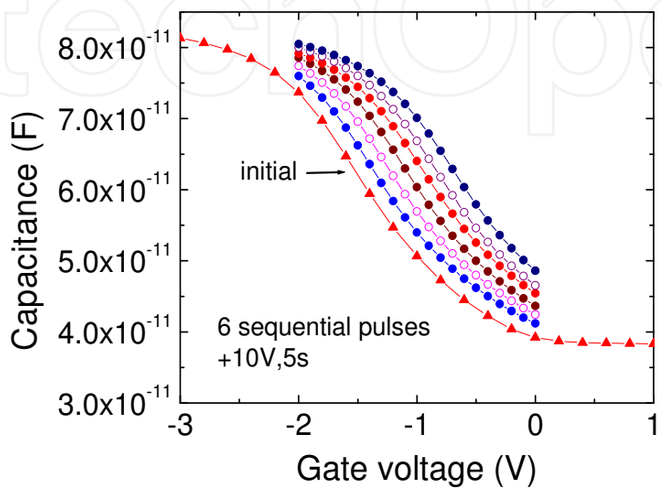


Fig. 13. C-V curves measured at 1 MHz of a MOS structure with Si nanocrystals charged with six sequential pulses, each of them with amplitude of +10 V and duration of 5 s. The initial curve is also presented.

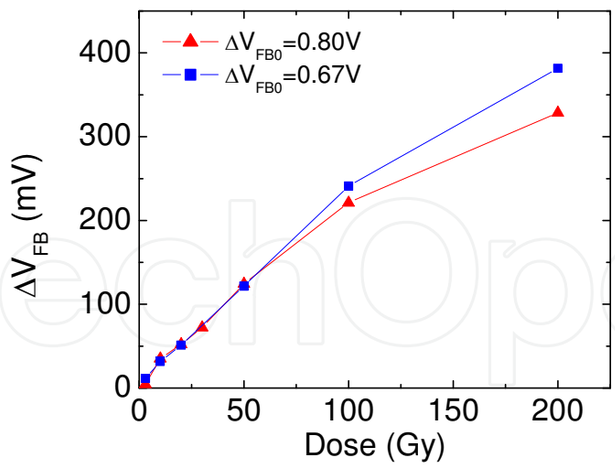


Fig. 14. Flatband voltage changes of p-Si MOS structures charged with electrons versus absorbed γ dose.

To test the possibility to reuse this type of dosimeters, structures irradiated to 200 Gy were recharged to the same ΔV_{FB0}, and subjected to a second γ-irradiation under the same conditions. The dependencies of the flatband voltage changes on the dose for the first and second irradiation for two dosimeters are shown in Fig. 15. As seen the curves have similar

shapes but the second irradiation causes smaller response. Most likely the higher sensitivity observed in the first irradiation experiment is partially due to capturing of holes in existing or generated by the radiation deep traps in the sputtered SiO_2 and/or in defects at the sputtered SiO_2/SiO_2-Si NCs interface, a process which is irreversible at room temperature. Thus, although the structures have the same initial change of the flatband voltage ΔV_{FB0} before both irradiations, their charge states were different, and this could be the reason for the different characteristics measured after the first and second irradiation.

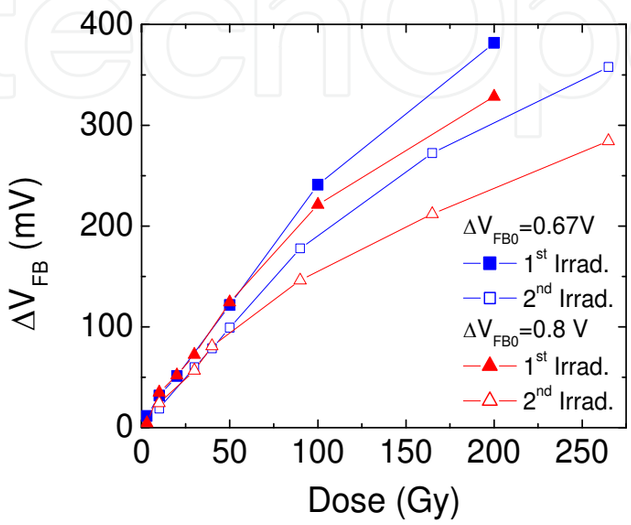


Fig. 15. Flatband voltage changes after the first and the second γ-irradiation.

To improve the quality of the control (top) oxide and at the same time to increase the sensitive volume of the sensor (the one which contains nanocrystals) a new approach for preparation of multilayer dielectric containing three-dimensional ensembles of silicon NCs has been proposed. The method is based on two-step annealing process at 1000 ^{0}C in different atmospheres. The first step is annealing in pure nitrogen to grow nanocrystals with a given size distribution; it is followed by a second annealing in nitrogen + oxygen atmosphere to complete the NC growth and at the same time to oxidize the already formed NCs, close to the top surface and thus to obtain a control SiO_2 region. By keeping the total annealing time 60 min it may be expected that the nanocrystals grown far from the top surface will have approximately the same size and spatial distribution as in the case of 60 min N_2 annealing. Figure 16 shows a XTEM micrograph of ~ 100 nm thick SiO_x (x = 1.3) film annealed for 50 min in pure N_2 and then for 10 min in 90 % N_2 + 10 % O_2 atmosphere. It proves that a two layer dielectric with ~ 75 nm SiO_2-Si NCs region and ~ 25 nm SiO_2 region free from nanocrystals has been successfully produced.

MOS structures with multilayer gate dielectric containing NCs obtained by the new two-step annealing process are currently tested as radiation dosimeters and NVMs.

5. Conclusions

In this paper, we have reviewed some interesting results of other research groups on MIS structures containing Si nanocrystals for non-volatile memory and detector applications. It

has been shown that nanoparticle memories continue to develop new ideas and technologies for nanoparticle formation and MIS structure arrangement as self-assembling techniques have been applied and proven to be very useful for structure preparation. Furthermore, a brief description has been made of the most important results in this field obtained during the last five years by the authors and their collaborators. MOS structures for non-volatile memory applications have been prepared with dielectric film containing amorphous or crystalline silicon nanoparticles in which the tunnel oxide layer is formed during the structure annealing. It has been shown that the defect density at the c-Si wafer/silicon oxide interface is lower in the structures with a-Si NPs than in those containing Si NCs which is due to epitaxial overgrowth and increased interface roughness after annealing at 1000 ^{0}C. Another essential advantage of the a-Si nanoparticle structures compared to the NC ones is the much slower discharging process observed, especially of trapped electrons. Both advantages in combination with the lower growing temperature required for the a-Si NP formation make them rather perspective for non-volatile memory applications.

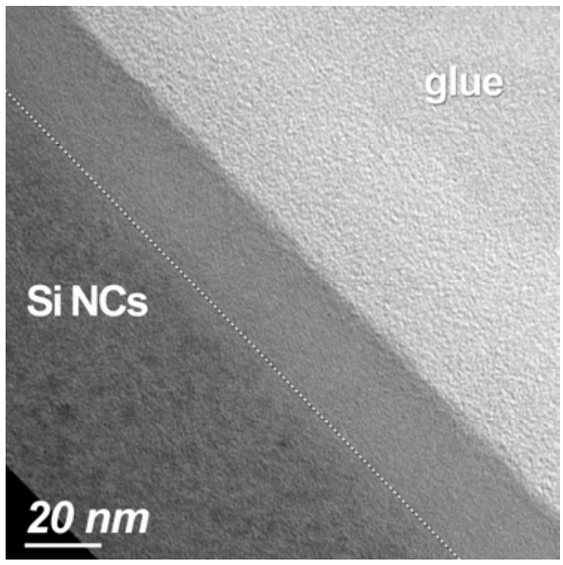


Fig. 16. XTEM micrographs of a two-step annealed SiO_x (x = 1.3) film with thickness of ~ 100 nm. The contrast observed in the image confirms that the second annealing step (oxidation) forms a free from nanocrystals region with thickness of ~ 25 nm.

Recent authors' data on preparation of MOS structures containing Si nanocrystals and their response to γ-radiation have also been presented. The detector operation is based on generation of electron-hole pairs in the SiO_2 when the structure is exposed to ionizing radiation and separation of the generated carriers by the local internal electric field which is created around each nanocrystal by a preliminary charging of Si NCs. Upon a negative preliminary charging of the Si nanocrystals no spontaneous nanocrystal discharge occurs for more than 2 weeks. The γ-irradiation with doses in the range 0-100 Gy causes approximately linear variation of the flatband voltage. An advantage of this detector when compared with those using conventional floating gate devices is the expected improved radiation hardness because of the suppressed lateral currents. A new two-step annealing procedure has been applied on SiO_x single layers deposited by thermal evaporation of SiO in vacuum on c-Si in order to prepare three layer MOS structures containing nanocrystals for device applications.

The above described authors' results indicate that the developed techniques for MOS structures preparation based on thermal evaporation of SiO in vacuum are well suited for preparation of Si nanoparticle memories and radiation detectors. All processing steps including the thermal annealing required for Si NP formation are compatible with the contemporary CMOS technology. Follow-up experiments should take place in a production environment and focus on the integration of the methods in the technology of commercial memory and detector devices.

6. Acknowledgements

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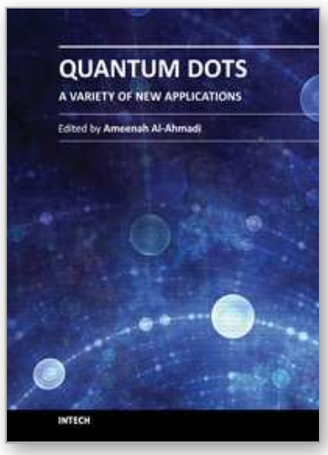

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The book “Quantum dots: A variety of a new applications” provides some collections of practical applications of quantum dots. This book is divided into four sections. In section 1 a review of the thermo-optical characterization of CdSe/ZnS core-shell nanocrystal solutions was performed. The Thermal Lens (TL) technique was used, and the thermal self-phase Modulation (TSPM) technique was adopted as the simplest alternative method. Section 2 includes five chapters where novel optical and lasing application are discussed. In section 3 four examples of quantum dot system for different applications in electronics are given. Section 4 provides three examples of using quantum dot system for biological applications. This is a collaborative book sharing and providing fundamental research such as the one conducted in Physics, Chemistry, Biology, Material Science, Medicine with a base text that could serve as a reference in research by presenting up-to-date research work on the field of quantum dot systems.

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