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Optimized Hybrid Modulation Algorithm to Control Large Unbalances in Voltage and Intensity in the NP Point of an NPC Converter

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1. Introduction

The role of power-converters is growing rapidly in importance. In part, this is due to an increased use of renewable energy, which gets injected into the grid as electricity that must satisfy minimum quality regulations (Hammons 2011).

One of the features of using multilevel converters, as opposed to one level converters, is that they operate with different output voltage levels and as a result, a lower harmonic distortion coefficient is achieved. Moreover, these topologies allow working with higher voltages than the transistor break-down voltage, therefore allowing higher power ratings (Bueno 2005).

NPC multilevel converters can be connected to photovoltaic panels in such a way as to optimize the efficiency. This means that fewer panels need to connect directly to the grid, as opposed to two-level topologies, while peak line voltage does not exceed DC-bus voltage.

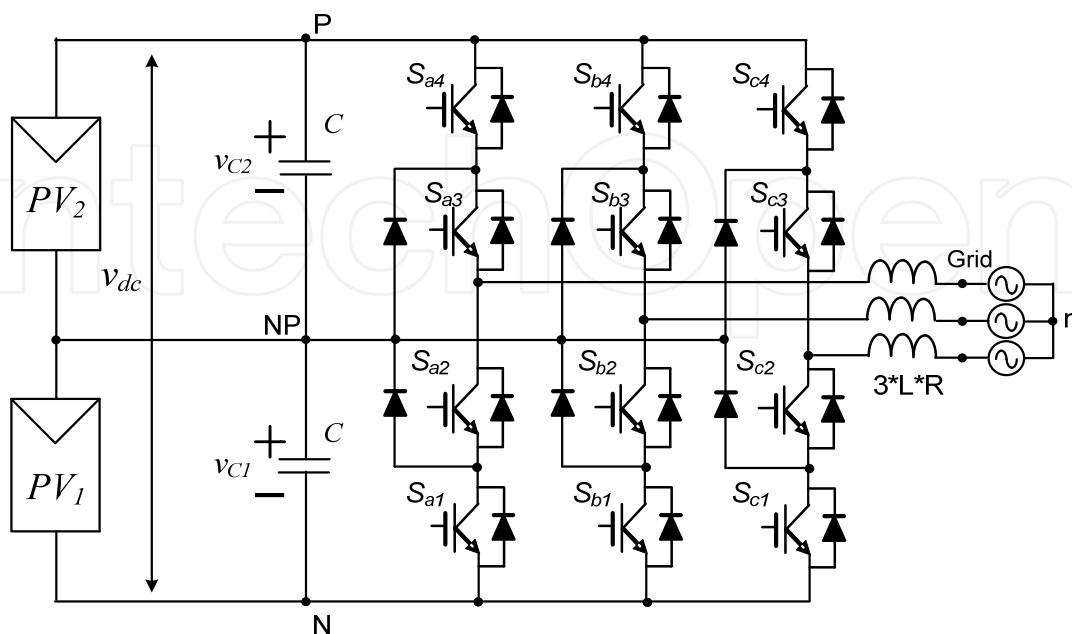


Fig. 1. Three-phase NPC converter, connected to a pair of independent photovoltaic-panel arrays.

There is however a drawback that comes up in the use of photovoltaic panels. Only low voltage can be supplied by these devices. This means that they must be connected in series, in order to achieve the desired voltage. Unfortunately, the lowest current supplying element sets the maximum current generated by the array.

Minimizing the number of panels connected in a series improves array efficiency once the converter is directly connected to a 400V grid and NP is connected between the two halves of the panel array. Furthermore, as these two arrays are independent, both can be set to inject maximum power at any moment.

Recently, there has been some work that has focused on transformerless photovoltaic inverters, and the influence of current leakage (Gonzalez et al., 2008), (Kerekes et al., 2009) (Kerekes et al., 2007). This is especially important for human safety. The German standard, VDE0126-1-1, deals with grid-connected PV systems, and gives the requirements for limiting ground leakage and fault currents. These works coincide in that the NPC is an ideal topology for regulatory compliance, and the algorithm proposed minimizes the NP ripple voltage, one reason why the current leakage exists. The voltage level achieved by the capacitors is studied in several works, which focus on the NP point ripple (Bueno et al., 2006), (Celanovic & Boroyevich 2000), (Ogasawara & Akagi 1993) (Qiang et al., 2003).

(Pou et al., 2007) proposes to eliminate low frequency ripple at the NP using two modulations which contribute to an increase in switching frequency for transistors, and therefore power losses. Work by (Cobreces et al. 2006), based on a single-phase inverter, applies a changing state strategy in a specific duty cycle which also contributes to an increase in switching frequency.

Usually, there is no intention to tackle the asymmetric supply issue since it is very common to implement the same voltage for both capacitors thus avoiding an independent power supply implementation.

This document takes a look at this problem and tries to increase the efficiency of renewable energy generation. In Section 2, system characteristics are determined, and we introduce an improved proposal for (Pou et al., 2007) reducing NP ripple voltage in ideal conditions: plugging symmetric or minimal asymmetric power supply into the DC-bus. Section III explains the underlying principle of the proposed algorithm and implementation details. Section IV shows simulations made under "ideal" power supply conditions, and analyzes their limits, characteristics and advantages. In Section V, the power supply imbalance issue, due to the fact that power supplied by PV1 and PV2 are different, is discussed: the imbalance tolerance limit will be shown analytically. Finally, in Section VI, conclusions will be drawn.

2. System characteristics

Several different works have investigated the NP imbalance and have proposed several solutions. In (Pou et al., 2007), low frequency ripple is almost completely reduced at the expense of increasing switching frequency.

After having simulated the proposed grid-connected through an L filter with the DC-bus specifications listed in Table 1., Figures 2 and 3 show capacitor voltage evolution, NP ripple, inverter phase voltage and inverter phase-to-phase voltage. Figure 2 shows the results without the implementation of the improving algorithm, while Figure 3 shows the implementation of the algorithm proposed in (Pou et al., 2007).

I_{PV1}	I_{PV2}	U_{refVc1}	U_{refVc2}
100 A	100 A	375 V	375 V

Table 1. Simulation conditions.

Figure 2 demonstrates that NP ripple is considerable. This ripple is due to a low frequency component that matches with the third harmonic of the grid frequency, and a high frequency component that matches the switching frequency.

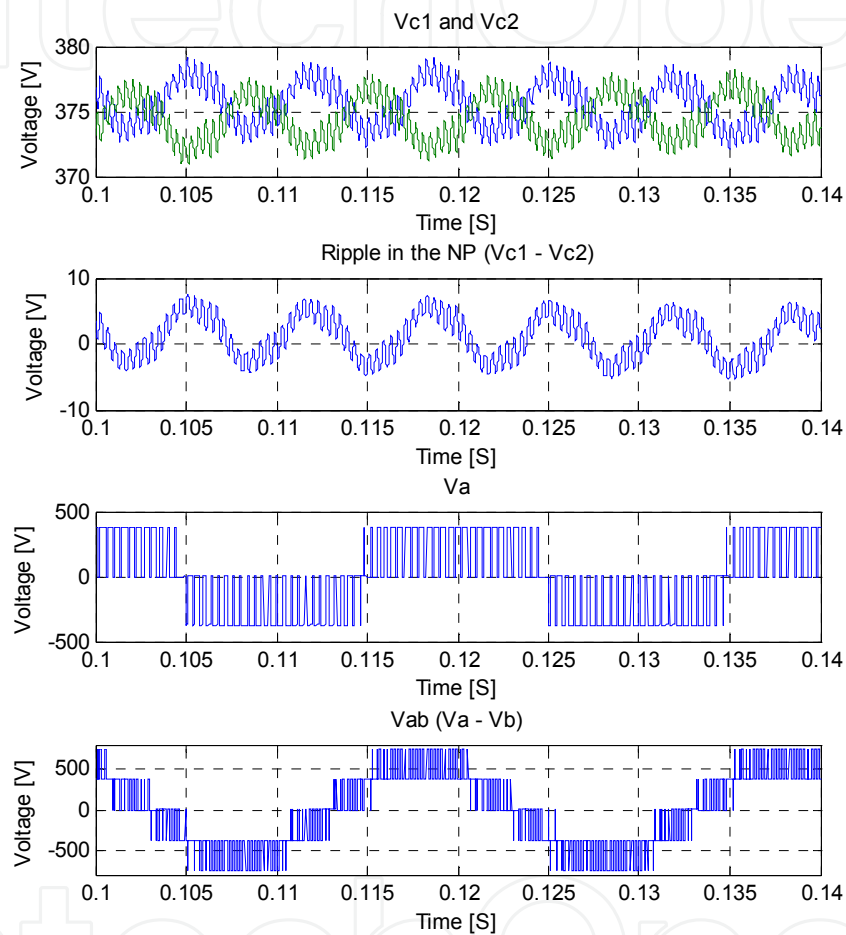


Fig. 2. Simulation results without the proposed algorithm. Capacitor voltage, NP ripple voltage, phase and line voltage.

Figure 3 show that the low frequency component is almost completely in the NP, but a high frequency component still exists.

Problems arise when the conditions in Table 1 change and voltage or current imbalances are introduced.

When this happens, and is due to small voltage imbalances, it is viable to introduce offsets and sort out the problem in both mentioned cases. An objection to this method is that modifying modulations may cause undesired over-modulation resulting in a discontinuous state. Moreover, falling into a discontinuous state becomes more likely when working close to the nominal power of the converter.

If this happens due to small current imbalances, it results in overcharging one capacitor, which brings an undesired voltage imbalance that can be solved with the same procedure, but with the same undesired consequences.

Therefore, connecting the NP to the middle point of a photovoltaic-panel array is an open field for investigation (Galvez et al., 2009) and (Busquets-Monge et al. 2008), and this technique is beginning to be applied to the connection of two wind turbine generators (Jayasinghe et al., 2010). However, currently, it is common to find arrays connected from UDC+ to UDC-. As shown in figure 4.

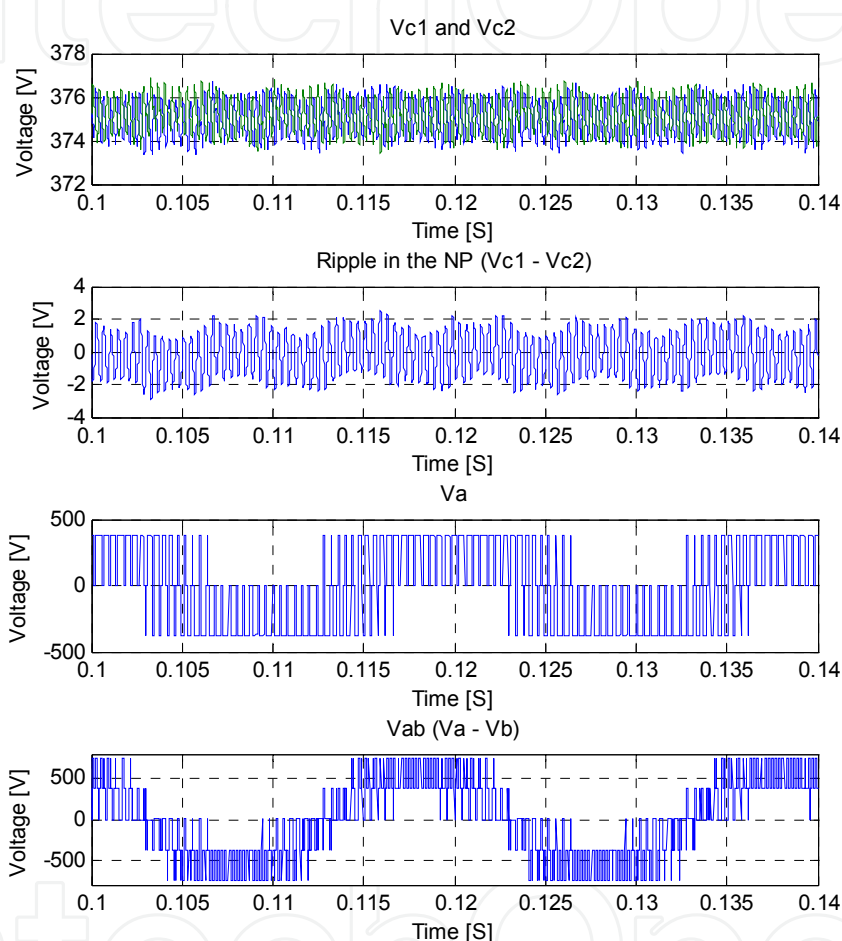


Fig. 3. Simulation results with algorithm proposed in (Pou et al., 2007). Capacitor voltage, NP ripple voltage, phase and line voltage.

The proposed algorithm solves this problem and improves performance even with bigger imbalances due to partial shading, a consequence of cloudy days and when some panels are dirty. Moreover the features of the panels, after manufacturing, are not identical for individual panels, and the photovoltaic panels performance changes over time are unequal.

What's more, there are some researchers who have proposed several topologies that work with more than one array of photovoltaic panels (Calais et al., 1998), and with special attention to the problem of current leakage (Gonzalez et al., 2008), (Kerekes et al., 2009) and (Kerekes et al., 2007).

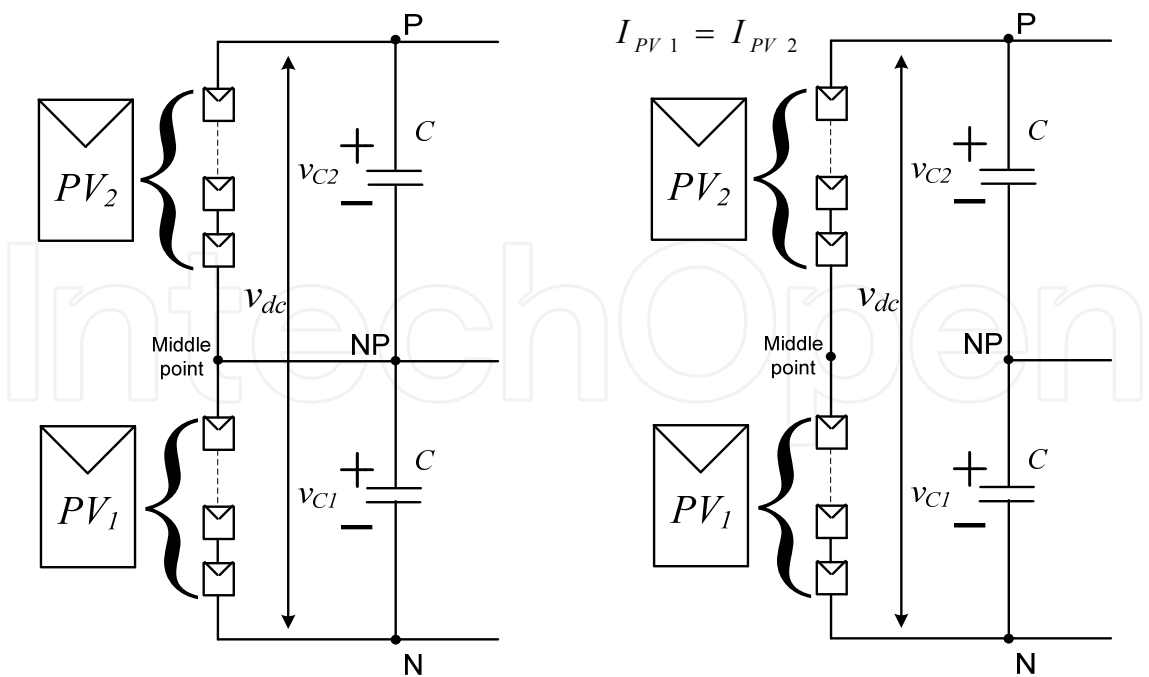


Fig. 4. Schematics of an array of photovoltaic panels. The left one with middle point connected and the right one unconnected.

3. Underlying principle of the proposed algorithm

Regardless of the modulation technique applied, either SPWM or SVPWM (Bueno et al., 2002), a set of states defines transistors in each phase. These states imply that each phase is connected to 1, 0 or -1, where 1 is P (U_{dc+}), 0 is NP (middle point) and -1 is N (U_{dc-}). Because the topology described in this document is triphasic, it is necessary to work with a three element vector, where each value is the state of each phase, typical of a three-phase converter.

The aim of a converter is to fix a specific phase-to-phase voltage in order to force a current flow through the grid filter. The system will work correctly as long as the appropriate voltage is applied, whichever phase it was connected to 1, 0 or -1. Figure 5 shows the schematic that works with two independent MPPTs, where the original vector is generated. There has been a lot of work done on Maximum Power Points (MPPT) for photovoltaic panels (Weidong et al., 2007), (Salas et al., 2006) and (Jain & Agarwal 2007), and in (Esrām et al., 2007) research focuses on the review of maximum power point tracking. In (Patel & Agarwal 2008), the influence of shadows on MPPTs is studied.

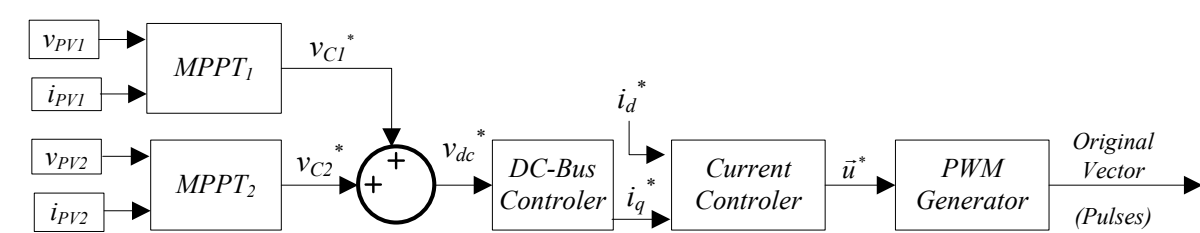


Fig. 5. Schematics of the control system.

The algorithm we propose explains how to calculate a fixed or dynamic voltage band around the reference voltage in NP, which can be $V_{dc}/2$ or something else. This voltage band, which will determine whether the measured NP voltage is above, below or within the range, will force the algorithm to increase, reduce or apply no offset to the NP voltage.

Once a reference shift is drawn, NP voltage must be changed, which means that one capacitor will charge as the other discharges with the same amount of energy. So, globally, energy and DC-bus voltage remain unchanged.

The instant power is distributed in the system in the following way:

$$P_G = P_{PV1} + P_{PV2} \quad (1)$$

where P_G is the total available or generated power,

$$p_{C1} + p_{C2} = P_{DC} \approx P_G - P_{Load} \quad (2)$$

and stored power in the capacitors is approximated, ignoring power losses in wires and the inverter. Nevertheless, this power can be considered more or less constant for transients, where $p_{C1} \neq p_{C2}$ is not only different, but not constant either; the variation being a consequence of the ripple in the NP. Hence, these powers can be separated into a continuous component and a variable component, as follows:

$$p_{C1} = P_{C1} + \frac{1}{2} C_1 \frac{du_{C1}^2}{dt} \quad (3)$$

$$p_{C2} = P_{C2} + \frac{1}{2} C_2 \frac{du_{C2}^2}{dt} \quad (4)$$

considering P_{DC} more or less constant, and existing for a short-period of time, we can say that:

$$\frac{1}{2} C_1 \frac{du_{C1}^2}{dt} \approx -\frac{1}{2} C_2 \frac{du_{C2}^2}{dt} \approx \Delta_p \quad (5)$$

and if (5) is substituted in (3) and (4), the equations become:

$$p_{C1} \approx P_{C1} + \Delta_p \quad (6)$$

$$p_{C2} \approx P_{C2} - \Delta_p \quad (7)$$

There are certain moments in which all phases are connected to the same capacitor, forcing that capacitor to get charged while the other one gets discharged. That is precisely the right time to change the normal behaviour.

The object is to modify the state vector in order to overrule the standard sequence and charge the appropriate capacitor.

A list with all shifted vectors is shown in Table 2, but some conditions have to be met: the appropriate state combination and a true need of shift.

Upper shifts						Lower shifts					
Original Vector			Shifted Vector			Original Vector			Shifted Vector		
0	0	1	-1	-1	0	-1	-1	0	0	0	1
0	1	0	-1	0	-1	-1	0	-1	0	1	0
0	1	1	-1	0	0	-1	0	0	0	1	1
1	0	0	0	-1	-1	0	-1	-1	1	0	0
1	0	1	0	-1	0	0	-1	0	1	0	1
1	1	0	0	0	-1	0	0	-1	1	1	0

Table 2. Vector-Shift implementation.

The results found when a shifted vector is applied are that signs in (6) and (7) get changed. This forces a modified offset in the NP with twice the value and opposite sign. This is different from the original offset when shift is not done, giving:

$$p_{C_1}^* \approx p_{C_1} - 2\Delta_p$$

(8)

$$p_{C_2}^* \approx p_{C_2} + 2\Delta_p$$

(9)

and keeping the relationship in (2):

$$p_{C_1}^* + p_{C_2}^* = p_{C_1} + p_{C_2} = P_{DC}$$

(10)

Therefore, both aims of not modifying DC-bus voltage and quickly applying an appropriate change to the NP voltage are achieved.

Figure 6 shows where the change of the original vector for the shifted vector is put.

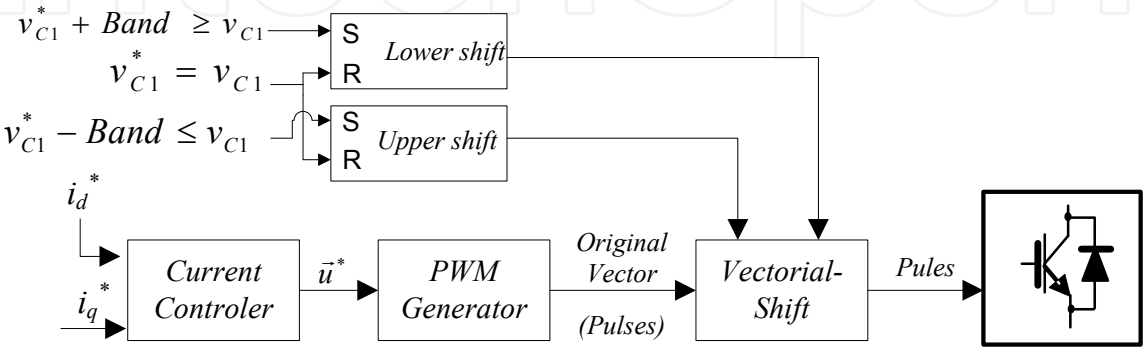


Fig. 6. Schematic with vector-shift implementation.

4. Characteristics of the proposed algorithm operation

The use of the proposed algorithm, not only achieves low frequency ripple reduction, but also cancels all of the components that make the NP voltage drop out of the limits of the desired band, making switching frequency dependent on the span of the ripple band.

First, we will start off with a system analysis performed under identical DC-bus conditions applied to Table 1.

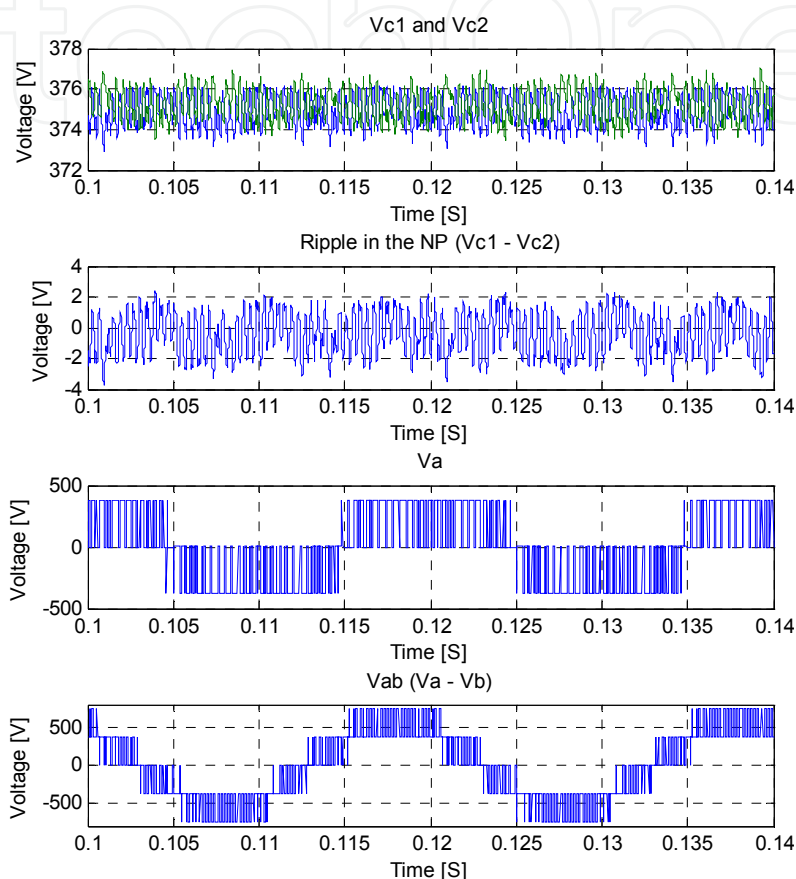


Fig. 7. Shows simulation results for a voltage band of ± 1 v.

Fig. 7 Simulation results with the proposed algorithm and ± 1 v band. C1 and C2 voltage ripple in the NP, phase voltage and line voltage.

Additionally, capacitor voltage could be checked to see if it is kept within the voltage range. It is possible to establish a narrow band in order to cancel even the high frequency components at the cost of increasing the switching frequency. So a decision must be made between ripple span or switching losses, considering the thermal limitation design to avoid any damage to the devices, and the transistors transient response.

Figure 8 shows simulation results for a voltage band of ± 2 v.

Moreover, it should be considered that DC-bus voltage is not truly constant, because the undesired ripple is dependent on the amount of power injected into the grid. Therefore, despite the fact that one capacitor benefits from a more limited narrow band, the other capacitor suffers from a wider band, the sum of that band and DC-bus ripple. That does useless to reduce ripple in the DC-bus.

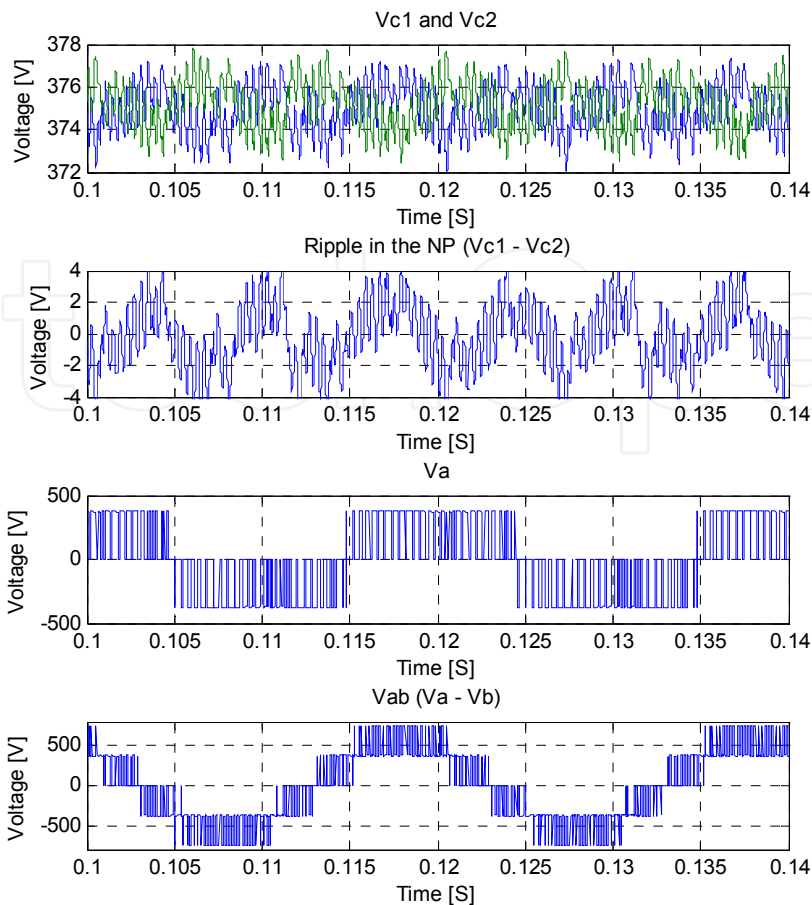


Fig. 8. Simulation results with the proposed algorithm and the $\pm 2v$ band, C1 and C2 voltage ripple in the NP, phase voltage and line voltage.

This effect is shown in Figure 9. The parameters represented are C1 voltage; ripple voltage in the NP and DC-bus voltage. Also, the influence of a $\pm 0.5V$ voltage band can be seen.

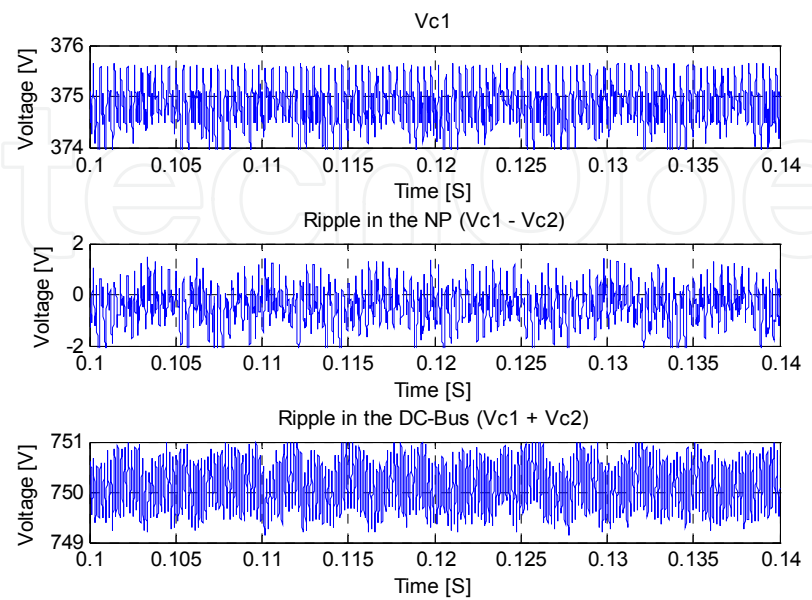


Fig. 9. Simulation results for C1 with $\pm 0.5V$ ripple.

Table 3 shows both the amount and the rate of increase of switches for the applied algorithm with different voltage spans.

	Amount	Increase Rate %
Without Algorithm	606	0%
Proposed in (Pou et al., 2007)	845	39,44%
±2V band	761	25,58%
±1V band	1027	69,47%
±0,5V band	1749	188,61%

Table 3. Amount and rate of increase of switches in different simulations.

Therefore, it can be affirmed that reducing the ripple to NP ripple values causes an increase in switches and, therefore, losses, but does not reduce ripple in the DC-Bus. Because of this, it is not effective to use NP ripple values lower than DC-Bus ripple values.

So, when the power injected into grid is lower, the NP ripple is also lower and the number of times that the algorithm has to shift, is lower, making the number of swiches lower as well.

5. Characteristics of the proposed algorithm operation with high imbalances

The main feature of the algorithm is that it keeps the voltage in the NP controlled, even when there are big current imbalances during capacitor charge. This means that PV2 injects a different current than PV1.

Figure 10 shows the system simulation results with the proposed algorithm under the DC-bus specifications listed in Table 4, for a ±2V band.

IPV1	IPV2	U _{refVc1}	U _{refVc2}
125 A	75 A	375 V	375 V

Table 4. Simulations conditions.

It can be seen that both capacitor voltages remain within the fixed band, and that line voltage matches with the one simulated in the Figure 3. This, however, is not true for phase voltage since it can be clearly seen that it tends to be connected to +U_{dc} for positive values, and to 0V for negative values. This does not happen when injected current into the bus is symmetric.

In this case the number of switches is 914, which means an increase rate of 50.82 % over the simulation without the algorithm. However, in this case there is no choice, as there is no way to keep bus balanced when such imbalances are applied.

As shown in Section II, the algorithm induces the vector shift at the moment that each phase is connected to the same capacitor, meaning that an adequate state combination happens. If

we consider that both capacitors have the same reference voltage, the maximum allowed imbalance can be calculated. If given:

$$D_V > 1 - m = 1 - \frac{U_{DC}}{\sqrt{2}V_L} \tag{11}$$

where D_V is the duty cycle when vector shift can be done, and m is the modulation index.

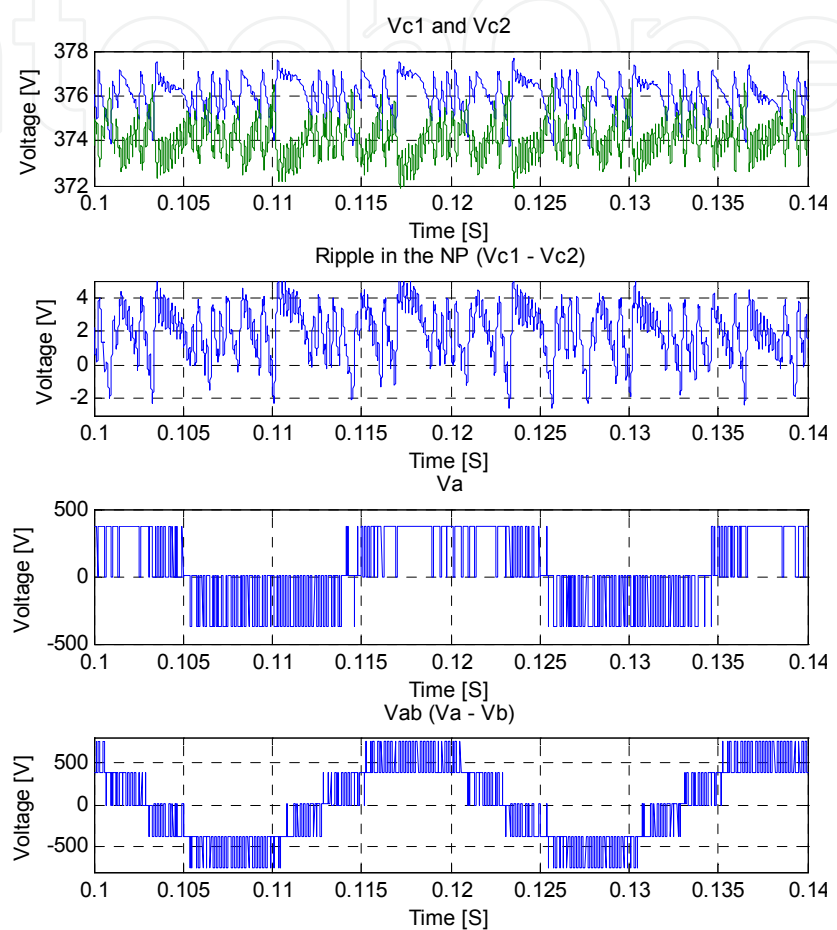


Fig. 10. Simulation results for a $\pm 2V$ ripple with $IPV2=0.6 \cdot IPV1$.

Now, consider the following equations in terms of D_V :

$$P_{PV_{max}} = \frac{P_G}{2}(1 + D_V) \tag{12}$$

And, also:

$$P_{PV_{min}} = \frac{P_G}{2}(1 - D_V) \tag{13}$$

The Umb_{Max} is:

$$Umb_{Max} = \frac{P_{PV_{min}}}{P_{PV_{max}}} \tag{14}$$

From (12), (13) and (14):

$$\frac{P_{PV_{\min}}}{P_{PV_{\max}}} = \frac{(1 - D_V)}{(1 + D_V)} \quad (15)$$

Now, the maximum imbalance condition can be given, guaranteeing functionality of the algorithm. From (11), (12), (13), (14) and (15):

$$Umb_{Max} = \frac{(1 - D_V)}{(1 + D_V)} > \frac{U_{DC}}{\sqrt{8V_L - U_{DC}}} \quad (16)$$

Taking into account that V_L is considered constant, maximum asymmetry is fixed by DC-bus voltage, which is typically variable when coming from photovoltaic panels. Therefore, the system will work at its maximum performance as long as maximum asymmetry is met.

As a solution for higher asymmetries than the maximum asymmetry, the DC-bus voltage can be increased, although when this happens, it moves output away from the maximum power point of the panels.

6. Conclusion

A new hybrid modulation algorithm to control NP voltage has been described, even under high voltage asymmetries in the DC-bus.

It has been simulated both in symmetric and asymmetric power supplies, achieving voltage and ripple in the NP under control.

This algorithm is ideal for use in photovoltaic panel power source applications, as it tolerates high imbalances. If two independent panel arrays get connected, during cloudy days asymmetries will certainly occur. Nevertheless, each capacitor voltage can be controlled independently, greatly improving global performance of the panels.

Something else to keep in mind with photovoltaic panels is that fixing a capacitor voltage is a quick process, faster than the DC-bus time constant. This is one of the parameters that has the most influence on the changes in MPPT response under rapid perturbations from the environment. Furthermore, a reduction of one capacitor does not necessarily reduce DC-bus voltage; but reducing the degradation of the quality of injected energy in to grid by the fact that MPPT fixes the capacitor reference voltage. Moreover, this algorithm creates a new line of investigation for the design of faster MPPTs and faster responses for better THD.

The proposed algorithm has been validated with simulations shown in this document.

7. Acknowledgment

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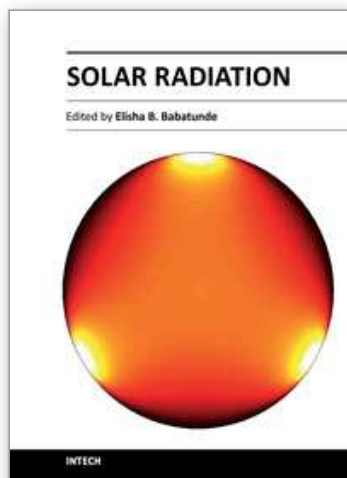
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