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Influence of Ionizing Radiation and Hot Carrier Injection on Metal-Oxide-Semiconductor Transistors

Momčilo Pejović[1], Predrag Osmokrović[2],
Milica Pejović[1] and Koviljka Stanković[2]
[1]University of Niš, Faculty of Electronic Engineering, Niš,
[2]University of Belgrade, Faculty of Electrical Engineering, Belgrade,
Serbia

1. Introduction

General characteristics of MOS components

Favourable characteristics of silicon dioxide (further referred to as oxide or SiO_2) as an almost irreplaceable dielectric in MOS (Metal-Oxide-Semiconductor) components have contributed to a considerable extent to the great success of the technology of manufacturing integrated circuits during the last decades. However, it has been proved that instabilities of electric charge in the gate oxide and at $Si-SiO_2$ interface, which inevitably occur due to the influence of ionizing radiation (γ and X-radiation, electrons, ions) (IR) and hot carrier injection (which includes Fowler-Nordheim high electric field Stress, avalanche hole injection, avalanche electron injection, and so on (HCI) during the operation of MOS transistors, lead to instabilities of their electric parameters and characteristics and present a serious problem to the reliability of MOS integrated circuits [1-4]. Studying these instabilities, particularly causes and mechanisms responsible for their occurrence, is very significant as it may help the manufacturer define appropriate technological parameters with the aim of increasing their reliability. Considering the rate of development and requirement that the components should be highly reliable, the investigation of their instabilities in normal working conditions is practically impossible. In order to determine, as quickly as possible, mechanisms that cause instabilities, accelerated reliability tests are used and they comprise of the application of strong electric fields (so-called electric stress) in static and impulse modes at room temperature and/or at elevated temperatures. In this context, reliability comprises probability that the component may fulfil its target function during a certain period and under certain conditions, i.e. that it may preserve the electric characteristics and the value of electric parameters under certain exploitation conditions during a certain period. Reliability is defined as a probabilistic category as no failure of the component can be predicted with certainty. Namely, if a group of components manufactured in almost the same conditions is subjected to stress, a smaller number of them will fail earlier (early failure), while a larger number of them will fail later. In order to remove from such a group of components those with the possibility of early failure, a selection procedure is applied to all the components. This procedure consists of a series of

tests the most significant of which is the burn-in test. This test is carried out in two steps: short-term burning (10 – 30 hours) in normal and somewhat intense working conditions, in order to remove components liable to failure due to their manufacturing defects, and sufficiently long burning in tough working conditions in order to remove components with manifested functional failures. A significant fact that should be emphasized in relation to MOS components is that, although the high quality of components guarantees a certain level of their reliability, many defects may remain hidden and manifest during the application thus leading to the degradation of the components and their failure.

In recent times, the development of MOS integrated circuits shows a tendency of increasing the complexity and constantly decreasing dimensions, which comprises a need for increasingly thin gate oxides. In addition, discrete power MOS components have been also developed. At the beginning of their development, it was deemed that they would very soon replace bipolar transistors in power electronics. However, technological processes used in the manufacture of these transistors were more complex in relation to bipolar transistors so that a real progress in power electronics was made when VDMOS (Vertical-Double-Diffused MOS) transistors were developed because the manufacture of them was much simpler. Due to their favourable electric characteristics (great operative speed, low switch-on resistance, high switching voltage, etc.), the VDMOS transistors have found their application in the fields such as automotive industry [5]. Switching characteristics of VDMOS transistors at high frequencies (higher than 100 kHz [6]) have also proved very good owing to which these transistors are applied as switching components for high-frequency sources of supply used in medical electronics, engine control systems, switching sources of supply in telecommunication researches, etc.

In addition to its favourable properties, SiO_2 used in the manufacture of MOS components and integrated circuits has some shortcomings as well. Namely, instabilities of electric charge in the gate oxide and in interface traps, which are inevitable due to the presence of the IR or HCI processes, during the operation of MOS components and MOS integrated circuits, also lead to instabilities of their electric parameters and characteristics. Due to this, instabilities represent one of the most serious problems in relation to a reliable operation of MOS integrated circuits [2, 3] particularly when these components are used in radiation surroundings.

Researches have shown [3] that MOS components are very sensitive to different types of ionizing radiation and that their sensitivity significantly depends on the manufacturing technology. Additionally, some technological processes such as lithography with the use of a ray of electrons, X-rays, and processes in plasma, etc. included in the technological sequence for the production of integrated circuits with the aim of decreasing the dimensions of their components, may be significant sources of defects in the oxide [3].

The attention of today's researches on the impact of the IR and HCI processes on MOS components is directed in two ways. One way comprises the production of components with the highest possible resistance to these types of processes, while the other way leads towards the production of MOS transistors sensitive to IR in order to produce sensors and dosimeters of ionizing radiation [3]. It should be emphasized that the first operating principles of PMOS sensors and dosimeters of ionizing radiation were published as early as 1974 [7]. Unlike the influence of IR and HCI on the reliability of commercial MOS transistors which is the subject of many researches worldwide, PMOS transistors as IR dosimeters are investigated to a much lesser extent.

2. Origin and characteristics of defects and electrical charges in oxide and at Si-SiO$_2$ interface

Electrical charges in the gate oxide and at the Si-SiO$_2$ interface may be divided into four groups as follows [2, 8, 9]: *mobile ions, charges at the traps, fixed centres charges and charges at interface traps*. However, if a division of charges based on their influence on the current-voltage characteristics of MOS transistors is made, only charges in the gate oxide (including mobile ions, charges at the trap centres, and fixed charges) and charges at interface traps may be distinguished. The main classification of charges in the gate oxide and at interface traps of MOS transistors is shown schematically in Figure 1.
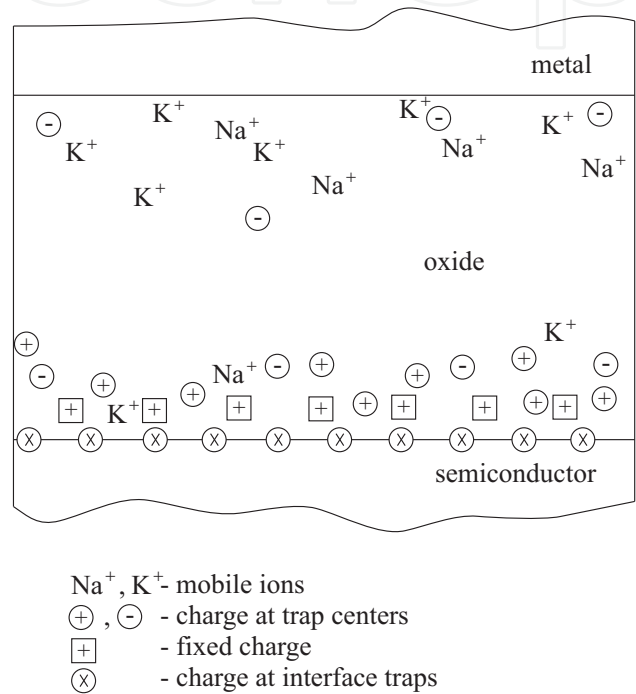

Na$^+$, K$^+$- mobile ions
$\oplus$, $\ominus$ - charge at trap centers
$\boxed{+}$ - fixed charge
$\otimes$ - charge at interface traps

Fig. 1. Classification of charge at Si – SiO$_2$ interface and in the gate oxide of MOS transistor.

Mobile ions in the gate oxide are mainly positive ions of alkali metals such as Na$^+$ and K$^+$, as well as hydrogen ions. They may be incorporated into the oxide during the mere processing of the wafer, or they may reach the oxide, coming from the surrounding surfaces, during the processes of passivation and packing [9, 10]. The existence of these ions in the gate oxide is associated with the fact that during high temperature processes, they easily diffuse into the oxide, from contaminated surfaces. Mobile ions are not distributed uniformly in the oxide, but most of them are located in the semiconductor or metal whereby many more ions are located in the metal as the attractive force towards the metal is much higher than the attractive force towards the semiconductor.

The most important instability mechanism related to electric charges in the gate oxide is the migration of positive ions to the oxide-metal interface and oxide-semiconductor interface under the influence of the positive polarization of the gate and elevated temperature. A series of treatments are taken with the MOS technology in order to minimize these instabilities. Besides the compulsory annealing at high temperature and high level of cleanliness of the technological space and materials used, some modifications in the oxide manufacturing technology have been made in order to minimize instability effects.

Furthermore, a generally accepted procedure for minimizing mobile ions is the introduction of chlorine into the oxide, which is achieved by introducing a certain quantity of HCl or Cl$_2$ into the oxidation atmosphere or by passing oxygen through trichloroethylene.
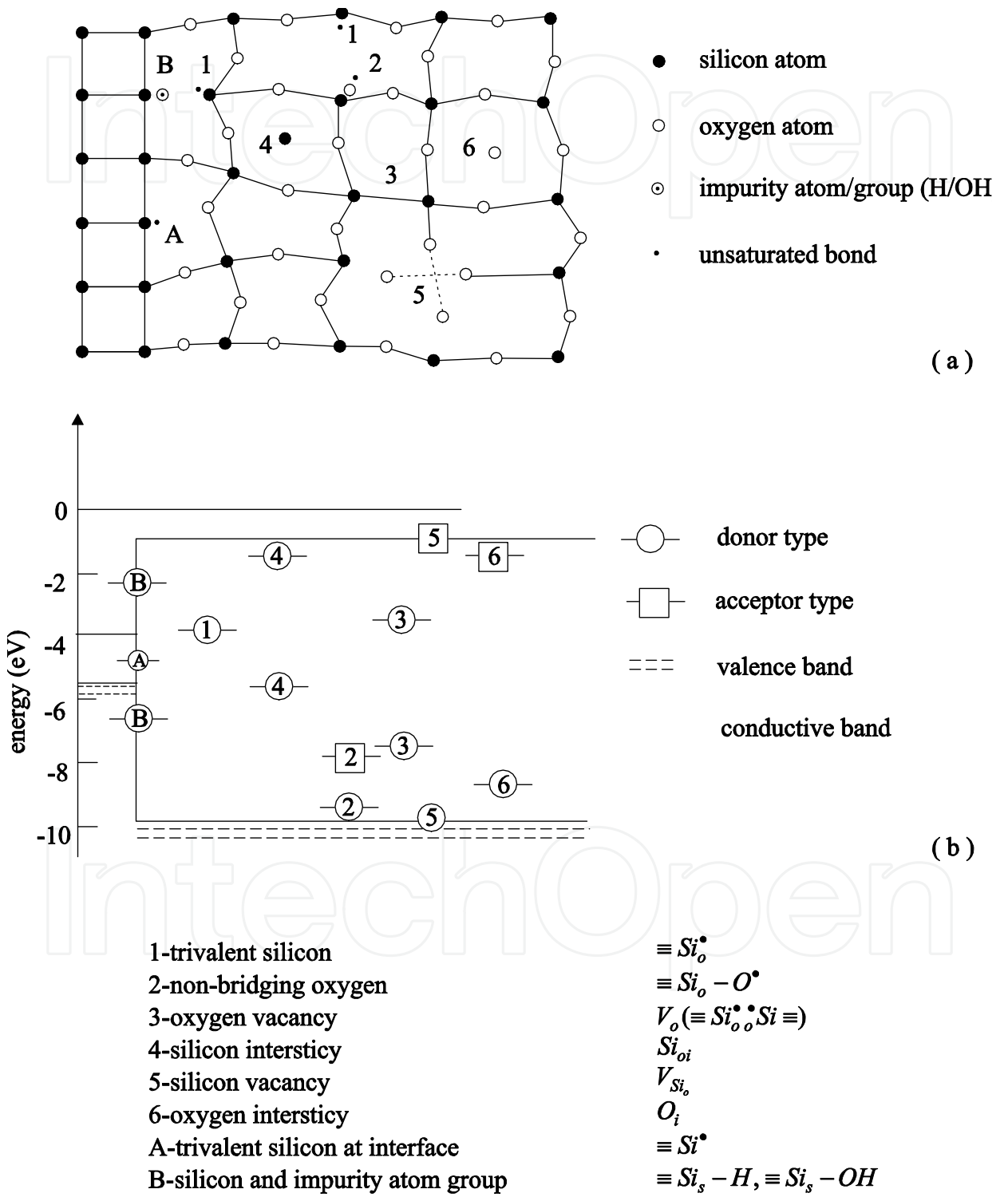

(a)

(b)

1-trivalent silicon	$\equiv Si_o^\bullet$
2-non-bridging oxygen	$\equiv Si_o - O^\bullet$
3-oxygen vacancy	$V_o (\equiv Si_o^{\bullet\bullet}Si \equiv)$
4-silicon intersticy	Si_{oi}
5-silicon vacancy	V_{Si_o}
6-oxygen intersticy	O_i
A-trivalent silicon at interface	$\equiv Si^\bullet$
B-silicon and impurity atom group	$\equiv Si_s - H, \equiv Si_s - OH$

Fig. 2. Most common defects in oxide and at $Si - SiO_2$ interface: (a) two dimensional model of chemical bonds; (b) energy band model.

Charges at the trap centres are defects and admixed atoms in the oxide which have permissible energy levels in the forbidden zone of the oxide. They are mainly located near the $Si – SiO_2$ interface, while their number inside the oxide is negligible. Figure 2 shows the model of chemical bonding and diagram of energy zones that illustrate the most significant defects in the oxide and at the $Si – SiO_2$ interface [4, 11]. Although this is not adequately shown in Figure 2a, it should be taken into account that the $Si – SiO_2$ interface does not spread through only one atom layer, but rather through several of them. As Figure 2b shows, due to a great difference in the widths of the forbidden zones of silicon (1.12 eV) and oxide (9 eV), discontinuity of energy zones occurs at the interface, and charge carriers encounter a high energy barrier (around 3.2 eV for electrons and 4.7 eV for holes) which in normal conditions prevents any movement of electrons and holes from the semiconductor into the oxide.

The origin of the traps varies. They may be formed both on ≡Si-O- bonds and on defects in the oxide (oxygen vacancies, ≡Si-H and ≡Si-OH bonds, other admixed atoms, etc.). This means that there are different energy levels of the traps depending on the type and quality of the oxide. The traps may be neutral or charged either positively or negatively. During exploitation in certain conditions, they may become electrically charged by capturing electrons or holes, and neutralized by releasing the same, a consequence of which is the instability of the density of effective electric charge captured on them. Therefore, the defects are mainly donor-type defects meaning that they may be positively charged or neutral, so that total electric charge in the oxide is positive. It is important to note that holes may be captured more easily than electrons. Thus the ratio between the number of captured holes and the total number of holes injected into the oxide is approximately one, while, on the average, out of 10^5 injected electrons only less than one is captured. Nevertheless, instabilities of charges at the traps caused by the electron capture may be equal to instabilities caused by the capture of holes or even more pronounced. The reason for this lies in the fact that electrons may be more easily injected into the oxide, which increases the possibility of their capture.

The most significant mechanisms that lead to the occurrence of free carriers in the oxide may be classified into three groups: a) tunnelling of electrons and holes from the semiconductor or metal into the oxide, 2) injection of hot electrons and holes from the semiconductor into the oxide, and 3) generation of electron-hole pairs in the mere gate oxide which may be a consequence of various factors such as ionizing radiation effects, photo-generation or application of a strong electric field. To the traps in the oxide or to the valence or conductive zone of the oxide, holes from the valence zone of the semiconductor or electrons from the conductive zone of the semiconductor or metal may be tunnelled. The processes of tunnelling electrons or holes from the traps into the conductive or valence zone of the oxide, or directly into the semiconductor are possible, which by analogy leads to instability of the charge density at the traps.

There are four mechanisms related to the injection of hot carriers from the semiconductor into the gate oxide. These are: 1) substrate hot electron injection, 2) channel hot electron injection, 3) drain avalanche hot carrier injection (whereby the injection of holes is preferred when the normal component of the field is directed towards the oxide, while the injection of electrons is preferred when the field is directed towards the semiconductor), and 4) hot electron injection caused by secondary ionization by holes in the substrate. It should be noted that such changes in the density of charges at the traps are not the only form of instability that occur during the exploitation of MOS transistors. Namely, new traps may be

formed which are neutral at the beginning, but which may become charged by capturing electrons and holes.

Fixed charge is located near the $Si-SiO_2$ interface at distances smaller than 8 nm and its density is constant regardless of changes in the threshold voltage of MOS components. This charge is always positive as it mainly consists of unsaturated bonds of silicon near the $Si-SiO_2$ interface. Fixed charge depends on the orientation of crystals and it is considerably higher with crystal orientation (111) than with crystal orientation (100). The quantity of fixed charge depends on the Technological conditions of oxidation (atmosphere and temperature). The oxide burn-in in nitrogen or argon at temperatures higher than $600^{\circ}C$ decreases the density of fixed charge. This is one of the reasons for which the oxide burn-in has been introduced as a standard procedure in the manufacture of CMOS integrated circuits. It should be emphasized that instability of fixed charges is rarely manifested separately from changes in other charges in the oxide. Instabilities of this type are commonly followed by simultaneous changes in charges at interface traps and oxide traps. This is why in literature fixed charge is mentioned in a much broader sense, although this term also refers to charge in the traps particularly considering the instability of charge in them. Since the origin of fixed charge and traps is frequently the same, it may be assumed that they differ in instability mechanisms. Namely, instability of charge in the traps is a consequence of capturing and releasing free electrons and holes in the oxide, while the instability of fixed charge reflects in its increase as a result of appropriate chemical reactions. One of such reactions is the dissociation of the *Si – H* bond near the *Si – SiO₂* interface. Under the influence of modest negative polarization of the gate and increased temperature, the *Si – H* group reacts with the *Si – O* group, whereby a interface trap is formed on the Si atom from the semiconductor, while released hydrogen and oxygen form an OH group which diffuses towards the interface. After the transfer of one electron into the semiconductor, the *Si* atom in the oxide remains positively charged and this represents the fixed charge. However, it is often impossible to determine a strict boundary between fixed charge and charge at the traps.

Charges at interface traps represent a significant group of electric charges in the oxide. Interface traps are located at the Si – SiO₂ interface the energy levels of which are in the forbidden zone of the semiconductor. These traps develop as a consequence of the semiconductor structure breaking because surface atoms remain with one unsaturated bond. This means that on clean areas of the semiconductor the number of interface traps is approximately equal to the number of surface atoms. However, thermal oxidation reduces the number of interface traps by several orders of magnitude as a great number of silicon atom bonds become saturated by bonding to oxygen atoms. From the aspect of the origin of interface traps, there is a complete analogy between them and fixed charge and thus with the trap centres. The difference is that fixed charge and the trap centres are in the oxide, while interface traps are at the Si – SiO₂ interface and they are easily accessible to free carriers from the semiconductor. The exchange of charge between interface traps and the semiconductor is relatively fast, so that the density of charge in interface traps at a given moment depends on the distribution of the interface traps energy levels and the position of the Fermi level in the semiconductor forbidden zone. Although the process of thermal oxidation considerably decreases the density of interface traps, an additional decrease is needed for a proper operation of MOS components. Today, a procedure commonly used is the oxide burn-in after metallization performed in nitrogen or in a mixture of nitrogen and hydrogen. In this manner, hydrogen is directly introduced in the oxide, or it is formed after the reaction of water and aluminium. This procedure decreases both the density of interface

traps and density of fixed charge and therefore it is applied in almost all standard technologies. Another favourable circumstance is that oxides that increase in the presence of hydrogen chloride also contain, in addition to chlorine that neutralizes mobile ions, hydrogen that decreases the density of interface traps.

The mechanisms of instability of charges in interface traps are a consequence of the formation of new interface traps. Almost all of the described mechanisms may be monitored through the increase in the density of interface traps. The mechanism of fixed charge formation has already been described, whereby interface traps are formed simultaneously. The ion drift towards the Si – SiO$_2$ interface may lead to an increase in the density of interface traps. It has been proved that the processes of electric charge injection in the oxide most easily form new interface traps that may be achieved by the IR and HCI processes. It is important to point out that owing to the passage of electrons through the Si – SiO$_2$ interface new interface traps may be formed whereby electrons will not be captured by the traps, which means that the density of charge in them will not change.

As it has already been mentioned, interface traps exchange charge with the semiconductor very rapidly, while this is not the case with the trap centres. On the other hand, a considerable number of defects in the oxide are located in the close vicinity of the interface and they may, like interface traps and regardless of the fact that their microstructure is the same as that of defects deeper in the oxide, exchange charge with silicon. However, unlike real interface traps, these defects are separated from charges in silicon by an energy barrier so that the exchange of charge between them and silicon is carried out through carrier tunnelling whereby the duration of such a process depends to a great extent on the interface distance and the barrier height, and it may range from 1 μs to several years. The long period over which these defects exchange charge with silicon indicates that there is no strict boundary between the effects of charge in the oxide and the effects of interface traps on the electric parameters of MOS transistors. This is why in literature these defects are called boundary traps [12-15]. They may act both as the traps in the oxide and as interface traps. Such nature of the boundary traps may lead to problems in the interpretation of electric measuring results and to difficulties in separating the effects of interface traps and electric charge in the oxide since, depending on measuring conditions (values of the polarization voltage, signal frequency), the boundary traps may behave as interface traps or/and traps in the oxide. By combining appropriate measuring techniques and analysis it is possible to separate the effects of electric charge in the boundary traps [16, 17], which is particularly significant for the characterization of MOS components with a thin gate oxide, where all defects in the oxide are located near the interface and where these defects with their density values are comparable to or even exceed interface traps [14]. In case of thick oxides, as with power MOS transistors, the standard division into the traps in the oxide and interface traps is generally acceptable. In this case, the participation of boundary centres is that at the electric characterization of components will be registered as interface traps or the traps in the oxide, to a great extent depends on the measuring speed and the frequency of the signal that is used during the measurement.

3. Classification of the traps according to their effects on electric characteristics

According to the above, it may be concluded that all charges may be divided into two groups: charges in the oxide and charges at interface traps. Changes of charge densities in

the oxide ΔN_{ot} and interface traps ΔN_{it} are directly responsible for changes of sub-threshold characteristics of MOS transistors during the IR and HCI processes. The participation of a certain type of defects in the values of ΔN_{ot} and ΔN_{it} primarily depends on their electric effects on the charge carriers in the channel of MOS transistors, as well as on their location in space. If the defects may capture carriers from the channel, due to which the sub-threshold characteristic slope decreases, it is deemed that they behave as interface traps and that value ΔN_{it} depends on them. If the defects act on carriers in the channel by attracting or rejecting them with Coulomb forces (depending on the mark of their electric charge), sub-threshold characteristics will be changed due to the change of ΔN_{ot}. It should be emphasized that the influence of defects developed in the IR and HCI processes on ΔN_{ot} and ΔN_{it} is determined primarily by their electric effects and after by their location. This indicates that some defects located at the $Si - SiO_2$ interface may behave as defects in the oxide (influence ΔN_{ot}), while some defects located in the oxide may behave as interface traps (influence ΔN_{it}) [3, 4, 18]. Although the influence of the location of defects on sub-threshold characteristics is smaller than their electric impact, it should not be neglected. For example, during recording sub-threshold characteristics (which is a fast process), only part of these defects may capture carriers from the channel.

The most common techniques for determining densities of the traps in the oxide and at the $Si - SiO_2$ interface are subthreshold-midgap (SMG) [19] and charge pumping (CP) techniques [20, 21] (a detailed description of these techniques is given in Section 6). Based on the position of the traps detected by these techniques, a new classification of the centres became necessary as with the use of the SMG technique both ΔN_{ot} (SMG) and ΔN_{it} (SMG) may be determined, while with the use of the CP technique only ΔN_{it} (CP) may be determined. The use of these two techniques is suitable as there is a great difference in effective frequencies (from several Hz for the SMG technique to 1 MHz for the CP technique). As a slower technique, SMG is used for determining two types of centres: fixed traps (FT) with a density of $\Delta N_{ft} \equiv \Delta N_{ot}$ (SMG) and switching traps (ST) with a density of $\Delta N_{st} \equiv \Delta N_{it}$ (SMG) [22, 23].

Fixed traps (FT) are traps in the oxide that do not exchange charges with Si substrate during recording sub-threshold characteristics by the SMG technique. They are commonly located deeper in the oxide, although they may also be near or at the $Si - SiO_2$ interface. A significant characteristic of FT is that they may be permanently annealed [22, 23].

Switching traps (ST) may be divided into faster switching traps (FST) and slower switching traps (SST). ST may exchange charges with Si substrate during the measurement. The speed of ST depends on their distance from the $Si - SiO_2$ interface [24]. This indicates that all defects developed in the IR or HCI processes, which are located near this interface and are capable of exchanging charges with the substrate, become part of ST. Furthermore, some ST may be located deeper in the oxide so that there is not sufficient time for them to exchange, during the the measurement, electric charges with carriers in the channel, meaning that ΔN_{ft} may contain a certain number of ST. FST which are located at the mere interface and which represent true interface traps (with density ΔN_{it}, i.e. meaning that $\Delta N_{it}(CP) \equiv \Delta N_{fst}$). SST (with density ΔN_{sst}) located in the oxide, near the $Si - SiO_2$ interface are frequently called slow states (SS) [21], anomalous positive charge (APC) [25], switching oxide traps (SOT) [26] or border traps (BT) [24].

Finally, it should be pointed out that during the measurement by the SMG technique, ST exchange charges during the measurement meaning that in case of an n-channel MOS transistor (NMOS) these centres capture charges from the channel but releases them when

the measurement is finished. It has been shown that ST may be temporarily annealed (compensation process) or permanently annealed (neutralization process), however not during the measurement but by exposing components to elevated temperatures.

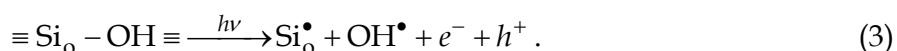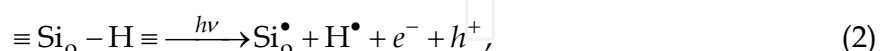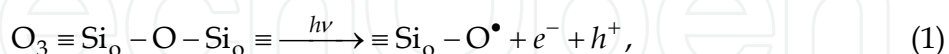### 3.1 Defects in SiO$_2$ and Si – SiO$_2$ interface caused by IR and HCI processes
3.1.1 Formation of electron-hole pairs in SiO$_2$

IR and HCI processes lead to the formation of similar defects in SiO$_2$ since the electrons play a crucial role in the energy transfer to the oxide in both cases, and the difference is in the electron energy. Namely, the secondary electrons released in the oxide by the gamma photons (IR), and the hot electrons (HCI), and, eventually, the secondary electrons released by the hot electrons play a main role in defect creations. However, it has been shown [22, 27-31] that a difference in electron energy has a significant influence on the created defect types. For instance, the highly energetic secondary electrons (the IR case) produce significantly less negatively charged FT than the low-energy hot electrons (the HCI case).

In the case of IR, the gamma photons interact with the electrons in the SiO$_2$ molecules mainly via Compton effect, releasing secondary electrons and holes, i.e. gamma photons break Si$_0$ – O and Si$_0$ – Si$_0$ covalent bonds in the oxide [3] (the index $_0$ is used to denote the oxide). The released electrons (so called "secondary electrons") which are highly energetic, may be recombined by holes at the place of production, or may escape recombination. The secondary electrons that escape recombination with holes travel some distance until they leave the oxide, losing their kinetic energy through the collisions with other secondary electrons or, what is more probable, with the bonded electrons in Si$_0$ – O and Si$_0$ – Si$_0$ covalent bonds in the oxide, releasing more secondary electrons (the latter bond represents an oxygen vacancy).

Each secondary electron, before it has left the oxide or been recombined by the hole, can break a lot of covalent bonds in the oxide producing a lot of new secondary highly energetic electrons, since its energy is usually much higher than an impact ionizing process energy (energy of 18 eV is necessary for the creation of one electron-hole pair [3], i.e. for electron ionization).

In the case of IR processes, gamma radiation breaks both covalent bonds in SiO$_2$ between oxygen atoms and weak $\equiv$ Si$_0$ – H and $\equiv$ Si$_0$ – OH bonds in the oxide. These processes develop in the following reactions [32, 33]

$$\mathrm{O_3 \equiv Si_o - O - Si_o \equiv} \xrightarrow{h\nu} \equiv \mathrm{Si_o - O^{\bullet}} + e^- + h^+, \tag{1}$$

$$\equiv \mathrm{Si_o - H} \equiv \xrightarrow{h\nu} \mathrm{Si_o^{\bullet}} + \mathrm{H^{\bullet}} + e^- + h^+, \tag{2}$$

$$\equiv \mathrm{Si_o - OH} \equiv \xrightarrow{h\nu} \mathrm{Si_o^{\bullet}} + \mathrm{OH^{\bullet}} + e^- + h^+. \tag{3}$$

As it can be noted, these reactions lead to the formation of electron-hole pairs (e$^-$ - h$^+$). A part of the electrons formed by reactions (1)-(3) break covalent bonds in the oxide (reaction (1)). It is obvious that the secondary electrons play a more important role in bond breaking than highly energetic photons, as a consequence of the difference in their effective masses, i.e. in their effective cross section. The electrons leaving the place of production escape the oxide rapidly (for several picoseconds), but the holes remain in the oxide.
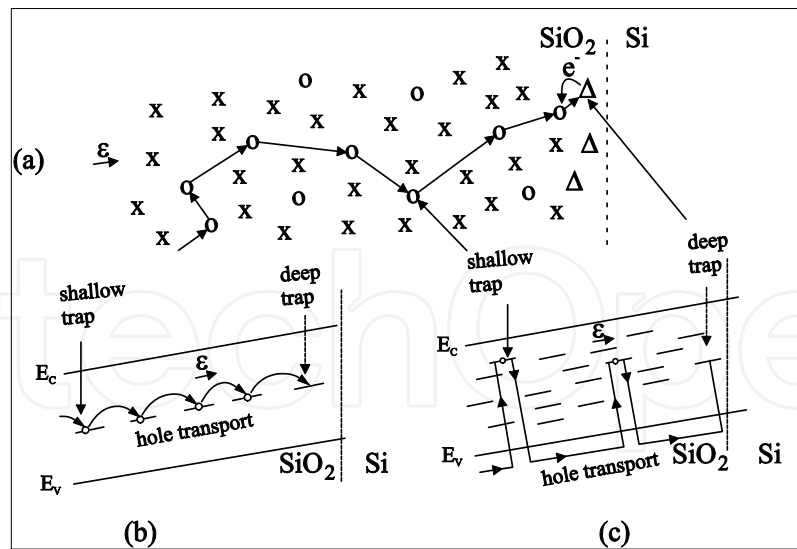
Fig. 3. Space diagram: (a) hole transport through the oxide bulk in the case of positive gate bias. "x" represents unbroken bonds and "o" represents broken bonds (trapped holes at shallow traps), respectively, and "Δ" represents the hole trap precursors near the interface (precursor of a deep trap). Energetic diagram: the hole transport (b) by tunneling between two localized traps and (c) by the oxide valence band.
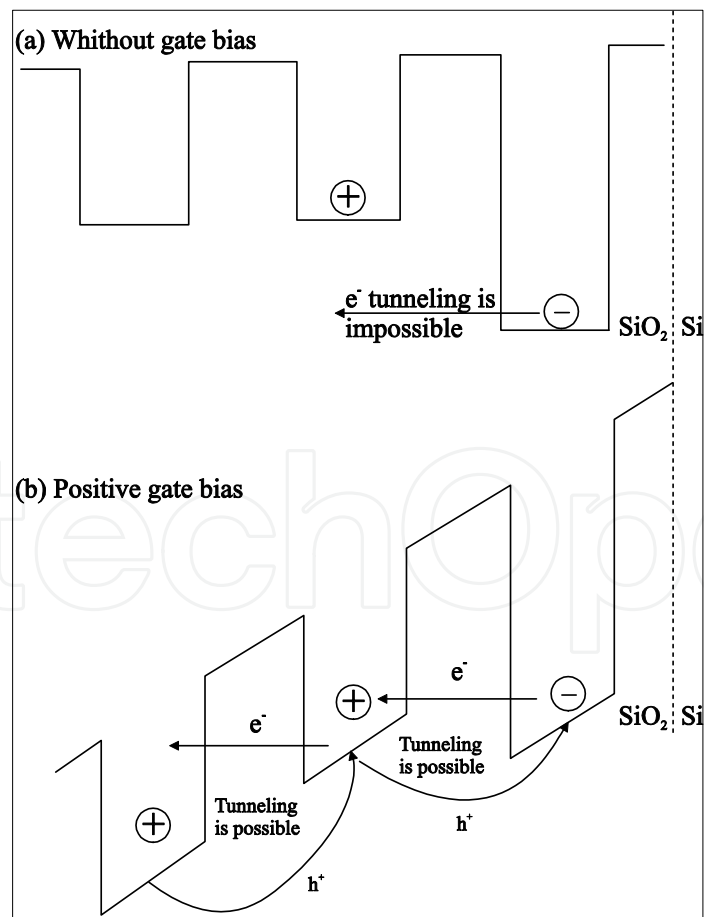

Fig. 4. The electron tunneling between adjacent centers: (a) shallow centre and (b) deep centre.

The holes released in the oxide bulk are usually only temporary, but not permanently captured at the place of production, since there are no energetically deeper centres in the oxide bulk. The holes move towards one of the interfaces (SiO_2 – Si or gate-SiO_2), depending on the oxide electric field direction, where they are trapped at energetically deeper trap hole centres (see Figures 3 and 4). Moreover, even in the zero gate voltage case, the electrical potential due to a work function difference between the gate and substrate is high enough for partial or complete holes moving towards the interface. In addition, some electrons could be trapped at the electron trapping centres of electron capture, but this is not very probable in the IR case [30].

In the case of HCI (e.g. Fowler-Nordheim tunnelling into the gate oxide), the hot electrons, having significantly lower energies than the secondary electrons created by IR, are injected either from the substrate or from the gate. Two cases should be considered: (1) thin oxide ($d_{ox} \leq 10$ nm) and (2) thick oxide ($d_{ox} > 10$ nm). In the former case, the hot electrons, tunnelling into the oxide conduction band, pass the oxide without collisions, since their travel distance is short and, consequently, the probability of the collision with the electrons in the covalent oxide bonds is low [34, 35]. The hot electrons reach the gate, if they are injected from the substrate, or reach the substrate, if they are injected from the gate, where they generate electron-hole pairs. The released (secondary) electrons are attracted by the gate or the substrate electrode, depending on the location of their release, while the generated holes are injected into the oxide.

In the case of thick oxide ($d_{ox} > 10$ nm), a hot electron passing through the oxide has to collide with the electrons bonded in the oxide, giving a certain amount of energy to them and performing the impact ionization [34, 36, 37]. The hot electrons, whose energies are usually higher than 9 eV representing the SiO_2 band gap, can break the Si_0 – O and Si_0 – Si_0 covalent bonds in the oxide by impact ionization and create electron-hole pairs.

The hot and secondary electrons after certain collisions with each other, and what are more probable, with bonded electrons, escape the oxide rapidly, but the holes transport towards one of the interfaces. The high electric field forces the holes to leave their production places, since there is no significant concentration of energetically deep trapping hole created in the oxide bulk, but these centres exist near the interfaces (see Figure 3). Besides, the hot and secondary electrons can produce more electron-hole pairs before they leave the oxide. In addition, some hot/secondary electrons could be trapped at electron centres creating negative charge, which is a very probable mechanism [31].

3.1.2 The defects created by electrons in the impact ionization process

The hot (HCI) and secondary electrons (IR and HCI) passing through the oxide bulk collide with bonded electrons in the most numerous bond: the non-strained silicon-oxygen bond, $\equiv Si_0 – O – Si \equiv$ (it could be also represented as $\equiv Si_0 {}^{\bullet\bullet} O {}^{\bullet\bullet} Si_0 \equiv$, where $\bullet\bullet$ represents two electrons making a covalent bond), by reaction [23]

$$\equiv Si_o - O - Si_o \equiv \xrightarrow{e^-} \equiv Si_o - O^\bullet + {}^+Si_o \equiv +2e^- , \quad (4)$$

$$Si_o - O - Si_o \equiv \xrightarrow{e^-} \equiv Si_o - O^+ + {}^\bullet Si_o \equiv +2e^- , \quad (5)$$
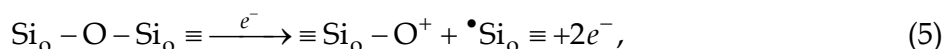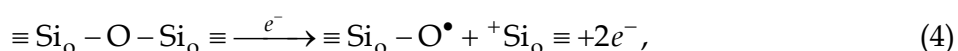
where $\equiv$, the indices $_0$ and $\bullet$ denote three Si_0 – O bonds ($O_3 \equiv Si_0$ – O), silicon atom in the oxide and an electron, respectively.

Reaction (4) represents the most probable reaction in the oxide bulk, since these are the most numerous centres. The formed $\equiv Si_o - O^{+\bullet}Si_o \equiv$ complex is energetically very shallow, representing the temporary hole centre (the trapped holes can easily leave it [11]). The creation of $\equiv Si_o - O^{+\bullet}Si_o \equiv$ complex, given in reaction (5) is less probable (the $\bullet$ denotes the unpaired electron, i.e. "uncoupled spin").

Nevertheless, the strained silicon-oxygen bond ($\equiv Si_0 - O - Si_0 \equiv$), mainly distributed near the interfaces, can also be easily broken by the passing hot/secondary electrons, usually creating the amphoteric non-bridging-oxygen (NBO) centre $\equiv Si_o - O^{\bullet}$, and positively charged E' centre, $\equiv Si_0^+$ [38] known as an E'_s centre [39] (the same process as in reaction (4)). A NBO centre is an amphoteric defect that could be more easily negatively charged than positively by trapping an electron:

$$\equiv Si_o - O^{\bullet} + e^- \rightarrow \equiv Si_o - O^-.\qquad(6)$$

Obviously, the NBO centre, as an energetically deeper centre, is the main precursor of the negatively charged traps (defect) in the oxide bulk and interface regions.

A hot/secondary electron passing through the oxide can also collide with an electron in the strained oxygen vacancy bond $\equiv Si_o - Si_o \equiv$, i.e. $\equiv Si_o^{\bullet\bullet}Si_o \equiv$, which is a precursor of an E'_γ centre ($\equiv Si_o^{\bullet}$) [40], breaking this bond and knocking out an electron:
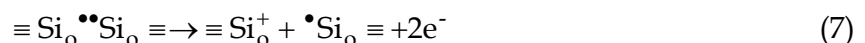
$$\equiv Si_o^{\bullet\bullet}Si_o \equiv \rightarrow \equiv Si_o^+ + {}^{\bullet}Si_o \equiv + 2e^-\qquad(7)$$

Moreover, this is a conventional structural model of the E'_γ centre: a hole trapped at an oxygen monovacancy ($\equiv Si_o^{+\bullet}Si_o \equiv$). The oxygen vacancy bonds are mainly distributed in the vicinity of interfaces.

The mentioned reactions could occur anywhere in the oxide: near the interfaces and in the oxide bulk. The trapped charge can be positive (oxide trapped holes) and negative (oxide trapped electrons) and the former is more important, since the holes trapping centres are numerous, including three types (E'_s, E'_γ and NOB centres), compared with one electron capture (NBO). The holes and electrons captured near the Si – SiO$_2$ interface have the greatest effect on MOSFET characteristics, since they have the strongest influence on the channel carriers.

3.1.3 Hole transport

The holes trapped at $\equiv Si_0^+$ centres form oxygen vacancies, and strained silicon-oxygen bonds are energetically deep and steady, at which the holes can remain for a longer time period, i.e. their filling with electrons is more difficult in relation to some shallowly captured holes. These centres exist near both interfaces, especially near the Si – SiO$_2$ interface. The holes created and trapped at the bulk defects (reaction (4)), representing energetically shallow centres, are forced to move towards one of the interface under the electric field, where they are trapped at deeper traps, since there are a lot of oxygen vacancies, as well as a lot of strained silicon-oxygen bonds near the interfaces, grouping all trapped positive charge there. The holes leave the energetically shallow centres in the oxide spontaneously and they are transported to the interface by a hopping process using either shallow centres in the oxide (Figure 3(b); the holes "hop" from one to another centre) or
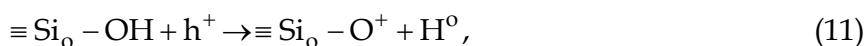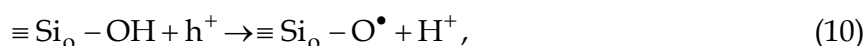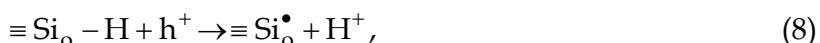
centres in the oxide valence band (Figure 3(c)) [41]. Figure 3 displays the holes transport in the space for the positive gate bias (a) and the energetic diagram for the possible mechanisms of this space process ((b) and (c)).

Figure 4 shows a possible hole (electron) tunnelling mechanism between adjacent centres: a shallow centre and deep centre. Figure 4(a) shows the case without gate bias, for the Si – SiO$_2$ interface. In this case, the holes, i.e. electrons tunnelling between these centres, are not possible. The holes are factious species representing the electron unoccupied places, and the hole movement is in fact the movement of bonded electrons, however the electron movement is the movement of free electrons.

When the MOS transistor is positively biased (Figure 4(b)), the bonded electron can tunnel from the deep centre to the shallow centre. It represents the hole tunnelling from shallow to deep centres, being permanently trapped at a deep centre. The electron, which is now in the shallow centre, can easily tunnel from this shallow centre to the next adjacent shallow centre, enabling the holes transport towards the interface. The pictures are similar for the negative gate bias [31].

3.1.4 The defects created by the holes

The holes can be created either in the oxide bulk (thick oxide) or in the gate/substrate and injected into the oxide bulk (thin oxide). Moving throughout the oxide, the holes can react with the hydrogen defect precursors ($\equiv Si_0 - H$ and $\equiv Si_0 - OH$) and create the following defects [42].

$$\equiv Si_o - H + h^+ \rightarrow \equiv Si_o^\bullet + H^+, \tag{8}$$

$$\equiv Si_o - H + h^+ \rightarrow \equiv Si_o^+ + H^o, \tag{9}$$

$$\equiv Si_o - OH + h^+ \rightarrow \equiv Si_o - O^\bullet + H^+, \tag{10}$$

$$\equiv Si_o - OH + h^+ \rightarrow \equiv Si_o - O^+ + H^o, \tag{11}$$

The hot and secondary electrons may also interact, in a similar way, with these defect precursors. However, these precursors are not so important for the hot and secondary electrons, since their concentration is significantly lower than the concentration of the precursors representing the non-strained silicon-oxygen bonds. Moreover, it could not be expected that the holes break bonds in the non-strained silicon-oxygen bonds. Because of that, the precursors described in reactions (8-11) are only important for the holes that are transported through the oxide since the hydrogen is relatively weakly bounded and the holes can easily break these bonds. Reactions (8-11) are particularly important for the creation of the interface trap since they produce the hydrogen ion H$^+$ and hydrogen atom H$^\circ$, which take part in defect creation at the Si – SiO$_2$ interface. The existence of these precursors in the oxide and, particularly, at the Si – SO$_2$ interface is very reasonable, since annealing in the hydrogen ambient is a standard step during the manufacture of numerous MOS devices.

When the holes reach the interface, they can break both the strained oxygen vacancy bonds $\equiv Si_0 - Si_0 \equiv$, forming $E_\gamma^{'}$ centres [38]

$$\equiv Si_O - Si_O \equiv + h^+ \rightarrow \equiv Si_O^{\bullet} + \equiv Si_O^+ \tag{12}$$
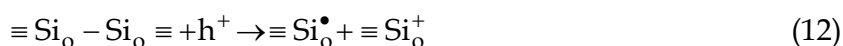
and the strained silicon-oxygen bonds $\equiv Si_0 - O - Si_0 \equiv$, creating the amphoteric NBO centres $\equiv Si_O - O^{\bullet}$ and $E_s^{'}$ $(\equiv Si_O^+)$ centres:

$$\equiv Si_O - O - Si_O \equiv + h^+ \rightarrow Si_O - O^{\bullet} \equiv Si_O^+ \tag{13}$$
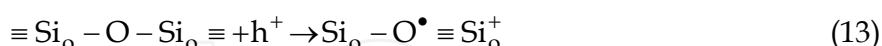
It could be assumed that the strained Si – O bonds, $\equiv Si_0 - O - Si_0 \equiv$ and oxygen vacancy, $\equiv Si_0 - Si_0 \equiv$, represent the main defect precursors in the oxide bulk and at the interfaces. However, these precursors exist mainly near the interface. It should be noted that $E_{\gamma}^{'}$, $E_s^{'}$ (reactions (12) and (13)) and NBO centre (reaction (13)) represent energetically deeper hole and electron trapping centres, respectively. The energetic levels of the defects created after the holes at $E_{\gamma}^{'}$ and $E_s^{'}$ centres and electrons at NBO centre, respectively, have been trapped, can be various. In the chemical sense same defects show different behaviours depending on the whole bond structure: the angles and distances between the surrounding atoms. It could be assumed that these defects represent fixed traps (FT) and slow switching traps (SST) [29, 30]. They can be positively and negatively charged, as well as neutral.

In the literature, there are many controversies about the oxide defects types induced by the IR and HCI processes and there are different names for the same or similar defects (see [23] for more details).

3.1.5 Gate oxide/substrate (SiO₂ – Si) interface

The defects at the Si — SiO₂ interface, known as the fast switching traps (FST), or true interface traps, represent an amphoteric defect $Si_3 \equiv Si_s^{\bullet}$ a silicon atom $\equiv Si_s^{\bullet}$ at the Si — SiO₂ interface back bonded to three silicon atoms from the substrate $\equiv Si_3$ and the FST are usually denoted as $\equiv Si_s^{\bullet}$ or $Si^{\bullet}$. They can be directly created by incident photons/hot electrons tunnelling from the substrate or the gate [43, 44], however this amount can be neglected. The direct creation of FST is only emphasized in the case of hot electrons for the positive gate bias applied to thin oxides (d_{ox} < 10 nm), where the electrons, tunnelling in the conduction band of oxide, pass the oxide without any collisions (the probability for collision process is small), accelerating themselves and reaching the interface with energy enough for an interface defect creation. Besides direct creation, the FST are mainly created by trapped holes (*h⁺* model) [45-48] and by hydrogen released in the oxide (hydrogen-released species model - *H*-model) [49-51].

The *h⁺* model proposes that a hole trapped near the interface create FST, suggesting that an electron-hole recombination mechanism is responsible [46]. Namely, when holes are trapped near the interface and electrons are subsequently injected from the substrate, recombination occurs. The interface trap may be formed from the energy released by this electron-hole recombination. It was supposed [23] that FST can be created by the reaction:

$$\equiv Si_O^+ + e^+ + \equiv Si_s - Si_s \rightarrow \equiv Si_O^{\bullet} + \equiv Si_O^{\bullet} + \equiv Si_O^{\bullet}. \tag{14}$$
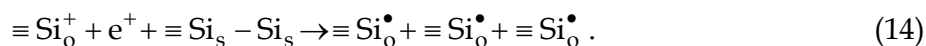
The main shortcoming of the h⁺ model is its impossibility in explaining the delayed creation of FST [51]. However, this fact cannot completely disqualify this model, and we can suppose that part of interface traps are created by it.

The H model proposes that H^+ ions, released in the oxide by trapped holes (reactions (8) and (10)), drift towards the $Si - SiO_2$ interface under the positive electric field. When an H^+ ion arrives at the interface, it picks up an electron from the substrate, becoming a highly reactive hydrogen atom $H°$ [52]:

$$H^+ + e^- \rightarrow H°. \tag{15}$$

Also, according to the *H* model, the hydrogen atoms $H°$ released in reactions (9) and (11) diffuse towards the $Si - SiO_2$ interface under the existing concentration gradient.

Highly reactive $H°$ atoms react without an energy barrier at the interface producing FST throughout the following reactions [53-55]:

(i) The creation of interface trap $Si_s^\bullet$, when $H°$ reacts with an interface trap precursor $Si_s - H$ [52]

$$Si_s - H + H^o \rightarrow Si_o^\bullet + H_2. \tag{16}$$

or an interface trap precursor $Si_s - OH$:

$$Si_s - OH + H^o \rightarrow Si_o^\bullet + H_2O. \tag{17}$$

Many investigations have shown that the P_{b_0} and P_{b_1} centres which exist at the (100) interface represent interface traps [56-58]. The P_{b_0} defect has the following structure: $Si_s \equiv Si_{s_0}^\bullet$, but the structure of P_{b_1} defect, here denoted as $\equiv Si_{s_1}^\bullet$, is not known (the remaining three bonds of the $\equiv Si_{s_1}^\bullet$ defect can be bonded to various species [59]).

(ii) The passivation of the interface traps, when $H°$ reacts with previously formed (fabrication process or IR and HCI processes induced) interface trap [53, 60]

$$Si_s^\bullet + H^o \rightarrow Si_s - H. \tag{18}$$

(iii) Dimerization of hydrogen, when $H°$ reacts with another $H°$ also existing near the interface [61, 62]

$$H° + H° \rightarrow H_2 \tag{19}$$

Reactions (16) and (17) are most probable at the start of the interface trap creation, since both have a large number of $Si_s - H(OH)$ precursors, and the effective cross sections for reactions (16) and (17) are higher than for reactions (18) and (19) [52].

4. Annealing of MOS components after IR and HCI processes

For the electric characteristics of MOS components, changes of charge in the oxide and changes in interface traps are significant both during the IR and HCI processes and after the end of these processes. Some of the mechanisms occurring after the end of the IR and HCI processes remain active, and new mechanisms also develop and last for a longer period of time. The generation of charge in the oxide takes place as long as an IR or HCI process goes on. When these processes end, the density of charge in the oxide starts to decrease, while the generation of interface traps continues and this process may occur for a longer period of

time [61, 63-73]. A process during which positive charge density in the oxide decreases with a simultaneous increase in interface traps density after an IR or HCI process, in which a large quantity of positive charge was incorporated in the oxide, is called annealing. This term is not fully adequate although it is frequently used, as only charge in the oxide is commonly "annealed" while the density of interface traps may increase. MOS components annealing may be performed spontaneously (in air atmosphere, at room temperature, without polarization), or at lowered or elevated temperatures, or in the presence of various intensity and direction electric field.

A number of experimental results [24, 74-80] have shown that the density of interface traps during annealing mainly does not change, while the density of trapped charge in the oxide decreases. Several models are proposed for the trapped charge annealing [75, 77]. It has been observed that during annealing part of trapped charge is permanently burnt-in (neutralized), while the other part may only be compensated, which leads to the effect of "inverse burn-in" (apparent increase in the density of trapped charge during annealing at gate negative polarization), which is attributed, by a group of authors, to the existence of the so-called Switching Oxide Trap (SOT) centres [77, 78]. Another group of authors attribute it to the existence of the so-called Anomalous Positive Charge (APC) centres [24, 79, 80]. Both groups explain inverse burn-in by the exchange of charge with substrate whereby such exchange, in case of SOT, is performed by electron tunnelling as the appropriate levels of these centres lay at the height of the substrate conductive zone [78], while APC are, similarly to interface traps, capable of performing direct exchange with the substrate as their energy levels are at the level of the forbidden zone [24, 79, 80]. Regardless of their different approaches, both groups have practically contributed to establishing the fact that SOT and APC are most probably the same centre, i.e. E' centre that, depending on the conditions of the experiment and measurement may exhibit various properties (burn-in, inverse burn-in or exchange of charges) and may be registered as a interface trap or the so-called boundary centre of capture.

A characteristic of these models of charge burn-in is that they are related to captured charge in the oxide and that they mainly do not exchange charge at interface traps, i.e. that they consider changes in the density of captured charge during annealing separately and independently of changes in the density of interface traps. This may be deemed the main disadvantage of this group of models, particularly because there are numerous experimental results that may be very accurately described by the above-described h^+ and H models. It is important to point out that according to h^+ and H models, the mechanisms of the formation of defects in the oxide and at the $Si - SiO_2$ interface take place not only during the IR or HCI processes, but after their cessation as well. This practically means that these two models are more comprehensive and more acceptable for explaining the annealing process than the charge burn-in model. It is important to emphasize here that most experimental results indicate the dominant role of hydrogen and that the H model in many cases gives a real picture of the processes in the oxide and at the $Si - SiO_2$ interface. Therefore, the processes of the captured charge density decrease and simultaneous increase in the density of interface traps, which take place within a shorter or longer time after the cessation of the IR or HCI processes, may be best described by the H model. However, this model may not describe the annealing processes in case in which the generation of interface traps begins and ends during mere tension so that their density do not increase during the annealing. In addition, none of the models mentioned so far may explain the phenomenon of a decrease in the

density of interface traps during the annealing for a long period [81-83] and a latent increase in the density of interface traps [28,84]. Furthermore, none of the mentioned models may explain the phenomenon of an increase and then decrease in the density of interface traps during annealing for a longer period of time [85-88]. On the other hand, the latent generation of interface traps that occurs during annealing is manifested through rapid increase in their density after reaching apparent saturation, and simultaneous rapid decrease in the density of trapped charge, which is characteristic of MOS transistors the oxide of which contains a high concentration of oxygen and bounded hydrogen [87]. It is deemed that it is not the hydrogen originating from the mere oxide that is responsible for the latent increase in the density of interface traps, but rather the hydrogen which is, during the IR or HCI processes, released in the form of molecules in the adjusted layers (polysilicon gate, protective oxide). The hydrogen molecule diffuses towards the gate oxide and through it further towards the oxide-semiconductor interface in the vicinity of which it reacts with a positively charged centre of capture, according to the following reaction:

$$\equiv Si_0^+ + H_2 \rightarrow \equiv Si_0 - H + H^+. \tag{20}$$

As it can be seen from the last reaction, the captured charge is neutralized and hydrogen ions are released which then diffuse towards the $Si - SiO_2$ interface and participate in the formation of a interface trap (reactions (16) and (17) [89]). The late increase in the density of interface traps is attributed to the long-lasting diffusion of hydrogen molecules which is particularly difficult through the polysilicon gate, as well as to a possibility that oxygen vacancies slow down the movement of hydrogen in the oxide [67, 89].

This explains the latent increase in the density of interface traps but cannot explain their decrease that occurs after the latent increase. Owing to this, based on experimental results of the annealing of irradiated power VDMOS transistors, the so-called Hydrogen-Water (H – W) model has been proposed, which can explain the behaviour of the densities of interface traps and captured charge during annealing including both the latent increase and the decrease in the density of interface traps [28, 85, 86]. According to this model, all free hydrogen (present in the oxide before the IR or HCI processes or released during these processes) is utilized for the so-called conventional generation of interface traps that ends with the cessation of the IR or HCI processes and/or in the initial stage of annealing immediately after the cessation of these processes. In the further stage of annealing, for initiating the latent generation of interface traps it is necessary and sufficient that a certain quantity (even a small one) of hydrogen ions appears at the interface. The origin of these ions will be discussed later. When these late ions reach the $Si - SiO_2$ interface under the influence of the electric field, they takeover electrons from the substrate (reaction 15) and form neutral atoms of hydrogen that may participate in one of the following processes:

(i) formation (depassivation) of interface traps (reaction (16)); (ii) pasivation of interface traps (reaction (18)); and (iii) dimerization (reaction (19)). Reaction (18) is more probable than the other two reactions because the concentration of $\equiv Si_s - H$ precursor is higher than the concentration of interface traps ($\equiv Si_s^{\bullet}$), as well as because the cross section of reactants is larger in this reaction in comparison to the other two, so that the density of interface traps begins to increase. In reactions (16) and (19), hydrogen molecules are released and therefore their concentration at the interface increases (concentration gradient occurs) due to which these molecules diffuse towards the inside of the oxide whereby on their way many of them react on with positively charged traps. The following reaction commonly occurs:

$$\equiv Si_0{}^+ + H_2 \rightarrow \equiv Si_0 - H + H^+. \tag{21}$$

Hydrogen ions formed in this reaction drift towards the interface, takeover electrons from the substrate and the processes (i) - (iii) are repeated. In this manner, for further formation of interface traps an additional source of H^+ ions is provided, and at the same time, burn-in of captured charge is performed, in compliance with results according to which the latent increase in the density of interface traps corresponds to the decrease in the density of captured charge.

Water molecules are deemed responsible for the decrease in the density of interface traps that occurs after the latent increase. Water molecules are mainly bounded (physically or chemically) in the thermal and/or protective CVD oxide. During annealing, they may be released (more expressed at higher temperatures) and after that they slowly diffuse towards the $Si - SiO_2$ interface where they finally react with interface traps according to the following reaction:

$$\equiv Si_s^{\bullet} + H_2O \rightarrow \equiv Si_s - OH + H^o. \tag{22}$$
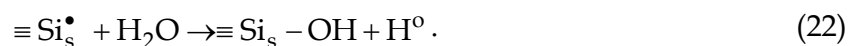
As it can be seen from the last reaction, the final contribution of water molecules after long annealing is the passivation of interface traps. Namely, in reaction (22) one interface trap is passivated and a neutral hydrogen atom formed in the same reaction may react with (i) another neutral hydrogen atom (reaction (19)) which will not change the result of reaction (22), meaning that one interface trap remains passivated, (ii) with the $\equiv Si_s^{\bullet}$ defect (reaction (18)) with which one more interface trap is passivated, or (iii) with the $\equiv Si_s - H$ precursor (reaction (16), the only one with which the effect of reaction (22) is annulled). In this manner, the H – W model covers the latent increase and, afterwards, the decrease in the density of interface traps. Based on this model, it may be concluded that a small quantity of any type of hydrogen particles (ions, neutral atoms or molecules) may trigger the latent generation of interface traps. Although the authors of this model [28] mention a possibility that this generation is triggered by hydrogen ions captured in the traps in the oxide, or by hydrogen molecules formed in reaction (22) from the water molecule after its slow diffusion through the oxide, they still believe that for triggering the latent increase in the density of interface traps, hydrogen molecules originating from the protective CVD oxide and/or polysilicon gate are most probably responsible. The cause of their late arrival to the oxide-semiconductor interface may be the reduced speed of diffusion through polysilicon, even through the gate oxide (as a consequence of a decrease in the diffusion constant in the oxide owing to the IR processes), as well as a possibility that hydrogen molecules may have reduced speed by being captured at oxygen vacancies from which they are subsequently released.

5. Influence of charges in the oxide and interface traps on MOS transistors parameters

Charges in the oxide, as well as interface traps have a significant influence on the characteristics of MOS transistors. The transfer characteristic of MOS transistors in the saturation region may be described by the following expression [2, 4]:

$$I_D = \beta \left(V_G - V_T \right)^2 / 2 , \tag{23}$$

where β is an amplifying factor and may be expressed as

$$\beta = \frac{\mu W C_{ox}}{L} \ .$$

(24)

In expressions (23) and (24), I_D is drain current, V_G is voltage at the gate, V_T is threshold voltage, μ is electric mobility in the channel, $C_{ox} = \varepsilon_{ox}/d_{ox}$ is the capacitance of the gate oxide per area unit (ε_{ox} and d_{ox} represent dielectric constant and oxide thickness, respectively), while W and L are the width and effective length of the channel, respectively. Based on these expressions it may be noticed that charges in the oxide and in interface traps may influence the electric characteristics of MOS transistors only through the influence on threshold voltage and mobility of carriers in the channel. Positive charge in the oxide influences carriers in silicon by its electric field, attracting electrons towards the interface and rejecting holes from it. This leads to a change in threshold voltage which is decreased with NMOS, and increased (by absolute value) with PMOS transistors. At the same time, electrons approaching the interface with NMOS transistors should increase, while holes moving away with PMOS transistors should decrease the dispersal of carriers on the uneven areas of the interface, by which the mobility of carriers would be decreased with NMOS, and increased with PMOS transistors. However, it is deemed that charges in the oxide have a low influence on the carrier mobility and that their impact is not electrostatic but it is rather a consequence of the carrier capturing process [4, 90]. Namely, carrier capture in interface traps will not change the total amount of charge in the channel region, which means that no electric effect is produced. The influence of interface traps may be explained in the following way: interface traps capture a certain number of electrons or holes induced by a change in the surface potential caused by the gate voltage, due to which the formation of a channel requires higher gate voltage comprising an increase in the threshold voltage both with NMOS and PMOS transistors. At the same time, capturing carriers at the interface traps with both types of MOS transistors leads to a decrease in the number of conductive carriers in the channel (to a decrease in current) which is manifested in a decrease in the slope of transfer characteristics, a decrease in the amplifying factor and thus a decrease in the mobility of carriers μ. Namely, the greater the density of interface traps, the greater the number of captured carriers in relation to a total number of induced carriers, which is manifested in an apparently greater mobility degradation. Through such a conclusion, the real situation (decreased number of mobile carriers in the channel) is replaced with an apparent one (unchanged number of mobile carriers with reduced mobility), but the effect on the conductivity in the channel (i.e. on the transistor current) remains absolutely the same. Due to this, the use of a simpler model given in expressions (23) and (24), whereby the so-called effective (or apparent) mobility is used instead of the real one, is much more purposeful than complicated consideration of the real situation which would require the knowledge about the accurate function of the interface trap energy levels distribution in the forbidden zone of silicon. This claim is supported by the definition of the mobility of carriers according to which this mobility is not a physical value but only the coefficient of proportionality in the expression for the dependence of drift rate on electric field. Therefore, the value of mobility is not constant but it is rather necessary to adjust it in order to maintain the applicability of Ohm's law to the transport of current in the semiconductor [4]. Owing to this, the concept of effective mobility is common in modelling the effects of various factors on transport processes in the semiconductor, such as doping effects, effects of electric field,

high levels of injection, surface dispersal, crystal orientation, as well as effects of charge in the oxide and effects of interface traps [4, 91-93]. Further in this text, the term mobility will be used, but it will comprise the effective value.

The considerations given so far suggest that with NMOS transistors a decrease in mobility should be expected with an increase in the density of either interface traps or charge in the oxide. Considering the dominant influence of interface traps, a decrease in mobility in general should be also expected for PMOS transistors, even in the case in which the density of charge in the oxide increases somewhat more rapidly than the density of interface traps. In literature, however, there are examples of an increase in mobility, one of which was recorded in a study of PMOS transistors with a polysilicon gate [94]. In the same experiment, PMOS transistors with an aluminium gate were irradiated and an expected decrease in mobility was recorded, while an expected increase in threshold voltage was almost the same with both types of transistors. By additional analysis, a great increase in the density of charge in the oxide was determined, approximately equal with both types of samples while at the same time an increase in the density of interface traps was much greater with the samples with aluminium gates in relation to the samples with polysilicon gates. An increase in mobility with PMOS transistors with polysilicon gates was explained by their high resistance to the formation of interface traps, i.e. by a disproportionately great increase in the density of charge in the oxide in relation to the increase in the density of interface traps during the IR processes. This result is not in accordance with the conclusion that charge in the oxide has low influence on mobility. It may be deemed even controversial as similar results with PMOS transistors with polysilicon gates [95, 96] showed the opposite result, i.e. reduced mobility. However, regardless of the contradiction of these results, it may be concluded that charge in the oxide has significant influence on the mobility of carriers in the channel, although such influence is lower than the influence of interface traps. This is indicated by the results of researches with PMOS dosimetric transistors which show that a considerable increase in the density of charge in the oxide leads to an increase in mobility [97].

Many experimental results have shown that the influence of charge in the oxide and the influence of interface traps on the threshold voltage of MOS transistors may be modelled by the following expression [98]:

$$V_T = V_{T0} \mp \frac{qN_{ot}}{C_{ox}} + \frac{qN_{it}}{C_{ox}} \tag{25}$$

where V_{T0} is the threshold voltage of an ideal MOS transistor without any charge in the oxide and without interface traps, while the second and third terms include their influence, whereby the sigh "-" in front of the second term refers to an NMOS transistor, while the sign "+" refers to a PMOS transistor. Therefore, the influence of charge in the oxide (qN_{ot}) is included as voltage drop that creates an electric field on the oxide, i.e. qN_{ot}/C_{ox}. On the other hand, it is claimed that the influence of interface traps on carriers in the channel reflects in their capture, so a that part of carriers induced in the channel by the gate voltage remain immobile. If, for given gate voltage, the number of captured carriers from the channel per area unit is qN_{it}, then part of the gate voltage amounting to qN_{it}/C_{0X} is spent not on the formation of mobile carriers but rather on the formation of captured ones. By this amount the gate voltage required for the formation of a channel is increased (according to

absolute value), which means that the influence of interface traps on threshold voltage is qN_{it}/C_{ox} .

In order to give consideration to the influence of charge in the oxide and of interface traps on mobility, several models may be used [99-101] which are based on the empirical expression for the dependence of effective mobility on charge in the oxide and the concentration of admixtures in the channel of NMOS transistors given in the paper [102]

$$\mu = \frac{\mu_0}{1 + \alpha N_{ot}} , \tag{26}$$

where μ_0 = 3440 – 164 1og N_A [cm^2/(Vs)] is mobility without charge in the oxide (N_A is the concentration of acceptor impurities expressed in cm^3) and α_{ot} = - 1.04 · 10^{-12} + 1.93 log N_A [cm^2]. Based on later researches [98] it has been shown that the above expression should be modified taking into account the contribution of interface traps as well. Therefore, mobility may be expressed in the following way:

$$\mu = \frac{\mu_0}{1 + \alpha_{it}N_{it} \pm \alpha_{ot}N_{ot}} , \tag{27}$$

where coefficients α_{it} and α_{ot} depend on technology, and due to greater influence of charge on interface traps $\alpha_{it} > \alpha_{ot}$. The sign "+" in front of the third term in the denominator refers to NMOS transistors, while the sign "-" refers to PMOS transistors. This is in accordance with the observation above that charge in the oxide, being almost always positive, may lead to an increase in mobility with PMOS transistors (although this happens rarely owing to the dominant influence of charge on interface traps).

Due to the increase in interface traps, the leakage current of the inversely polarized connection increases as well. Leakage current consists of free electrons and holes generated in the depletion region of the inversely polarized junction, which are transferred through the field into the n-type or p-type semiconductor. The generation of free holes in the presence of interface traps takes place through the transfer of electrons from the valence band to the energy level of interface traps near the Fermi level, while the generation of free electrons takes place through the transfer of electrons from the energy level of interface traps near the Fermi level to the conductive band of the semiconductor. Therefore, electrons pass from the valence band into the conductive band through interface traps. This process leads to the occurrence of leakage current of the inversely polarized junction. The leakage current directly depends on the density of interface traps.

The low-frequency noise of MOS transistors also increases with the increase in the density of interface traps. This noise appears because interface traps capture carriers that move through the channel retaining them for a certain period of time and then emitting them back into the channel. This is a process of accidental nature and it modulates the channel current which may be particularly observed at low frequencies and high densities of interface traps.

The avalanche breakdown of the inversely polarized drain-substrate junction is a consequence of the presence of charge in the gate oxide originating from mobile ions, fixed charge, and charge in the traps. The sum of all these charges gives effective charge per area unit which is almost always positive. This charge transforms the drain-substrate p$^+$-n junction in PMOS transistors into the p$^+$-n$^+$ junction meaning that breakdown voltage is reduced. In NMOS transistors, the substrate is of p-type, and charge in the oxide depletes it

leading to a reduction of the field at the drain-substrate n+-p junction and thus to an increase in avalanche breakdown voltage.

It is important to emphasize that it is impossible to give an appropriate typical quantitative picture of the described instabilities. There are differences not only in the values of changes in corresponding parameters, but also in the occurring instability mechanisms, and as it has been already mentioned these differences may lead to changes in an observed parameter even in opposite directions. The next important difference is in time dependencies of respective instabilities meaning that even if the same initial instability is manifested with this group of MOS transistors, the instabilities may significantly differ after some time. In addition, time dependences of respective parameters instabilities may have very complex forms as they are frequently defined by simultaneous activities of several mechanisms. Such differences in the behaviour of MOS transistor parameters are conditioned by differences in the manner of the gate oxide formation and by conditions of the component exploitation, and they may lead to qualitatively different forms of instabilities of the MOS transistor parameters.

6. Techniques of determining electric charge density in oxide and interface traps

Change of electric charge density in gate oxide and interface traps, which occur during IR and HCI processes, are studied through the application of certain techniques. An important role in that procedure is played by changes in electric parameters, primarily threshold voltage and amplification factor (considering that the influence of electric charge in oxide and interface traps on electric characteristics are transferred through them), which are determined on the basis of recorded I-V characteristics.

It is already known that a change in threshold voltage of MOS transistors due to IR and HCI processes can be expressed in the following way:

$$\Delta V_T = \Delta V_{ot} + \Delta V_{it} , \tag{28}$$

where ΔV_{ot} and ΔV_{it} are contributions to the change in threshold voltage due to the electric charge in oxide and in interface traps, respectively. By using the expression (25), the change in surface electric charge density in oxide ΔN_{ot} and the change in interface traps density ΔN_{it} can be determined as

$$\Delta N_{ot} = \pm \frac{C_{ox}}{q} \Delta V_{ot} , \; \Delta N_{it} = \frac{C_{ox}}{q} \Delta V_{it} , \tag{29}$$

where the signs "+" and "-" refer to p-channel and n-channel MOS transistors, respectively. ΔV_T (expression (28)) represents an experimentally determined value of threshold voltage $\Delta V_T = V_T - V_T(0)$ and the corresponding change in the electric charge densities in oxide $\Delta N_{ot} = N_{ot} - N_{ot}(0)$ and the interface traps $\Delta N_{it} = N_{it} - N_{it}(0)$ (expression (29)), where $V_T(0)$, $N_{ot}(0)$ and $N_{it}(0)$ are values of corresponding values prior to, and V_T, N_{ot} and N_{it} after IR or HCI processes.

There are several techniques used to determine electric charge density, and/or to separate the influence of electric charge density in gate oxide and interface traps, and each of these techniques has its own advantages and deficiencies [3,103]. Here we will describe the two

techniques most commonly used today. These are subthreshold midgap (SMG) technique which is used to determine electric charge density in gate oxide and interface traps, and charge pumping (CP) technique which is used only to determine change in interface traps density.

6.1 Subthreshold midgap technique

The subthreshold midgap (SMG) technique is based on the analysis of change in the subthreshold transfer characteristics of MOS transistors [19]. Theoretically, the subthreshold characteristic (dependence of drain current on the gate voltage for the given voltage on drain V_{DS}) can be described by the expression [2]:

$$I_D = \mu \frac{W}{L} \cdot \frac{N_A L_D kT}{\sqrt{2}} \left(\frac{n_i}{N_A} \right)^2 \exp\left(\frac{q\varphi_s}{kT} \right) \cdot \left[1 - \exp\left(-\frac{qV_{DS}}{kT} \right) \right] \cdot \sqrt{\frac{kT}{q\varphi_s}}, \tag{30}$$

where N_A is the concentration of impurities in the p-channel area, L_D is Debye length, φ_s is surface potential which represents the voltage function at the gate [2]. The last expression clearly expresses exponential dependence of drain current on the surface potential, and thereby on the gate voltage as well. The subthreshold characteristics of n-channel MOS transistor prior to and after being subjected to the IR process, as well as the necessary elements to explain the technique are given on the Figure 5 [19].
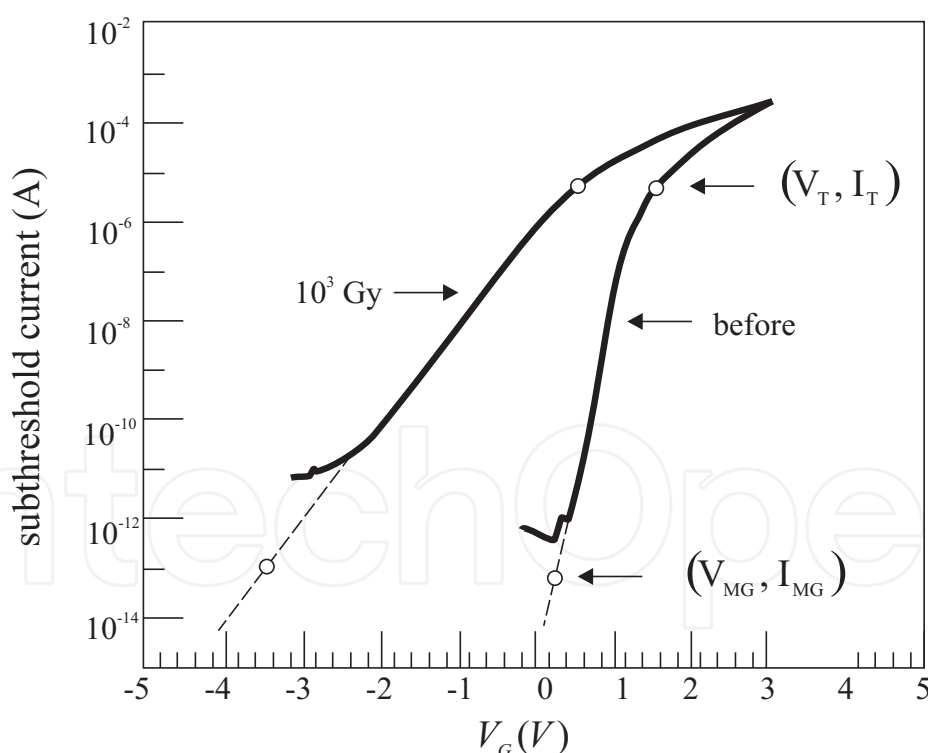
Fig. 5. Subthreshold current as a function of gate voltage, before irradiation and after gamma radiation dose of 10³ Gy.

From the viewpoint of subthreshold characteristic, an increase in interface traps density, as already mentioned before, under the influence of IR or HCI processes, is manifested through the change in its slope. Namely, as an increase in gate voltage is followed by capture of

carriers in interface traps, the "response" of surface potential will be decreased, and along with it, the drain current as well, to the changes in gate voltage, and therefore the voltage of subthreshold characteristic will be milder.

In case when Fermi level of semiconductors on the Si – SiO₂ interface is located in the middle of the forbidden zone, the total electric charge on interface traps, regardless of the disposition within the forbidden zone of the substrate, is equal to zero. This means that the shift on the voltage axis between two subthreshold characteristics in that case is solely the consequence of change in electric charge density in oxide. The gate voltage in which Fermi level on the *Si – SiO₂* interface is located in the middle of the forbidden zone is marked with V_{MG} (midgap voltage), and is calculated as abscissa of the point (V_{MG}, I_{MG}) on the subthreshold characteristics. The above-mentioned point is determined on the basis of its ordinate, i.e. I_{MG} current (midgap current) which is calculated on the basis of the expression (30) by replacing appropriate values of surface potential $\varphi_s = \varphi_F$ and experimentally determined mobility μ. As the mobility of carriers depends on several parameters such as temperature, admixture concentrations, degree of component degradation (and thereby also the electric charge density in the oxide and interface traps), it must be determined experimentally for each component and for each radiation dose or duration of HCI process. It is determined from the slope of the curve $\sqrt{I_D} = f(V_G)$ [19], as the drain current of MOS transistors in saturation is given through the following expression:

$$I_D = \mu \frac{W}{2L} C_{ox} (V_{GS} - V_T)^2 \ . \tag{31}$$

The I_{MG} current in V_{MG} voltage is very small (order of magnitude of picoampere or smaller, depending on the size of transistor), i.e. it is often significantly smaller than the lowest measured level of subthreshold current, determined by the leakage current. For this reason, the point (V_{MG}, I_{MG}) is located on the extension of the most linear part of subthreshold characteristics marked by the dashed line on Figure 5. Therefore, change in electric charge density in oxide, formed under the influence of IR or HCI process is generated as [19]

$$\Delta N_{ot} = \frac{C_{ox}}{q} \big(V_{MG}(0) - V_{MG} \big) \tag{32}$$

where $V_{MG}(0)$ is the value of V_{MG} voltage prior to IR or HCI processes.

Other two important points on the Figure 5 are the points (V_T, I_T), which are located on subthreshold characteristics prior to and after the radiation. These points could be determined in a similar way as the points (V_{MG}, I_{MG}), and/or on the basis of the expression (30) and the definition of threshold voltage, and/or on the basis of the expression (30) and the definition of surface potential for the case of strong inversion. However, these points can be determined with highest reliability on the basis of knowledge about their abscissas, i.e. used generated values of threshold voltage, which avoid any ambiguity in the definition of threshold and/or start of strong inversion. The threshold voltage is most frequently determined as section of extrapolated dependence of the square root of drain current in MOS transistor in saturation from the threshold voltage at the gate (expression (31)), with V_G axis.

Presence of interface traps changes the slope of subthreshold characteristics, i.e. the difference between the voltage V_T and V_{MG} which represents the measure of "stretch-out" and is marked as V_{S0} (stretch-out voltage)

$$V_{S0} = V_T - V_{MG} , \tag{33}$$

Accordingly, an increase in electric charge density on interface traps which causes change in subthreshold characteristics inclination, i.e. V_{S0} voltage is now more simply determined on the basis of the expression [19]

$$\Delta N_{it} = \frac{C_{ox}}{q}(V_{S0} - V_{S0}(0)) , \tag{34}$$

where $V_{S0}(0)$ is the value of stretchout voltage prior to, and V_{S0} after IR or HCI process.

6.1.1 Charge-pumping technique

As opposed to the SMG technique, the charge-pumping (CP) technique does not give changes in charge densities in oxide and in interface traps, but is used solely to determine interface traps density while charge density in oxide can be subsequently determined on the basis of the expression (29) under the condition that the change in threshold voltage is known [20, 21, 104].

The charge-pumping effect can be explained on the basis of the diagram shown in Figure 6 [104]. The source and the drain of the transistor are short-circuited, and the p-n junction of source and drain with the substrate are inversely polarized with V_R voltage. In the absence of signal at the gate, under the influence of inverted polarization at the junction source-substrate and drain-substrate, the inverted saturation current of these connections will flow. When a train of rectangular pulses of sufficiently high amplitude is brought to gate (with pulse generator), a change of current direction in the substrate occurs. The intesity of that current is proportional with the pulse frequency, and "pumping" of the same amount of electric charge towards the substrate. As current cannot flow through oxide, the electric charge in the substrate come through p-n junctions of source and drain. In this way, in the case of n-channel MOS transistors, a channel is formed under the gate in positive pulse half-period, whereby electrons are captured on interface traps. During the negative half-period, when the channel area turns into the state of accumulation, mobile electrons from the channel are returned to the source and drain, and the captured electrons are recombined
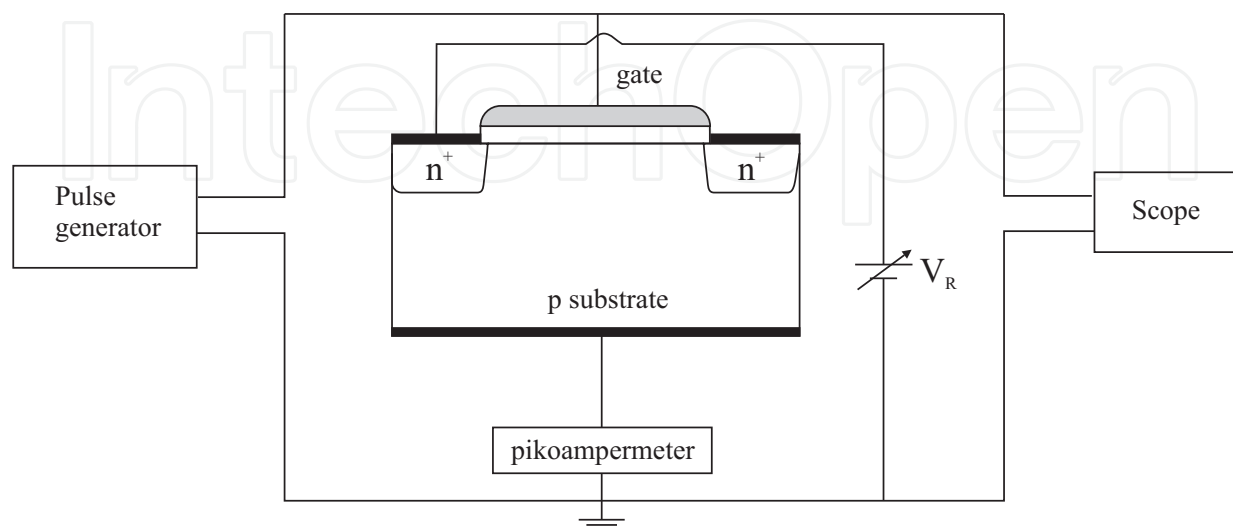
Fig. 6. Schematic diagram of charge pumping measurement.

with holes from the accumulated layer, thereby generating CP current which is proportional with the number of recombination centers, i.e. interface traps:

$$I_{CP} = q \cdot A_G \cdot f \cdot N_{it} \tag{35}$$

where A_G is gate surface, and f is pulse frequency. In order to avoid recombination with the channel electrons, it is necessary to ensure their return to the source and drain before overflow of cavities from the substrate occurs, which is accomplished by using reverse polarization of p-n junction or using a train of trapezoid pulses or triangular pulses with sufficient time for rise time t_r and fall time t_f pulse. However, part of the electrons whose capture is shallowest, are in the meantime thermally emitted into conductive band of the substrate, reducing the width of interface traps energy range measured by the CP technique, so that CP current is generated by interface traps within the range [21]

$$\Delta E = -2kT \ln \left(\upsilon_{th} n_i \sqrt{\sigma_n \sigma_p} \frac{|V_T - V_{FB}|}{|\Delta V_G|} \sqrt{t_r t_f} \right) \tag{36}$$

which is 0.5 eV from the middle of the forbidden band. In the expression (36) υ_{th} is thermal velocity, σ_n and σ_p are cross-section surfaces of carrier captures, n_i is self-concentration of carriers in the semiconductor, and ΔV_G is pulse height

Using of expression (35), interface traps density can be calculated on the basis of the measured maximum value of CP current. Maximum CP current is directly proportional to the pulse frequency, and a small-size transistor with usual state density needs a frequency of at least several kHz to enable the charge-pumping current level reach the order of magnitude of picoampere. Due to this, CP measuring is most often conducted with frequencies in the range between 100 kHz and around 1 MHz, whereby only real (FST) interface traps are registered (in some frequencies, CP is also contributed by part of SST which also captures electrons from the channel [105]).

As the CP technique requires a separate outlet for the substrate, it could be concluded that it is not applicable for power VDMOS transistors, in which the p-bulk is technologically connected to the source. However, thanks to the very structure of these transistors [106], the CP technique is applicable in a somewhat altered form; as shown in Figure 7 [25, 107]. It should be pointed out that VDMOS power transistor represents a parallel connection of a large number of cells (elementary transistor structures) with a large surface, which is especially suitable for the CP technique (higher level of current which is easier to measure).

The role of source and drain, as minority carrier in power VDMOS transistors (Figure 7) are taken over by p⁻ body areas of two adjacent cells, while the role of substrate (source of majority carriers) is played by n⁻ epitaxial layer between the cells which is directly connected to the n⁺ area of the drain. In this case, the CP current is generated through recombination through interface traps which are located on the interface oxide – n-substrate, and VDMOS structure acts as a PMOS transistor. In this way, the CP technique practically perform characterization of interface above the epitaxial layer, and not above the channel area, which must be taken into consideration when calculating interface traps density with use of the expression (35), whereby an adequate value of the active surface above the epitaxial layer should be taken as A_G. The oxide above the channel and the oxide above the epitaxial layer have the same characteristics and thickness, as they are made simultaneously in the production process, which also refers to the polysilicon gate. On the

other hand, it is known that the surface interface traps do not depend on the type of semiconductor on which the oxide is formed. This means that, within the qualitative analysis, it can be considered that the conclusions attained on the basis of the CP measurements also refer to the interface above the channel surface.
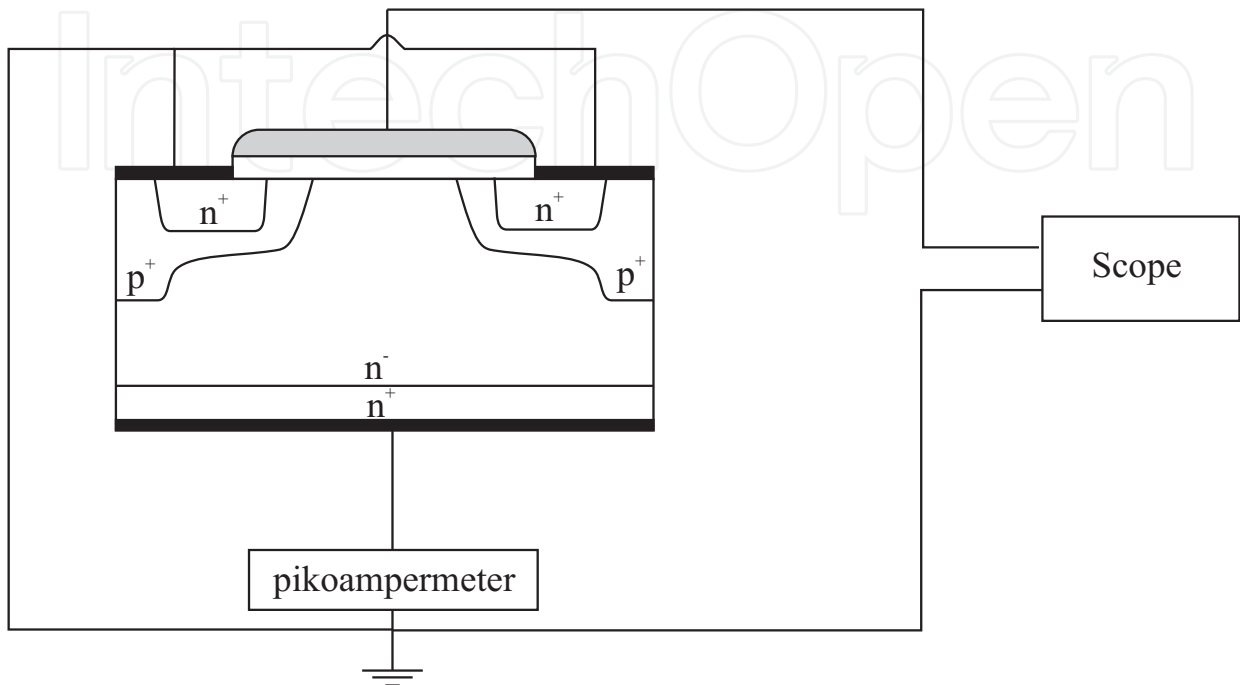

Fig. 7. Schematic diagram of charge pumping measurement for power VDMOS transistor.

7. Some results of IR and HCI processes and later annealing of MOS transistors

7.1 Behavior of CMOS transistors with Al gate from integrated circuits of the CD4007UB type in the course of IR process and subsequent annealing

The results of radiation with gamma rays, X-rays and electrons, as well as of subsequent annealing of MOS transistors with Al-gate from the integrated circuits CD4007UB are displayed in several papers [108-115], in which CMOS (NMOS and PMOS) transistors were used. This made it possible to directly evaluate the instability of electric parameters and characteristics of these integrated circuits on the basis of the data on instability of electric parameters and characteristics of these transistors.

Figures 8 and 9 display changes in the threshold voltage of CMS transistors during the radiation with gamma rays and later annealing on the temperature of 115°C for 0 V gate polarizations [111, 112]. As it can be seen, the threshold voltage in NMOS transistor (Figures 8) decreases down to the value of the absorbed dose of gamma radiation of 200 Gy, and then rises again, while in PMOS transistors (Figure 9], it continually rises. Change in threshold voltage also takes place during the annealing at elevated temperature, but in such a way as to approximate their values to the ones present prior to the radiation. It has been shown [112] that the annealing process can be accelerated by positive polarization on the gate.
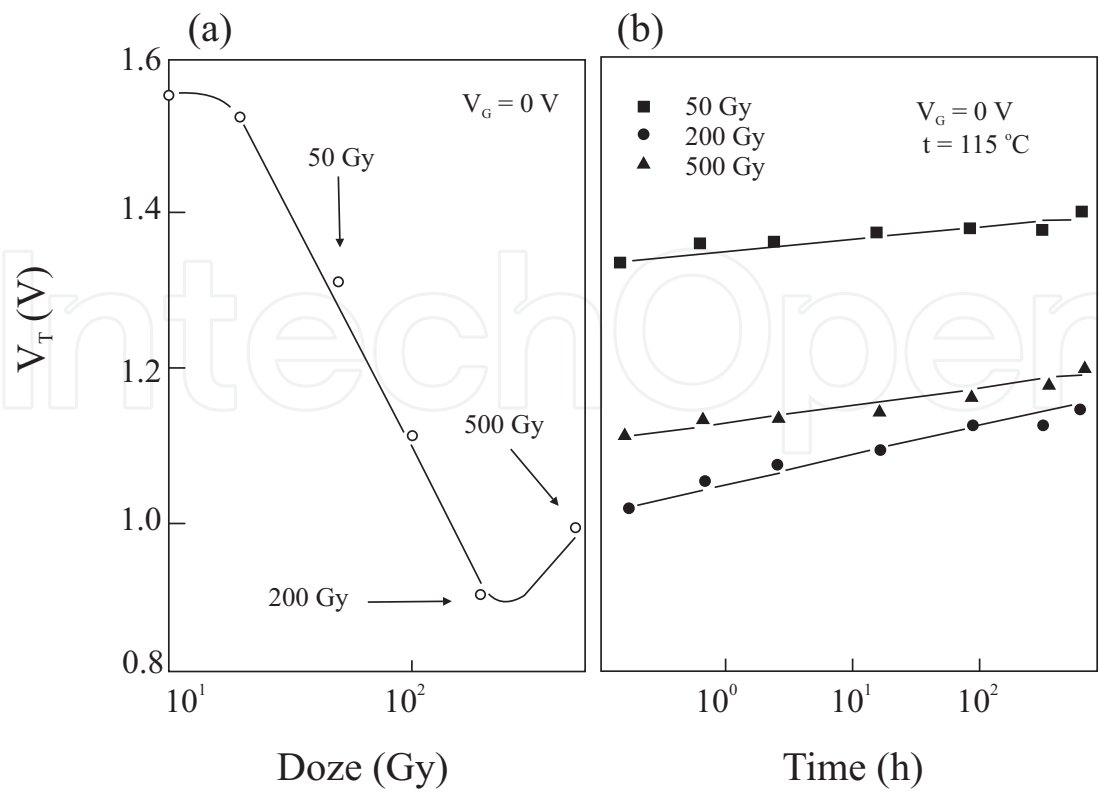
Fig. 8. Threshold voltage shift (ΔV_T) for NMOS transistor during gamma irradiation, V_G = 0 V (a) and thermal annealing, V_G = 0 V (b).
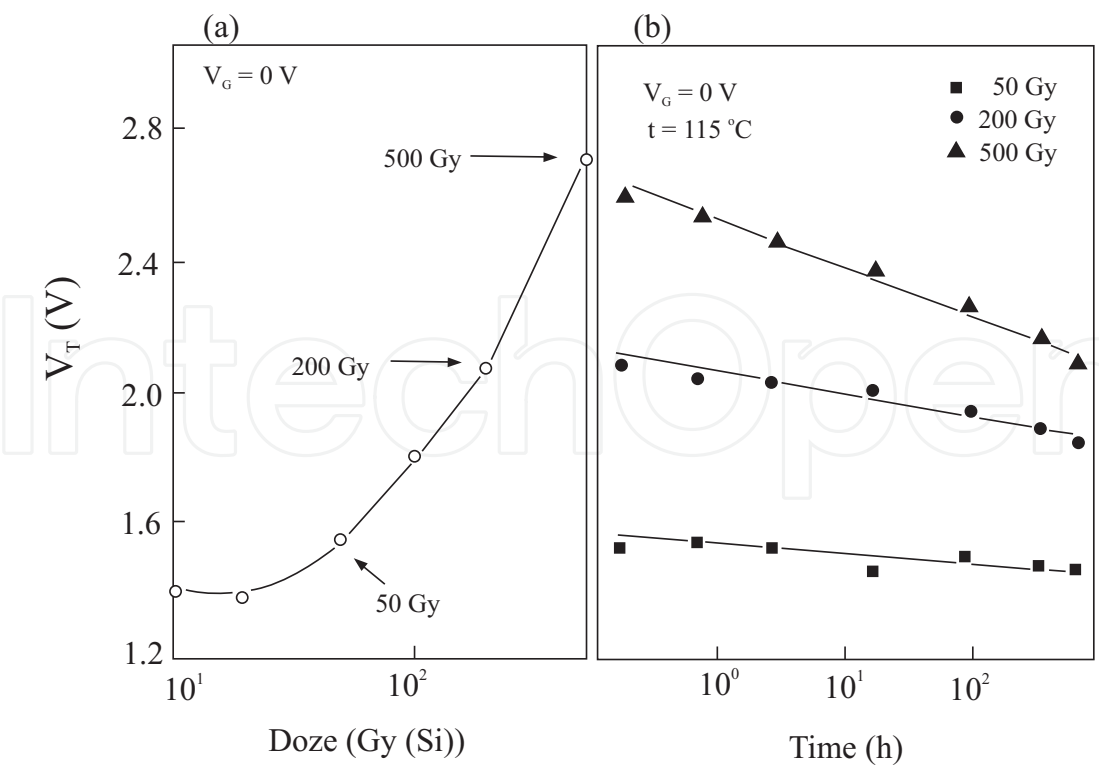
Fig. 9. Threshold voltage shift ΔV_T for PMOS transistor during gamma irradiation, V_G = 0 V (a) and thermal annealing, V_G = 0 V (b).
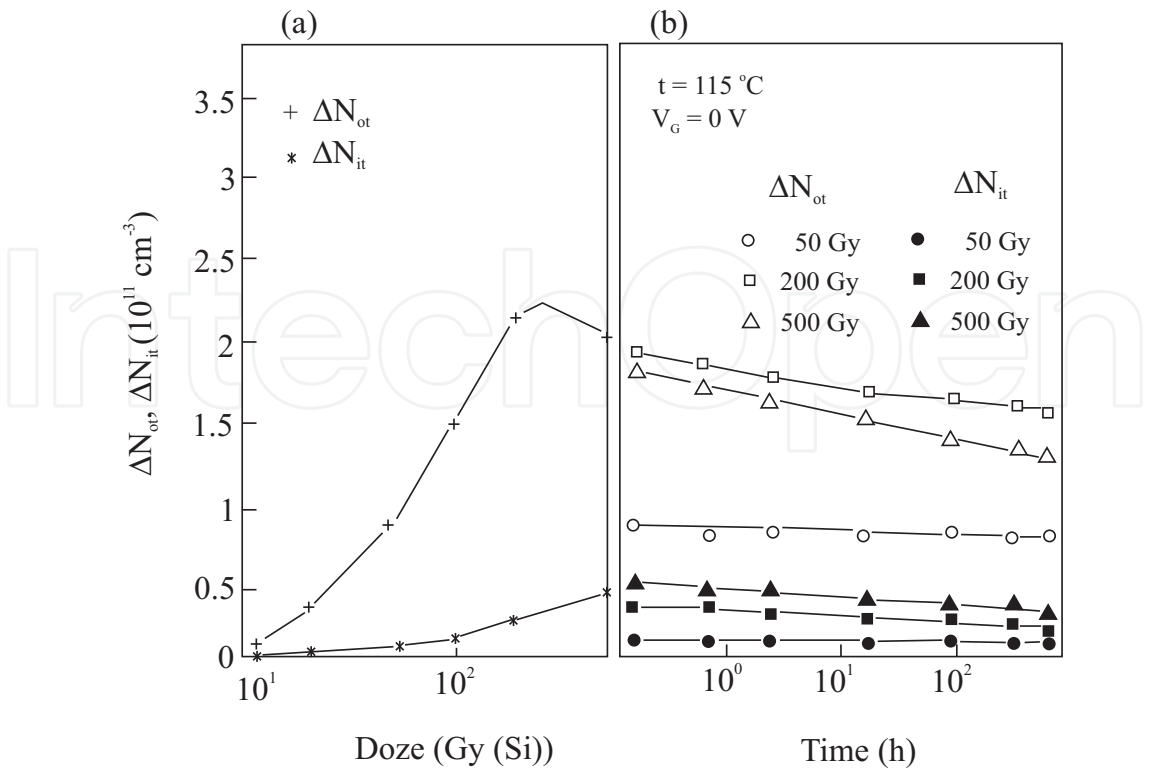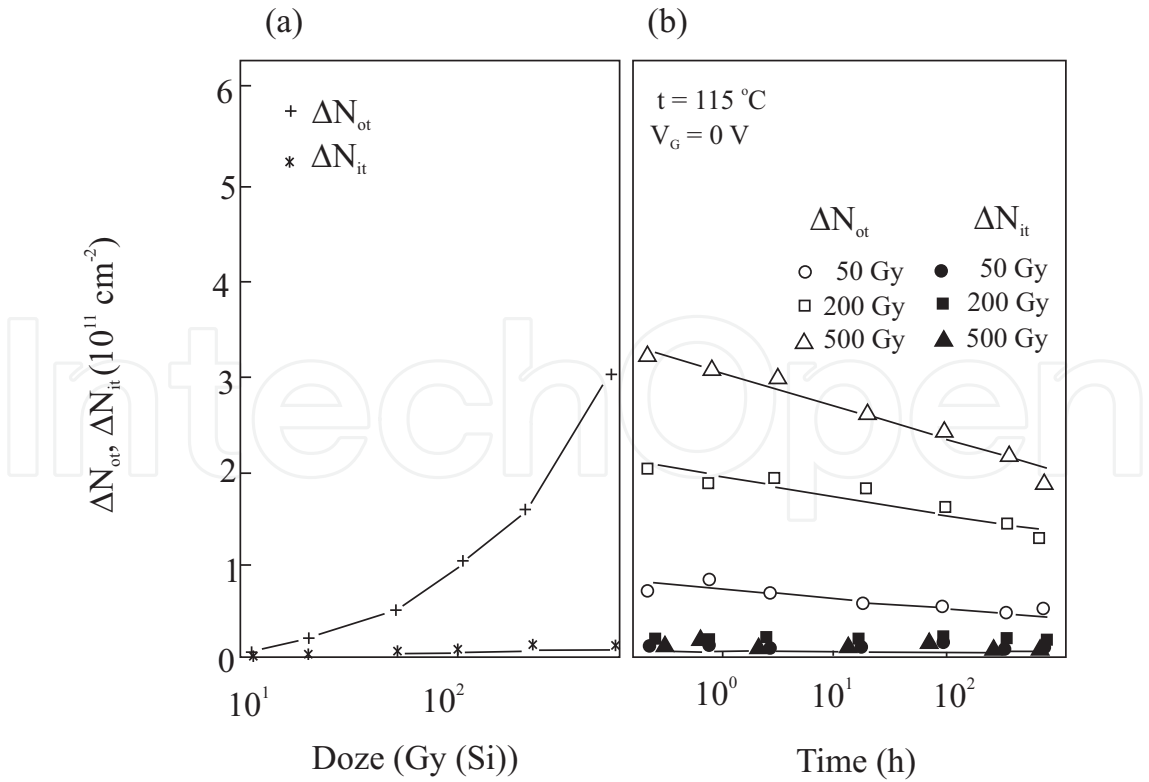
Fig. 10. The oxide trap (ΔN_{ot}) and interface traps (ΔN_{it}) density of NMOS transistor during gamma irradiation, V_G = 0 V (a) and thermal annealing, V_G = 0 V (b).

Fig. 11. The oxide trap (ΔN_{ot}) and interface traps (ΔN_{it}) density of PMOS transistor during gamma irradiation, V_G = 0 V (a) and thermal annealing, V_G = 0 V (b).

Figures 10 and 11 show changes in charge density in gate oxide and interface traps during radiation with gamma rays and later annealing in the temperature of 115°C for 0 V gate polarizations for the same transistors for which the change in threshold voltage (Figures 8 and 9) was monitored [111, 112]. The method described in the paper [90] was used to determine these densities. From the behavior of the curves in Figures 10 and 11, it was concluded that the annealing of radiated transistor is carried out through annealing of radiation defects described in detail in chapter 3. Namely, both the density of charge in the gate oxide and the density of interface traps show the tendency of decreasing during the burn in. It has been shown that the annealing of defects caused by gamma radiation depends not only on the conditions of transistor annealing, but on the conditions of their radiation as well, which can also be detected in Figures 10 and 11. Namely, the level of radiation exposure dictates the degree of annealing and the speed of the process of burn in the defects, so that the annealing is smaller in higher degrees of radiation exposure, considering the higher density of defects, but their annealing is more intense. This fact is supported by radiating a CMOS transistor with electrons and X-radiation whose energies amount to 10 MeV and later annealing with low-energy UV radiation [109].

In order to be able to consider the temperature annealing or annealing or annealing by low-energy UV radiation of gamma radiation degraded of electric characteristics of CMOS transistors as successful, it is necessary to ensure conditions in which the degraded electric parameters will become stable after annealing. It has been shown [110] that these conditions can be fulfilled by annealing on the temperature of 115° C and positive polarization at the 10 and 15 V gate. Check of characteristics stability was performed by continuing the annealing in an increased temperature and without polarization of the gate, and it was observed that the threshold voltage remains stable. Besides being definitive, the annealing process is accelerated by polarization at the 10 and 15 V gate. With lower voltage values in the continued temperature treatment of radiation-exposed transistors, the threshold voltage starts decreasing, which can most probably be attributed to the effect of the so-called "inverted" annealing.

7.2 Behavior of power VDMOS transistor during the IR process and the subsequent annealing

Electric parameters behavior of MOS transistors with polysilicon gate during gamma radiation was studied for many years [4]. For the commercial components can be said that they are mostly known. Figure 12 shows typical changes in threshold voltage during radiation of n-channel power VDMOS power transistors of the type EF1N10 at room temperature, and with gate voltages V_G = 0 and 10 V [116]. It can be seen that the threshold voltage decreases along with the increase in radiation dose and that the changes are more pronounced with higher values of gate voltage. It was also shown that the mobility is decreased during the radiation, and the changes are greater when the gate voltage is 10 V than when it is not applied.

Change in the oxide traps charge density density ΔN_{ot} and interface traps ΔN_{it} during the IR process for the same transistors in which the change in threshold voltage was monitored (Figure 12), determined by use of SMG technique, are displayed in Figures 13 and 14, respectively [116]. An increase in ΔN_{ot} and ΔN_{it} values during gamma radiation can be observed, and these changes are greater in the case V_G = 10 V. It has also been observed that the increase in the oxide trap density is substantially greater than the increase in interface traps density.
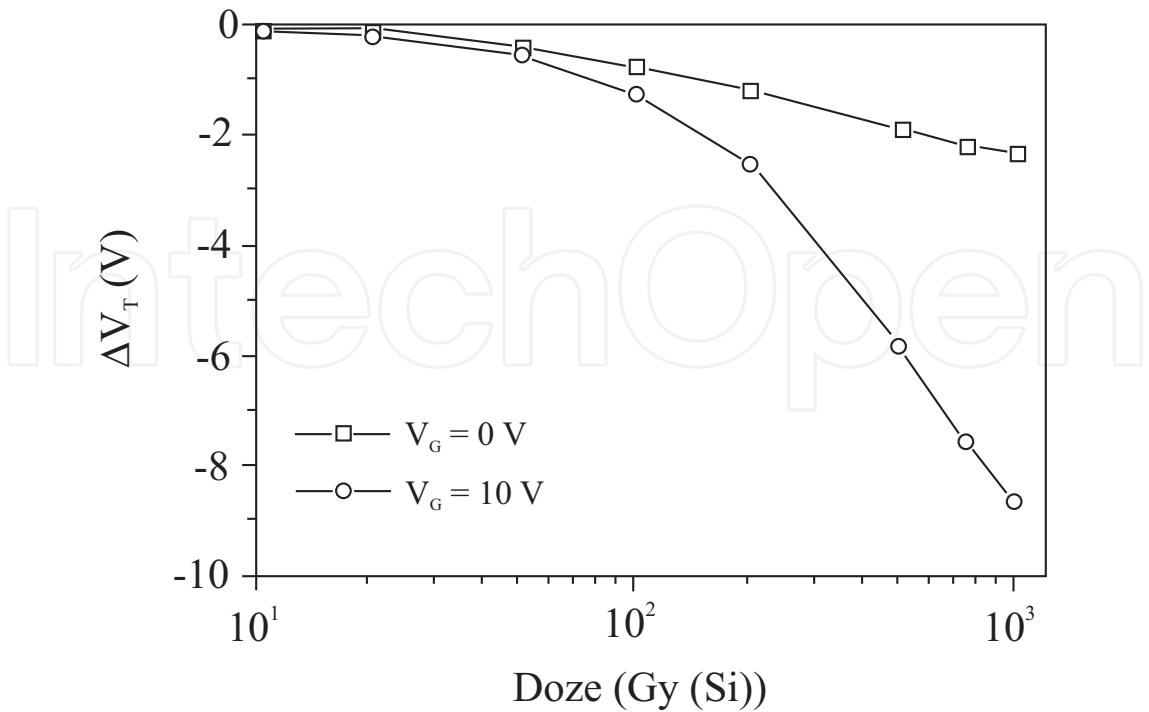
Fig. 12. Threshold voltage shift (ΔV_T) of n-channel power VDMOS transistor during gamma irradiation for V_G = 0 V and V_G = 10 V.
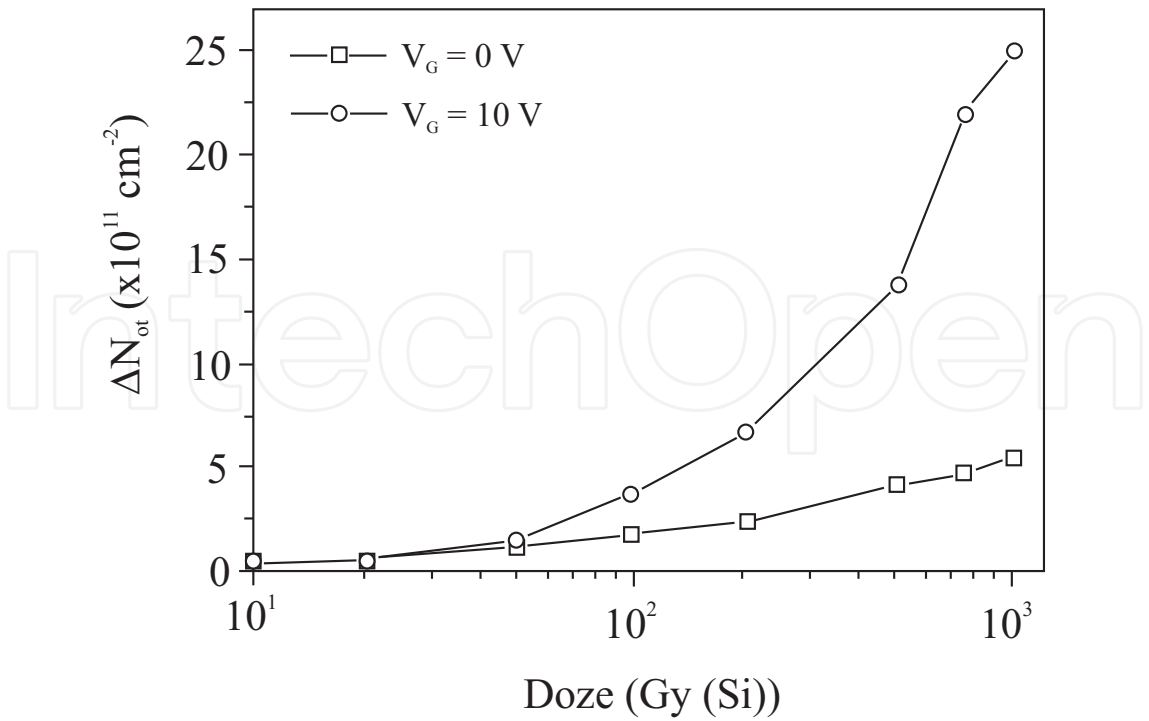

Fig. 13. The oxide traps charge density density (ΔN_{ot}) of n-channel power VDMOS transistor during gamma irradiation for V_G = 0 V and V_G = 10 V.
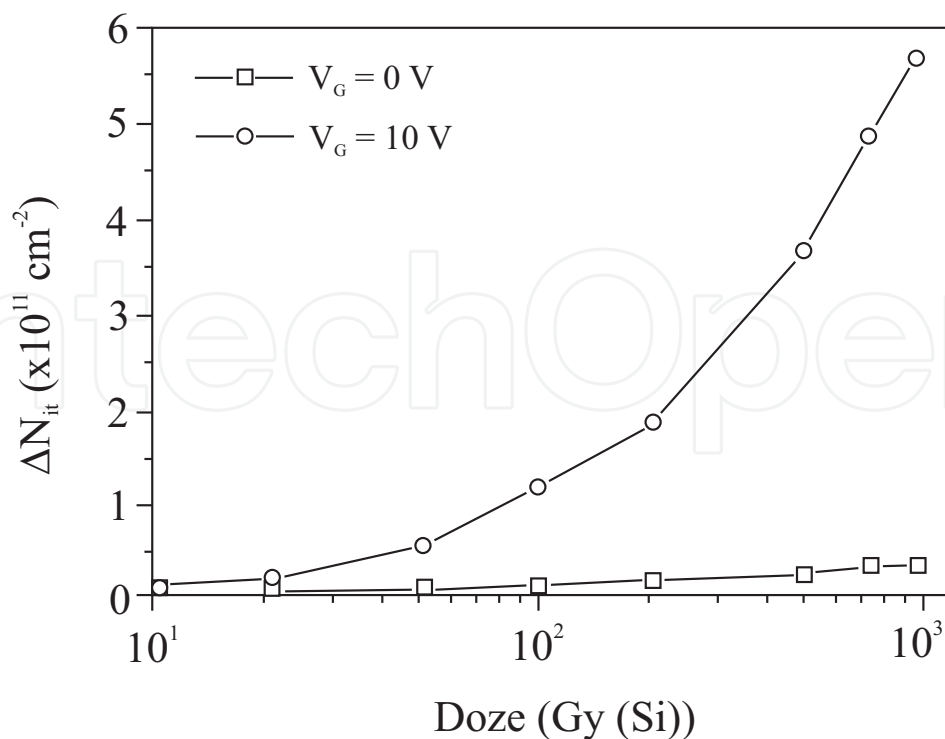
Fig. 14. The interface trap density ($\varDelta N_{it}$) of n-channel power VDMOS transistor during gamma irradiation for V_G = 0 V and V_G = 10 V.

Several papers [22, 27, 28, 85, 86, 88, 117-124] displayed the results of annealing the radiation-exposed power VDMOS transistors in room temperature and elevated temperatures. Figure 15 displays changes in threshold voltage of VDMOS power transistor of the type EFL1N10 when, during the gamma radiation, there was no voltage at the gate, and during the annealing it amounted to V_G = 10 V, while the annealing was conducted at room temperature, 55° C and 140° C. Figure 16 refers to the same annealing conditions, except that the voltage at the gate during the gamma radiation amounted to V_G = 10 V [27]. As it can be seen from these figures, a greater and faster change in threshold voltage ΔV_T occurs in case of higher temperature, and occurrence of super-recovery was detected only in transistors for which radiation was conducted when there was no polarization at the gate, and when their annealing was conducted on the temperature of 140° C.

The influence of temperature and voltage at the gate on the change in density of oxide traps charge ΔN_{ot} and interface traps ΔN_{it} for the same transistors for which a change in threshold voltage was monitored (Figures 15 and 16) are displayed in Figures 17 and 18 [27], and these changes are determined by using SMG technique. It can be seen that the density of interface traps after some annealing time starts increasing, while the time period prior to the start of increase can be very long. As mentioned before, this phenomenon of increase of ΔN_{it} value after some saturation is known in literature under the title latent increase (latent generation) of interface traps. The time interval prior to the occurrence of latent increase in interface traps density depends on the annealing temperature, it being shorter if the annealing temperature is higher. Also, a direct link between the latent increase in interface trap density and the latent decrease of density of the oxide trapped charge have been detected, as well as the fact that, after the latent increase in interface traps density, comes their decrease (passivization) during exposure to elevated temperature.
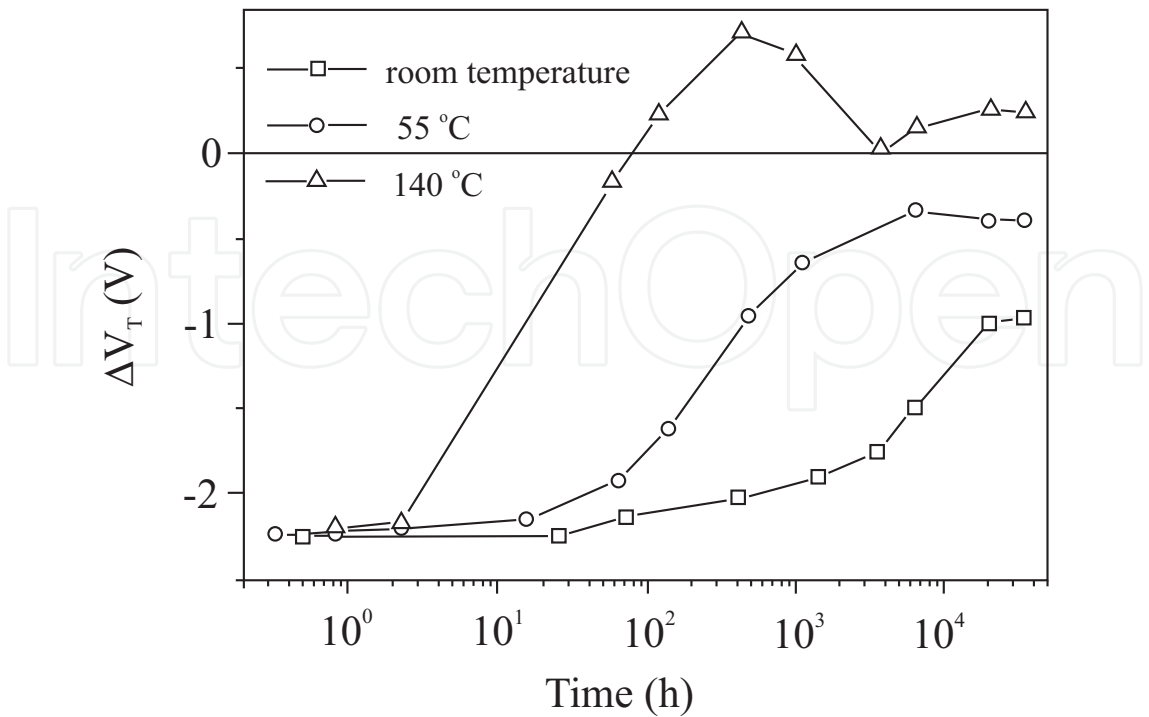
Fig. 15. Threshold voltage shift (ΔV_T) of n-channel power VDMOS transistor during annealing; V_G = 0 V during irradiation and V_G = 10 V during annealing.
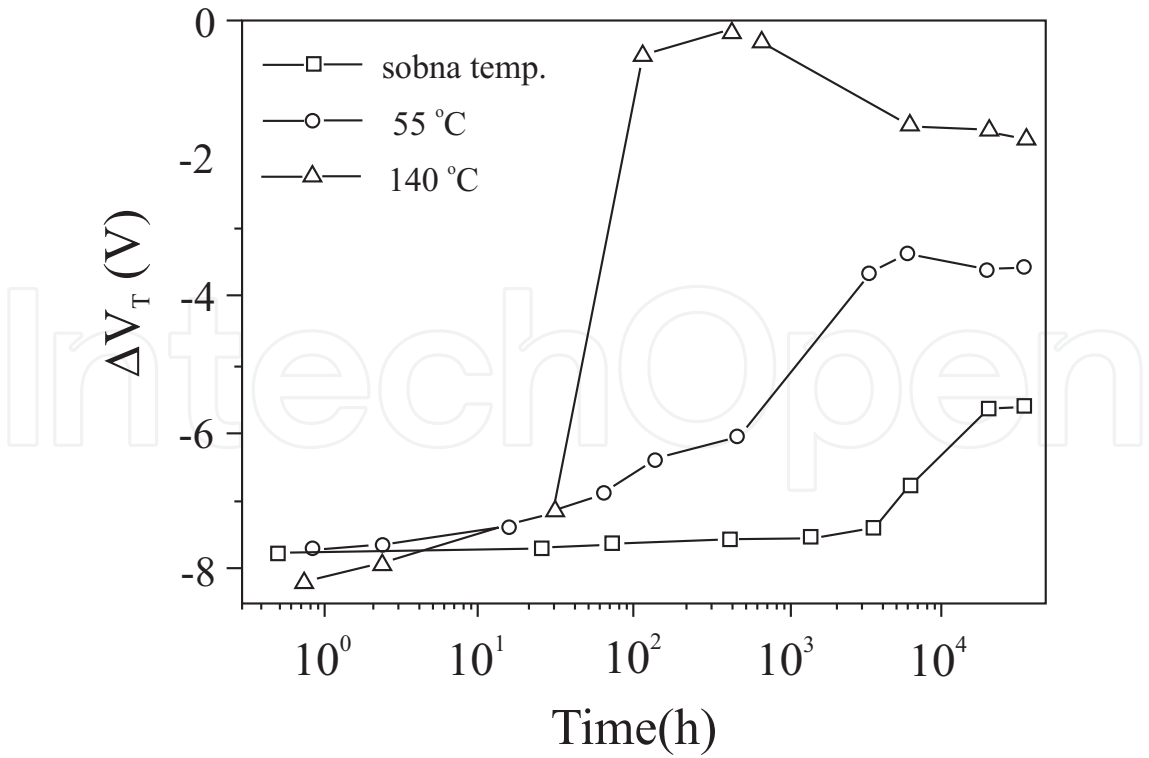

Fig. 16. Threshold voltage shift (ΔV_T) of n-channel power VDMOS transistor during annealing; V_G = 10 V during irradiation and annealing.
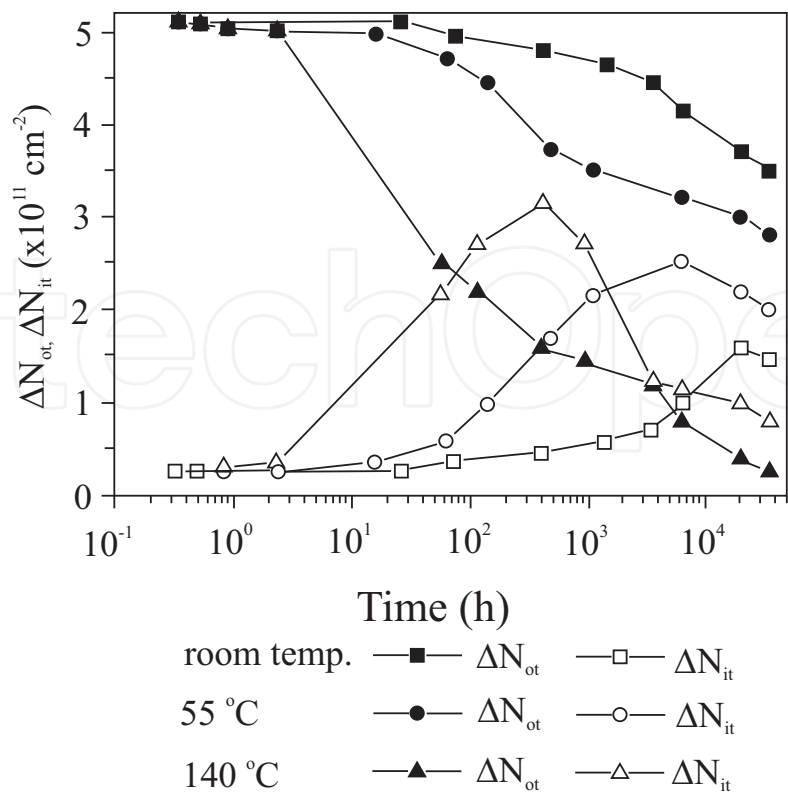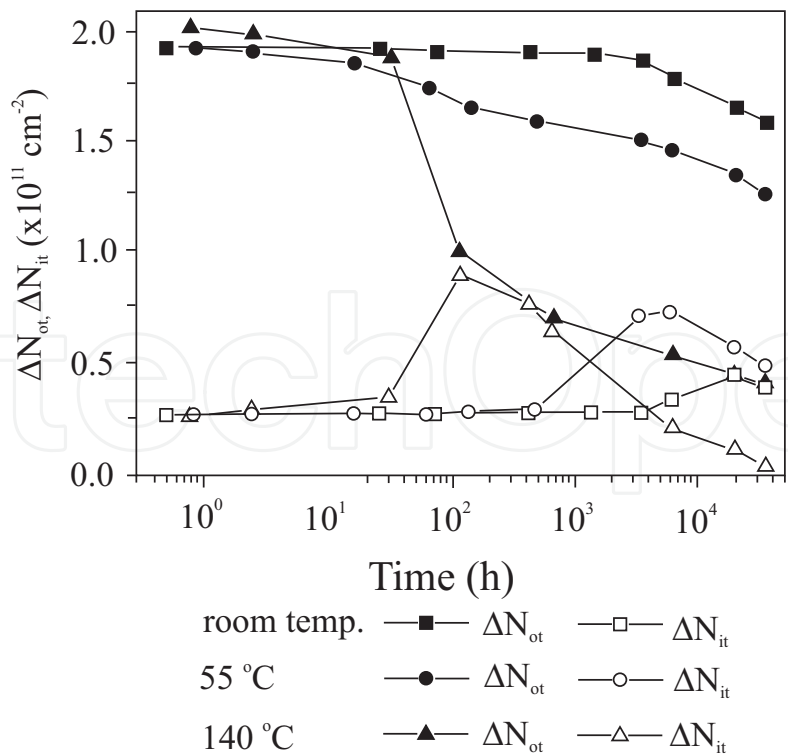
Fig. 17. The oxide traps charge density (ΔN_{ot}) and interface traps (ΔN_{it}) density during annealing for n-channel power VDMOS transistor irradiated for V_G = 0 V.

Fig. 18. The oxide traps charge density (ΔN_{ot}) and interface trap (ΔN_{it}) density during annealing for n-channel power VDMOS transistors irradiated at V_G = 10 V.

One of the important parameters which influence changes in density of oxide trapped charge ΔN_{ot} and interface traps ΔN_{it} during the annealing of power VDMOS transistors which have previously been exposed to gamma radiation is the value of voltage at the gate during the annealing. Experimental studies [119] have shown that the recovery of radiation-exposed transistors on the temperature of 140° C for the polarizations at the gate amounting to $V_G = 0$, 5 and 10 V, leads to latent increase in interface traps density and latent decrease in the density of oxide trapped charge. In the case $V_G = 0$, when only an electric field is present in the oxide due to the difference of work function of poly-Si gate and substrate, these changes are significantly smaller, when compared to the changes caused by the gate voltage of 5 and 10 V. The values of maximum densities of interface traps formed during the annealing, for $V_G = 5$ and 10 V have very few mutual differences. Also, there are certain differences in the time interval prior to the start of latent increase in ΔN_{it}.

Changes in densities of captured electric charge and interface traps shown in Figures 13 through 18 are very well described by H-W model [27, 28], whose more detailed description is given in chapter 4.

7.2.1 Isochronal annealing of power VDMOS transistors after the IR process

The isochronal annealing implies to the annealing of MOS transistors after IR or HCI processes with variable temperature. Figure 19 shows behavior of density of the oxide trapped charge and interface traps during an isochronal annealing of radiation-exposed power VDMOS transistors of the type EFP8N15 in the temperature range between 50° C and 290° C [121]. These densities were followed by using SMG technique. Duration of annealing at every temperature amounted to 5 min, while the temperature change amounted to 10° C, and the gate voltage during the annealing amounted to $V_G = 10$ V. As it can be seen, the
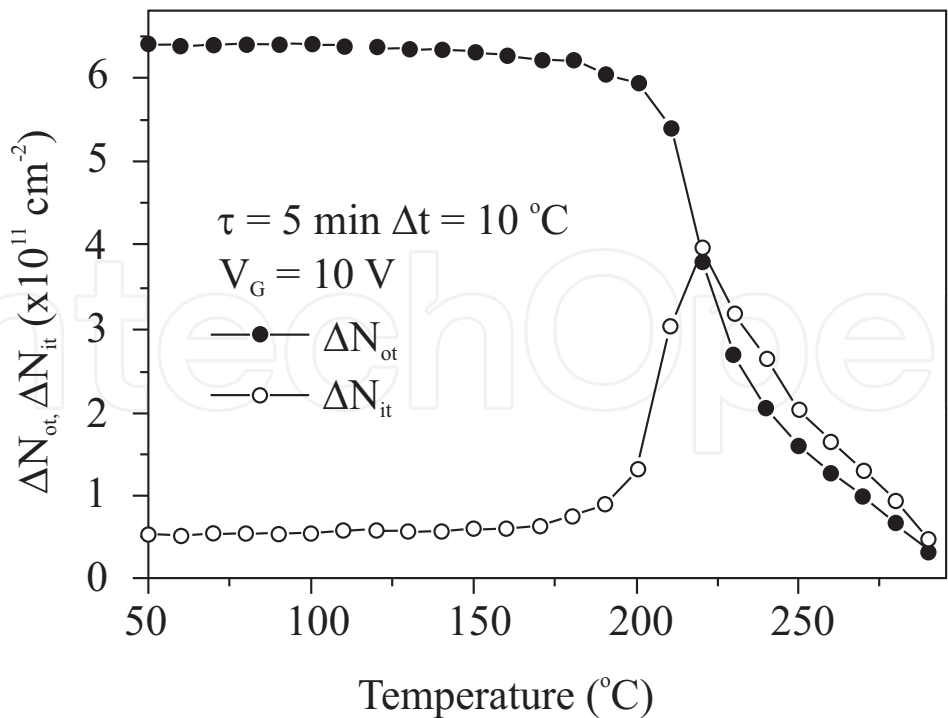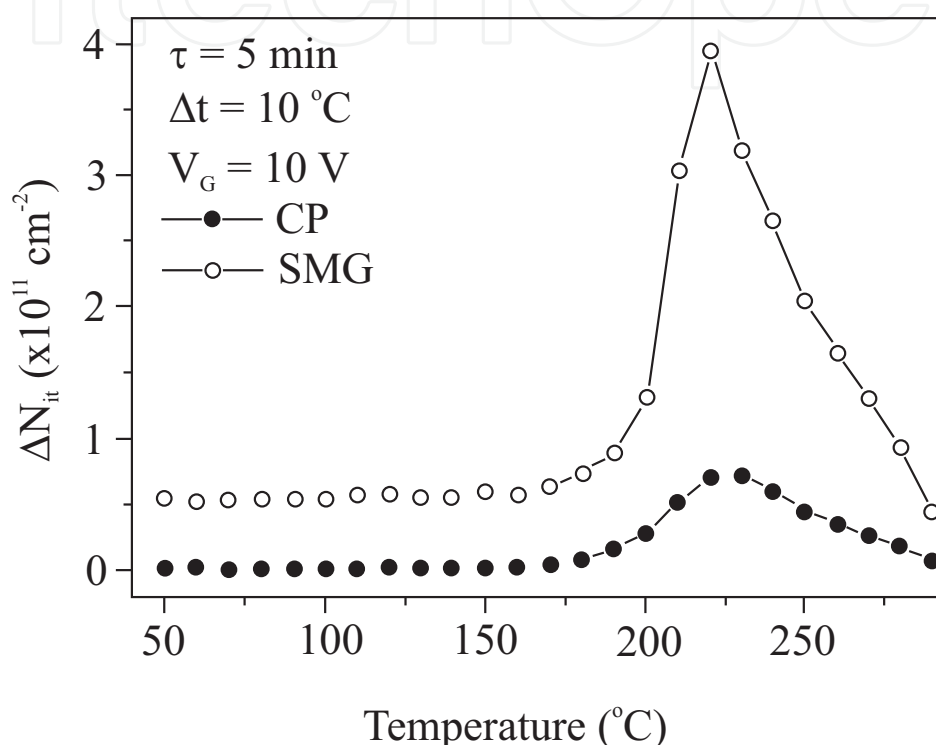

Fig. 19. The oxide traps charge density (ΔN_{ot}) and interface trap (ΔN_{it}) density for n-channel power VDMOS transistors during isochronal annealing determined using SMG technique.

values of ΔN_{ot} and ΔN_{it} are insignificantly changed up to the temperature of approximately 175° C, while at higher temperatures there occurs a rapid increase in interface traps densities, followed by decrease in the density of oxide trapped charge. The interface traps density starts decreasing from the temperature t=225° C. Figures 20 shows behavior of interface traps density with the temperature of isochronal annealing, generated by SMG and CP techniques. Similarities in behavior of these curves can be seen, but the values of ΔN_{it} generated by SMG technique are significantly higher, in accordance with the discussion given in chapter 6.

Fig. 20. The interface trap (ΔN_{it}) density for n-channel power VDMOS transistor during isochronal annealing determined using SMG and CP techniques.

7.2.2 Influence of voltage polarization at the gate during the annealing of power VDMOS transistors which had previously been subjected to gamma radiation

Figure 21 shows changes in the density of oxide trapped charge and interface traps during the annealing of power VDMOS transistor of the type EFP8N15 which had previously been subjected to the IR process. Annealing was conducted under alternating change in the voltage polarization at the gate and temperatures of 200° C and 250° C, while each phase, for one direction of electric field lasted for 1 h [116]. The densities of the oxide trapped charge and interface traps were determined by SMG technique. It can be seen from the figure that during the first phase for V_G = 10 V, there occurred a latent increase in interface traps density and latent decrease in the density of oxide trapped charge, for both temperatures. The first phase is similar to the results shown in Figures 17 and 18. During the second phase (V_G=-10 V), at the annealing temperature of 200° C, the value of ΔN_{it} continues to decrease, which could be expected on the basis of the H-W model, as the diffusion of water molecules is not dependent on the direction of electric field in oxide, while at the temperature of 250° C

there is no change in this density, as almost all interface traps have already been passivated during the first phase. However, in the third phase (V_G=+10 V), the behavior of interface traps density is different from the behavior in the first phase. Namely, there is no latent increase in interface traps density, although the value of ΔN_{it} at first insignificantly raise at the very start of the annealing at the temperature of 250° C, and then continued to decrease, while at the temperature of 200° C, a mild increase was detected, and then slow decrease of this density (these changes are significantly smaller than during the first phase). On the basis of such behavior of interface traps and the application of H-W model, it was concluded that there were no hydrogen particles during the third phase (and especially no H_2 molecules) which could cause latent increase of ΔN_{it}.

The paper [116] also shows the results of ΔN_{it} generated through the application of CP technique for power VDMOS transistors of the type EFP8N15 annealing under the same conditions as shown in Figure 21. The behavior of this density is very similar to the behavior of the density generated through the SMG technique, but the values of ΔN_{it} generated with CP technique are significantly lower, which is in accordance with the sensitivity of the method discussed in chapter 6.
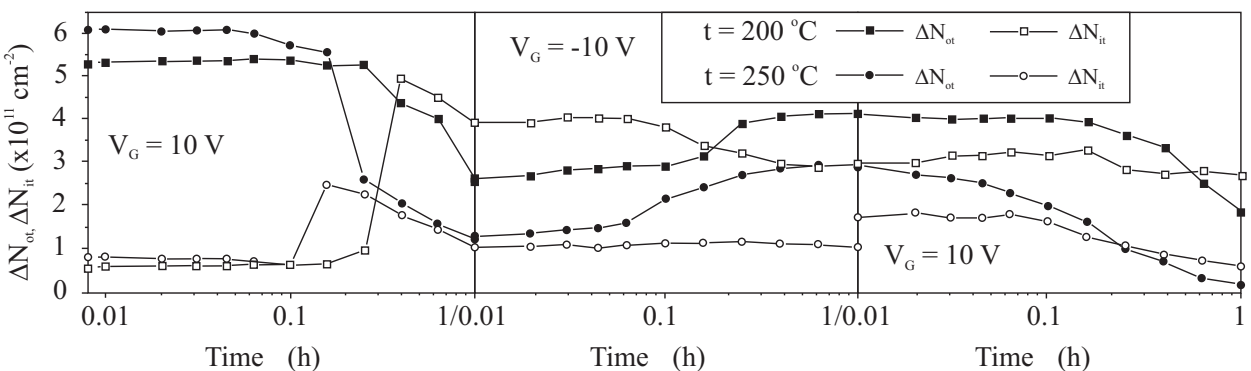

Fig. 21. The oxide traps charge density (ΔN_{ot}) and interface trap (ΔN_{it}) density during annealing with positive and negative polarization on the gate ($V_G = \pm 10$ V) for n-channel VDMOS transistors.

7.3 Behavior of power VDMOS transistor during the HCI process and subsequent annealing

Figure 22 shows the changes in threshold voltage of power VDMOS transistor EFL1N10 during the HCI process, with gate voltages of +80 V and -80 V [126]. It can be seen that the HCI process leads to significant changes in the threshold voltage ΔV_T. An initial decrease in the value of ΔV_T (during the first 40 min under positive, i.e. 20 min under negative gate voltage) and subsequent increase until the end of tension implies the occurrence of the "turn-around" effect. Similar behavior was also detected in power VDMOS transistor of the type IRF510 [29].

Figure 22 also shows the change in threshold voltage during the second HCI process. Namely, after the first HCI process, transistors were annealing at the temperature of 150° C in the duration of 3000 h, and then subjected to the HCI process again. It can be seen that the behavior is similar, while the changes in ΔV_T are more pronounced in the first HCI process, for both polarization signs at the gate.
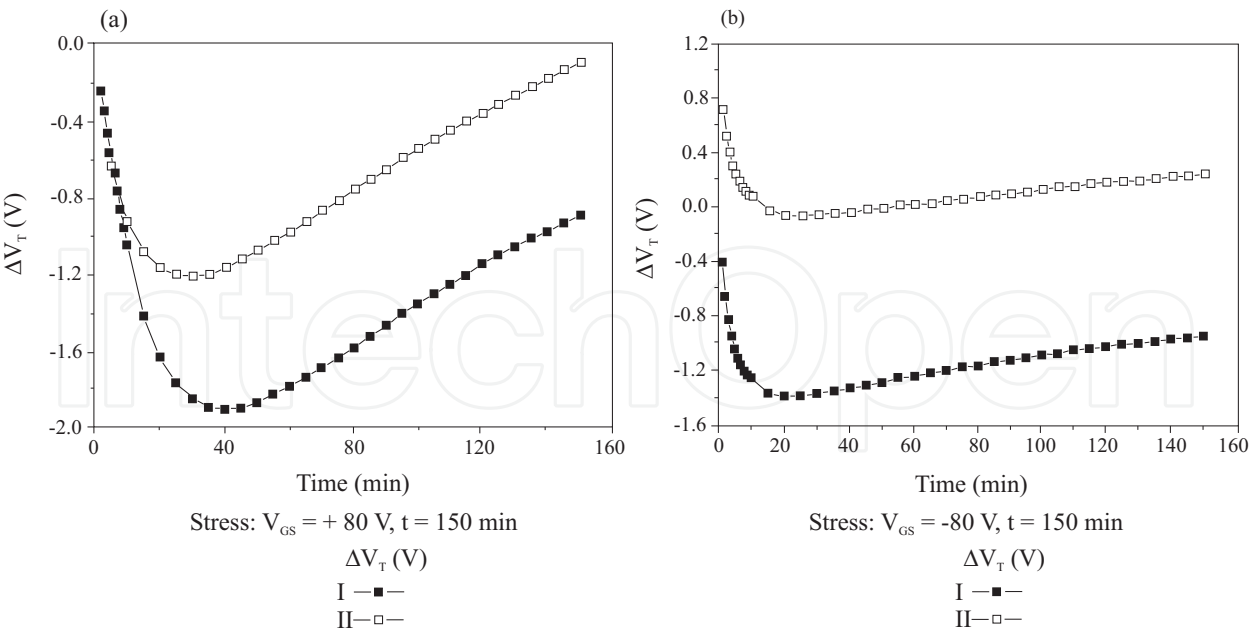
Fig. 22. Threshold voltage shift (ΔV_T) of n-channel power VDMOS transistors for positive ((a) $V_{GS} = 80$ V) and negative ((b) $V_{GS} = -80$ V) HCI during the first and second stress cycle.
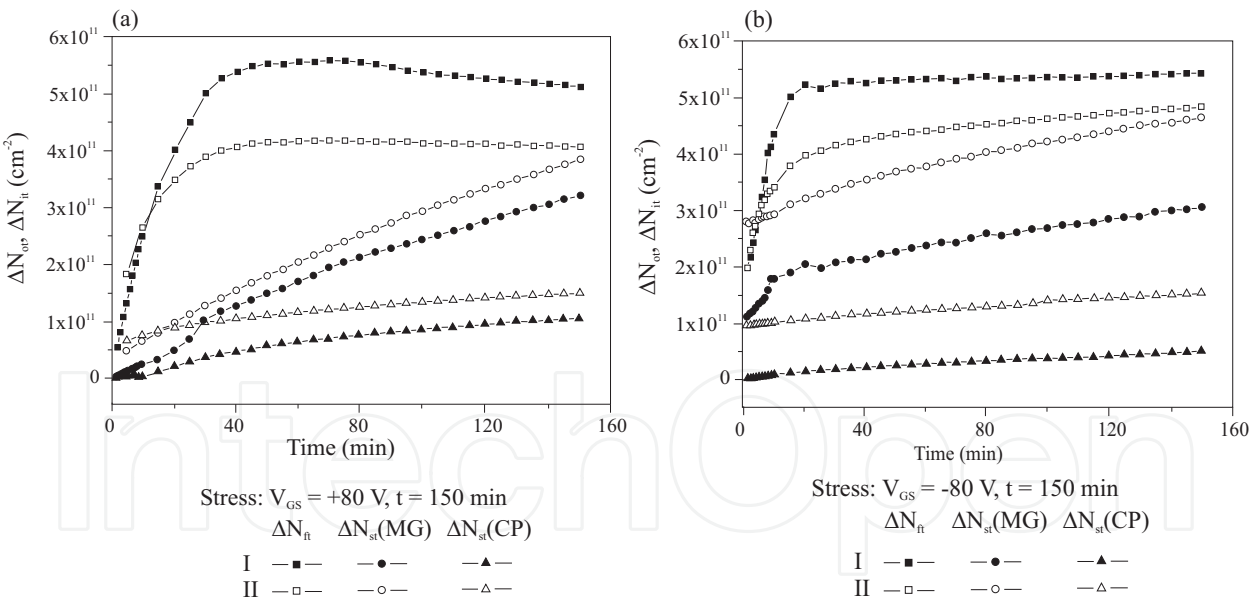

Fig. 23. The oxide traps charge density (ΔN_{ot}) and interface trap (ΔN_{it}) density of n-channel power VDMOS transistors for positive ((a) $V_{GS} = 80$ V) and negative ((b) $V_{GS} = -80$ V) HCI during the first and second stress cycle.

Figure 23 shows the changes in oxide trapped charge density in the gate oxide ΔN_{ot} determined by SMG technique and the changes in interface traps density ΔN_{it} (SMG) determined by SMG technique and ΔN_{it} (CP) determined by CP technique for the same transistors that were subjected to the HCI procedures during the monitoring of change in

threshold voltage (Figure 22) [126]. From the figure it can be seen that the behaviors of ΔN_{it} (SMG) and ΔN_{it} (CP) are qualitatively the same, while there are significant quantitative differences between them. On the basis of the discussion given in section 3, the quantitative concurrences should not be expected, as the share of ST in the densities ΔN_{it} (SMG) and ΔN_{it} (CP) is different. Besides that, SMG and CP techniques in power VDMOS transistors register interface traps in two different areas of gate surface. SMG technique registers current in the p⁻ -area of the channel, while CP technique registers interface traps in the n⁻ -epi area of power VDMOS transistors.

Park et al [127] studied this problem in detail in a large number of similar samples and concluded that the initial values of threshold voltage in these two interfaces are significantly different. Another cause of quantitative difference in the values of ΔN_{it} (SMG) and ΔN_{it} (CP) is the fact that these two techniques record different areas of the silicon forbidden band. Namely, SMG technique records the defects in the area located at about 0.45 eV of the upper part of the silicon forbidden band, while CP technique records the defects at the same distance, but in the lower part of this area [127].

The initial increase ΔN_{ot} shown in Figure 23 is a consequence of the formation of positively charged FT at the early stage of HCI process [126]. ΔN_{it} achieves saturation at the later stage of this process, as the number of electrons captured by NBO centers increases. The increase in ΔN_{it} value for the entire duration of the HCI process is necessitated by the reaction of H⁺ ions which are released in the oxide (H model) and the holes drifting towards the Si – SiO$_2$ interface and forming interface traps (h^+ model). Greater changes of ΔN_{it} (SMG) occur because this technique comprises all ST (ST=SST+FST), while ΔN_{it} (CP) comprises only FST.

Figures 24 shows the changes in threshold voltage of ΔV_T, while Figures 25 shows the changes in the density of oxide trapped charge ΔN_{ot} and the change in interface traps
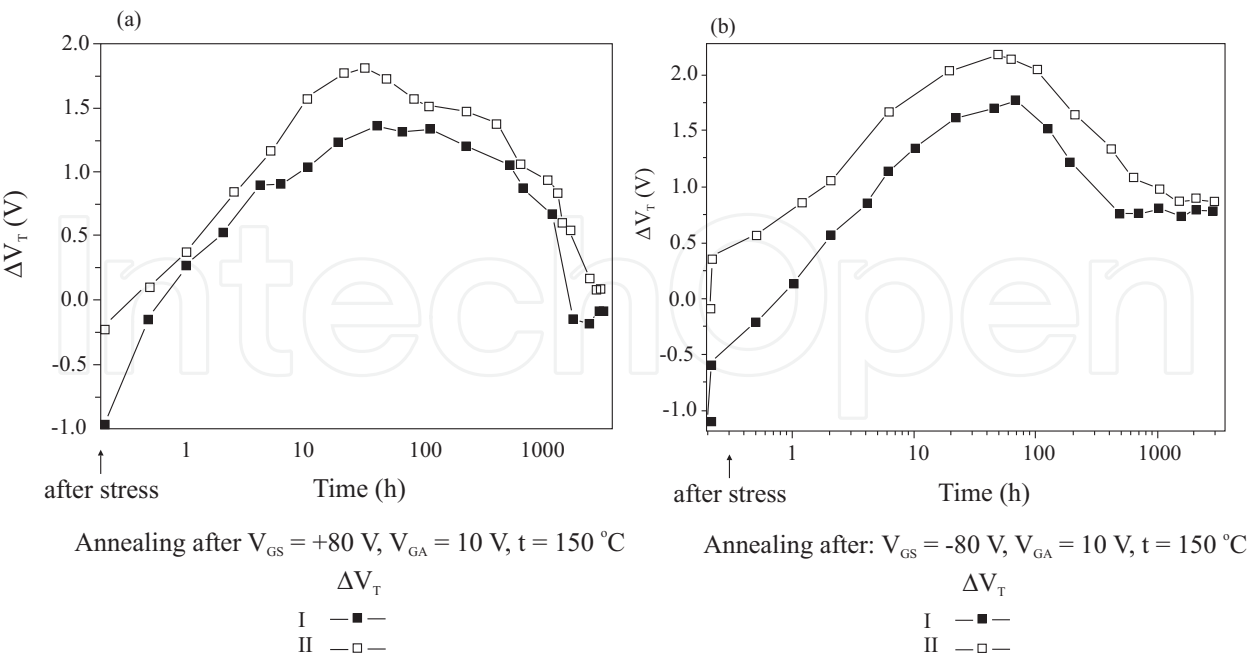

Fig. 24. Threshold voltage shift (ΔV_T) of n-channel power VDMOS transistor during the first and second thermal post HCI annealing cycle following (a) positive and (b) negative HCI.

densities determined by SMG technique (ΔN_{it} (SMG)) and CP technique (ΔN_{it} (CP)) during the annealing of power VDMOS transistor of the type EFL1N10 which had previously been subjected to the HCI process under gate voltages of +80 V and -80 V, annealing at the temperature of 150° C, and then subjected to HCI process again [126]. It can be seen that ΔV_T rises during the first 10 hours of recovery, then it decreases and achieves saturation in case of duration of 1.000 h of annealing, and that the behavior of ΔV_T is very similar in both polarization cases. The only difference is that ΔV_T achieves saturation sooner in the annealing preceded by HCI process with a negative gate polarization.

From Figure 25 it can be seen that there are no differences caused by the opposite sign of a gate polarization during the HCI process. Nor do the trends of the monitored changes differ during the first and the second recovery. As expected, the density of ΔN_{ot} decreases during annealing. ΔN_{it} (SMG) initially rises, while its decrease would occur during a longer annealing period, until the saturation is achieved. Very similar behavior also applies to the values of ΔN_{it} (CP), but this change is significantly smaller than the change ΔN_{it} (SMG) for the reasons discussed previously. The behavior of ΔN_{ot}, ΔN_{it} (SMG) and ΔN_{it} (CP) during annealing is very well described by the H-W model which details are given in chapter 5.
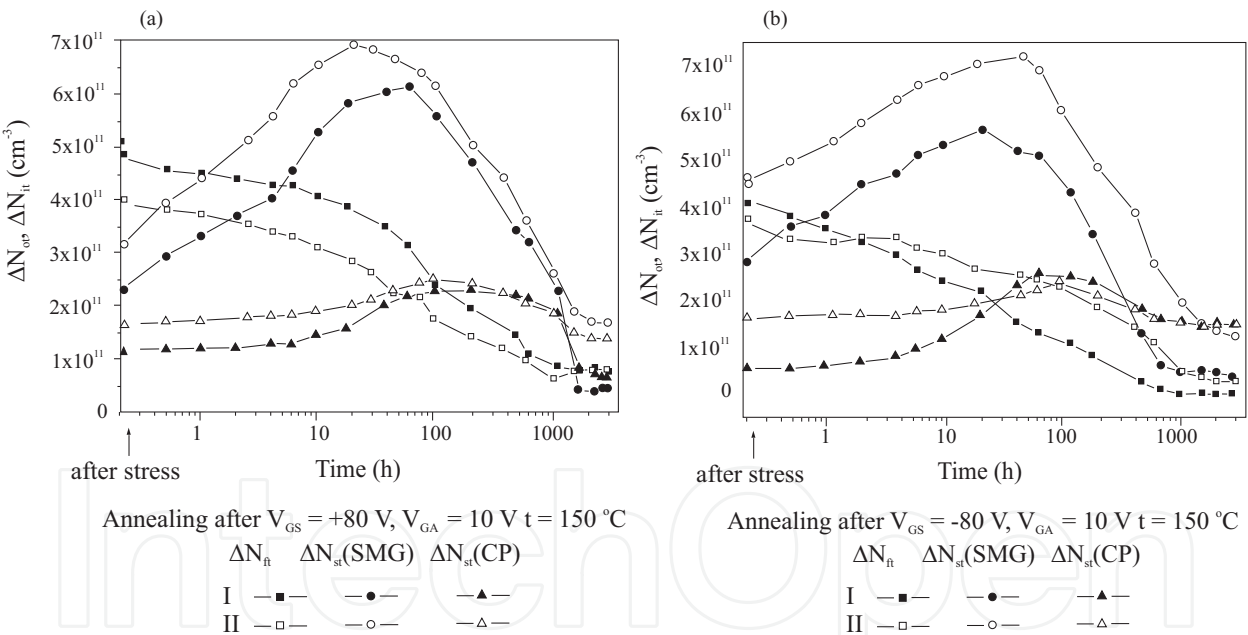

Fig. 25. The oxide traps charge density (ΔN_{ot}) and interface trap (ΔN_{it}) density of n-channel power VDMOS transistors during the first and second thermal post HCI annealing cycle following (a) positive and (b) negative HCI.

In the paper [22] shows comparative results of annealing of the n-channel power VDMOS transistor of the type EFL1N10, where a certain number of them is subjected to gamma radiation, and others to the HCI (Fowler-Nordheim high electric field stress) process. The changes in ΔN_{ot}, ΔN_{it} (SMG) and ΔN_{it} (CP) were monitored. It was noticed that, during annealing of transistors that had previously been subjected to gamma radiation there is a

latent increase in interface trap density, both with SMG and CP technique. For transistors that had previously been subjected to the HCI process, a latent increase in interface trap density during the annealing occurs when only CP technique is used to determine their density. This shows that there is a difference in the nature of capture centers emerged during the IR and HCI processes. Finally, it should be pointed out that the behavior of ΔN_{it} (SMG) and ΔN_{it} (CP) after exposure to IR process given in the paper [127, 128], is identical to the behavior of ΔN_{it} (SMG) given in the paper [126] in case of the HCI process. The experiment was conducted with the samples that are structurally the same, but not identically processed as the samples in the work [126]. This comparison only illustrates the complicated nature of defect behavior occurring during the gamma radiation and the HCI process.

7.4 Application of PMOS transistor with Al-gate as a sensor and dosimeter of ionizing radiation

As early as 1974, there emerged an idea on the possibility of application of MOS transistors for the detection of the absorbed dose of ionizing radiation [7]. It was followed by the design and production of radiation-sensitive PMOS transistor with Al gate which is known under the title RADFET (radiation sensitive field effect transistors) which could be used as both sensor and dosimeter of ionizing radiation (gamma and X-radiation) [7]. These dosimeter transistors have so far found partial application in modern aircrafts [129, 130] (in which higher values of absorbed doses are measured) in medicine (in radiology, where they have the role of radiation sensors) [131, 132], in nuclear industry [132] and military [133, 134]. However, no PMOS dosimeter for small doses of radiation measuring, which could be used as a personal dosimeter has yet been realized.

The basic parameter for PMOS dosimetric transistor is the threshold voltage V_T, on basis of which the absorbed radiation dose is determined. The change in threshold voltage, as already said above, is a consequence of oxide trapped charge density ΔN_{ot} and interface traps ΔN_{it} caused by the IR process. In the case of PMOS transistors, the increase in these densities leads to the increase in V_T, as opposed to NMOS transistors, in which an increase of ΔN_{ot} reduces V_T, and increase of ΔN_{it} increases its value.

In general, the change in threshold voltage ΔV_T with an absorbed dose of radiation D is given by the following expression:

$$\Delta V_T = A \cdot D^n ,$$
(37)

where A is the constant, and n is the degree of linearity. For $n = 1$, the constant A represents the sensitivity S of dosimetric transistor

$$S = \frac{\Delta V_T}{D} ,$$
(38)

Figure 26 represents the single-point method, which is primarily used to determine the threshold voltage of PMOS dosimetric transistors [135]. It consists of the establishing constant current through the channel I_D (the value of 10 μA is usually taken) and measuring of V_0 voltage which corresponds with this current. It is also considered that the change in this voltage (ΔV_0) corresponds with the change in threshold voltage (ΔV_T).
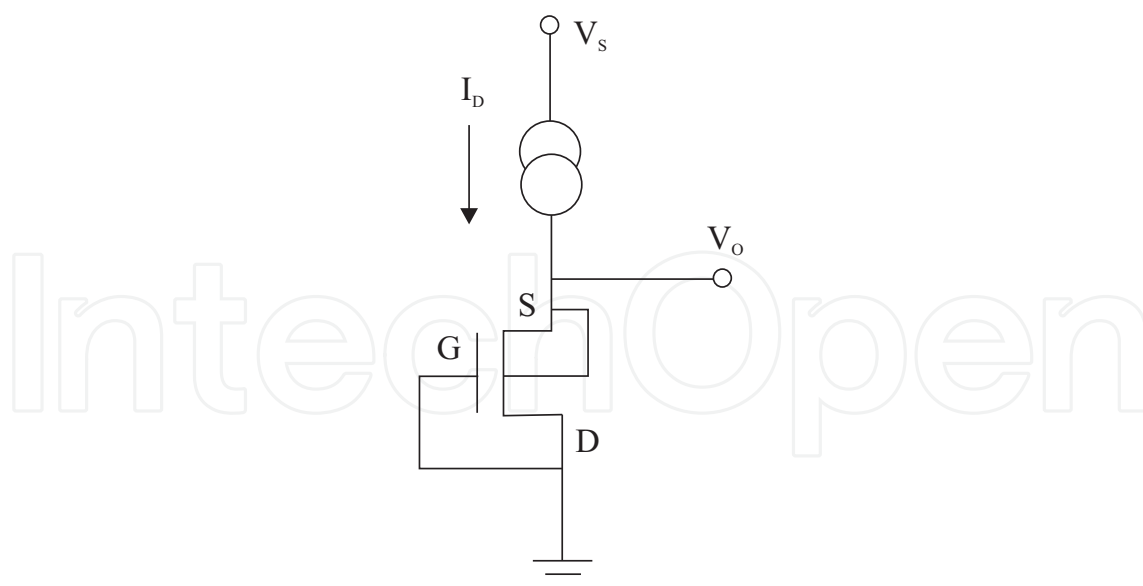
Fig. 26. The threshold voltage determination using single point method.

The second important parameter of PMOS dosimetric transistors is the recovery of threshold voltage after the radiation, which is known under the term fading f(t). It can be expressed in the following way:

$$f(t) = \frac{V_T(0) - V_T(t)}{V_T(0) - V_{T0}} = \frac{V_T(0) - V_T(t)}{\Delta V_T(0)} ,$$ (39)

where V_{T0} is the threshold voltage prior to radiation, $V_T(0)$ immediately after irradiation, $V_T(t)$ after annealing time t and $\Delta V_T(0)$ is the threshold voltage shift immediately after irradiation of PMOS dosimetric transistor.

Fading can also be determined on the basis of the values ΔN_{ot} and ΔN_{it} [136, 137]

$$f(t) = \frac{\Delta N_{ot}'(t) + \Delta N_{it}'(t)}{\Delta N_{ot}(0) + \Delta N_{it}(0)} ,$$ (40)

in which $\Delta N'_{ot}(t) = \Delta N_{ot}(0) - \Delta N_{ot}(t)$ ("the annealing part" of the oxide trapped charge) and $\Delta N'_{it}(t) = \Delta N_{it}(0) - \Delta N_{it}(t)$ ("the annealing part" of the interface traps), $\Delta N_{ot}(0)$ and $\Delta N_{it}(t)$ are the densities of oxide trapped charge and interface traps after the annealing for the time t, respectively, while $\Delta N_{it}(0)$ and $\Delta N_{it}(t)$ are adequate densities after the radiation, i.e. at the start of annealing.

The papers [136-143] show the results of exposure to gamma radiation and subsequent annealing of PMOS dosimetric transistors manufactured in the company Ei-Microelectronics, Nis, Serbia, while the papers [135, 143-145] show the results of radiation and annealing of PMOS dosimetric transistors manufactured in Tyndall National Institute, Cork, Ireland. Figure 27 shows change in threshold voltage with an increase in absorbed dose of gamma radiation for the transistors with oxide thickness of 1.23 μm [136]. It can be seen, that this dependence can be displayed in a coordinate system with log-log scale, with a straight line for all applied voltages at the gate. Also, changes in threshold voltage are greater in the case of positive voltages at the gate, although sensitivity grows with the increase of the absolute value V_G in both polarization modes (the smallest value applies to

the zero polarization). This means that the increase of ΔV_T takes place regardless of the direction of the electric field in oxide, but the size of these changes is dependent on it.
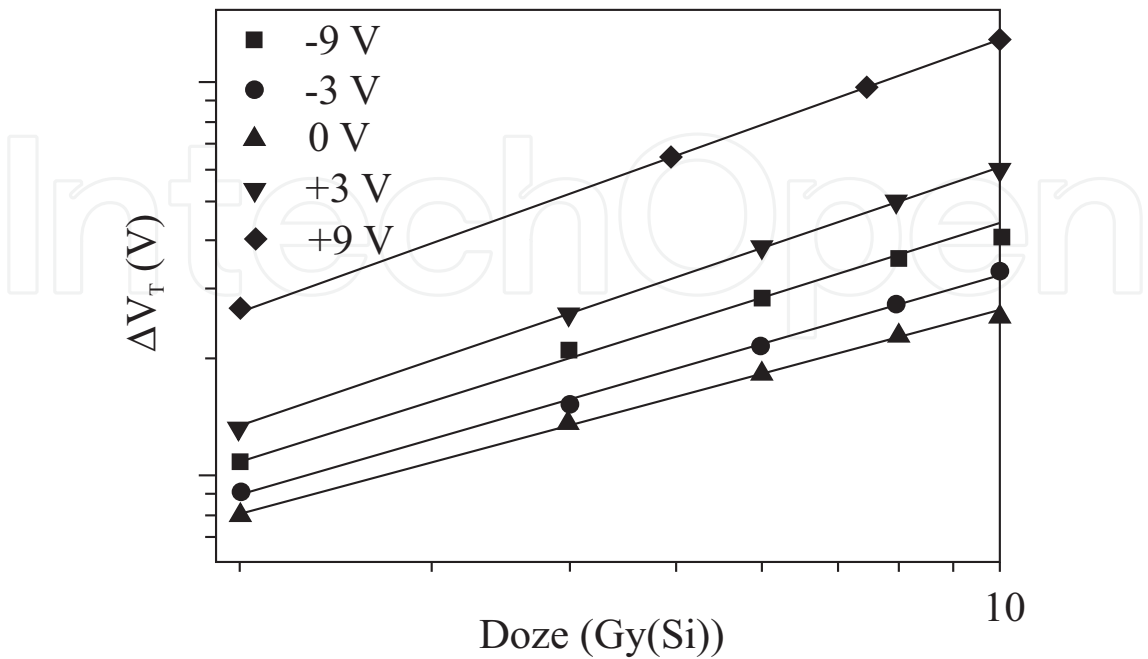

Fig. 27. Threshold voltage shift (ΔV_T) during irradiation of pMOS transistor, with 1.23 μm thick oxide.

Figure 28 shows change in threshold voltage as a function of absorbed dose of gamma radiation for different oxide thicknesses, for the gate voltage of V_G = 3 V [139]. It can be seen
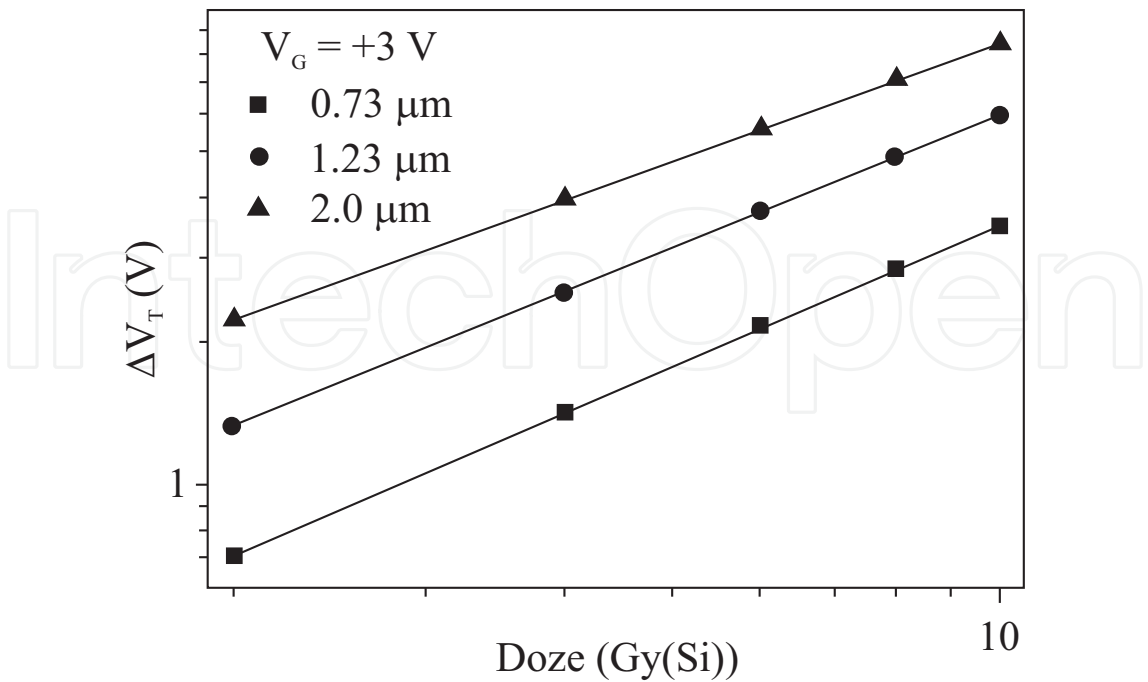

Fig. 28. Threshold voltage shift (ΔV_T) during irradiation of pMOS transistors with different oxide thickness and gate polarization of +3 V.

that the sensitivity grows along with the thickness of gate oxide, and as the tested PMOS dosimetric transistors have thermal oxide with the same thickness, these results show a significant role of CVD oxide in the change of threshold voltage. The gate voltage for these transistors was the same, i.e. the electric field in the thickest oxide was smallest, which affected their sensitivity.

The paper [135] shows changes in the threshold voltage of PMOS dosimetric transistors for the oxide thicknesses of 100 mm for the values of absorbed gamma radiation doses between 50 and 300 Gy, while the paper [143] stated this dependence for the dose range between 100 Gy and 500 Gy for gate voltages during radiation V_G=0 and 5 V (Figure 29). It was found that there is a linear dependence between the threshold voltage change and the absorbed radiation dose when the dose range amounted between 10 Gy and 500 Gy (Figure 29).
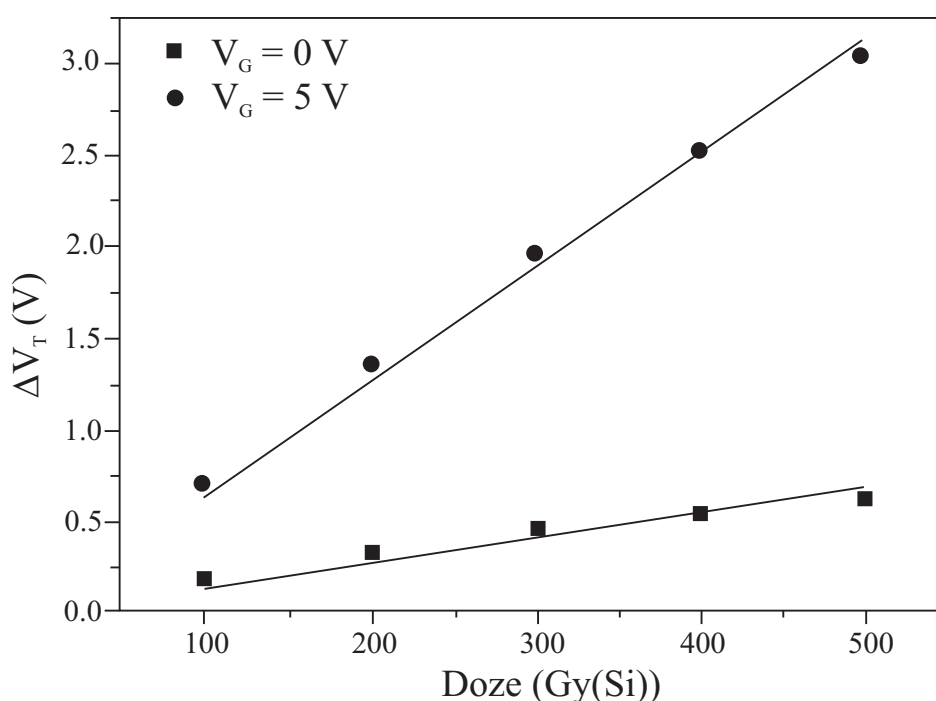
Fig. 29. Threshold voltage shift (ΔV_T) of pMOS transistors during irradiation for V_G = 0 V and V_G = 5 V.

Change of fading, as the other important parameter for PMOS dosimetric transistors, during annealing at room temperature is shown in figures 30 and 31 [116] for the transistors with oxide thickness of 1.23 and 2.0 μm. The radiation and recovery were conducted with the same voltage values at the gate. It can be seen that the transistors having oxide thickness of 2.0 μm show a more pronounced negative fading. On the basis of fading behavior of transistors with the same oxide thickness, but with different gate polarization, it is obvious that no concrete conclusion which would apply to all radiation-exposed transistors can be given. Lack of knowledge about the explicit form of dependence of fading behavior since the recovery time is not a deficiency of these PMOS transistors (which cannot be said for the sensitivity), as the practical application requires solely that it be smaller than some previously set value (usually, fading should be no less than ± 10% after three months of annealing at room temperature). On the basis of these results, it can be seen that for the oxide thickness of 2.0 μm, when the sensitivity is at its peak, the fading has a small value,

and therefore in the case V_G=9 V, the sensitivity is S = 2 V/Gy for the absorbed dose D = 10 Gy(Si) and fading 5.9 % for annealing time of 3500 h
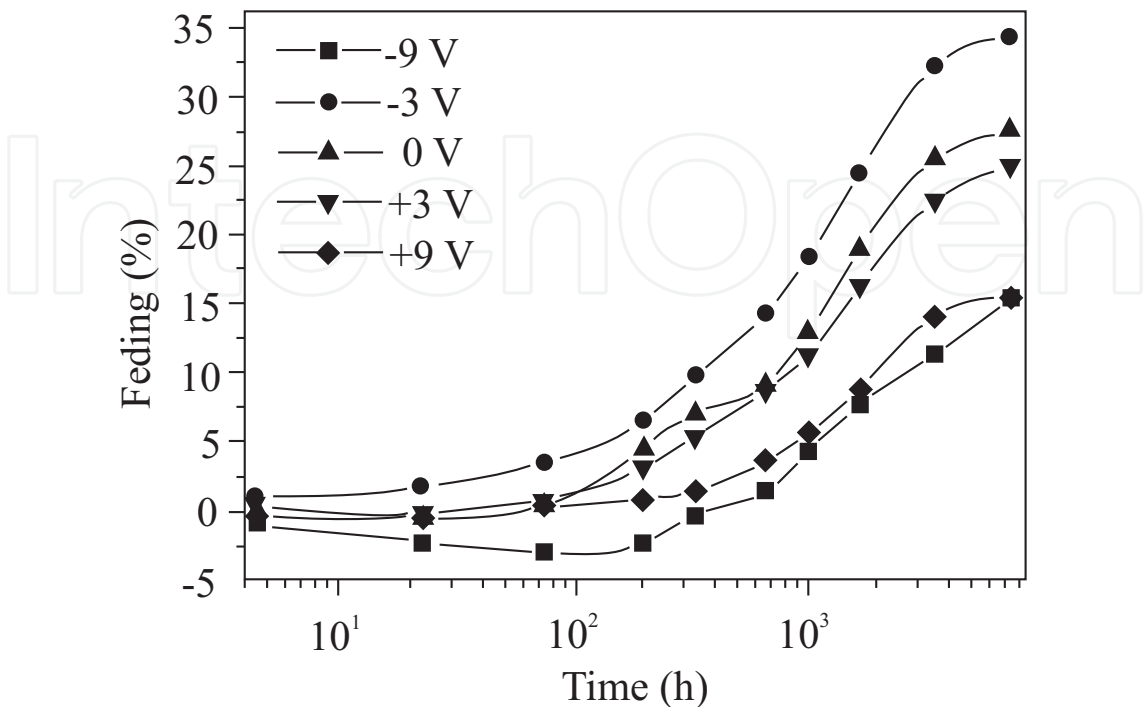

Fig. 30. Fading of irradiated pMOS transistors, with gate oxide thickness of 1.23 μm, during room temperature/bias annealing.
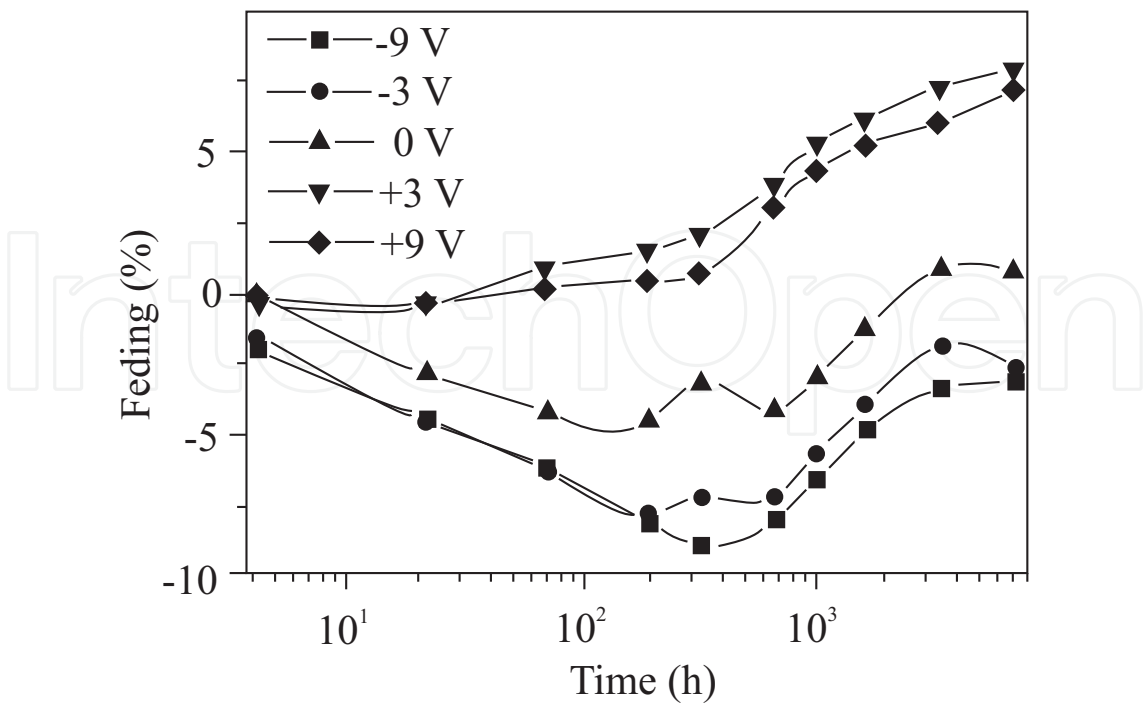

Fig. 31. Fading of irradiated pMOS transistors, with gate oxide thickness of 2.0 μm, during room temperature/bias annealing.
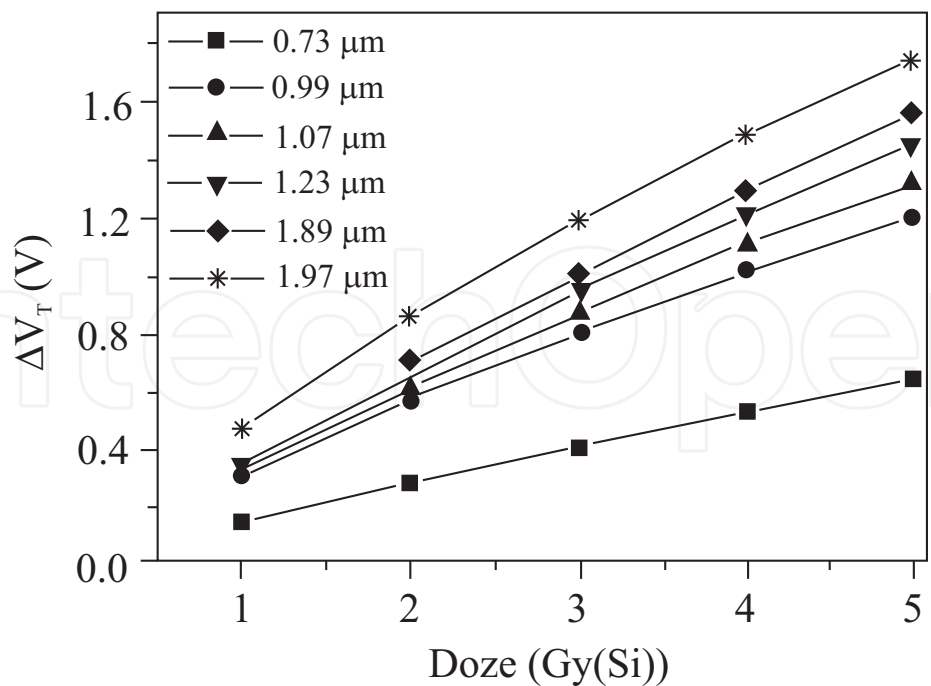
Fig. 32. Threshold voltage shifts (ΔV_T) during irradiation at dose rate $1.2 \cdot 10^{-3}$ Gy/s for different gate oxide thickness of pMOS transistors.
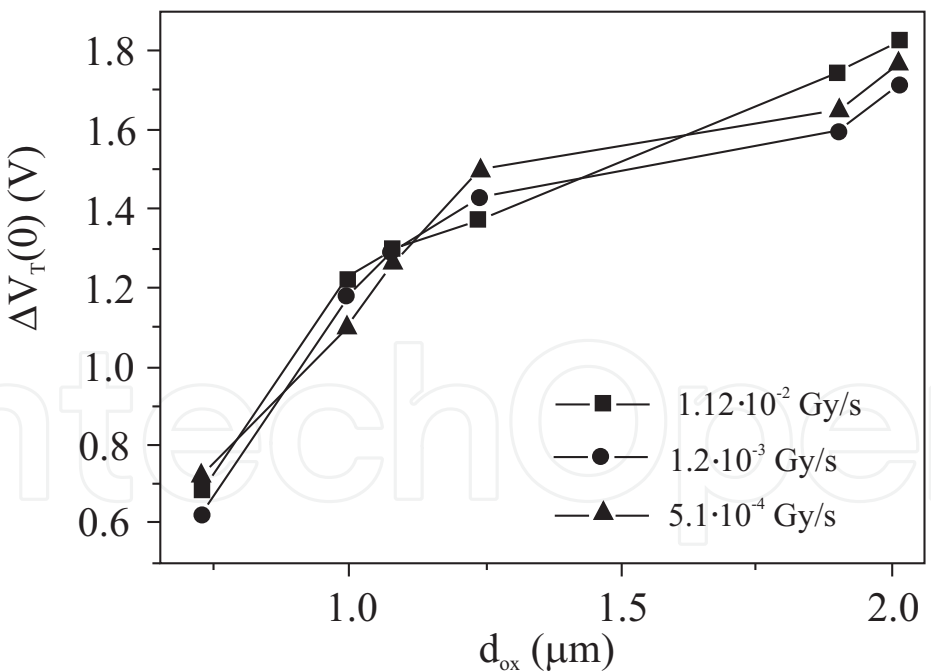

Fig. 33. Threshold voltage shifts (ΔV_T) for different pMOS transistors irradiated up to 5 Gy(Si).

Figure 32 shows changes in the threshold voltage from a dose of gamma radiation of PMOS dosimetric transistors with different gate oxide thicknesses (the thickness of thermal oxide was 0.3 μm, and the thickness of CVD oxide were different) during radiation with the dose

of 1.2 $\cdot 10^{-3}$ Gy [138]. It can be seen that the sensitivity grows along with the gate oxide thickness. This is clearly displayed in Figure 33 which shows changes in threshold voltage immediately after radiation, i.e. prior to annealing at room temperature for three dose speeds. On the basis of these figures, it can be concluded that the main influence on sensitivity is exerted by the total oxide thickness, and then the thickness of CVD oxide. Namely, the transistors with oxide thickness of 1.97 μm are more sensitive that a transistor with oxide thickness of 1.89 μm, although they have smaller thickness of CVD oxide (the same applies to the oxide thicknesses of 1.07 μm and 0.99 μm). A cause for such behavior can be the thickness and the type of thermal oxide.

As opposed to the results shown in Figures 32, in which the sensitivity of the tested PMOS transistors is given in the range between 1 and 5 Gy, Figures 34 shows their sensitivity in the dose range between 0.003 and 1 Gy for the case when there was no gate polarization during radiation [116].
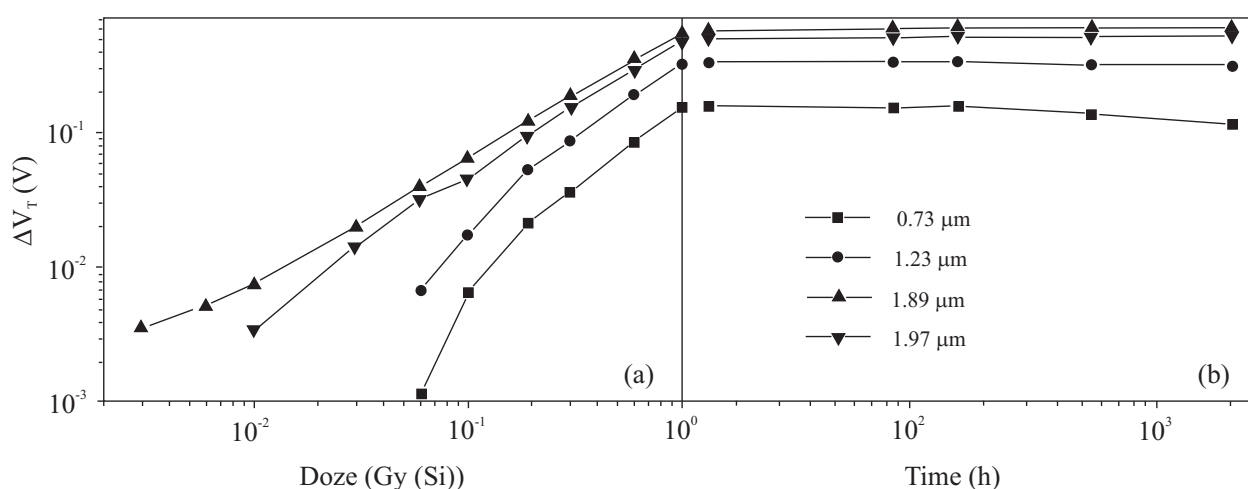

Fig. 34. Threshold voltage shifts (ΔV_T) of pMOS transistor during irradiation with dose rate of $7.51 \cdot 10^{-5}$ Gy/s (a) and annealing at room temperature (b), for different values of gate oxide thickness.

As it can be seen from the figure 34, the greatest sensitivity is displayed by the transistors with oxide thickness of 1.89 μm, which can register radiation doses in the order of magnitude cGy. As this transistor has the greatest thickness of CVD oxide, it can be assumed that this oxide would have a significant role in the area of small doses. The changes in threshold voltage during annealing of up to 2000 hours are insignificant for any oxide thickness (Figure 34b). Results with transistors of this oxide thickness show that their sensitivity increases with the increase of gate voltage during the gamma radiation, especially when the doses are higher than 0,01 Gy.

8. References

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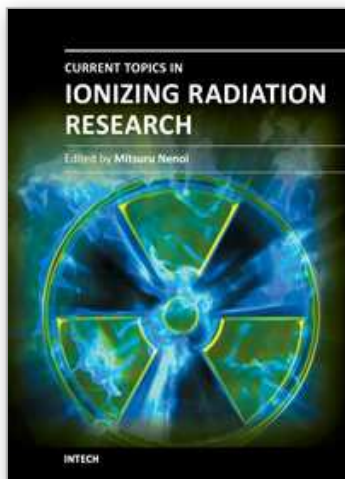
Current Topics in Ionizing Radiation Research

Edited by Dr. Mitsuru Nenoi

Since the discovery of X rays by Roentgen in 1895, the ionizing radiation has been extensively utilized in a variety of medical and industrial applications. However people have shortly recognized its harmful aspects through inadvertent uses. Subsequently people experienced nuclear power plant accidents in Chernobyl and Fukushima, which taught us that the risk of ionizing radiation is closely and seriously involved in the modern society. In this circumstance, it becomes increasingly important that more scientists, engineers and students get familiar with ionizing radiation research regardless of the research field they are working. Based on this idea, the book "Current Topics in Ionizing Radiation Research" was designed to overview the recent achievements in ionizing radiation research including biological effects, medical uses and principles of radiation measurement.

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