# 1

# Implantable Cardioverter Defibrillators

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## 1. Introduction

In recently years, Artificial Neural Networks have been studied extensively and applied in medical field, and have been demonstrated to have much better pattern recognition ability. In this chapter we present a VLSI chip to be implemented using 0.35 μm CMOS technology which is the implantable cardioverter defibrillator (ICDs).
Implantable cardioverter defibrillator is a device which monitors the heart and delivers electrical shock therapy in the event of a life-threatening arrhythmia.
At present most ICDs are often using time information from leads to classify rhythms. (Leong, P. H.W &Jabri, M.A November 1995) This means they cannot distinguish some dangerous rhythms from the safe one, as in the case of ventricular-tachycardia arrhythmia. (R. Coggins et al., 1995)
Our chip is used to distinguish between two types of arrhythmia; The Sinus Tachycardia (ST) arrhythmia and the Ventricular Tachycardia (VT) arrhythmia. The ST is a safe arrhythmia occurs during vigorous exercises and is characterized with rate of 120beat/minute. The VT is a fatal arrhythmia with the same rate. They can be separated only by detecting the morphology changes in each one. (Acherya,U,R.,2004)
Most morphology changes are appeared in the QRS-complex. The QRS-complex for both the ST and VT arrhythmia's are shown in fig.1. (Dale Dublin, 2000)
Since most morphology changes are appeared in the QRS-complex, for classifying the arrhythmias we must separate QRS complexes from ECG, consequently a new circuit for detecting QRS is designed. In this circuit the R-R distance between two QRS complexes and also the pulse width of QRS complex are used to improve the detection algorithm.
By using fuzzy logic and some parameters of ECG (pulse width, R-R interval and peak) we can separate QRS complex from ECG and after that apply this part to a Neural Network for classification.
The proposed analog VLSI chip can detect such morphology changes. It has the following advantages:

- It is easily interfaced to the analog signals in an ICD (in contrast to the digital systems which require analog to digital conversion).
- Analog circuits are generally small in area.
- Low voltage circuits are used to decrease battery weight and size and to extend battery life time which required for portable and modern wireless equipment.
- Hamming network did not need to have a training system and the reference vectors determine the weights.

- Although temperature variation is a major source of drift problems, no need for temperature compensation as the human body is considered a stable environment.

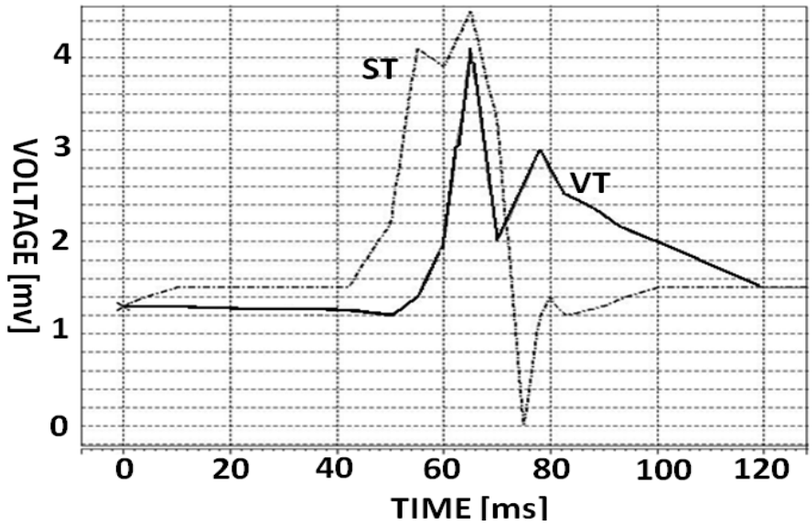


Fig. 1. Morphology change of QRS complex for both ST & VT.

This chapter deals with the design of Analog VLSI chip for implantable cardioverter defibrillator (ICDs). We first present the structure of system. Next, we describe each part separately and characteristic of each parts are described. Then, We show the circuits that are used for implementing of each part. Finally, we present the total block diagram of system with some simulations that verifies the functionality of system.

## 2. Architecture

The proposed chip consists of 3 main parts:

- QRS detector circuit
- Extracting QRS from an ECG circuit
- Classifying QRS complex circuit

First these parts will be explained separately and then the block diagram of the chip will be presented.

### 2.1 QRS detector circuit

The dominant component of the ECG is the QRS complex, which indicates the electrical depolarization of the muscles in the ventricle of the heart. Several clinical applications including implantable defibrillator require accurate QRS detection algorithms whiles The QRS is easily recognized by a human observer.

Various types of automated algorithms were proposed in the literature for detecting QRS. (K.Akazawa and K.Motoda 2001; Pan.J & Tompkins W.J 1985; Y. Suzuki, 1995) These algorithms use multiple features of the EGG including RR internal, pulse duration and amplitude, to detect QRS complexes. By processing several features, it is less likely that large amplitude but short duration noise would be mistaken for a QRS. Similarly, it is more likely that a true QRS with low amplitude, but normal width and RR internal would be correctly detected.

Fuzzy inference systems are well-suited for this application (fig.2), since detection in this system based on a few amounts of uncertainly which is very similar to the medical reasoning process.(O.Wieben, W.J Tompkins & V.X. Afonso 1999) Moreover the decision process is extremely easy to understand by human; consequently such easy interpretability allows external changes by experts on the decision process.
In this work, we are using a fuzzy inference system to identify QRS complexes. In this system QRS complex will be detected provided that a square wave synchronizes with them, consequently we use a fuzzy controller to adjust this square wave with QRS complexes.R-R internal, pulse duration and amplitude are features that enter to a controller as inputs parameter. Fuzzy controller evaluates these features and adjusts the output pulse of VCO to be synchronized with QRS complexes.

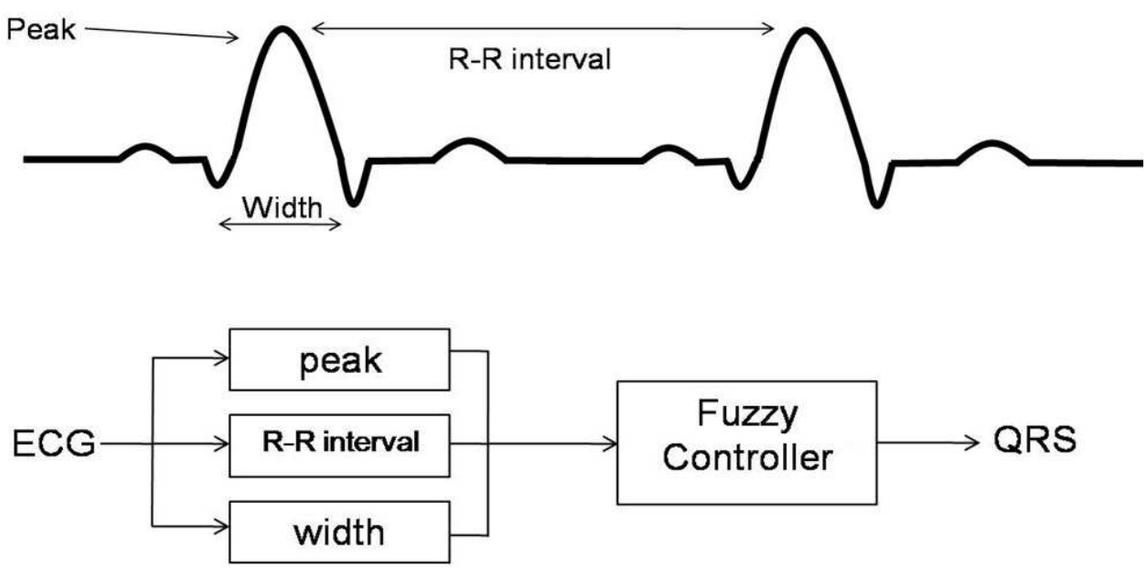


Fig. 2. QRS detection algorithm.

A feedback is used to correct the synchronization process. This feedback is produced by error between the output pulse of VCO and the pulse that show the width of QRS complex. This feedback is also enter to controller and processed by fuzzy controller. Finally, the output of fuzzy controller goes to VCO circuit and makes the output pulse of VCO to be synchronized with QRS complex (fig.3).

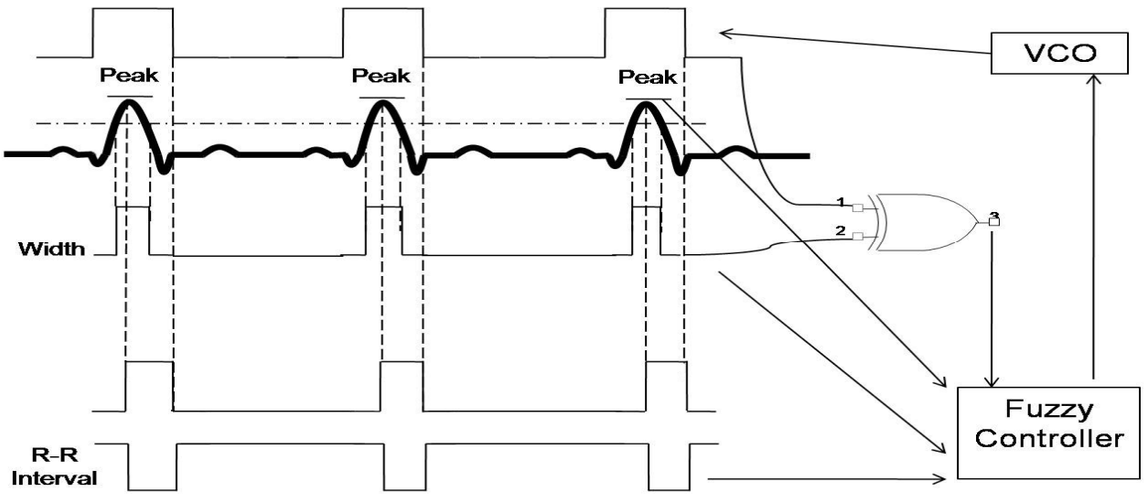


Fig. 3. QRS detection algorithms that is used in this project.

## 3. Extracting QRS from an ECG circuit

To separate QRS complexes, we passed ECG signals and synchronize VCO trough an analog median filter. (fig.4). Median Filter passes the median part of the input signals which, in this case, is QRS complexes.

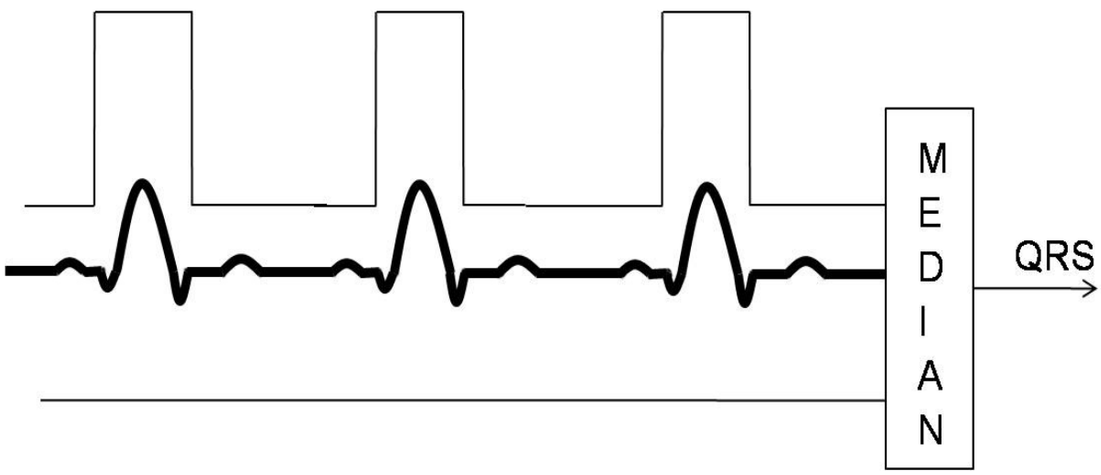


Fig. 4. Median Filter.

## 4. Classifying QRS complexes

The QRS complexes which were detected and separated from the rest of ECG signals are applied to an arrhythmia classifier. This classifier is used to distinguish between two types of arrhythmia: The Sinus Tachycardia (ST) arrhythmia and the Ventricular Tachycardia **(**VT**)** arrhythmia. The ST is a safe arrhythmia occurs during vigorous exercises and is characterized with rate of 120beat/minute. The VT is a fatal arrhythmia with the same rate. They can be separated only by detecting the morphology changes in each one.
Since the most morphology changes are appeared in the QRS complex, we apply QRS complex to an arrhythmia classifier to classify it. This arrhythmia classifier consists of three building blocks: a sample and hold (S/H) circuit, a mapping circuit and a Hamming neural network classifier. Fig.5 represents a block diagram of the chip. First, the rhythm is inputted to a sample and hold circuit to obtain 10 samples of the input signal. These 10 samples are inputted to mapping circuits in parallel to map into unit length [-1 1]. The outputs of mapping circuits are input to Hamming Neural Network, which has two neurons in its output layer. Each neuron responds to a specified type of the input arrhythmia.

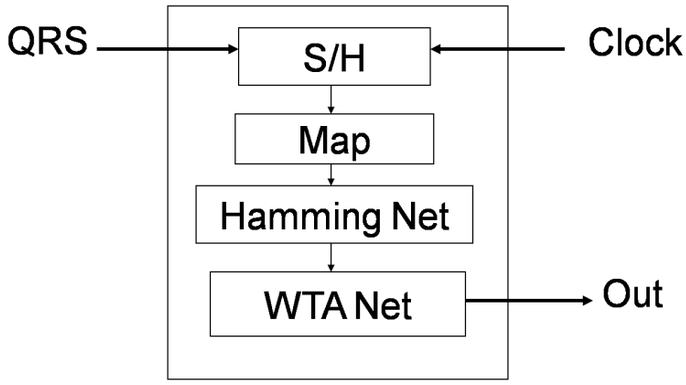


Fig. 5. Block diagram of QRS classifier.

### 4.1 Hamming Neural Network

A Neural Network classifier is made of a Hamming network, which is a maximum likelihood classifier network that can be used to determine which of several exemplar vectors are the most similar to an input vector (Laurene Fausett,1994 & M. B. Menhaj,2000). Fig.6 shows the simplest structure of a competitive layer.

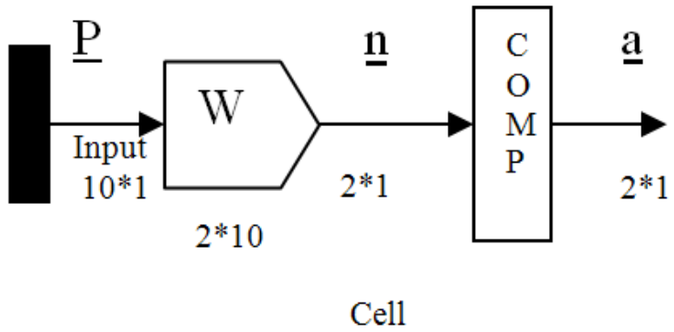


Fig. 6. A competitive cell.

$$\underline{a} = comp(W\underline{P}) \tag{1}$$

$$a_i = \begin{cases} 1, & i = i^* \\ 0, & i \neq i^* \end{cases} \tag{2}$$

i* is number of the cell that has the highest $n_i$ for our application i=1, 2.
In the Hamming Network, reference vector determines the weights (w) of the network.The hamming distance between input vector (P) and reference vector is calculated by n vector (equation 3). (Laurene Fausett,1994 & M. B. Menhaj, 2000)
Winner cell is determined with multiplying input vector to weights. The largest value corresponds to the smallest angle between input and weights vector if they are both of unit length [-1 1] (Laurene Fausett,1994 & M. B. Menhaj, 2000).

$$\underline{n} = W\underline{P} = \begin{bmatrix} W_{11} & W_{12} & ..... & W_{110} \\ W_{21} & W_{22} & ..... & W_{210} \end{bmatrix} \underline{P} = \begin{bmatrix} \cos\ \theta_1 \\ \cos\ \theta_2 \end{bmatrix} \tag{3}$$

## 5. Circuit design

The designing method of blocks show in fig.5 is given below:

### 5.1 Sample and hold (S&H) circuit

The Sample and hold delay circuit is made of 10 cascaded stages to obtain 10 samples of the input pulse. Fig. 7 shows S/H circuit.

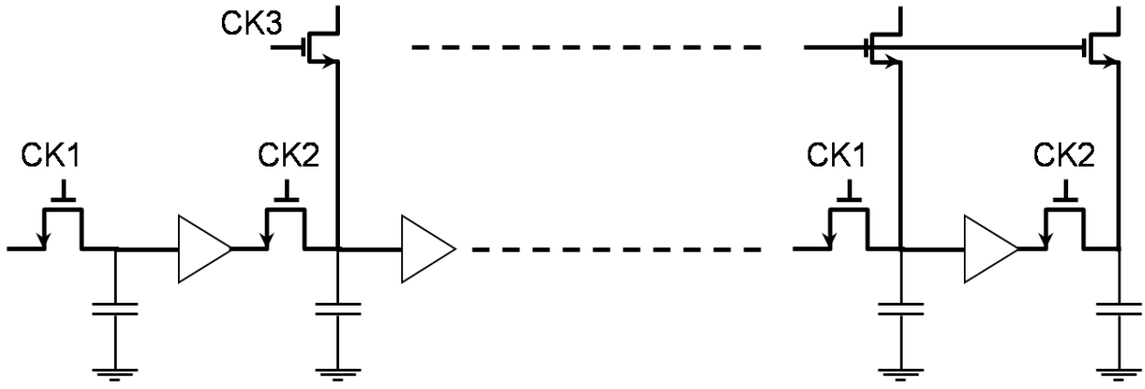


Fig. 7. Three stages of S/H circuit.

Two-phase non-overlapping clock ($CK_1$,$CK_2$) is used to control S/H. The sampled signal $x_i$ then are inputted mapping circuit through another analog switch $m_i$ controlled by $CK_3$. The timing diagram of $CK_1$, $CK_2$, $CK_3$ and the simulation result of the 1st stage of sample and hold circuit are shown in fig. 8.

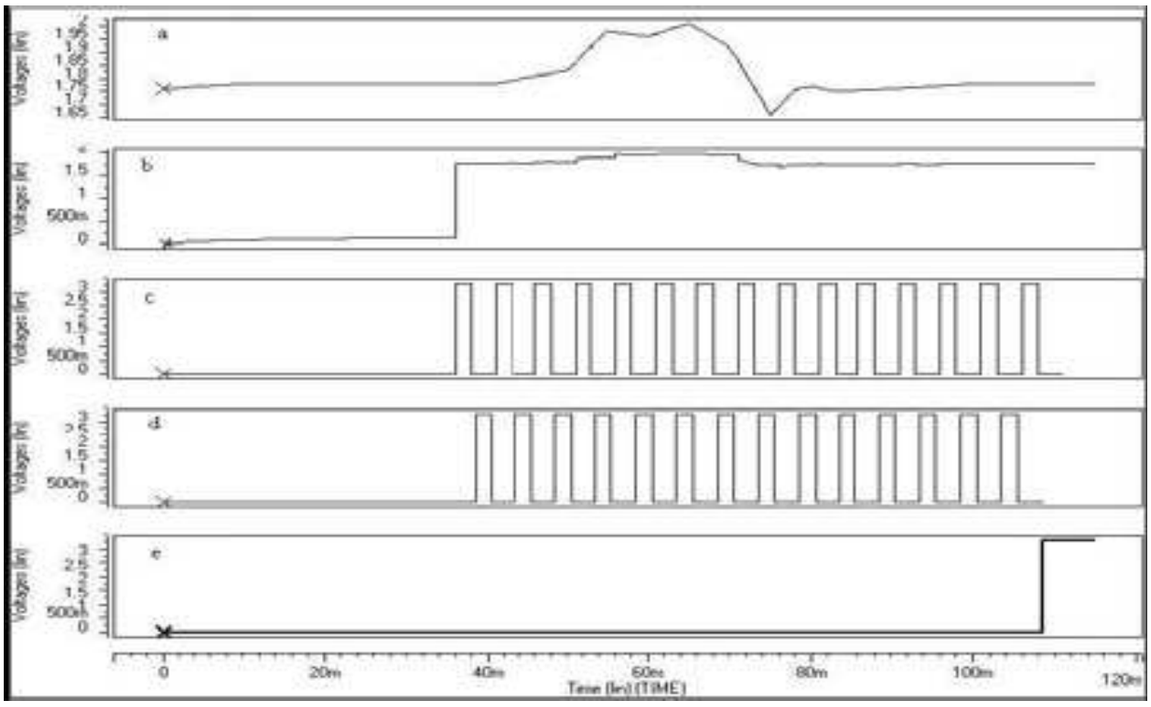


Fig. 8. (a) Input to S/H circuit. (b) Sampling signal of the 1st stage. (c) CK1. (d) CK2. (e) CK3.

In Fig. 8, the input rhythm of ST is applied to the S/H circuit and output of 1st stage is shown.

### 5.2 Mapping circuit

Before applying sampled data to Neural Network We have to map them into unit length [-1 1]. Figure 9 shows schematic of mapping circuit.

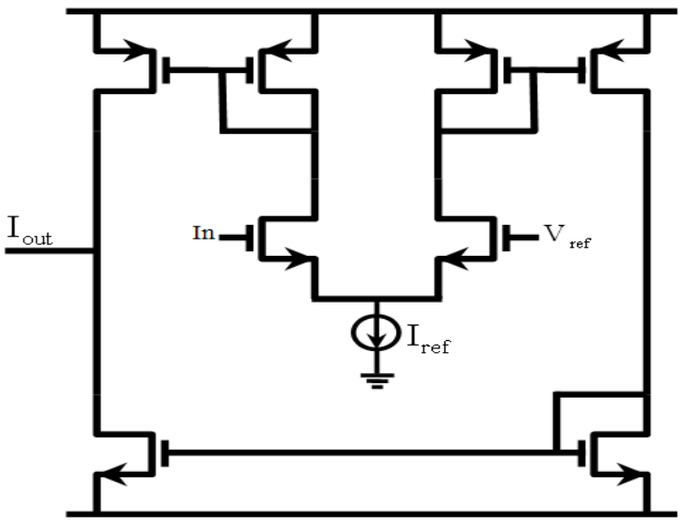


Fig. 9. Mapping circuit.

We use a simple differential pair in order to map input signal (sampled data) to unit length space [-1, 1]. By changing $V_{ref}$ and W/L ratio of input stage of differential pair, we can map any space to unit length space. (Wilamowski, B 1999)

### 5.3 Hamming Neural Network classifier

The Hamming Network consists of two groups of synapses and two layers of neurons. The first group with weight vector $W_1$= ($W_{11}$, $W_{12}$, $W_{13}$, …, $W_{115}$) is connected to first neuron layer. The second layer with weight vector $W_2$= ($W_{21}$, $W_{22}$, $W_{23}$, …, $W_{215}$) is connected to second neuron layer, each neuron in the output layer responds to a specified class of input arrhythmia. Figure 10 shows the structure of Network

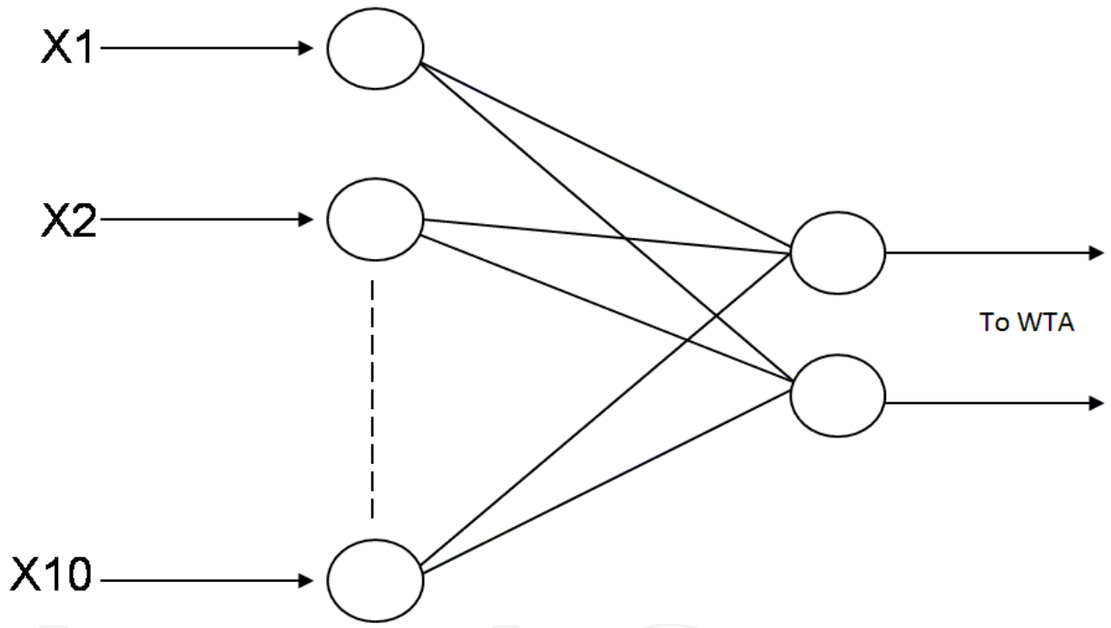


Fig. 10. Hamming Neural Network.

#### 5.3.1 Synapse

The computation of inner product between input signal and the local interconnection weight is called synapse and is mostly done by using an analog multiplier.(S. T.Lee; H. Shawkey 1999)

We use a new low voltage low power four quadrant analog multiplier as a synapse. Since output of a synapse is current, output of 10 synapses can be summed at a single node of circuit.

The circuit consists of four quadratic cells is shown in figure 11 where the relationship between the input current, $I_{in}$, and the output current, $I_{out}$, are quadratic. The quadratic cell is made of two transistors $M_n$ and $M_p$ which are biased to operate in triode region and $M_c$ which operates at saturation region.

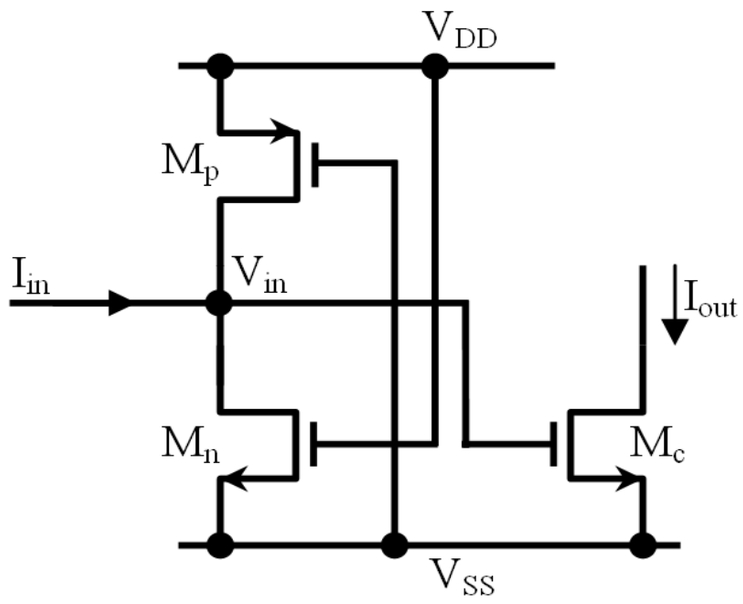


Fig. 11. Quadratic cell.

If $M_n$ and $M_p$ have the same transconductance, $\left( k_p = \mu_p C_{ox} \frac{W}{L} = k_n = \mu_n C_{ox} \frac{W}{L} = k \right)$ Then, it can be easily shown that the voltage ($V_{in}$) and the current ($I_{out}$) are given by

$$V_{in} = aI_{in} + b \tag{4}$$

$$I_{out} = k\left(c + I_{in}\right)^2 \tag{5}$$

Where a, b and c are $\frac{1}{k(2V_{DD} - |V_{tp}| - V_{tn})}$, $\frac{V_{DD}(V_{tn} - |V_{tp}|)}{2V_{DD} - |V_{tp}| - V_{tn}}$ and $\frac{2V_{DD}(V_{DD} - |V_{tp}|)}{2V_{DD} - |V_{tp}| - V_{tn}} - V_{tn}$ respectively.

Figure 12 shows the proposed four quadrant current multiplier circuit. The input currents of a multiplier are the sum of currents $I_X$ and $I_Y$ and the subtraction of the input currents $I_X$ and $I_Y$. By using quadratic relationship between input and output currents which are derived from Equation (5) drain currents of $M_{C1}$, $M_{C2}$, $M_{C3}$ and $M_{C4}$ would be

$$I_{C1} = k[c + a(I_X + I_Y)]^2 \tag{6}$$

$$I_{C2} = k[c - a(I_X + I_Y)]^2 \tag{7}$$

$$I_{C3} = k[c + a(I_X - I_Y)]^2 \tag{8}$$

$$I_{C4} = k[c - a(I_X - I_Y)]^2 \tag{9}$$

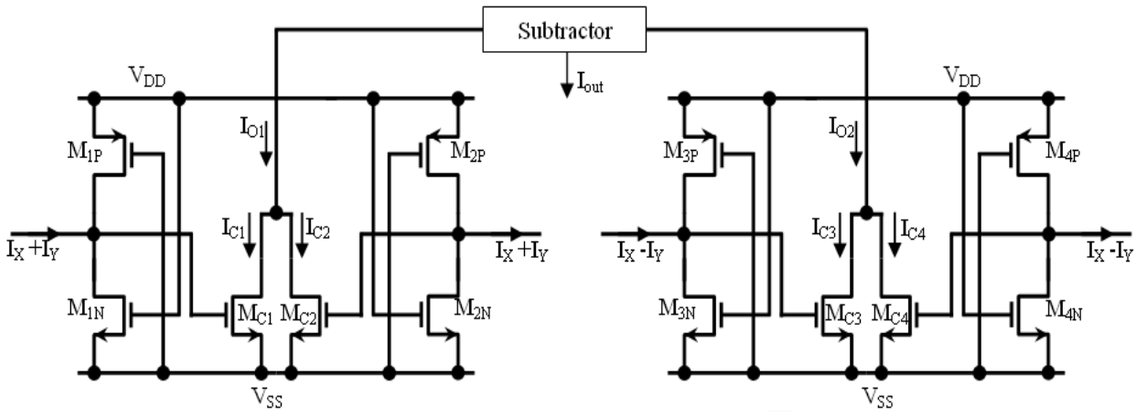


Fig. 12. Multiplier as a synapse.

According to Fig. 12, $I_{O1}$ is the combination of $I_{C1}$ and $I_{C2}$ while $I_{O2}$ is the combination of $I_{C3}$ and $I_{C4}$. $I_{O1}$ and $I_{O2}$ can be shown as

$$I_{O1} = k[2c^2 + 2a^2(I_X + I_Y)^2] \tag{10}$$

$$I_{O2} = k[2c^2 + 2a^2(I_X - I_Y)^2] \tag{11}$$

The output current of the four quadrant current multiplier $I_{out}$ is the difference between $I_{O1}$ and $I_{O2}$ and is given by

$$I_{OUT} = I_{O1} - I_{O2} = 8ka^2 I_X I_Y \tag{12}$$

Fig. 13 Shows DC characteristic of current multiplier circuit under input current ranging from -20 µA to 20 µA.

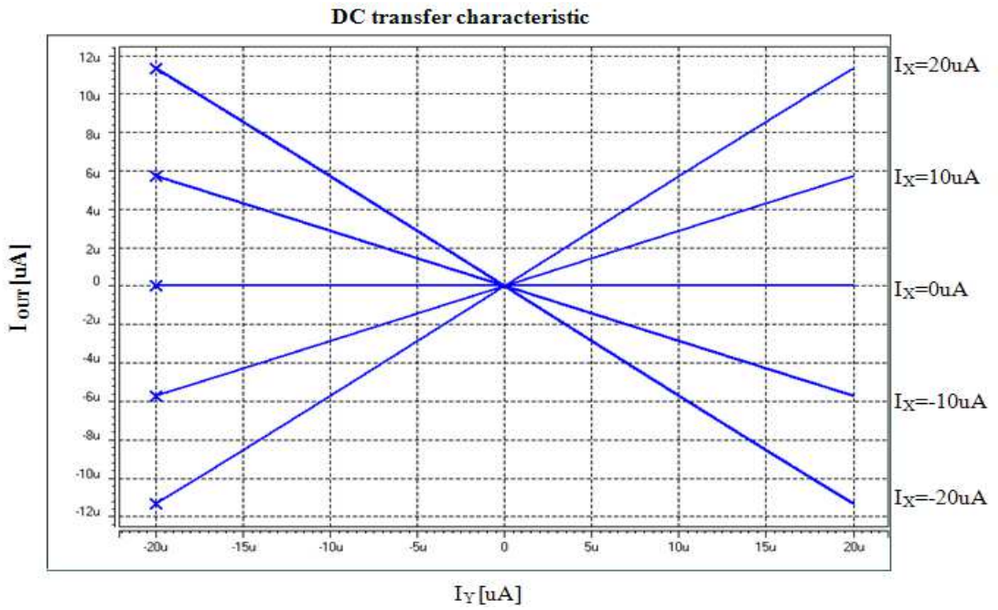


Fig. 13. DC transfer characteristic of four quadrant current multiplier.

### 5.3.2 Winner take all

The function of the WTA is to accept input signals, compare their values and produce a high digital output value (logic 'one') corresponding to the largest input, while all other digital outputs are set to low output value (logic 'zero').(J.Ramirez-Angulo et al., 2005)
Fig. 14 shows the block diagram of the WTA circuit. The circuit includes a 2-input current maximum selector with a simple voltage inverter.(.Ramirez-Angulo et al., 2005)

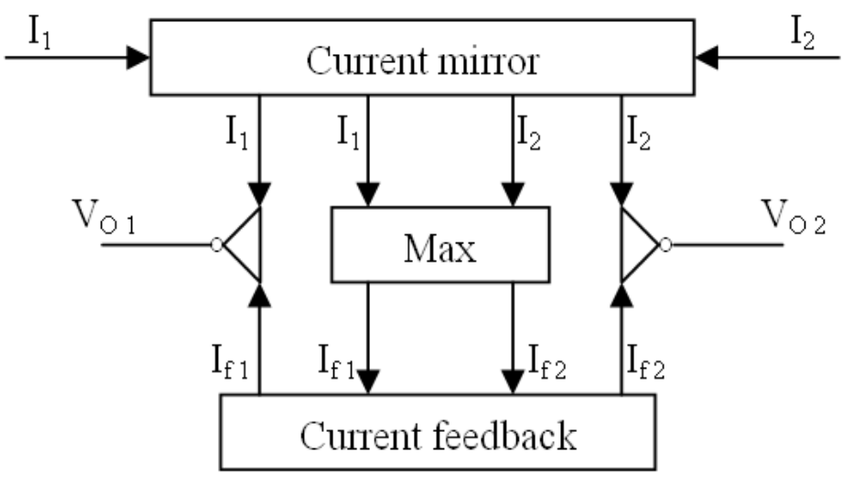


Fig. 14. Winner take all circuit.

### 5.3.3 The current max selector

The 2-input current maximum selector is shown in Fig. 15. The proposed current max selector has 2 input branches and each branch consists of an FVF (R.G. Carvajal et al., 2005), which is formed by voltage follower $M_{ai}$, and current sensing transistor $M_{ci}$.

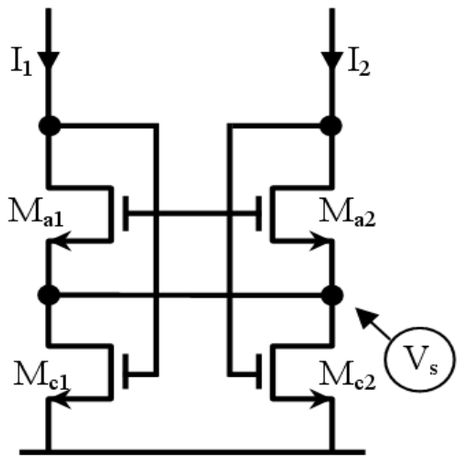


Fig. 15. 2-input max circuit.

Transistor $M_{ai}$ in an FVF performs as an improved voltage follower and the Gate-Source voltage drop of this transistor is constant (neglecting second-order effect) and independent of the load.
Transistor $M_{ci}$ operates as a current sensing device. It can sink large current by keeping its Drain voltage approximately constant. Moreover, the existing impedance at the Source of transistor $M_{ai}$ is very low due to the feedback loop.
The principle of operation of the circuit is as follow. The voltage at node "$V_S$" follows the maximum of input currents $I_1$, $I_2$, with a DC level shift $V_{GSn}$ where n denotes the maximum current.
In this condition the transistor ($M_{a1}$ or $M_{a2}$) which carrying the minimum current, has the greater Gate-Source voltage than the value that should have to operate in saturation mode, at this condition this transistor operates in triode mode with Drain-Source voltage value close to zero, thus the current sensing transistor is turning off in this branch and minimum and maximum currents passed through current sensing transistor of winning branch due to properties of FVF cell.

### 5.3.4 The overall structure of WTA circuit

The circuit of the 2-input WTA is shown in Fig.16. The currents ($I_1$, I2) are the inputs of the circuit.
Each current is mirrored into current max Selector, as well as, into the feedback circuit due to PMOS current mirror $M_{12}$, $M_{22}$.
Thus the input current of each voltage inverter is:

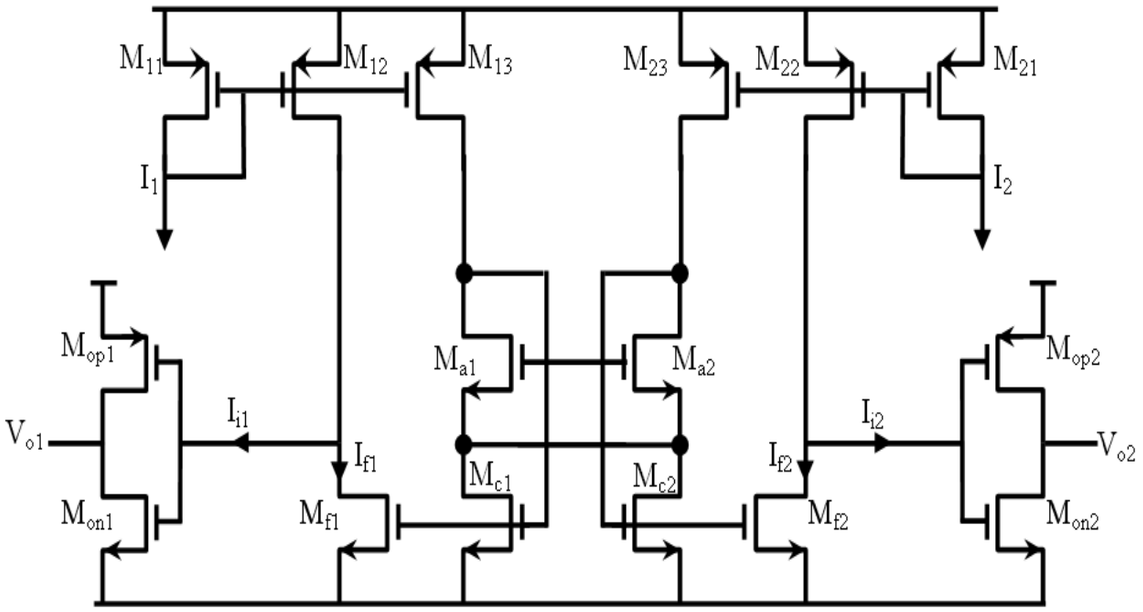


Fig. 16. 2-input WTA circuit.

$$I_{i1} = I_1 - I_{f1} \tag{13}$$

$$I_{i2} = I_2 - I_{f2} \tag{14}$$

We assume at the steady state, the current $I_1$ is the largest input current $I_1$=max ($I_1$, $I_2$)
So

$$I_{f1} = I_1 + I_2 \tag{15}$$

$$I_{f2} = 0 \tag{16}$$

From the Equation (13) – Equation (16) the input current of each voltage inverter is:

$$I_{i1} = I_1 - (I_1 + I_2) = -I_2 \tag{17}$$

$$I_{i2} = I_2 - 0 = I_2 \tag{18}$$

This means that only one input current of the voltage inverter, which is correspond to minimum current, is positive and all the other currents are negative. Thus the digital voltage outputs of the circuit will be at logic

$$\begin{cases} V_{o1} = \text{'one'} \\ V_{o2} = \text{'zero'} \end{cases} \tag{19}$$

Fig.17 shows the block diagram of the proposed QRS classifier

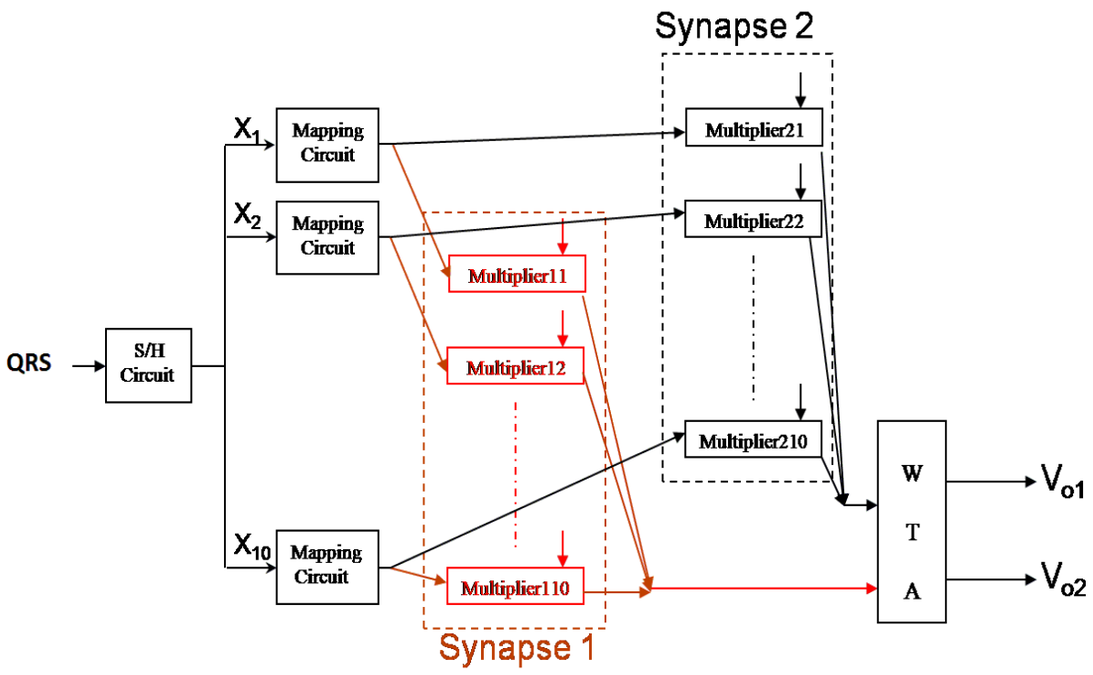


Fig. 17. Block diagram of the proposed QRS classifier.

## 6. The proposed arrhythmia classifier chip

The block diagram of proposed system is presented in fig.18.
In this system, multiple features of ECG are measured by analog circuit. These features are applied to a fuzzy controller to be processed. The output of fuzzy controller goes to a VCO which is used to synchronize the output pulse of VCO with the specific part of ECG. Finally, the QRS complexes which are filtered by median filter are applied to arrhythmia classifier provided that the error of detection algorithm is below a normal value. Moreover, the arrhythmia classifier has 2 outputs that each one responds to a specific type of the input arrhythmia.

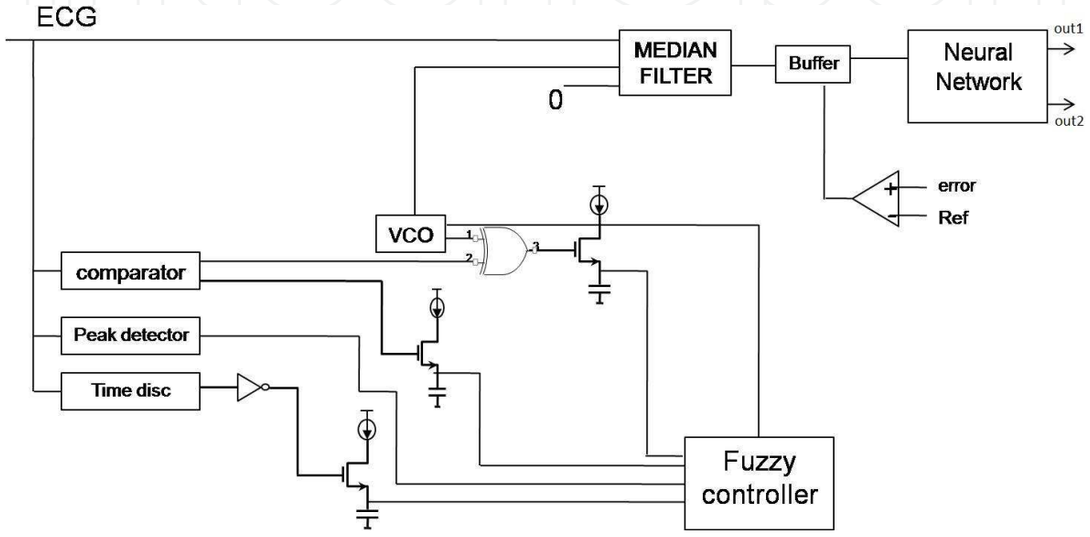


Fig. 18. Block diagram of proposed system.

Simulation result of the system in both cases is shown in figure 19 and 20.
In fig.19 the inputting rhythm of ST is applied to system caused to digital outputs of OUT1 goes to "One" and OUT2 goes to" Zero".

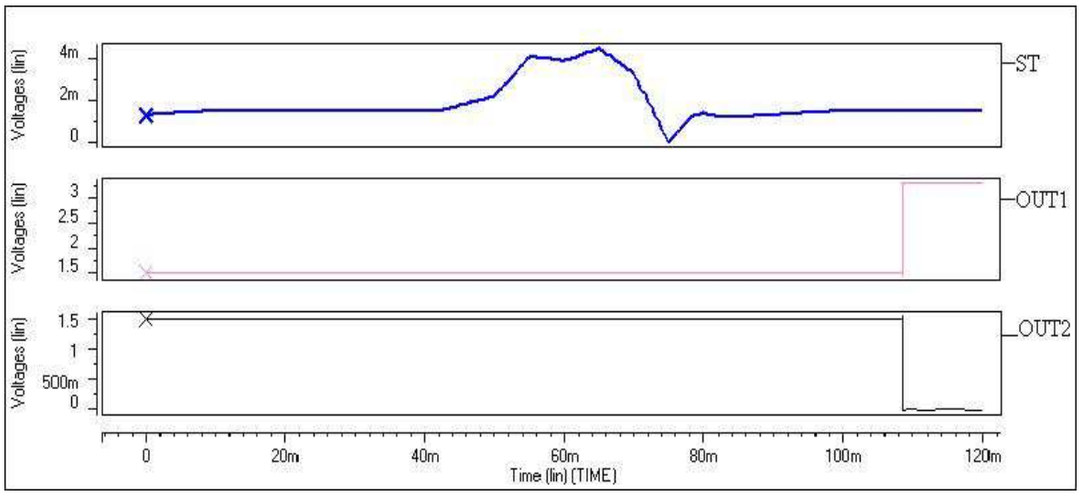


Fig. 19. Output of system for ST input.

In fig.20 the inputting rhythm of VT is applied to system caused to digital outputs of OUT1 goes to "Zero" and OUT2 goes to "One".

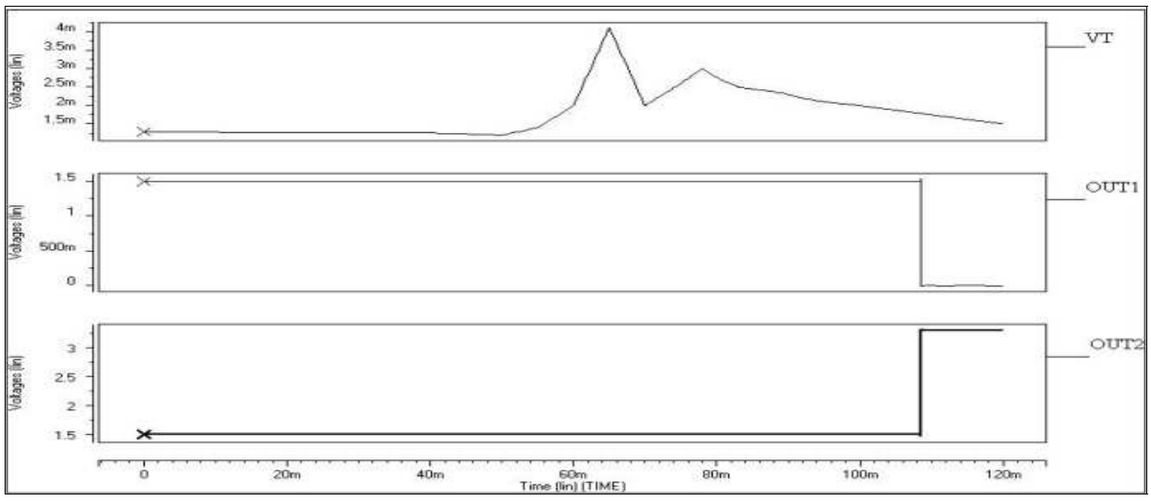


Fig. 20. Output of system for VT input.

## 7. Conclusion

In this chapter a VLSI Analog chip for arrhythmia classification is presented.
The proposed Network has the following features:

- No need for A/D converter between the ECG and the classification system.
- The system operates in the low frequency range, so that the parasitic of the layout likely have no effect on the operation of the chip.
- This system can be extended to distinguish m types of arrhythmias by using m number of neurons in the output layer of the Hamming Neural Network circuit.

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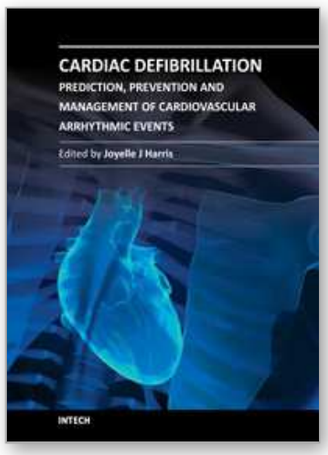


**Cardiac Defibrillation - Prediction, Prevention and Management of Cardiovascular Arrhythmic Events**

Edited by Dr. Joyelle Harris

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Millions of people throughout the world currently depend on appropriate, timely shocks from implantable cardioverter defibrillators (ICDs) to avoid sudden death due to cardiovascular malfunctions. Therefore, information regarding the use, applications, and clinical relevance of ICDs is imperative for expanding the body of knowledge used to prevent and manage fatal cardiovascular behavior. As such, the apt and timely research contained in this book will prove both relevant to current ICD usage and valuable in helping advance ICD technology. This book is divided into three comprehensive sections in order to cover several areas of ICD research. The first section introduces defibrillator technology, discusses determinants for successful defibrillation, and explores assessments of patients who receive defibrillation. The next section talks about predicting, preventing, and managing near catastrophic cardiovascular events, and research presented in the final section examine special cases in ICD patients and explore information that can be learned through clinical trial examinations of patients with defibrillators. Each chapter of this book will help answer critical questions about ICDs.

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