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Source and Drain Junction Engineering for Enhanced Non-Volatile Memory Performance

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1. Introduction

There is strong demand to maintain the trend of increasing bit density and reducing bit cost in Flash memory technology. To this end, aggressive scaling of the device dimension and multi-level cell (MLC) or multi-bit cell (MBC) have been proposed in NAND and NOR Flash memory architectures. However, especially in NAND Flash memory, bit cost is expected to rise in the near future, because the process cost will increase more rapidly than the shrink rate. One solution to avoid such challenges is the use of three dimensionally stacked array structures, based on polycrystalline silicon (poly-Si). The utilization of poly-Si in the channel not only increases pass disturbs but also reduces the worst case string current. Indeed, for every doubling in density, the worst case string current halves. Since the channel of these devices is poly-Si and source/drain (S/D) regions are not formed (*i.e.*, a junction-free structure), the worst case string current (all cells in a string with high threshold voltage (V_T)) will quickly tend toward unreadably low values as density increases (Walker, 2009). Therefore, it is worthwhile to note that the impact on the S/D structures becomes important. Moreover, Fowler-Nordheim (FN) tunneling for programming is still very slow for certain applications that require high-speed operation.

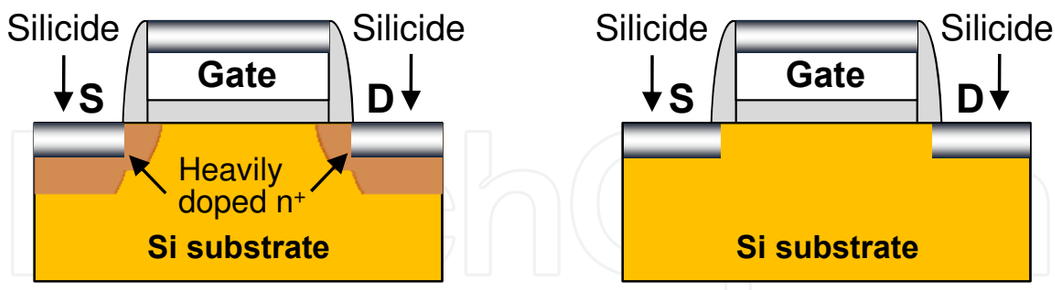
In NOR Flash memory, channel length scaling has threatened continued scaling and approaching its end point. For uniform channel hot electron injection (CHEI) programming, a robust margin for punch-through is a pre-requisite for cell transistors. However, CHEI programming aggravates immunity against punch-through by increasing the drain voltage to a level that will trigger CHEI. It is clear that the drain voltage window to guarantee both programming speed and margin from drain disturbance is narrowed as the channel length scales down. Moreover, the low injection efficiency compromising from vertical and lateral fields and the high parasitic resistance at the S/D junctions also impose a constraint on scaling the cell size reduction. Consequently, the lower effective program voltage due to the high parasitic S/D resistance in an extremely scaled cell results in a small V_T window and thereafter retards the program speed.

Herein S/D engineering for enhanced performance of Flash memory for two novel structures is demonstrated: (i) a dopant-segregated Schottky-barrier device (DSSB), and (ii) a junctionless MOSFET. First, we utilized dopant-segregated metallic silicide S/D junctions on charge trapping memory cells. They boosted the program speed even at a low program bias with the aid of abrupt band bending at the edge of metal silicided junctions. Second, the

structure of the junctionless transistor was examined from S/D junction engineering and cell size scaling points of view.

2. Schottky-Barrier (SB) MOSFET

SB-MOSFETs were initially proposed by Lepselter and Sze four decades ago (1968 – Bell Labs.), shortly after the invention of the current type of MOSFET by Kahng and Attala (1960 – Bell Labs.). Being different from the conventional MOSFET with doped/diffused S/D junctions, the SB-MOSFET has metallic silicided S/D junctions, realizing by employing a self-aligned silicide process, as shown in Fig. 2-1. The operating principle is based on gate induced electronic band bending to modulate the S/D thermionic and tunneling barrier (Larson et al., 2006). One remarkable advantage of the SB-MOSFETs is their low interface contact resistivity: $\rho_c \sim 10^{-9}$ Ω·cm² for metallic S/D compared with $\rho_c \sim 10^{-7}$ Ω·cm² in standard doped S/D junctions. Moreover, it is easier to control the abruptness/shallowness of the S/D junctions in metallic S/D junctions than in standard doped S/D junctions, and the solid solubility limitation associated with doping can also be resolved. From a fabrication viewpoint, the silicidation process is fully compatible with the standard CMOS technologies and does not require a high temperature annealing process; this prevents thermal degradation (in particular, for high-k gate dielectric layers and metal-gates) and reduces fabrication costs. However, for typical SB-MOSFETs, the on-state current is significantly limited by the existence of a SB height (SBH) at the S/D junctions; thus, the performance of SB-MOSFETs is still not comparable with that of conventional MOSFETs with highly doped S/D junctions. Therefore, it is necessary to find an appropriate material with a low SBH and develop a method to reduce the effective SBH, such as a dopant-segregation technique (Kinoshita et al., 2004), in order to enhance the performance of SB-MOSFETs.



(a) (b)

Fig. 2-1. Simplified schematic of (a) the conventional and (b) the SB devices

SB-MOSFETs are also interesting devices from a physics perspective. They can be used for high speed devices in highly scaled regimes because they have an abrupt energy band bending, which results from a large voltage drop at the source to the inversion channel. Importantly, a high lateral electric field exists around not the drain but the source edge. The carriers, *e.g.*, electrons for an n-channel SB-MOSFET, injected from the source thermally or via tunneling are accelerated by this electric field and become hot around the source edge. These properties are very useful and interesting for both logic and memory devices.

2.1 Operating principle of SB-MOSFETs

A band diagram schematically depicting the different operations of SB-MOSFETs is shown in Fig. 2-2. A small off-state current is possible at a gate voltage of 0 V as a result of the high effective barrier height for both electrons and holes. The effective barrier height for holes at a gate voltage of 0 V consists of two components: the intrinsic barrier for holes (Φ_{bp}) and the contact barrier ($\Phi_{contact}$). The contact potential results from the built-in potential energy (ψ_b) arising from the metal-semiconductor interface and the surface potential energy (ψ_s) resulting from the gate ($\Phi_{contact} = \psi_b + \psi_s$) (Fig. 2-2(a)). As a negative gate bias is applied, the effective barrier for holes is reduced to the intrinsic barrier height (Φ_{bp}) and the current increases as holes are ejected over the barrier primarily via thermionic emission (Fig. 2-2(b)). Note that when the effective barrier height ($\Phi_{effective} = \Phi_{bp} + \Phi_{contact}$) is the same as the intrinsic barrier height, the flat band source-to-body condition is formed (*i.e.*, $\Phi_{contact} \sim 0$ eV). For small gate voltage values, the drain voltage will mostly drop at the source, *i.e.*, the reverse bias contact, and current transport can be performed by the thermionic emission. This also holds in the subthreshold regime (small gate voltage). Further increases of the gate bias cause the bands to bend upwards and holes to tunnel through the barrier either directly or with thermal assistance (Fig. 2-2(c)). As noted above, the SBH limits the current flow in the subthreshold regime and becomes conductive in the on-state, where the channel resistance limits the current flow in an ideal case.

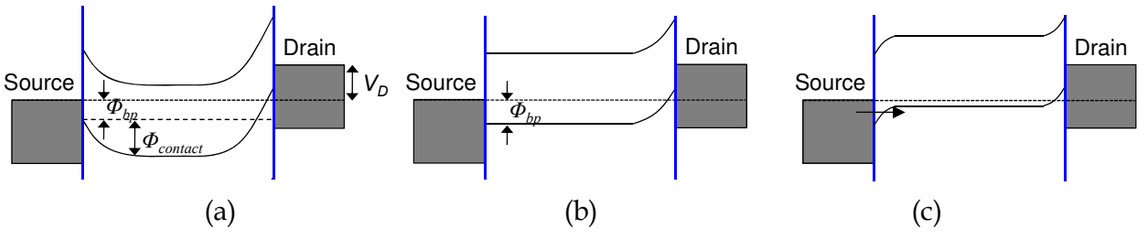


Fig. 2-2. Band diagrams of the different operating regimes of an SB-MOSFET: (a) off-state, (b) subthreshold regime, and (c) on-state.

2.2 Dopant-segregation technique

As mentioned earlier, the SB can limit the current drivability if an appropriate low SB material is not used. The dopant-segregation technique, an attractive technique to enhance the current density, has been introduced to SB-MOSFETs. If silicidation is performed on the doped silicon regions, the dopants can be redistributed at the interface between the silicide and silicon, which significantly affects the electrostatic properties of the SB junctions (Muraka, S. P. et al., 1087). The redistribution of dopants is determined by the diffusivity and solid solubility of dopants in the silicide and the presence of point defects at the interface between the silicide and silicon. Thermal annealing of silicide materials on ion implanted or doped (*i.e.*, activated or non-activated) silicon can induce redistribution of dopants during the silicidation process. In particular, dopants are segregated at the interface between the silicide and silicon as a result of the different solid solubility of these materials. Atoms of nickel (Ni), a candidate material in SB-MOSFETs, are the moving species, supplied by diffusion through the growing silicide layer to the silicide/Si interface. Subsequently, the covalent bonding of Si atoms is softened by the diffusion of Ni atoms. A significant change of volume occurs when the silicide is formed, which leads to high strain at the interface. As

a result, point defects (self-interstitial or vacancies) can be generated to partially relieve the stress. Due to the formation of vacancies, the diffusivity of the arsenic in the silicon is enhanced and it is forced out of the silicon after the silicide is formed. The arsenic dopants move towards the interface where they accumulates at the moving interface between the silicide and silicon. Although the dopant concentrations are generally below the solid solubility limit in the silicides and silicon, the point defects induced by the high strain interface can lead to the increment of local dopant concentrations that are higher than the solid solubility. This segregation of dopants is possible with boron, antimony, sulfur, chlorine, etc. as well as arsenic. The segregated dopants form a thin layer with a high concentration, which causes strong upward or downward band bending depending on the type of dopants, as shown in Fig. 2-3. As a consequence, the tunneling probability of the carriers through the effectively lowered Schottky barrier increases significantly. Although dopant-segregation is performed at relatively low temperatures, a fraction of the dopants is located at substitution sites in the silicon lattice and is therefore activated. Therefore, owing to enhanced injection efficiency, dopant-segregated SB (DSSB) MOSFETs have attracted considerable attention as a candidate for a high performance devices in future ULSIs.

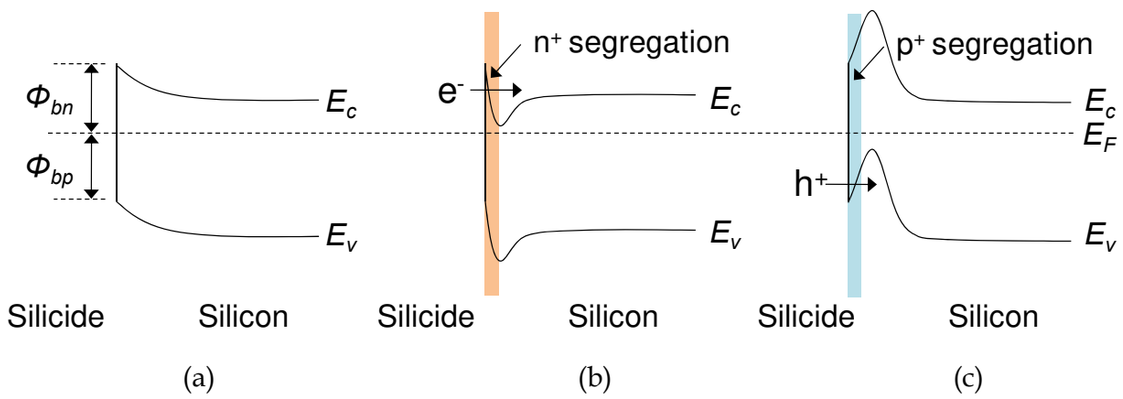


Fig. 2-3. Schematic band diagrams of (a) a mid-gap silicide with equal SB-heights for electrons and holes, (b) band bending induced by segregated n-type dopants, and (c) band bending induced by segregated p-type dopants.

2.3 Application to non-volatile memory devices

The metal-semiconductor SB diode is also known as a 'hot carrier diode'. The injected carriers from the semiconductor to the metal electrode, regardless of whether the injection mechanism is thermionic emission or tunneling, are forward biased Schottky barrier diodes, and they can obtain higher energies than the Fermi energies at the metal side. Moreover, the carriers injected from the metal to the semiconductor in the reverse biased junction can obtain higher energies than the Fermi energies in the semiconductor side, as shown in Fig. 2-4.

Both SB and DSSB MOSFETs at the on-state have an abrupt lateral voltage drop at the source end of the device due to the reverse biased source Schottky diode (Uchida et al., 2000, Kinoshita et al., 2006); therefore, a natural high electric field exists around the source edge. The carriers injected from the source electrode thermally or by tunneling will be accelerated by this electric field and will become hot around the source edge.

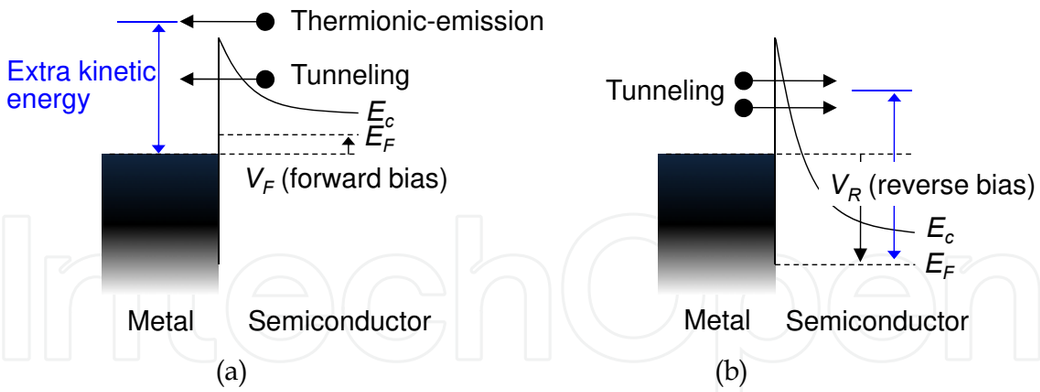


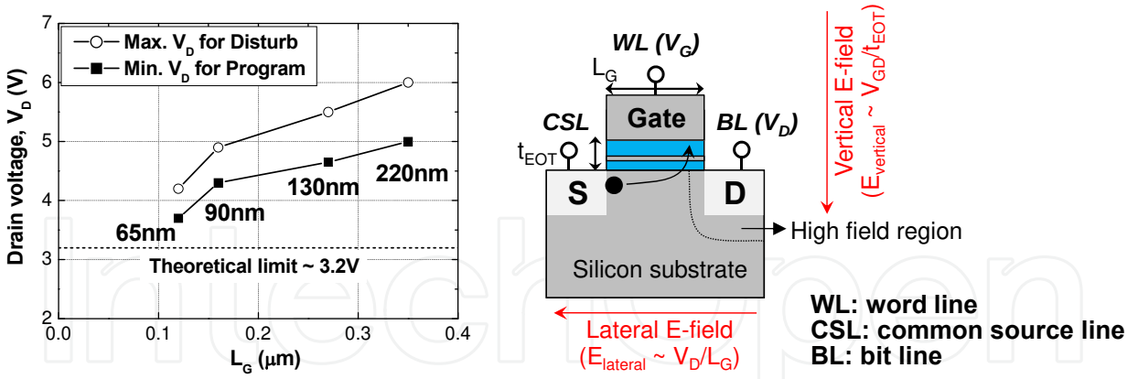
Fig. 2-4. (a) Conceptual explanation of hot carriers in (a) forward biased and (b) reverse biased in Schottky barrier diodes.

3. SB Flash memory

3.1 Hot-carrier program in double-gate DSSB FinFETs

Gate length scaling is the most critical limit in a NOR Flash memory cell, which uses a program method known as CHEI. This method aggravates immunity against punchthrough by increasing the drain voltage to a level that can trigger CHEI, as shown in Fig. 3-1(a). In addition, the low injection efficiency of the hot electrons generated at the drain side and the high parasitic resistance at the S/D also impose a constraint on scaling the cell size down. Consequently, the lower effective program voltage due to the high parasitic S/D resistance in an extremely scaled cell results in a small V_T window and thereupon retards the program speed. CHEI programming in conventional NOR-type Flash memories also poses a constraint on the choice of the proper gate voltage (V_G) and drain voltage (V_D), as shown in Fig. 3-1(b). A high V_D is necessary to induce a high lateral electric field for the generation of hot electrons. Furthermore, a high V_G is indispensable for attaining a sufficient vertical electric field for the injection of hot electrons into a charge storage node. Simultaneous optimization of the lateral and vertical electric fields is very difficult. Moreover, the high voltage needed to generate an adequate amount of hot electrons for programming consumes a large amount of power.

The source-side injection of hot electrons for programming at low voltage is therefore attractive because of its high injection efficiency and the absence of constraints on the co-optimization of V_G and V_D. Previous reports on source-side injection by the decoupling of hot electrons from the drain field demonstrated a fast low-voltage programming operation (Wu et al., 1986); however, it is difficult to adapt this approach to NOR-type Flash memory as it requires extra processes and different circuitry. In this section, an intensive analysis of NOR Flash memory, where double-gate (DG) DSSB FinFET silicon-oxide-nitride-oxide-silicon (SONOS) devices are employed, is carried out. The program speed is boosted even at a low program bias owing to the improved CHEI, which is enabled by the inherent sharp band bending of the DSSB at the source side. The DSSB structure provides several benefits, including increased lateral and vertical fields, excellent injection efficiency into the charge storage node, and a drain disturbance-free feature against a conventional device composed of diffused p-n junctions.

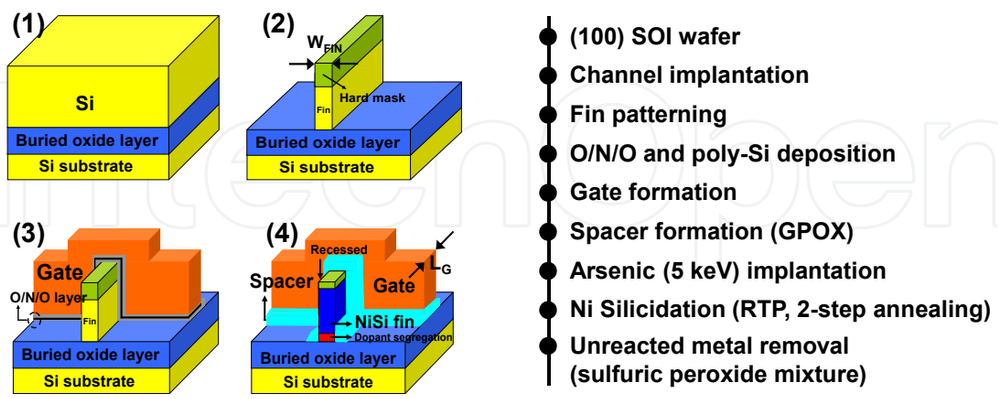


(a) (b)

Fig. 3-1. (a) Scaling trend of drain biases. Minimum bias for programming speed and maximum bias for allowable drain disturbance are drawn for NOR flash generations. (b) Trade-off relations between vertical field and lateral field in the conventional CHEI programming method.

3.1.1 Device fabrication

The process schematics and sequences are summarized in Fig. 3-2. The process flow of the DSSB FinFET SONOS device is the same as that of the conventional FinFET except for the formation of gate spacers and the silicided S/D junctions. Using a shallow implantation of arsenic (As) after the formation of gate spacers, the SB height is effectively modulated by using segregated dopants. During the formation of the gate spacers, the S/D regions are recessed so that they subsequently provide a uniform S/D along the fin depth (vertical direction). This task is challenging with only S/D implantation and activation. Finally, the DSSB S/D was formed by means of nickel silicidation (NiSi) in a two-step rapid thermal processing (RTP), which can minimize the lateral diffusion of NiSi.



(a) (b)

Fig. 3-2. Flow chart of the DSSB FinFET SONOS device. In the silicidation process, a two-step RTP is used to reduce any overgrowth of NiSi and mitigate lateral diffusion. Since the SB height is effectively modulated by the dopant concentration, a shallow implantation (5 keV) of As was applied.

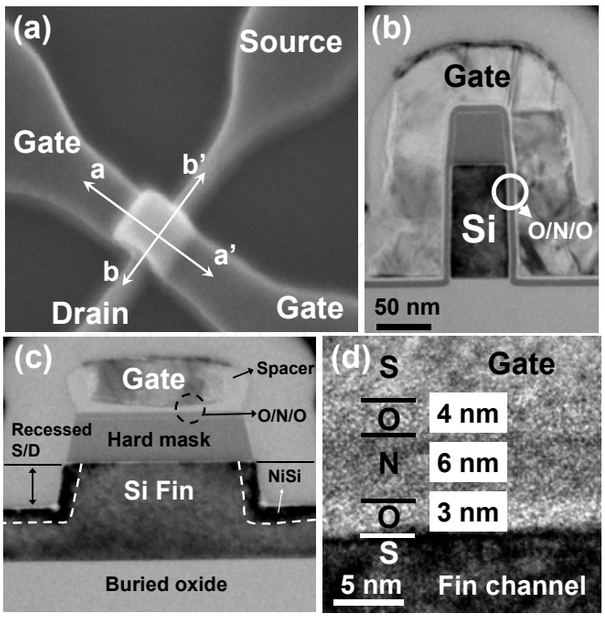


Fig. 3-3. SEM and TEM images of the fabricated devices (Choi et al., 2008).

The SEM photograph in Fig. 3-3(a) shows a bird's-eye view of the fabricated DSSB FinFET SONOS device. Fig. 3-3(b), 3-3(c), and 3-3(d) are cross-sectional TEM images from various points of view of the DSSB FinFET SONOS device. The device has a gate length of 220 nm and a fin that ranges in width from 30nm to 100nm. For the control group, a conventional FinFET SONOS device with a diffused p-n junction was also fabricated. In Fig. 3-4, the results obtained from a scanning TEM image for verification of dopant segregation are shown. Dopant segregation at the interface between the silicon and the silicide is clearly observed.

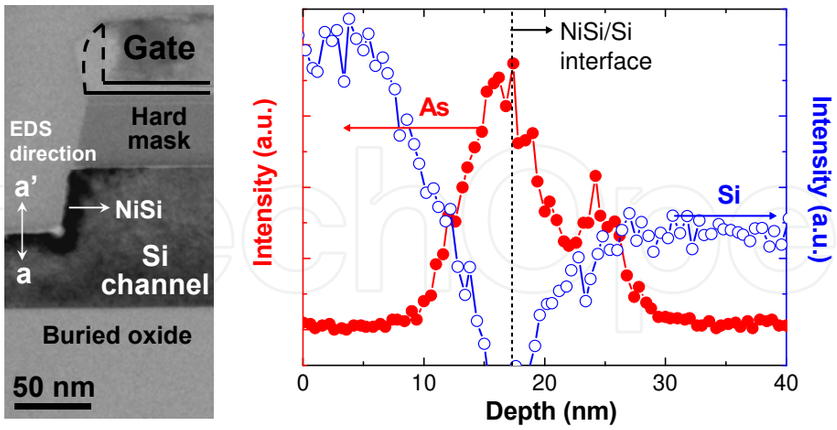
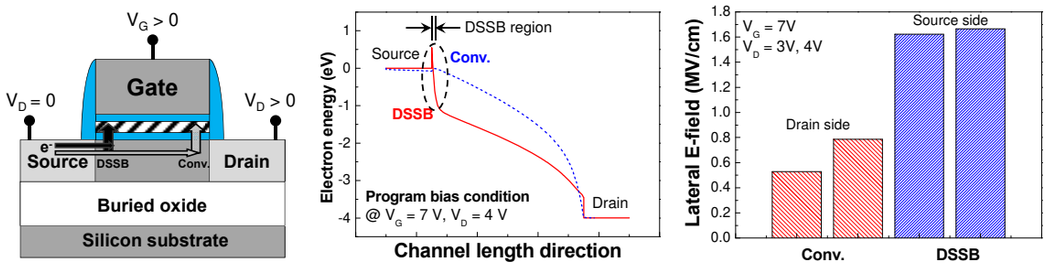


Fig. 3-4. TEM image of DG DSSB SONOS and STEM energy dispersive spectromotry (EDS) analysis. (Choi et al., 2009a)

3.1.2 Memory characteristics

Fig. 3-5(a) schematically illustrates the different injection mechanism of hot electrons for the DSSB Flash memory device and the conventional Flash memory device under the

programming bias condition of CHEI ($V_G > 0$ and $V_D > 0$). In the case of the conventional Flash memory device, hot electrons are generated near the drain-side where the device is under a high lateral electric field; the hot electrons are then injected into the drain-side charge storage node. However, the drain-side region has a low vertical electric field due to the low gate-to-drain potential difference ($V_{GD} = V_G - V_D$). As a result, the injection efficiency is lowered. Moreover, due to high V_D, a Flash memory cell that uses a conventional CHEI method is not suitable for applications with low power operation and high density. In contrast to the conventional device, however, the DSSB device has an abrupt band bending capability near the source-side region, and this capability provides a naturally built-in high lateral electric field that generates sufficient source-side hot electrons, even at a low voltage. In addition, this source-side region experiences a high vertical field due to the high gate-to-source potential difference ($V_{GS} = V_G - V_S$, V_S = grounded). As a result, hot electrons are injected into the source-side storage node rather than the drain-side storage node; consequently, the DSSB device has higher injection efficiency than the conventional device. Fig. 3-5(b) shows a simulated energy band diagram for both cases at the programming state. The magnitude of the simulated lateral electric field in a programming state is also shown in Fig. 3-5(c) for different drain voltages. Note that the DSSB FinFET SONOS device has a larger lateral electric field than the conventional FinFET SONOS device under the same programming conditions. This is mainly attributed to the intrinsic sharp band bending of the DSSB junction at the source-side, which is marked by dashed circle in Fig. 3-5(b).

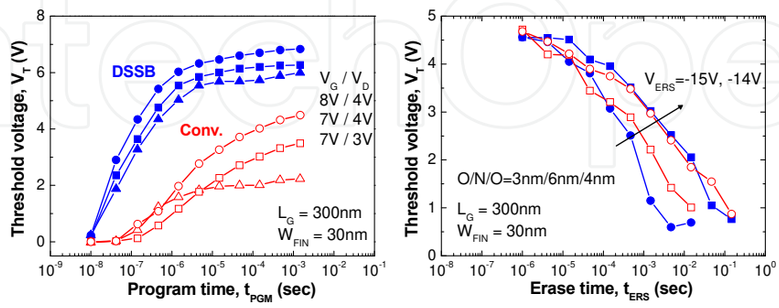


(a) (b) (c)

Fig. 3-5. (a) Comparison of the DSSB device and the conventional device in terms of the charge injection point of hot electrons. (b) Simulated energy band diagrams of both devices at the programming state. The sharp energy band bending should be noted. (c) Simulated lateral electric field for the DSSB device at the source-side and the conventional device at the drain-side. (Choi et al., 2009a)

Fig. 3-6 illustrates the measured programming and erasing transient characteristics. A comparative study was performed with a conventional FinFET SONOS device with the diffused p-n junction as a reference. Under program conditions of $V_G = 7$ V and $V_D = 4$ V with $t_{PGM} = 350$ ns, a V_T shift of approximately 4.5 V is observed in the DSSB FinFET SONOS device. The DSSB FinFET SONOS device and a conventional FinFET SONOS device for programming show a difference of roughly 3.5 V in the V_T shift value at a programming time of 350 ns. This difference is attributed to the high lateral and vertical electric fields at the source-side, which would originate from the sharp band bending caused by the dopant segregated region as well as the intrinsic band profile. In the programming state, electrons injected from the source electrode via thermionic emission or a tunneling process are accelerated by the high lateral electric field and can become hot at the source-side. The

electrons can subsequently surmount the tunnel oxide barrier around the source-side. As a result, the programming is more efficient. On the other hand, in the erasing state created by FN tunneling, there is no significant difference between the DSSB FinFET SONOS device and the conventional FinFET SONOS device. However, it can be straightforwardly expected that the erasing characteristics can be enhanced by engineering of the gate stack, such as metal-gate (with high workfunction) or bandgap.



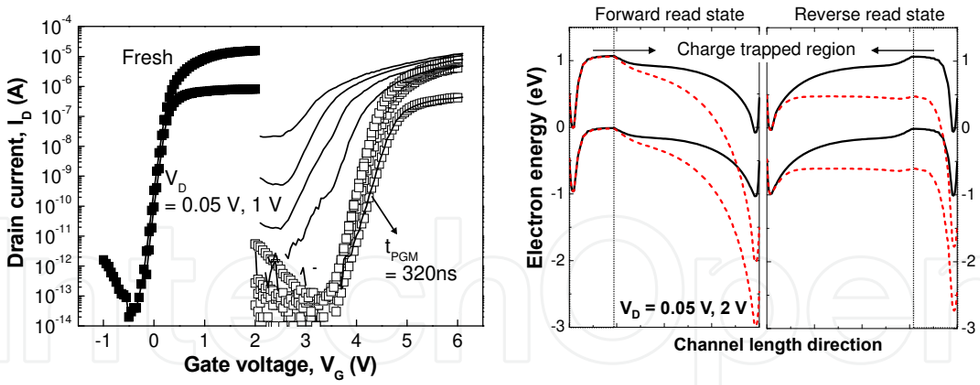
(a) (b)

Fig. 3-6. (a) Program and (b) erase characteristics for DG DSSB and DG conventional SONOS devices (Choi et al., 2009a)

To trace the position of the injected charges experimentally, the transfer characteristics were analyzed after CHEI programming, and the results are shown in Fig. 3-7(a). The observations confirm that hot electrons preferentially inject into the source-side in the DSSB FinFET SONOS device. The behavior of the DSSB FinFET SONOS device is exactly opposite to that of the conventional FinFET SONOS device. After the CHEI programming, the surface potential of the DSSB FinFET SONOS device is more sensitive to V_D in the reverse state than in the forward state because of the source-side injection of hot electrons. Even though the V_T shift as well as the degradation of the subthreshold swing (SS) caused by captured hot electrons at the drain-side is shown in the forward read state (t_{PGM} = 320 ns), the amount of captured electrons at the drain-side is much smaller than at the source-side. As a result, the V_T shift as well as the degradation of SS is not shown in high drain bias of the forward read state. Furthermore, Fig. 3-7(a) shows increased off-state current in relation to V_D during the reverse read operation. As shown in Fig. 3-7(b), the simulated energy band diagrams of the forward and reverse read operation are plotted to explain the V_T shift and the changed off-state current with varying V_D voltage in Fig. 3-7(a). The off-state current in the Schottky-barrier (SB) MOSFET is known to originate from hole tunneling because of the narrowed tunneling width at the drain-side. In a reverse read operation (*i.e.*, the charge trapped region is at the drain-side and read voltage is applied to the drain), the trapped charge can narrow the tunneling width of the drain-side in the off-state. As a result, the off-state current is more sensitive to V_D in the reverse read state than in the forward read state; it also increases in relation to the increment of V_D.

The retention characteristics of the DSSB FinFET SONOS device at various 1k post-cycled programmed states are illustrated in Fig. 3-8. The characteristics are measured at room temperature. The V_T window at t_{PGM} = 1 ms is expected to have a value exceeding 4 V after 10 years.

The drain disturbance of a programmed cell with a relatively high program bias (V_D = 5 V) was also characterized. In Fig. 3-9, the memory architecture in NOR Flash memory is



(a) (b)

Fig. 3-7. (a) The I_D-V_G characteristics as a parameter of V_D at the fresh and programmed states in forward and reverse read operations. (b) The simulated energy band diagram of the forward and reverse read state at the off-state. The trapped charges can narrow the tunneling width of the drain-side in the off-state. (Choi et al., 2009b)

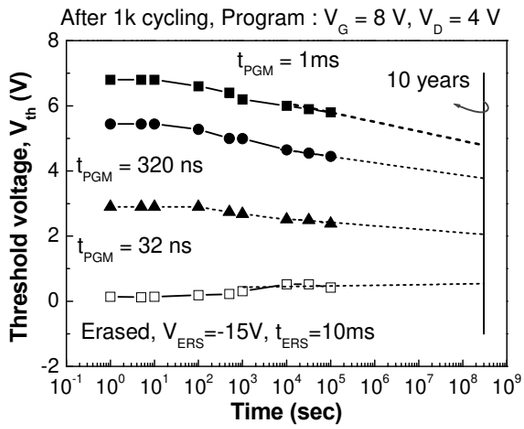


Fig. 3-8. Retention characteristics of a DG DSSB device for MLC in NOR Flash memory operation. (Choi et al., 2009a)

illustrated and the low drain disturbance in DSSB devices is conceptually explained. For the case of cell A (programmed cell), electrons are captured at the source side rather than the drain side. On the other hand, in the case of a conventional device (cell B), trapped electrons at the drain side increase the potential for hot holes to be generated, which results in a drain disturbance (*i.e.*, soft erase). Therefore, improved immunity against drain disturbances is achieved in the DSSB NOR Flash device, as shown in Fig. 3-10. This is primarily due to the trapped electrons located at the source side, as they inhibit hot holes from being injected into the trapped regions.

3.2 Fowler-Nordheim tunneling program in double-gate DSSB MOSFETs

One of the advantages of SONOS type Flash memory devices is natural immunity to floating-gate coupling issues, thereby allowing downscaling to the nano-regime. SONOS-type devices can operate with very few electrons without displaying erratic behavior.

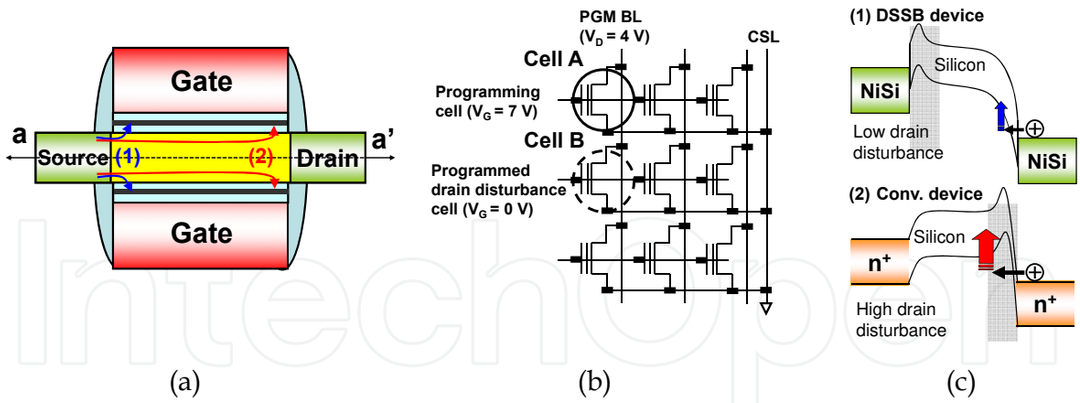


Fig. 3-9. (a) Schematic of the DG DSSB FinFET SONOS device. (b) Architecture of NOR Flash memory. (c) Conceptually illustrated energy band diagrams at the programmed state for the DSSB and the conventional device. (Choi et al., 2009a)

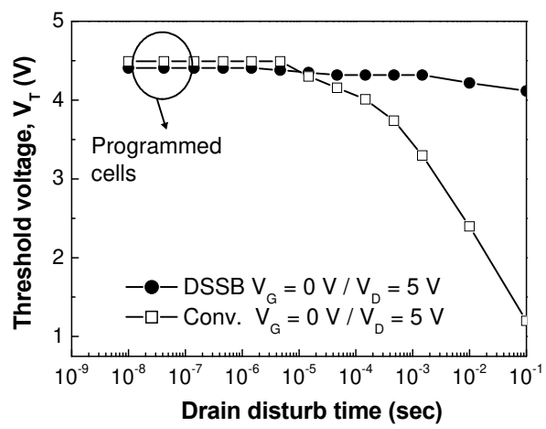


Fig. 3-10. Drain disturbances of DG DSSB and DG conventional devices: Compared to the conventional device, high immunity to drain disturbance is achieved in the DG DSSB device. (Choi et al., 2009a)

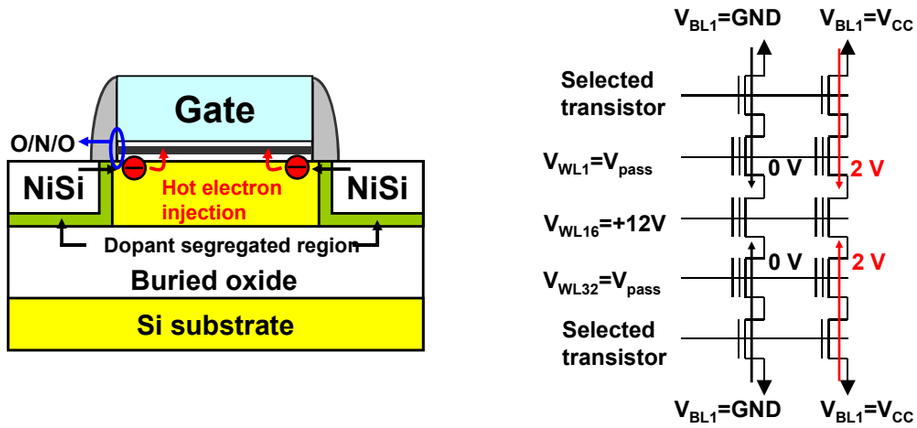
However, their programming time is excessively long, falling in a range of 10^{-6} ~ 10^{-3} sec due to the Fowler-Nordheim (FN) tunneling mechanism in conventional NAND Flash memory. This makes it difficult for applications requiring high-speed application such as solid-state drive (SSD). In addition, the conventional diffused S/D with deep junctions obstructs further aggressive scaling in the SONOS type memory devices.

Current research on NAND Flash memory is mainly focusing on a 3-D stacking structure realized by deposition of a poly-Si channel. In addition, a junction-free structure, *i.e.*, S/D junctions are not formed, is indispensable, as the formation of S/D junctions is quite difficult due to vertical stacked 3-D Flash memory (Lue et al., 2008). However, this structure cannot be directly applicable to Flash memory with poly-Si channel because of high resistance at the S/D junctions, as aforementioned. Therefore, another method to form S/D junctions is needed. In this section, a novel NAND Flash architecture implemented in the same double-gate DSSB FinFETs SONOS is demonstrated. Fast programming is achieved due to the electrons with extra kinetic energy, *i.e.*, hot carriers, on the dopant segregated

S/D side. These hot electrons require neither high programming voltage nor long programming time. With the same ground voltage on the S/D junction, hot electrons triggered by sharp energy band bending at the edge of silicided S/D junctions are naturally generated.

3.2.1 Memory characteristics

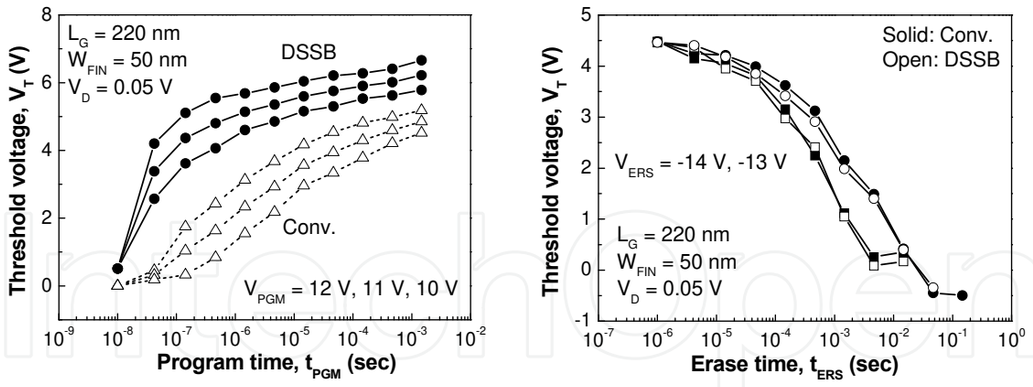
Fig. 3-11(a) explains the operating principle at the programming state. Fast programming is achievable by applying the same ground voltage on both S/D junctions simultaneously (Fig. 3-11(b)). In this case, a locally high lateral of electric field is generated by a sharpened band structure at the dopant-segregated region. Thus, electrons thermally injected or tunneled from S/D edges, *i.e.*, with extra kinetic energy, are energized by this high electric field and are mainly used to program the NAND Flash device. Therefore, fast programming with low voltage is feasible with enhanced tunneling probability. Note that most of trapped electrons in short programming time can be located at the edge of S/D junctions.



(a) (b)

Fig. 3-11. (a) Schematic of the operating principle of the DSSB FinFET SONOS. (b) The hot electrons energized by the DSSB are used to program for a NAND Flash application by applying the ground voltage on the S/D junctions. (Choi et al., 2009c)

Figs. 3-12(a) and 3-12(b) illustrate the programming and erasing transient characteristics, respectively. As a reference, a conventional FinFET SONOS with a diffused p-n junction is compared. The results demonstrate the excellent program efficiency of the DSSB FinFET SONOS. The program conditions V_{PGM} = 12 V with t_{PGM} = 100 ns exhibit a V_T shift of 4.5 V in the DSSB FinFET SONOS. It should be noted that a significant V_T shift for programming was achieved within a few tens of nanoseconds, which is approximately 1000 times faster than the conventional device. The difference in the V_T shift between the DSSB FinFET SONOS and a conventional FinFET SONOS for programming was approximately 3 V at 100 ns programming time. This difference is attributed to hot carrier injection energized by sharp band bending at the dopant segregated S/D junction edge. These outstanding results are among the best results in terms of V_T window and programming/erasing speed reported to date for FinFET structure flash memory devices. However, there is no significant difference in the erase characteristics of the DSSB FinFET SONOS as compared with a conventional FinFET SONOS because electron de-trapping from the nitride to the silicon substrate is not different between them.



(a) (b)

Fig. 3-12. Program (a) and erase (b) transient characteristics with various program voltages. Excellent program efficiency compared to the control group is achieved due to hot electrons energized by sharp band bending at the S/D. (Choi et al., 2009c)

The tunneling oxide of conventional devices may be non-uniform due to the non-uniform etching profile of the narrow silicon channel; therefore the tunneling probability of electrons at the channel fluctuates significantly in conventional devices. However, for the case of DSSB devices, the trapped electrons are mainly located at the edges of the S/D junction. Therefore, a more parallel V_T shift can be achieved in the DSSB device. As shown in Fig. 3-13, a parallel shift among programmed states was found in the DSSB device but not in the conventional device. This implies that two-sided charge injection at the S/D prevails in the DSSB FinFET SONOS device. Note, on the other hand, that an unwanted non-uniform charge injection by FN tunneling occurs in the conventional FinFET SONOS device, resulting in an oblique shift and degradation of the slope.

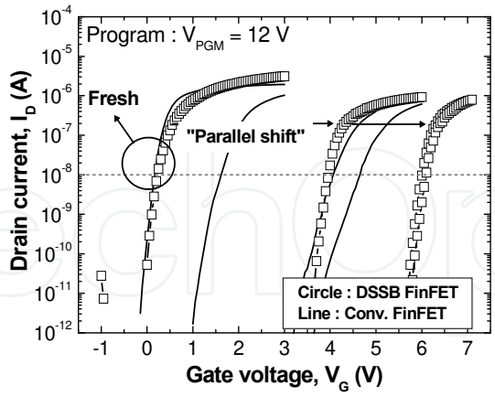
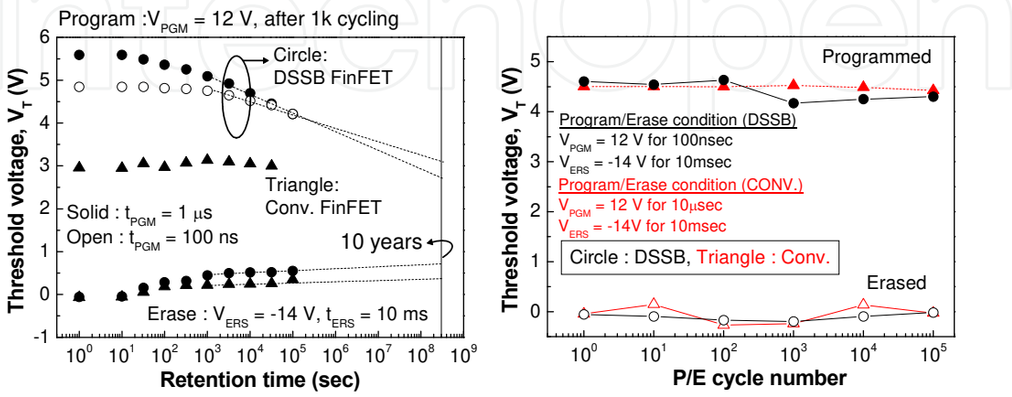


Fig. 3-13. Comparison of the I_D-V_G shift among various programmed states. A two-sided injected charge produces a parallel shift of I-V. (Choi et al., 2008)

The retention characteristics after 1k cycling and P/E cycling endurance of the DSSB FinFET SONOS were compared to the control group, a conventional FinFET SONOS, and the results are presented in Figs. 3-14 (a) and 3-14(b), respectively. These characteristics were measured at room temperature. Fig. 3-14(a) shows that a rapid degradation of the retention characteristics was monitored during longer programming time. Under this condition the

stored charges are more likely to be lost due to larger damage by hot carriers, degrading the tunneling oxide quality. Nevertheless, the V_T margin of the DSSB FinFET SONOS after ten years is larger than that of the conventional device. This is attributed to the high efficiency of programming originating from the sharpened energy band bending by the DSSB structure. P/E endurance characteristics are also plotted in Fig. 3-14(b). After 10^5 P/E cycles, only a negligible V_T shift can be seen, thus verifying that the reliability characteristics are satisfactory.



(a) (b)

Fig. 3-14. (a) Post cycling retention comparison of the DSSB FinFET SONOS and a conventional FinFET SONOS. Due to damage of hot electrons, the charge loss of the DSSB FinFET SONOS is larger than that of the conventional device. (b) Measured endurance characteristics of the DSSB FinFET SONOS and the conventional device. A negligible V_T shift is observed in the P/E states. (Choi et al., 2009c)

4. Junctionless MOSFETs

Flash memory has recently scaled rapidly down to a 20 ~ 30 nm node. However, with researchers relying on conventional approaches, critical scaling limits are being faced, foreshadowing the possibility that further downscaling will eventually be impossible. Hence, a new and innovative device structure is urgently required. Most importantly, among the crucial limitations, the short-channel effects (SCEs) have increasingly become unavoidable technical challenges, as it is difficult to scale the equivalent oxide thickness (EOT) below 10 nm due to the nature of multi-layered gate dielectrics. Shallow junctions are very important to suppress the SCEs; however, it is difficult to precisely control the junction depth and profile. Moreover, the formation of such shallow junctions becomes a serious concern with 3-dimensional (3D) multi-stacking integration due to the large thermal budget required. For this reason, a "junction-free transistor" based on junction-free virtual S/D for NAND Flash memory was previously reported, and the concept was applied to other types of 3D integrated Flash memory such as Bit Cost Scalable (BiCS) memory (Tanaka et al., 2007), Vertical-Stacked-Array-Transistor (VSAT) memory (Kim et al., 2009), and Terabit Cell Array Transistor (TCAT) memory (Jang et al., 2009), among others (Hubert et al., 2009). However, it can be expected that current flowing through a string of NAND Flash memory will be significantly degraded by pre-existing high resistance regions, *i.e.*, undoped source/drain (S/D) regions, despite that these regions can be transformed into low

resistance regions via an inversion process by fringing the field from the gate. This can therefore lead to severe back-pattern dependency or result in the failure of read operations. These challenging issues tend to be more severe in 3-D multi-stacked Flash memory where poly-crystalline silicon (poly-Si) is used as a channel (Walker et al., 2009).

Recently, a nanowire transistor known as a "junctionless transistor" or a "gated resistor" was introduced (Colinge et al., 2010). It consists of n^+ (or p^+ for a p-channel device) homogenously doped silicon nanowire (SiNW), *i.e.*, an n^+ source - n^+ channel - n^+ drain (or a p^+ source - p^+ channel - p^+ drain) for the p-channel device, with a gate electrode. Junctionless transistors have several advantages compared to traditional inversion-mode transistors: (i) they are easily fabricated; (ii) they are free from S/D junctions therefore have less dopant fluctuation; (iii) they can reduce SCEs; (iv) they can reduce mobility degradation by surface roughness scattering; and (iv) they relax the stringent requirements reducing the gate dielectric thickness. These intrinsic strengths make the concept proposed here attractive for application of a junctionless transistor to Flash memory. However, existing junctionless transistors have an inherent limitation in that they primarily implemented on a SOI wafer.

In this section, an all-around-gate (AAG) junctionless transistor is applied to oxide-nitride-oxide (O/N/O) type charge-trapping Flash memory. By utilizing a deep reactive ion etching (RIE) system (Ng et al., 2009), a junctionless transistor with a suspended SiNW channel with a width of 4 nm (W_{NW} = 4 nm) and a length of 20 nm (L_G = 20 nm) is fabricated, where the channel is completely separated from the bulk substrate. The performance is comparable to that of currently reported Flash memory, but it can be scaled down further, below the 20 nm node, due to the simplified process and the advantages inherited from the junctionless transistor.

4.1 Operating principle of junctionless MOSFETs

The operational principle of an n-type junctionless MOSFET is different from that of a standard n-type conventional MOSFET. In the subthreshold region, shown in Fig. 4-1(a), the highly doped channel is fully depleted, and hence it can hold a large electric field. By increasing the gate voltage, the electric field in the channel reduces until a neutral region is created in the center of the channel. At this point, it is possible to define the threshold voltage, because bulk current starts to flow through the center of the channel, as illustrated in Fig. 4-1(b). Then, by further increasing the gate voltage, the depletion width reduces until a completely neutral channel is created, as seen in Fig. 4-1(c). This occurs when the gate voltage equals the flat band voltage. At the onset of this condition, the bulk current reaches its maximum value. Thereafter, by increasing the gate voltage further, negative charges accumulate on the surfaces of the channel, as shown in Fig. 4-1(d). These charges result in surface current, which is similar to the current in a standard n-type conventional MOSFET.

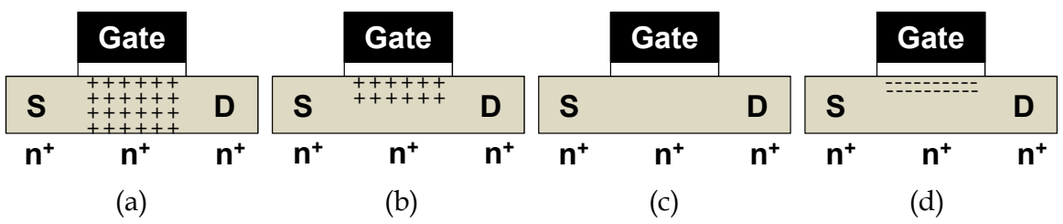
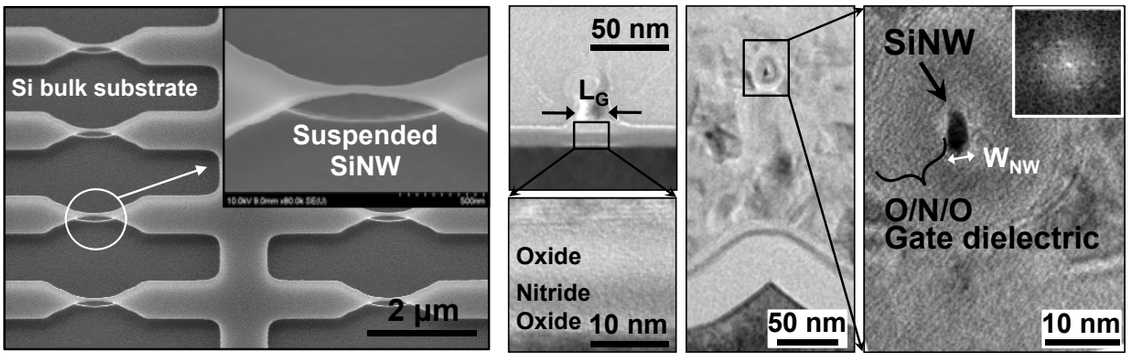


Fig. 4-1. (a) Fully depleted channel in subthreshold mode, (b) semi-depleted channel in bulk current mode, (c) flat band mode, and (d) accumulation mode.

4.2 Device fabrication

A (100) bulk silicon wafer is used as a starting material. First, the top of a silicon bulk wafer is uniformly doped by ion implantation with arsenic for the n-channel devices. The implant energies and doses are chosen to yield uniform doping of 2×10^{19} /cm^3. High doping is required in the junctionless transistor to ensure a high driving current and good source/drain contact resistance. After patterning the active region with W_{NW} = 30 nm, the Bosch process enabled by the RIE system is employed to form the suspended SiNW separated from the bulk substrate. The suspended SiNW via the Bosch process is achieved by balancing anisotropic etching and passivation steps. Details of the Bosch process can be found in the literature (Ng et al., 2009). The scanning electron microscopy (SEM) images in Fig. 4-2 clearly show the suspended SiNWs. The gap distance between the SiNW and bulk substrate is approximately 250 nm. After the formation of the SiNWs, channel stop implantation with boron ions is applied. Subsequently, two iterations of sacrificial oxidation are employed for further reduction of the width (W_{NW} = 4 nm) of the SiNW and to make the channel smooth, followed by the formation of shallow trench isolation (STI). Next, an O/N/O layer with a thickness of 2.8nm/6.2nm/7nm (using a thermal oxide and LP-CVD nitride/TEOS oxide) and an in-situ n^+ poly-Si gate (using LP-CVD poly-Si) are formed sequentially. Afterwards, a gate length (L_G) of 20 nm is patterned. Horizontal and vertical transmission electron microscopy (TEM) images of the fabricated junctionless transistor are also shown in Fig. 4-2.



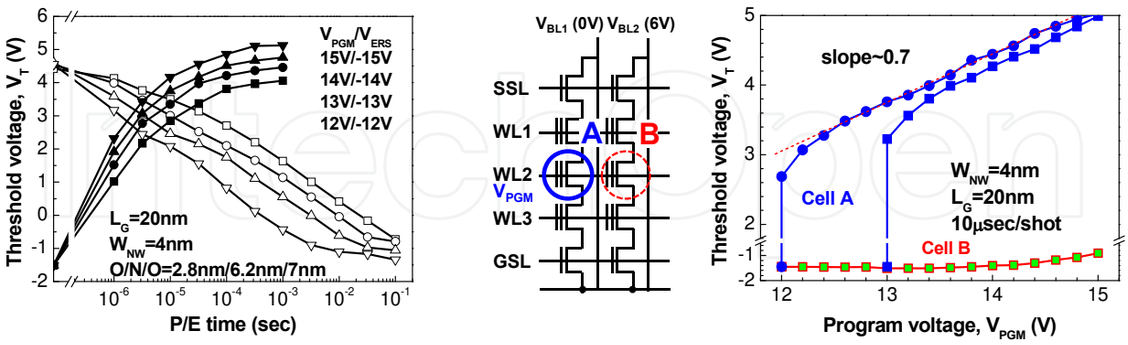
(a) (b)

Fig. 4-2. (a) SEM image and magnified views of the suspended SiNW on the bulk substrate and (b) Horizontal and vertical TEM images in the L_G direction in the AAG junctionless transistor with the O/N/O gate dielectric. The width (W_{NW}) and length (L_G) of the SiNW channel are approximately 4 nm and 20 nm, respectively. The thickness of the O/N/O layers for the charge storage node is 2.8nm/6.2nm/7nm. (Choi et al., 2011)

4.3 Memory characteristics

Fig. 4-3(a) shows the P/E transient characteristics of junctionless AAG SONOS devices with a 20 nm L_G and a 4 nm W_{NW} for various P/E conditions. A large P/E window (ΔV_T) up to 6.5 V was attained with the aid of a GAA structure despite the highly scaled device size, demonstrating the cell suitability for MLC operations. No erase saturation phenomenon was observed, even at -15V, despite the n^+ poly-Si gate. This indicates that there is no need to use a metal-gate or high-k blocking oxide. Moreover, as seen in Fig. 4-3(b), program inhibition is

achieved by direct raising of the unselected bit-line potential. It is implicit that there is no need to introduce a complex self-boosting method. A high incremental step pulse program (ISPP) slope (0.7) is also attained, even with a L_G value of 20 nm.



(a) (b) (c)

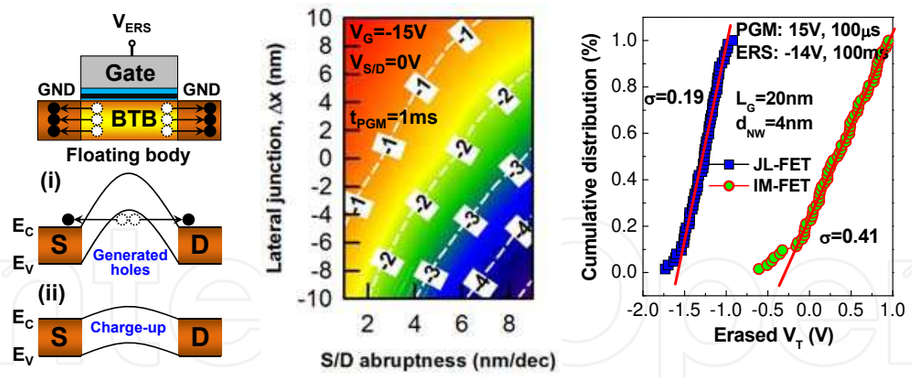
Fig. 4-3. (a) Program and erase transient characteristics of the junctionless AAG SONOS device. (b) ISPP programming and related inhibit method. Program inhibition is achieved by directly raising the unselected bit-line potential. For a programmed cell, a higher incremental step pulse program (ISPP) slope is also attained, even at 20nm L_G. (Choi et al., 2011)

3D NAND structures with a floating body require careful consideration when designing S/D junctions for enhanced erase characteristics. To fix the floating body potential during erase operations effectively, a sufficient number of holes must be generated by band-to-band tunneling from the S/D junctions. Therefore, the S/D junctions need to be heavily doped, abrupt, and uniform. Unless 3D NAND structures satisfy the aforementioned demands, uniform and efficient erase characteristics cannot be ensured in conventional diffused S/D and junction-free virtual S/D structures (Figs. 4-3(a) and 4-3(b)). Fig. 4-3(c) compares the distribution of the erased V_T for the junctionless and inversion-mode AAG SONOS devices. Contrary to the inversion-mode devices, the S/D of junctionless devices is precisely controlled by the gate electric field. As a result, a uniformly distributed erased V_T is successfully obtained without any V_T correction methods.

Because the conduction of a junctionless device initially occurs in the center of an n^+-doped SiNW channel, the device can be less sensitive to the interface trap generated from P/E cycles compared to a conventional inversion-mode device, as shown in Fig. 4-4. In a TCAD simulation, it is confirmed that the acceptor-type interface trap does not significantly affect the V_T shift in a junctionless device. Note that the higher the doping concentration of a SiNW channel is, the stronger the P/E endurance becomes. Moreover, reasonable post-cyclic data retention characteristics were achieved.

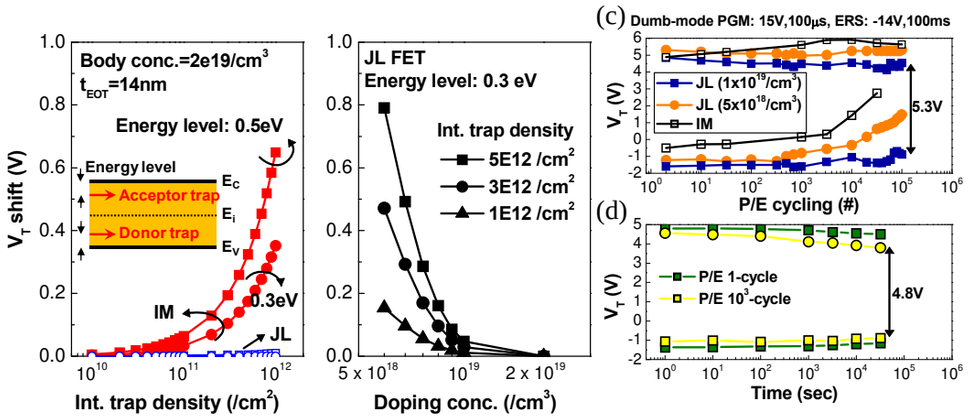
5. Conclusions

In this chapter, as we confront challenges of current Flash memory technology and as the design rule deviates from the historical scaling paradigm, a new type of Flash memory cell based on the structure of dopant-segregated Schottky-barrier (DSSB) MOSFETs, which has an ultra-thin pocket layer with high-dose dopants surrounding the interface between the



(a) (b) (c)

Fig. 4-3. (a) Erase operations for the 3D NAND structure with a floating body: (i) First, the floating body potential follows the gate potential (V_{ERS}). As a result, holes are generated by band-to-band tunneling. (ii) Second, the generated holes can pin the floating body potential. (b) TCAD simulation of the floating body potential during the erase operation. (c) Distribution of erased V_T values for junctionless and inversion-mode AAG SONOS devices. (Choi et al., 2011)



(a) (b)

Fig. 4-4. (a) Simulated V_T shift versus interface trap density (N_{it}) as a parameter of the energy level of both acceptor- and donor-type traps. (b) Simulated V_T shift versus doping concentration of the SiNW channel in the junctionless device. (c) Dumb-mode P/E cycling (without any P/E verify) endurance test. (d) Post-cycling retention characteristics of the junctionless device. (Choi et al., 2011)

metallic silicide material for source/drain (S/D) and the channel, is proposed. The hot carriers intrinsically generated from the shallow DSSB S/D junctions can be utilized for the advancement of both the NAND and the NOR type Flash memory cell. With the aid of hot carriers that can be generated by elevated electric field at the DSSB S/D junctions stemming from the abrupt band bending, the probability to be trapped into a charge storage node of Flash memory, such as polysilicon layer in the floating gate memory device or the nitride layer in the SONOS memory device, is enhanced. Therefore, the DSSB MOSFET shows very fast programming time at low programming voltage, compared to conventional MOSFET

based on p-n S/D junctions. Besides, the superior scalability resulting from the abrupt and shallow junctions can also be achieved without the constraint of the parasitic resistance due to metallic silicided material. Therefore, the DSSB devices can be a premier choice for future nano-electronics applications of the logic and Flash memory device since they do not only enable continuation of device scaling due to the improved electrostatics but also provide benefits for an alternative memory cell.

Moreover, a highly scaled AAG junctionless transistor SONOS memory cell with acceptable P/E behaviors, cycling endurance, and data retention is also demonstrated. The junctionless transistor memory cell inherited the scaling advantages of not only the AAG structure but also the junctionless transistor. Therefore, the junctionless transistor memory cell, together with DSSB MOSFETs, is an excellent candidate for the next-generation 3-D NAND Flash memory.

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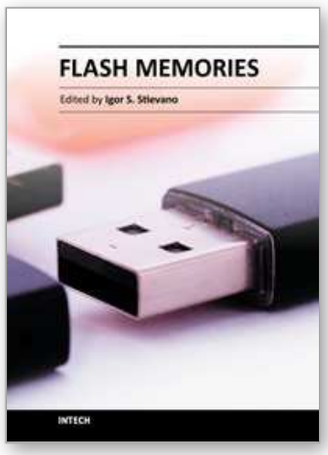
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Flash memories and memory systems are key resources for the development of electronic products implementing converging technologies or exploiting solid-state memory disks. This book illustrates state-of-the-art technologies and research studies on Flash memories. Topics in modeling, design, programming, and materials for memories are covered along with real application examples.

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