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Transmitter Multi-Path Equalization and Receiver Pulse-Injection Locking Synchronization for Impulse Radio Ultra-Wideband Communications

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1. Introduction

Impulse radio systems have received much attention as a possible architecture for UWB transceivers due to the large data bandwidth, low spectral interference with nearby channels, and simplicity of UWB transmitter/receiver architectures using mostly digital implementations. Due to the low emitted power spectral density of -41.3dBm/MHz mandated by the FCC, impulse radio is especially well suited for low-cost, low-power, and short-range wireless communications. This paper presents an IR UWB transceiver for a typical short-range wireless communication application as shown in Fig. 1 within computer

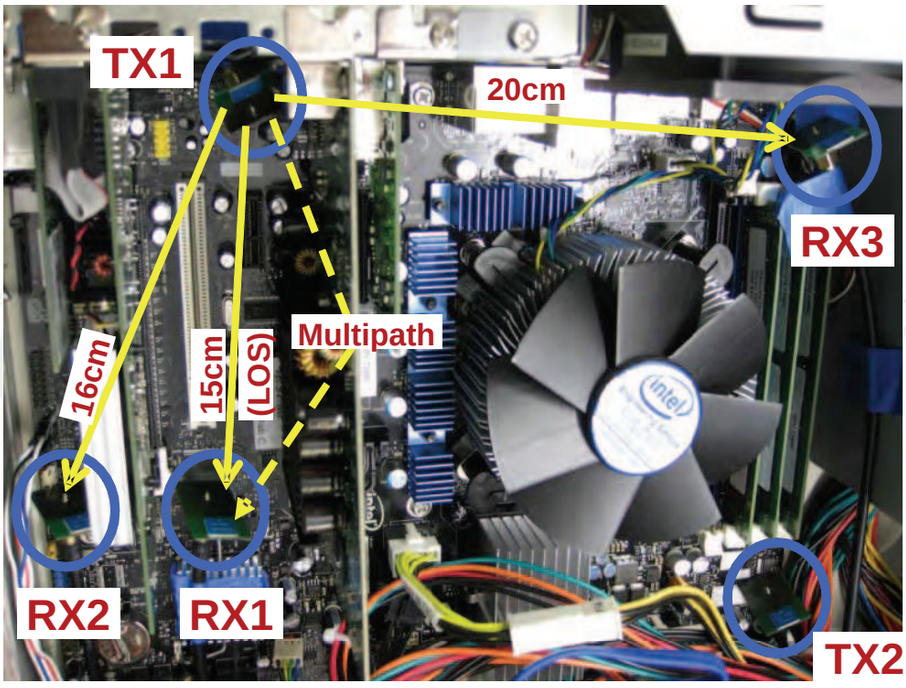


Fig. 1. Inter-chip wireless communication within computer chassis

chassis chip-to-chip wireless interface. However, it is not limited to this; any short-range, high-data-rate wireless communication is applicable.

1.1 Conventional impulse-radio receiver architectures

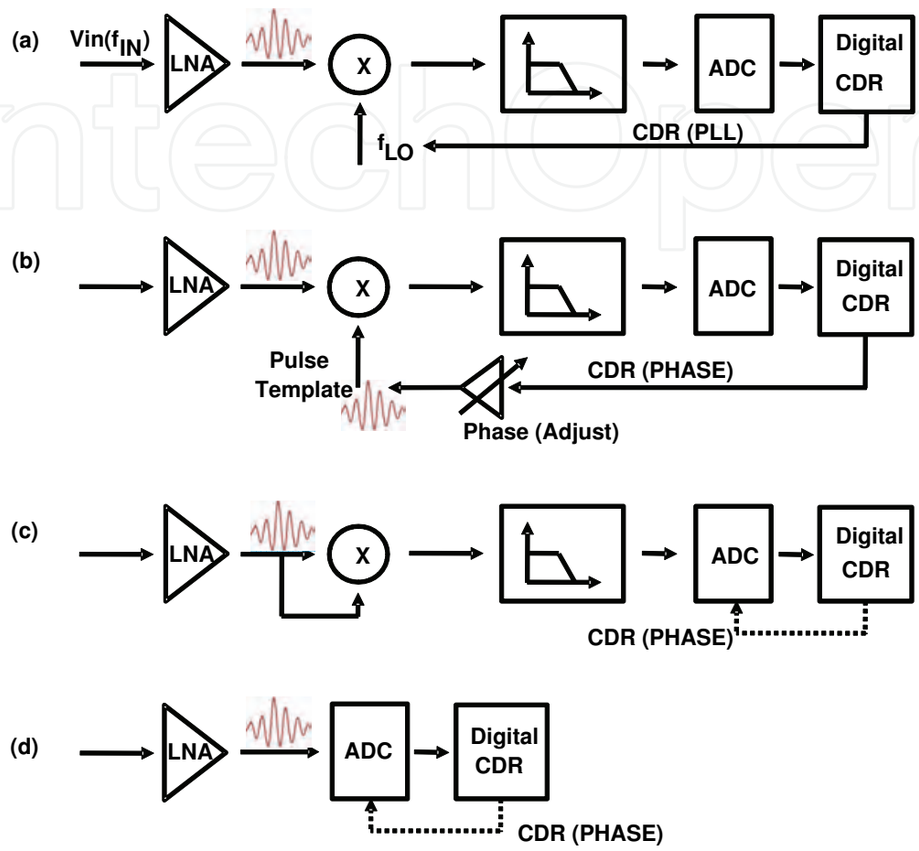


Fig. 2. RX architecture overview

While recent research has demonstrated the energy-efficiency of impulse-based UWB transmitters (Lachartre et al., 2009; Wentzloff & Chandrakasan, 2007), the more critical problem lies within the receiver. Due to the short timing duration of the transmitted impulse, determining the exact arrival of the UWB pulse is extremely difficult, placing most of the system complexity and power burden on to the design of the receiver architecture.
Conventional IR-UWB receiver architectures can be summarized in Fig. 2 above: a) direct-conversion receiver with a local oscillator multiplier/correlator; b) direct-conversion receiver using pulse template multiplier (Zhou et al., 2009); c) non-coherent receiver with self-correlation Lee & Chandrakasan (2007); and d) direct over-sampling analog-digital converter (ADC)O'Donnell & Brodersen (2006). The LO direct-conversion architecture is the most common, and is similar to narrow-band receiver systems. This approach typically consumes the most power due to the clock generation of the high-frequency local oscillator. In addition, due to the large data bandwidth, the low-pass filter is difficult to design, and ADC oversampling is still required to recover the optimal ADC sampling position. In addition, a CDR is still required, as the local receiver clock may be plesiochronous from the transmitter clock. The pulse-template, direct-conversion architecture is commonly used in coherent

IR-UWB RX, but RX phase synchronization is power-consuming and difficult because accurate alignment between TX impulses and RX templates must be achieved. Furthermore, the transmitted impulse from the channel and the antennas may be significantly distorted, increasing the difficulty in generating an accurate pulse template. The non-coherent, self-correlating receiver is an attractive option, as it simplifies the pulse-template generation and synchronization. Unfortunately, bit-error rate will increase as the receiver will not be able to discriminate between noise and transmitted data. In addition, the design of a CDR loop is still required, as the demodulated data needs to be phase-locked with the local receiver clock. The direct over-sampling ADC method is the most straightforward, as the pulse input is directly quantized by the ADC, moving the demodulation and CDR requirements to the digital baseband. Unfortunately, the power overhead for the over-sampling ADC is extremely expensive, as a multi-gigahertz, medium resolution ADC is necessary for the 3.1-10GHz receiver bandwidth.
One overarching constraint of all of these conventional structures is that some mechanism for synchronizing the receiver sampling clock with the incoming transmitted data is required. Because the eventual goal for IR-UWB systems is several hundred Mbps, the design of an over-sampling CDR loop adds both system complexity as well as additional power consumptionZheng et al. (2006).

1.2 Proposed architecture: Receiver pulse injection-locking phase synchronization

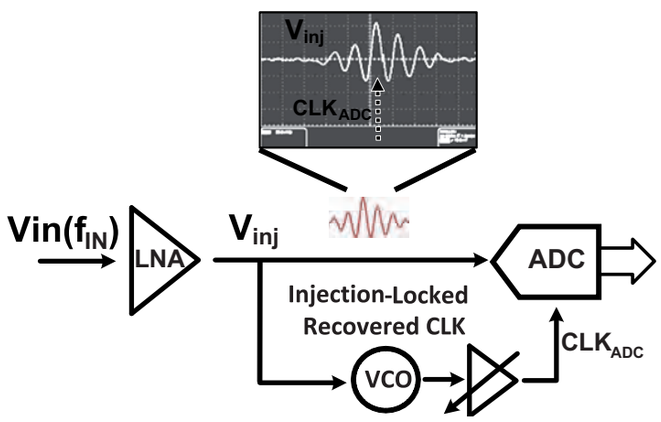


Fig. 3. RX_IL_VCO

In this work, we present a new receiver phase synchronization method using pulse injection-lockingHu et al. (2010), as shown in Fig. 3. This technique provides several advantages over the previously described architectures. First, no CDR is necessary, as the received local oscillator is injection-locked to the incoming pulses and hence is automatically phase-aligned with the transmitted clock. Second, the architecture is inherently a feed-forward system, with no issues with feedback loop stability as seen in phase-locked loops. The proposed system is similar to a "forwarded clock" receiver approach used for high-speed links which have been shown to be extremely energy-efficientHu, Jiang, Wang, O'Mahony & Chiang (2009). The difference here is that the receiver sampling clock is locked to the actual incoming transmitted pulses, eliminating any requirement for a separate clock channel. Third, since the receiver clock is now injection-locked and synchronized with the transmitter, the ADC sampling requirements can be severely relaxed and can now run at the actual data rate. This is a significant advantage for power reduction, as a multi-gigahertz, over-sampling ADC is no longer necessary.

2. System analysis and operation principle

2.1 Transmission power and pulse shaping

For the 3.1-10.6GHz UWB band, the FCC limits the maximum transmitting power spectrum mask to -41.3dBm/MHz. Therefore, the maximum allowable transmitted power within 3-5GHz is -8.3dBm, but no such a pulse can meet the FCC mask in practice, assuming a filling coefficient of k ($0 < k < 1$), or spectral efficiencyWentzloff (2007). The filling coefficient (spectral efficiency) k of a pulse is the loss incurred from incomplete filling of the -10dB channel bandwidth, calculated by:

$$k = \frac{E_{ch}}{P_{EIRP} BW_{-10dB}} \tag{1}$$

where Ech is the pulse energy within the -10dB channel bandwidth, PEIRP is the maximum average power spectral density, and BW-10dB is the -10dB bandwidth.

Due to this filling coefficient, the maximum transmission power will be much smaller. To improve this filling coefficient, many techniques for baseband pulse shaping have been investigated since the release of the UWB FCC mask *First Report and Order* (n.d.). For example, a gaussian pulse is theoretically the ideal pulse shaping technique, but it is difficult to implement Wentzloff & Chandrakasan (2007); Zheng et al. (2006).

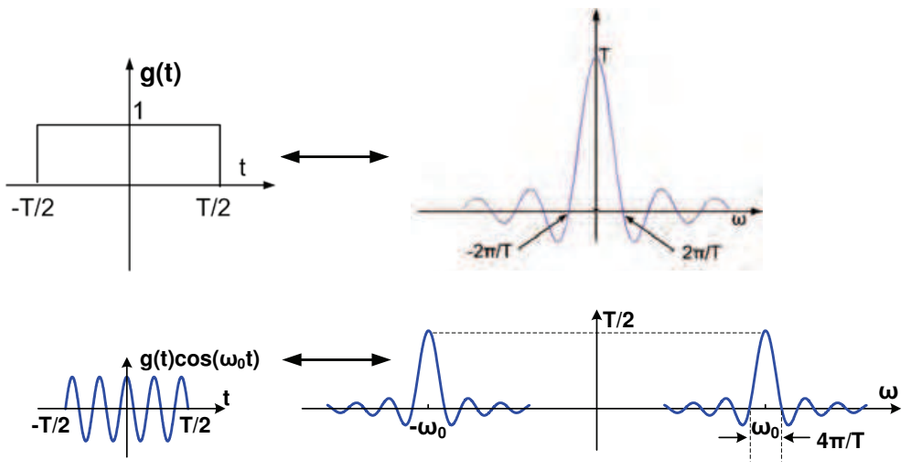


Fig. 4. Rectangular baseband and sine-wave modulated pulses in time and frequency domain

Fig. 4Lathi (n.d.) shows the Fourier transform of a baseband rectangle pulse and a rectangle pulse modulated by a sine wave. Notice that the spectral bandwidth is inversely proportional to the pulse width, where for a rectangle pulse of T(s) pulse width, its frequency bandwidth is 2/T(Hz). For the 3-5GHz UWB band, the maximum bandwidth is 2GHz when the carrier frequency is 4GHz, with a minimum pulse width W_{pulse} of 1ns. Assuming a 1ns pulse width, the pulse amplitude will depend on the pulse repetition frequency (PRF or data rate), limited by the maximum allowed transmission power. For data rates of 500Mbps, 250Mbps, and 125Mbps, with equal probability of "1" and "0" symbols, a filling coefficient of k=0.5, and a 50ohm antenna load, the corresponding pulse amplitudes required will be 172mV, 243mV, and 344mV, as derived from Equation 2:

$$V_p = \sqrt{\frac{2R \cdot P}{0.5 \cdot DR \cdot W_{pulse}}} = \sqrt{\frac{200 \cdot k \cdot P_{max}}{DR \cdot W_{pulse}}} \tag{2}$$

2.2 Modulation scheme

Several modulation schemes have been used for IR-UWB transceivers, such as binary-phase shift keying (BPSK)Zheng et al. (2006), pulse-position modulation (PPM)Wentzloff & Chandrakasan (2007), and on-off keying (OOK)Lachartre et al. (2009). To recover the clock phase information from the data using pulse injection locking, OOK is chosen for this transceiver due to simplicity, although PPM and amplitude modulation (AM) would also work. Note that to maintain a sufficient number of transmitted impulses necessary to insure receiver phase locking, DC balancing and maximum run length limiting are required for the proposed system, such as 8b/10b encoding.

2.3 Path loss

Ideal free space (FS) propagation (no multipath reflections) exhibits a path loss that is proportional to the square (α=2) of the separation distance "d", with λ the wavelength*UWB Channel Modeling Contribution from CEA-LETI and STMicroelectronics* (n.d.):

$$PL_{dB}(d) = \alpha \cdot 10\log_{10}(\frac{4\pi d}{\lambda}) = \alpha \cdot 10\log_{10}(d) + c \tag{3}$$

where α is the path loss exponent and c is a power scaling constant obtained after channel calibration. $Frris's$ formula suggests that for a propagation distance of 1m, the path loss equals to 44.5 dB at a 4GHz center frequency; a 25cm distance exhibits a path loss of 32.5dB, assuming antenna gains of 0dBi for both the transmitter and receiver.

2.4 Link budget

For a targeted bit error rate(BER) of 10^{-3}, coherent OOK modulation requires E_b/N_0 of 9dB.

$$SNR = \log_{10}(E_b/N_0 \cdot DR/B) \tag{4}$$

where DR is the data rate, and B is the signal bandwidth.
For a 500Mbps data rate, after converting E_b/N_0 to SNR using Equation(4), 9dB E_b/N_0 is equivalent to an SNR of 3dB, and 0dB SNR is required for 250Mbps.
Assuming a 3-5GHz UWB spectral mask filling coefficient of k=0.5 or -3dB, 44.5dB line-of-sight (LOS) loss at 4GHz, and data rate 500Mbps, the link budget is estimated as follows:

$$SNR = P_{TX} - PL - N_{channel} - NF - I \tag{5}$$

$$N_{channel} = -174dBm/Hz + \log_{10}(B) = -81dBm \tag{6}$$

$$\begin{aligned} NF + I &= -11.3dBm - 44.5dB + 81dBm - 3dB \\ &= 17.2dB \end{aligned} \tag{7}$$

Therefore, a 17.2dB noise figure NF(including implementation loss I) is sufficient for a communication data rate of 500Mbps, assuming a raw BER of 10^{-3} through a distance of 1mVan Helleputte & Gielen (2009). Note that the calculation above is an estimation, as many other factors, such as receiver clock jitter, are not considered.

2.5 Synchronization

RX phase synchronization with the incoming TX impulses is a critical issue in conventional coherent transceiversVan Helleputte & Gielen (2009). Initially, the receiver has no information

about when the transmitted pulses are arriving. Therefore, for the receiver to synchronize with the incoming impulses, conventional systems undergo two modes of operation: data acquisition and data reception. During data acquisition, a known header is transmitted. The receiver synchronizer scans all the possible window positions for this header and measures the received signal energy in each window. These correlation algorithms run in the digital back-end, which control the analog-front-end (AFE). Once the proper window is found, the receiver is locked to the transmitter and is then switched to data reception mode.
Unfortunately, practical conventional IR-UWB transceivers exhibit a frequency offset drift between transmitter and receiver. This small offset will result in a slow but gradually increasing phase difference between the received pulse and receiver pulse template window. As a result, the received impulse will move out of the receiver pulse template window, such that receiver must switch to data acquisition mode again, consequently reducing the data rate and increasing BER. One possible solution is implementing a matched filter receiver within a control loop that locks to the peak value of the correlated received signal, but in practice, this is extremely difficult due to the small received input signal.
In this work, the receiver clock is extracted from the received impulses using pulse injection-locking. Hence, the receiver clock is automatically phase aligned with the received pulse, exhibiting neither clock offset nor phase drift. Additionally, the phase difference between the received impulse and the receiver clock can be statically adjusted by a programmable phase shifter in the receiver clocking path, aligning the receiver sampling point with the optimal SNR position of the incoming impulses . Hence, the proposed clock synchronization technique solves the conventional synchronization issue without requiring a CDR.

3. IR-UWB transceiver implementation

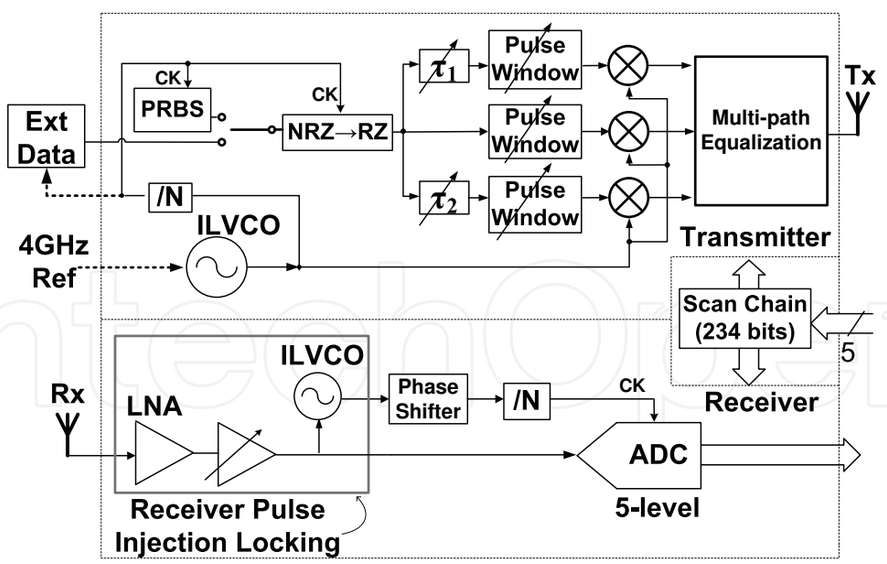


Fig. 5. IR-UWB transceiver architecture

The proposed IR-UWB transceiver is shown in Fig. 5, consisting of a UWB transmitter with multi-path equalization, a pulse-injection-locking receiver with an integrated ADC, an on-chip PRBS TX-generator and RX-checker, and a 234-bit scan chain for controlling low-frequency calibration of DC calibration bits such as current sources and resonant tank tuning. In the transmitter, OOK modulation is generated from a passive modulator, using

a $2^{15} - 1$ bit pseudo-random bit sequence (PRBS) selectable during testing operation. An on-die, 3-5GHz LC-VCO is clock-gated that generates the transmitted pulses, followed by a pulse-shaping control block that enables tunable pulse widths between 0.4-10ns.
In the receiver, the received pulse is amplified by a two-stage LNA before being directly injected into both a five-level flash ADC and a 3.4-4.5GHz, injection-locked VCO (IL-VCO). After the receiver VCO is injection-locked and phase-synchronized with the transmitted pulses, it is phase-shifted and divided down to provide the baseband ADC sampling clock. After the ADC sampling clock is divided down to the same frequency as the incoming data rate, the sampling clock is phase locked and aligned to the peak of the received input pulse, eliminating any requirements for baseband clock/data recovery. Setting the optimal phase position of the ADC sampling clock can be achieved by measuring the BER and building a bath-tub curve, sweeping through all possible phase positions. The five-level flash ADC is designed using dynamic sense amplifiers with offset-adjustable, current-steering DACs. The phase-shifter, which enables programmable, tunable phase delay of the ADC sampling clock, uses a Gilbert-cell, current-summing DAC that achieves a minimum step size of 0.5ps.

3.1 Multi-path equalization

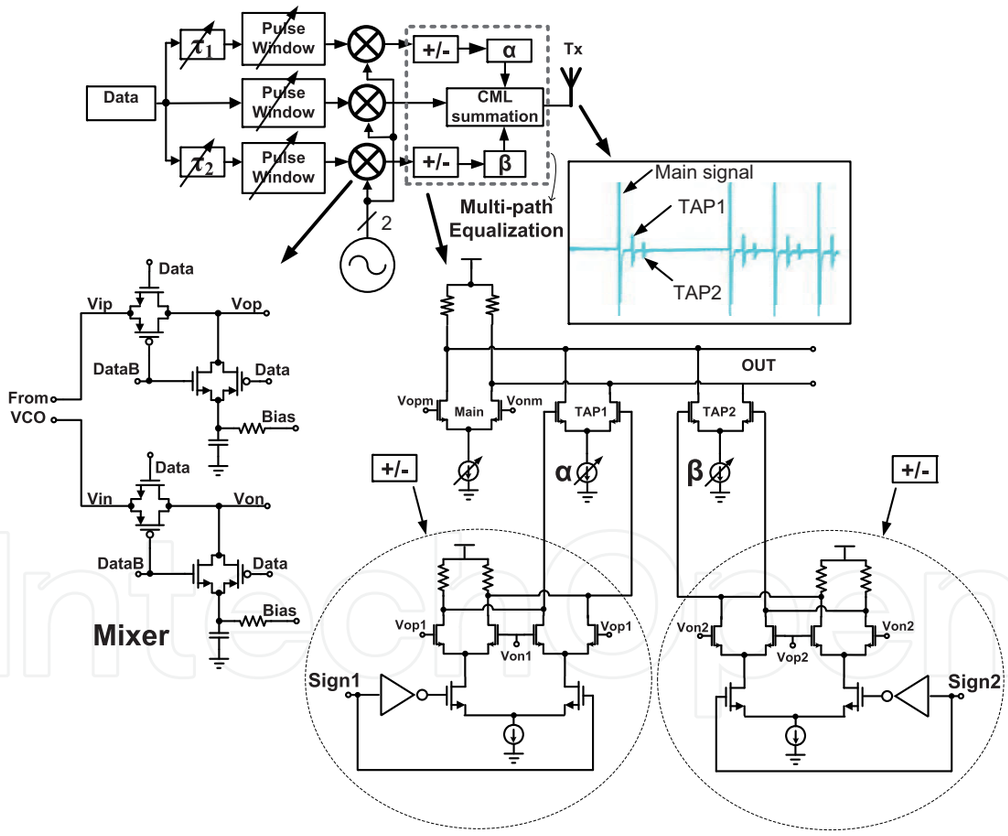


Fig. 6. Transmitter equalization

Some UWB environments exhibit severe multi-path interference, such as within a computer chassis Chiang et al. (2010), severely degrade the receiver BER, especially at high data rates. To reduce the interference from nearby reflections, a multi-path transmitter equalizer is designed that can reduce the two most severe multi-path reflections Hu, Redfield, Liu, Khanna, Nejedlo & Chiang (2009). Tap1 and Tap2 are delayed versions of

the main signal, with sign and coefficient control, depending on the actual multi-path channel environment Hu, Redfield, Liu, Khanna, Nejedlo & Chiang (2009).
Fig. 6 shows the transmitter block diagram and schematic of the pulse gating mixer and equalizer. The pulse windowing circuit controls the baseband pulse width and consequently the modulated pulse width, enabling control of the spectral bandwidh. The delay control circuits τ_1 and τ_2 control the Tap1 and Tap2 signal delay for the equalization implementation.

3.2 Receiver pulse injection-locking

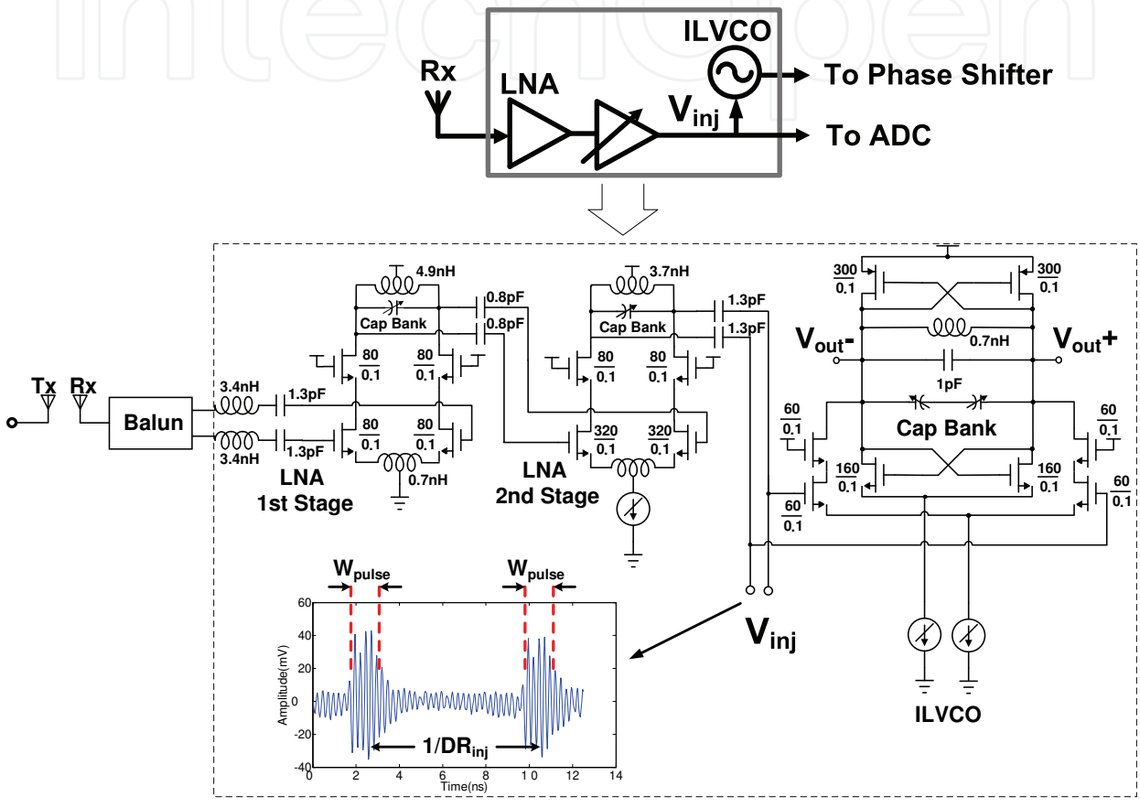


Fig. 7. Receiver injection locking

Receiver clock phase synchronization and acquisition with the received UWB pulses is critical for achieving low power consumption, as discussed in the introduction. Fig. 7 shows the injection-locking block diagram, consisting of a two-stage LNA and an IL-LCVCO.
The first stage of the LNA is source-degenerated with on-chip input matching to 50 Ohms. The LNA second stage is a source-degenerated, cascaded gain stage, with its input conjugate matched to the output of the first stage. Low Q differential inductors are used to achieve wideband frequency response. For example, staggered center frequencies of f_1=3.5GHz(first stage) and f_2=4.5GHz(second stage) are designed to achieve a broad frequency response from 3.1GHz to 5GHz. Additionally, digitally tuned capacitor banks at the outputs of both the first and second stage help to compensate for any process variations or model inaccuracies. Digital calibration loops for determining the correct capacitor values have been previously proposed in Jayaraman et al. (2010).
Due to the limited bandwidth within the LNA, the LNA output exhibits inductive tank oscillations that will elongate the received pulses width to more than 1ns. These may cause

inter-symbol-interference (ISI), limiting the highest achievable data rate to approximately 500Mbps.
In the injection-locked VCO (ILVCO), a 4-bit cap bank is used to tune the VCO free-running frequency, so that the input pulse carrier frequency is close to the ILVCO free-running frequency and injection locking will happen. The smaller the frequency difference, the smaller is the jitter of recovered clock.

3.2.1 Phase noise

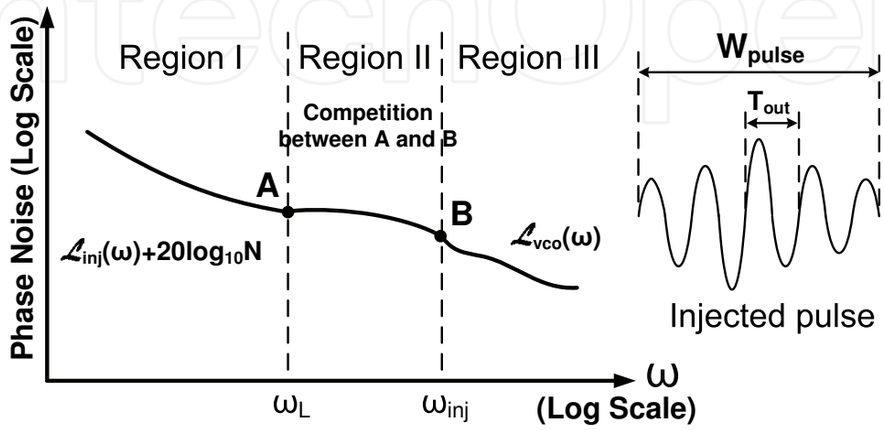


Fig. 8. Phase noise model of injection-locked VCOsLee et al. (2009)

The proposed receiver clock recovery uses pulse injection-locking from the transmitted pulses, similar to sub-harmonic injection-locking proposed in Lee et al. (2009),Lee & Wang (2009). As shown in Fig. 8, Region I denotes the region where the offset frequency is smaller than the locking range of the injection-locked VCO, where the VCO noise is suppressed by the injected signal. Region II is the competition region, where the VCO phase noise is the result of the competition between the injected signal and the VCO free-running signal. In Region III, beyond the injected signal frequency, the VCO phase noise is dominated by the VCO free running phase noise. Similar to a sub-harmonic-injection-locked PLLLee & Wang (2009), for this pulse-injection-locked VCO, the effective division ratio N can be expressed as:

$$N = \frac{f_{out}}{\alpha \cdot \beta \cdot DR_{inj} \cdot n} = \frac{f_{out}}{\alpha \cdot \beta \cdot DR_{inj} \cdot (W_{pulse}/T_{out})} = \frac{1}{\alpha \cdot \beta \cdot DR_{inj} \cdot W_{pulse}} \quad (8)$$

where α is the probability that data is "1"; β is the roll-off coefficient due to pulse-shaping at the Tx output compared with an uniformly-gated, sine-wave pulse; DR_{inj} is the data rate; f_{out} and T_{out} are the the ILVCO output signal frequency and period; and W_{pulse} is the pulse width, as shown in Fig. 7. Similar to Lee et al. (2009), the phase noise degrades as $20logN$ dB, compared with the injected signal. From Equation8, we can see that an increase in the injection pulse rate or pulse width reduces the phase noise of ILVCO output, because more external clean energy is injected into the noisy oscillator.

3.2.2 Locking range

An injection-locked VCO suppresses the noise within the locking range, similar to a first-order PLL, where the bandwidth ω_{BW} is equal to the locking range ω_L. Similar to the sub-harmonic injection-locked PLL, the locking range ω_L degrades as N increases. The locking range of a sine-wave-injected VCO is described in Razavi (2004), Adler (1973):

$$\omega_L = \frac{\omega_{out}}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \tag{9}$$

where Q represents the quality factor of the tank, and I_{inj} and I_{osc} represent the injected and oscillation currents of the LC-tank VCO, respectively. With pulse injection-locked VCOs, the effective injection current is $I_{inj,eff} = I_{inj}/N$, because less current is injected when compared with full sine-wave injection. Consequently, the locking range of a pulse-injection-locked VCO is modified as:

$$\omega_L = \frac{\omega_{out}}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{N} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2 \cdot N^2}}} \approx \frac{\omega_{out}}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{N} \tag{10}$$

3.3 Phase shifter

The phase shifter uses a current-steering DAC that supplies tail current to the two differential pairs while sharing the same resistive loadingBulzacchelli et al. (2006), as shown in Fig. 9. The bottom current-steering pair controls the weight of the current of the input clock phase for the two differential pairs. For example, the input phases of Φ_1, Φ_2, Φ_3, and Φ_4 are 0°, 90°, 180°, and 270° respectively. When the current-steering is changed, the combination of Φ_1 and Φ_2 can be rotated from 0° to 90°. The DAC-controlled current-steering employs 8-bit binary weighted cells with another half that are statically fixed, such that the output phase can be adjusted with a total range of 70ps and a minimum step size of 0.5ps, which is small enough for aligning the ADC clock with the received signal.

3.4 ADC

Fig. 10 shows the five-level flash ADC that incorporates latched sense-amplifiers as the comparatorsSchinkel et al. (2007). Different quantizer offsets/thresholds can be digitally programmed with the current DACLee et al. (2000), allowing for different comparator references. The sampling clock is directly derived from received recovered output from the injection-locked VCO after passing through the phase shifter and divider. The ADC sampling rate is the same as the impulse data rate, resulting in significant power savings over a conventional 2x-Nyquist sampling. The total power consumption for the ADC is about 2mW for a data rate of 500Mbps.

4. Measurement results

Fig. 11 shows the measurement setup. A laptop installed with Labview controls the on-chip scan-chain via a Ni-DAQ interface. Free-space measurements are performed with two 0dBi gain UWB antennas across a 10-20cm distance. Compared to a wired connection measurement (BER $< 10^{-3}$), the interference noise in the air degrades the BER significantly.

The $2mm^2$ IR-UWB transceiver is built in a 90nm-CMOS, 1.2V mixed-signal technology as shown in Fig. 12. The chip is mounted on a PCB using chip-on-board (COB) assembly with an off-chip, low-speed scan interface implemented through a NIDAQ/Labview module.

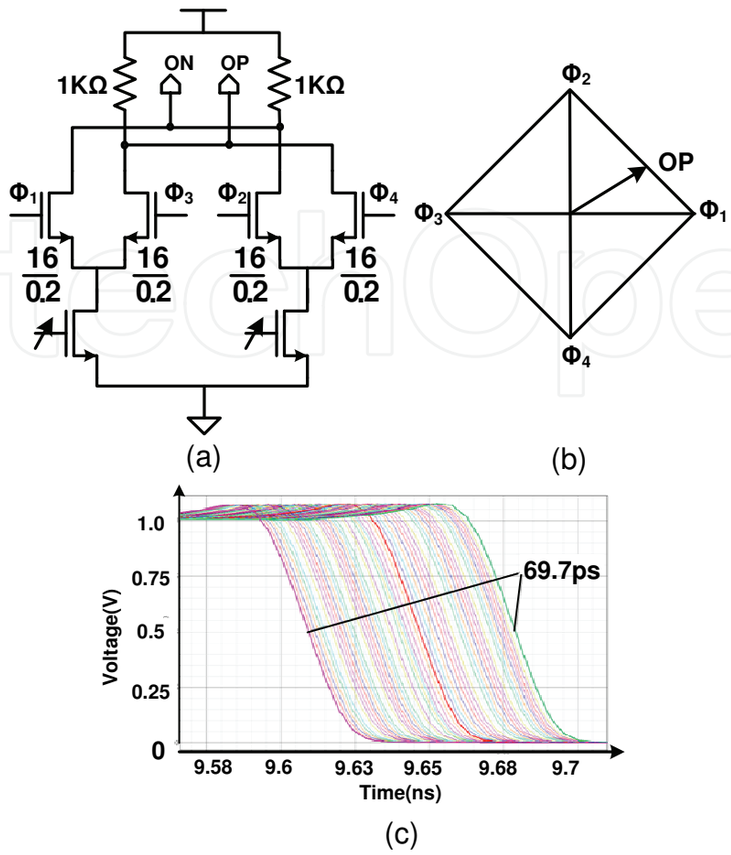


Fig. 9. Phase shifter: (a) Simplified schematic: (b) Phase shifter operation; (c) Phase shifter simulation results.

4.1 Free-space measurement

The measured transmitted signal and its spectrum are shown in Fig. 13. The amplitude of the pulse is 160mVpp, with a nominal pulse width of 1ns. The frequency spectrum fulfills the FCC UWB spectral mask except for the GPS band, which can be easily improved by incorporating more design attention to spectral shaping in the transmitter output Zheng et al. (2006). The maximum transmission data rate is 500Mbps.

Fig. 14 shows the S11/S21 simulation results of 2-stage LNA as well as S11 measurement of the receiver input. The measured S11 is centered at 4GHz, < -10dB is achieved for frequencies between 3.1-5GHz. Digital capacitor banks in LNA1 and LNA2 can adjust the inter-stage matching.

Fig. 15 shows the recovered IL-VCO clock locked to the LNA output, after phase/data alignment of the pulse zero crossing is achieved with the ADC sampling clock. With a 1ns pulse width, data rate of 250Mbps, the recovered clock jitter is 7.6ps-RMS. For the same pulse width, data rates of 125Mbps and 500Mbps are also measured, with RMS jitter of 8.0ps, and 23ps. Due to the limited bandwidth of LNA, the ISI (inter-symbol-interference) seems worse at the high data rate of 500Mbps, increasing the clock jitter.

Fig. 16(a) shows the measured injection-locking range versus varying pulse width and pulse repetition rate. As can be seen, wider pulse width and higher data rate will improve the locking range, as more transmitted pulse energy synchronizes the receiver IL-VCO. Fig. 16(b) shows the measured close-in phase noise, from free-running without injection, to pulse

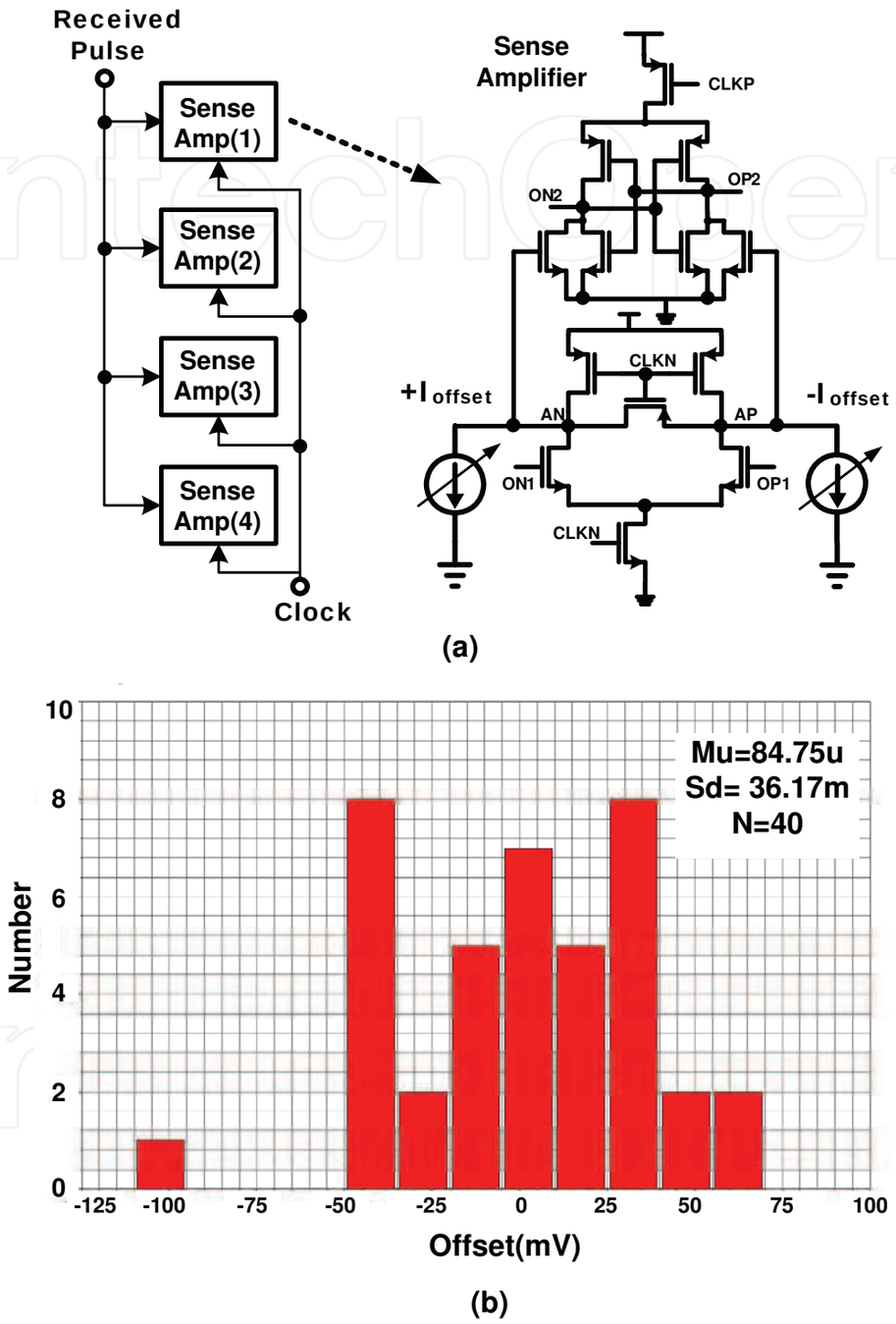


Fig. 10. Flash ADC: (a) flash ADC block diagram and comparator; (b) Monte Carlo histogram simulation results of the comparator offset with process variation and mismatch

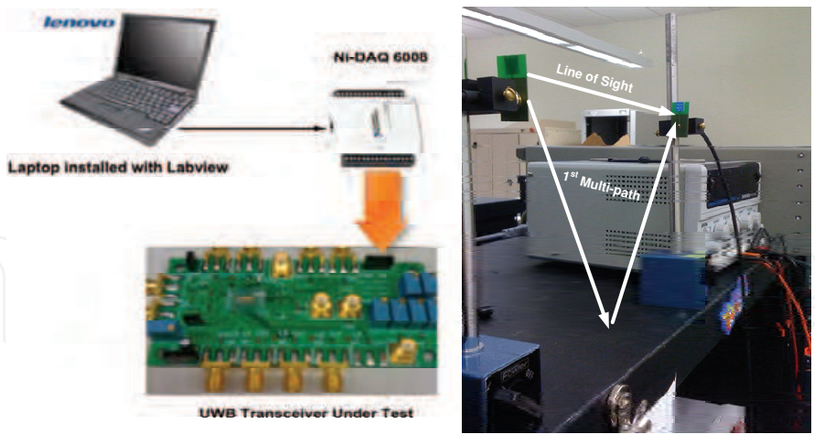


Fig. 11. Measurement setup

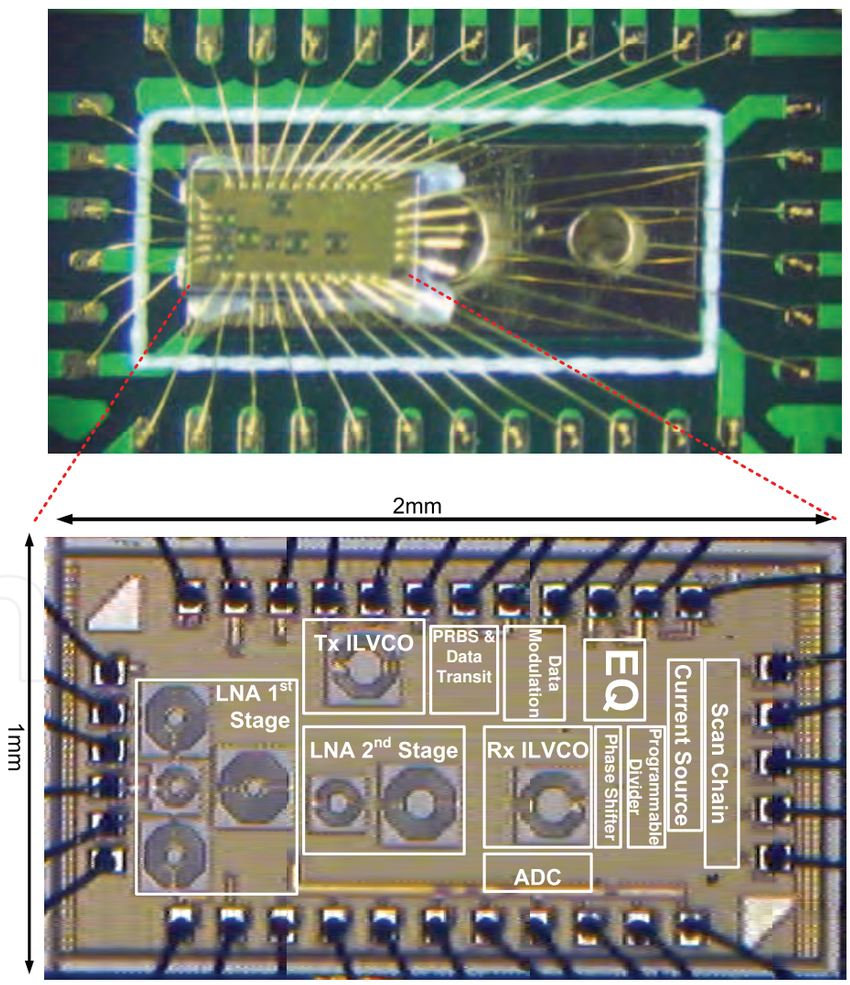


Fig. 12. COB and die photo

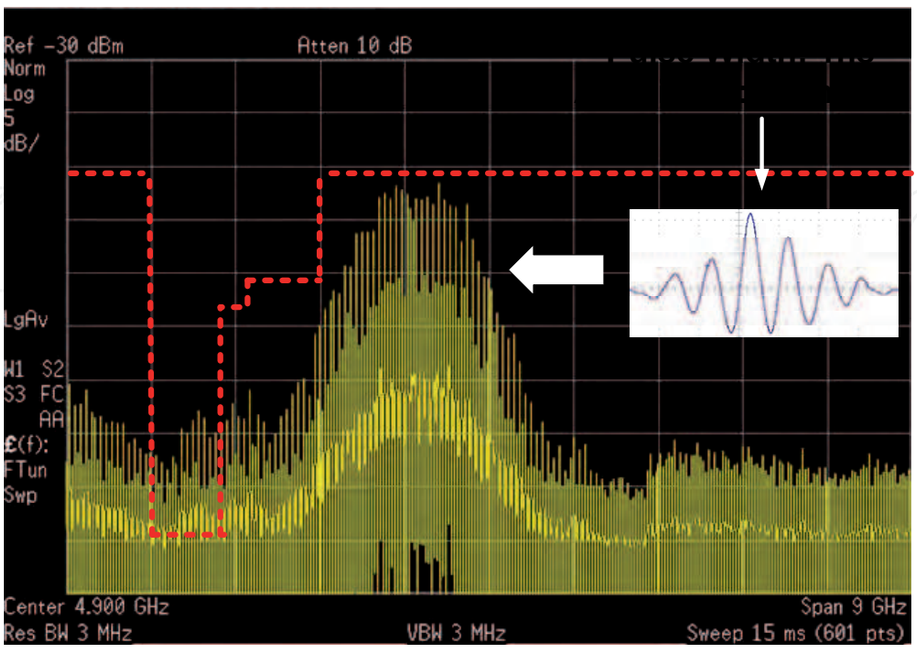


Fig. 13. Transmitted signal and power spectrum

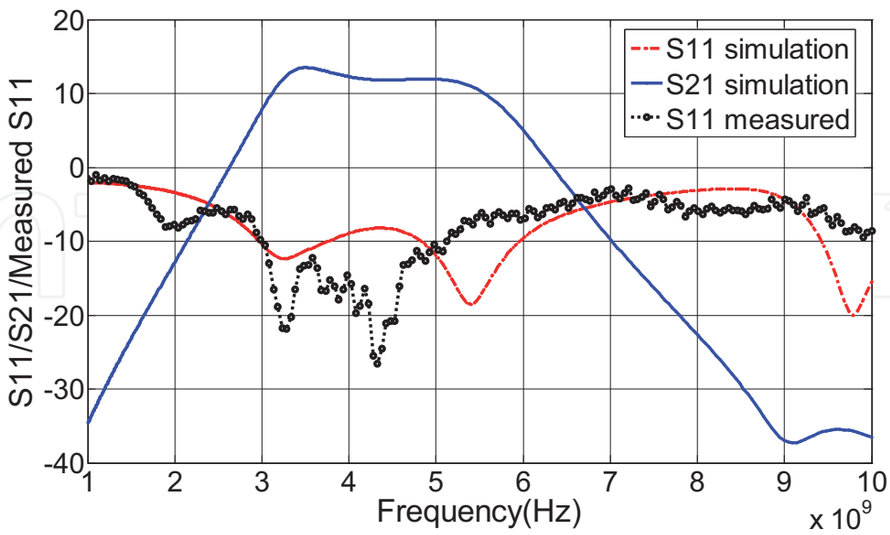


Fig. 14. S11/S21 simulations results of 2-stage LNA and S11 measurement of receiver input

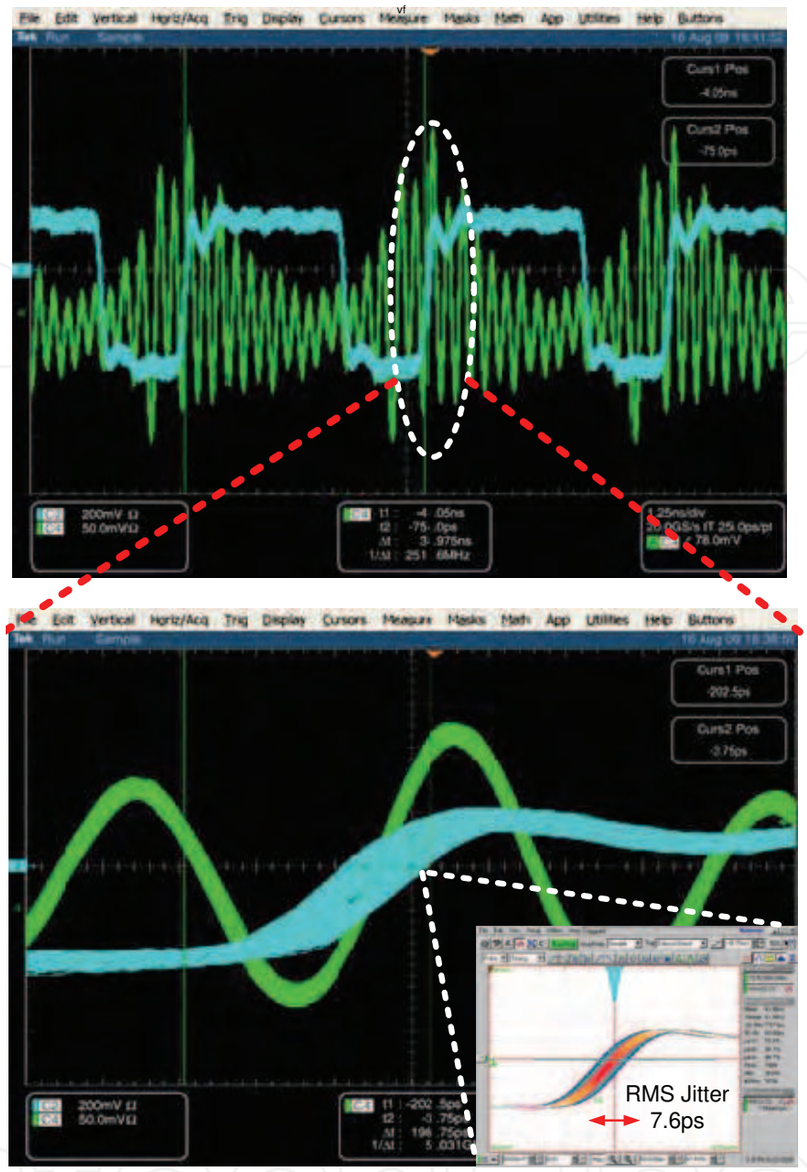


Fig. 15. ADC clock and received signal alignment measurement

repetition frequencies of (DR_{inj}) 125Mbps and 500Mbps, and finally sine-wave injection. Lower phase noise is exhibited at higher injection rates, as the phase updates occur at a higher frequency, similar to the dynamics in a first-order phase-locked loop (PLL). The results also verify Equation 8, showing approximately a 12dB phase noise difference between 125Mbps and 500Mbps pulse injection rates. Without pulse injection, the free running VCO shows very large phase noise at a low-frequency offset.

While a long string of empty data transitions would result in loss of phase synchronization, conventional DC-balanced codes such as 8b/10b can limit maximum run length. Transmission using the on-chip PRBS-15 modulator, exhibiting a maximum string length of fourteen zeros, showed no loss in receiver phase synchronization.

The free-space measurement setup uses two UWB antennas that are placed 10cm away. Fig. 17(a) and (b) show the transmitted digital data, received pulses after LNA gain, the

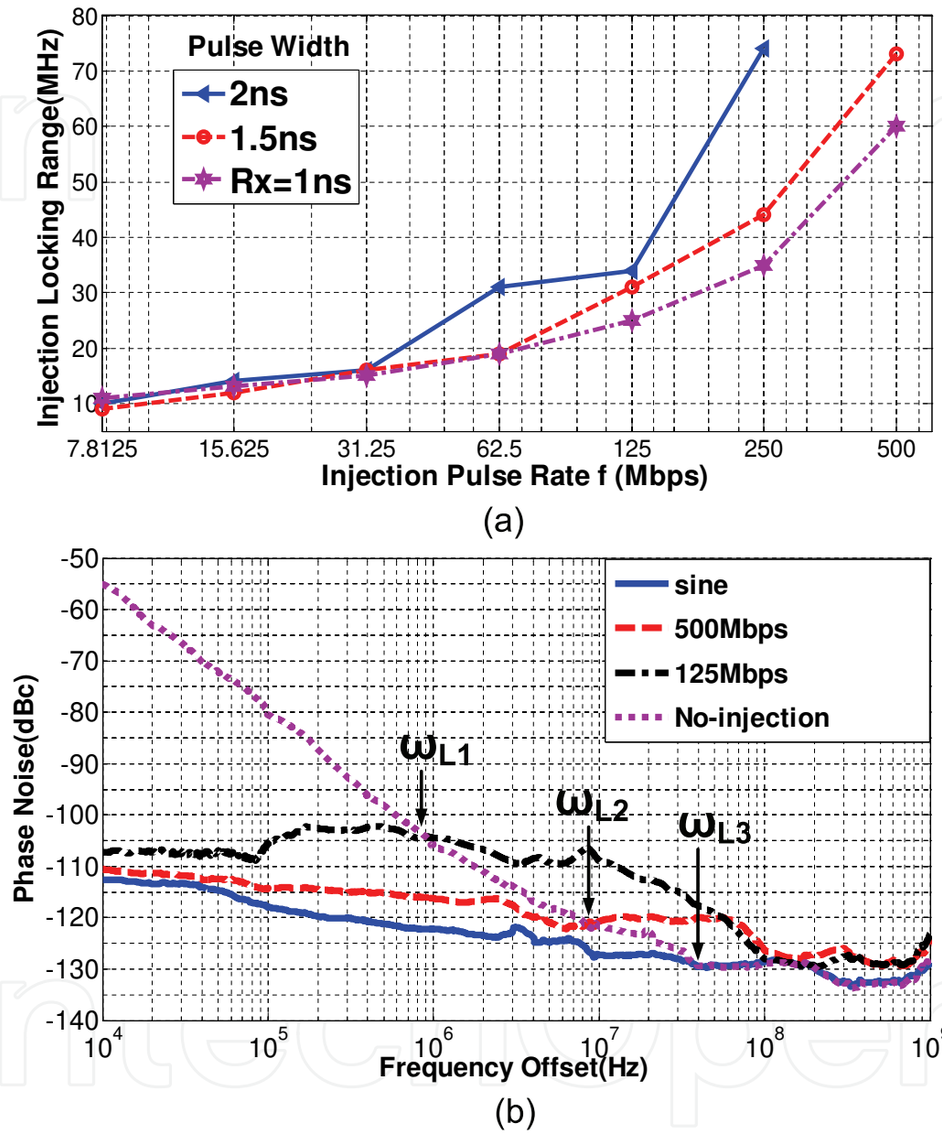


Fig. 16. Injection-locking measurement: (a) Pulse injection lock range vs. pulse width and pulse rate, (b) Pulse-injection-locked VCO phase noise vs. pulse rate. (ω_{L1}, ω_{L2} and ω_{L3} are the estimated locking range when injection data rate are 125Mbps, 500Mbps, and full sine-wave injection.)

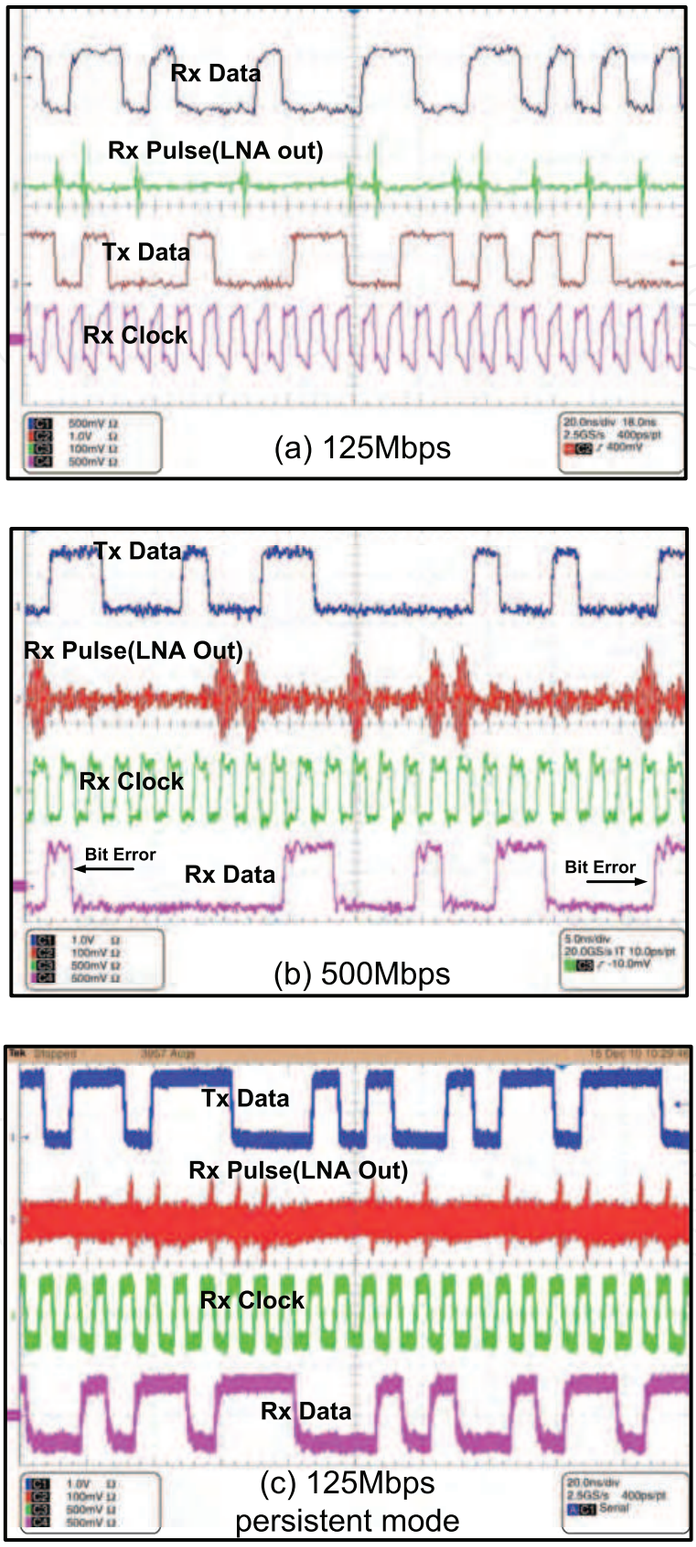


Fig. 17. Measured Tx data, Rx clock, received pulse and recovered data (125Mbps, 500Mbps) through 10cm: (a) 125Mbps, (b)500Mbps, (c) 125Mbps in infinite persistent mode.

recovered Rx clock, and finally the received demodulated data at 125Mpbs and 500Mbps. In addition to the above, at 125Mbps, 8cm distance with less multi-path reflection environment, infinite persistent mode is measured with a data pattern as in Fig. 17(c).

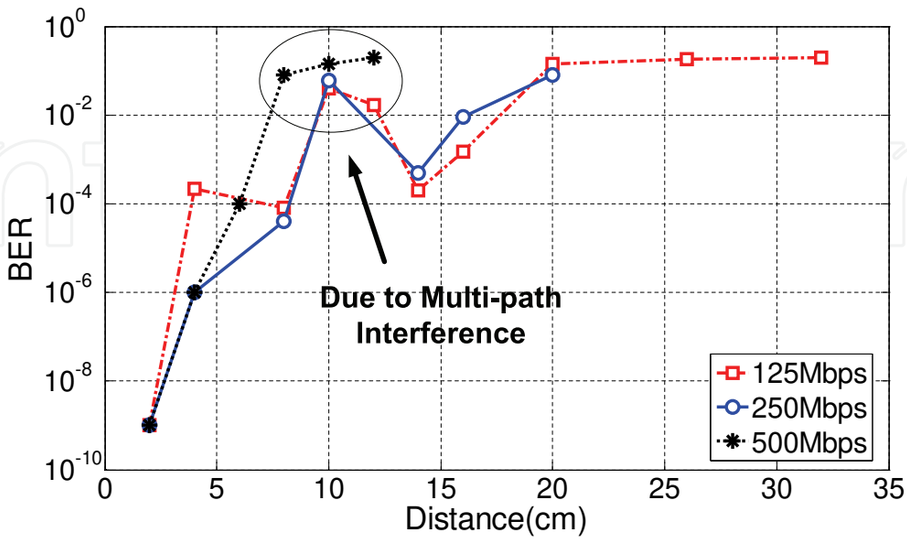


Fig. 18. Measured receiver BER versus distance @125Mbps, 250Mbps and 500Mbps with 110mVpp 1ns wide pulse

Free-space BER measurement is done with different distances for data rates of 125Mbps, 250Mbps, and 500Mbps, as shown in Fig. 18, while the transmitting pulse amplitudes are set to 110mVpp. Due to multi-path interference, it can be seen that at around 10cm, the BER is worse than that at 14cm distance because the multi-path reflections happen to be out of phase with the direction path signal at 10cm distance.

Because this receiver is injection-locked, interferer will increase the recovered clock jitter and increase the BER, so it is important to measure interference performance. By putting a single tone interferer through a UWB antenna close to the receiver antenna, characterizing the received interference power at receiver input, and increasing the interference power until the BER reaches 10^{-3}, we get the maximum tolerable power at receiver input. With a communication distance of 14cm, 125Mpbs 110mVpp 1ns wide pulses are transmitted for the interferer test. The measurement interference performance is shown in Fig. 19 for both in-band and out-band. The maximum tolerable interferer power is -50dBm at 4GHz and -25dBm at 2.4GHz.

Eight PCB evaluation boards are measured, showing consistently good measurement results. Measured performances are summarized in Table 1. Table 2 compares the performance with prior state-of-the-art, energy-efficient IR-UWB transceivers.

4.2 Multi-path equalization measurement

Multi-path reflections affect the signal differently in short-distance channels and long-distance channels (relative to the data rate): 1) For short channels, multi-path reflections are close to the main signal (direct path), causing intra-symbol interference; (while OOK modulation is somewhat enhanced by this additive energy from multi-path reflections, BPSK modulation would be severely limited due the sign change inversion.) 2) For long channels, multi-path reflections show longer delay from the main signal and may fall in the next symbol. Both intraference and interference can degrade the BER.

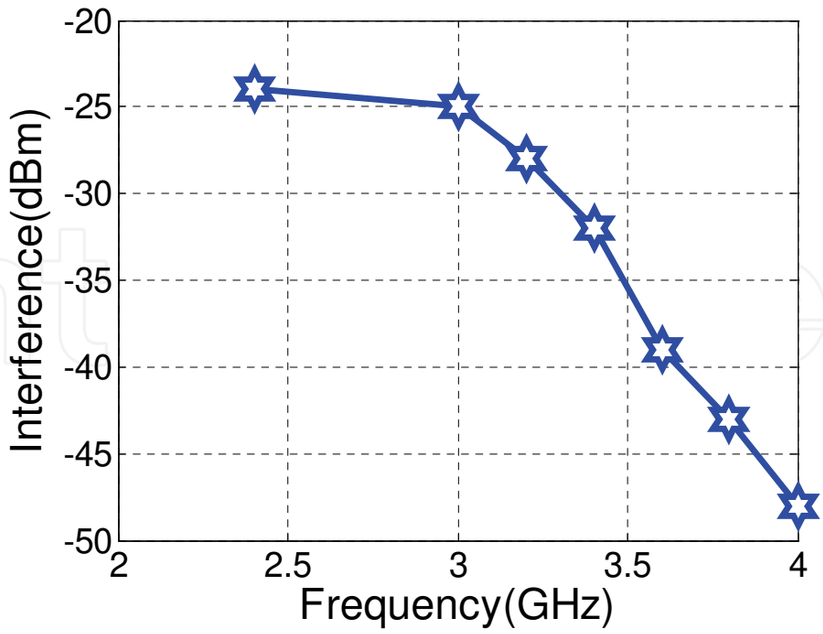


Fig. 19. Measured maximum tolerable interference power to maintain 10^{-3} BER at 125Mbps and 14cm distance when transmitting 110mVpp 1ns wide pulse.

The multi-path equalizer can cancel multi-path reflections in both short-distance and long distance channels for this OOK IR-UWB transceiver. For short channels, intra-symbol interference helps to increase the symbol energy but degrade the clock jitter, while the equalizer can help to remove intraference to reduce recovered clock jitter, consequently improving BER. For long channels, the equalizer can cancel inter-symbol interference, reduce recovered clock jitter, and improve the BER.

Measurements of the UWB transceiver were obtained for short-range, high data-rate communications inside a computer chassisChiang et al. (2010). A pre-distorting equalizer in the IR-UWB transmitter was activated in order to reduce ISI (intra-symbol-interference/inter-symbol-interference) caused by the existence of multi-path reflections from nearby metallic reflections. Fig. 20 (a) shows the simulated multi-path intra-symbol-interference of the main symbol (or baseband pulse) and the two most dominant multi-path interferer. Note that the combined energy of all three pulses sums to a symbol amplitude that exceeds the direct-path symbol. For short-distance channels, these multi-path reflections typically are a result of the main symbol generating post-cursors off of nearby reflections. For example, a time-of-flight of 1ns is equivalent to a 30cm propagation distance. For higher data rates, proceeding symbols may additively combine with current symbols, causing multi-path interference that affects the maximum data rate.

In the equalization measurement setup, all antennas are stationary, resulting in a fixed amplitude and time delay for the multi-path signal that arrive at each receiver. Hence, the two-tap coefficient delay, amplitude, and sign of the equalizer were calibrated at reset time, and adjusted differently for each of the multi-path propagations.

Fig. 20 (b) shows the pulse response (after squaring and low-pass filtering) before and after equalization is applied, for one of the receivers on the motherboard. On the left, a single pulse response is observed with several multi-path pulse interferer causing a long pulse tail. On the right, a single pulse is observed where the first tap equalization is activated, significantly reducing the multi-path reflections. At a data rate of 250Mbps, the recovered ADC clock jitter

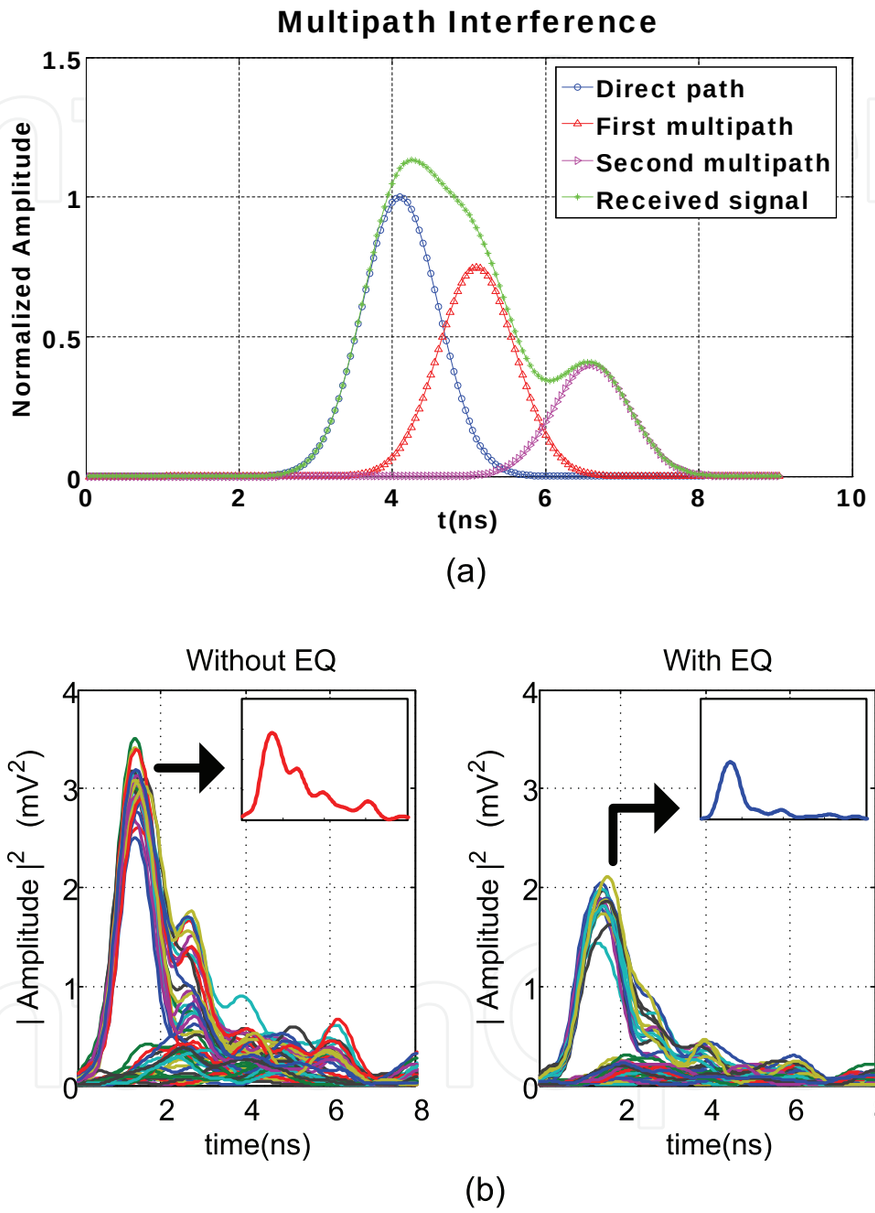


Fig. 20. Multi-path interference: (a) Simulated multi-path interference, (b) Measured received signal with and without multi-path equalization inside computer chassis

was improved significantly after applying the equalizer, reducing RMS clock jitter by 27.4% at RX1 in Fig. 1 while the motherboard was operational. Within an enclosed chassis that exhibits significant multi-path interference, at 250Mbps BER is improved from 0.0158 to 0.0067 without/with first-tap equalization enabled respectively. While the proposed equalization can help cancel the multi-path reflections, it is difficult in practice to eliminate them completely.

5. Conclusion

A fully integrated, single-chip IR-UWB transceiver with ADC in 90nm CMOS is presented. A novel pulse-injection-locking method is used for receiver clock synchronization in the receiver demodulation, leading to significant power reduction by eliminating the high-power oversampling ADC and mixer. The complete transceiver achieves a maximum data rate of 500Mbps, through a 10cm distance, consuming 0.18nJ/bit. Measured BER achieves 10^{-3} at 125Mbps through 10cm of free space. Due to the FCC transmitted power limitation, the pulse amplitude for higher data rates will be smaller, limiting the communication distance to up to half a meter. Further improvements include increasing the communication distance and reducing the BER by adding gain to the RF front-end, investigating pulse spectral shaping, and incorporating receiver pulse integration and low-pass filtering.

Technology	90nm CMOS
Die Size	1mmx2mm
Modulation	OOK
Data Rate	7.8125-500Mbps
VCO Range	3.7-4.5GHz
Power Dissipation	70mA@1.3V
Transmitted Pulse Width	0.5-10ns
Rx Sensitivity(Free space)	-64dBm@125Mbps, BER $< 10^{-3}$
Rx Sensitivity(Free sapce)	-60dBm@500Mbps, BER $< 10^{-1}$
BER(within chasis, w/o EQ)	1.7×10^{-3}@15cm
BER(within chasis, w/ EQ)	3.3×10^{-4}@15cm
Energy Efficiency(W/ADC)	Tx: 90pJ/b; Rx:90pJ/b

Table 1. Chip performance summary

paper	CMOS (nm)	Frequency (GHz)	Energy(pJ/b) Tx	Energy(pJ/b) Rx	Modulation	ADC	Data (M
Zheng et al. (2008)	180	3.1-9	740	6500	BPSK	No	1
Verhelst et al. (2009)	130	0-0.96	-	110	BPSK	No	
Lachartre et al. (2009)	130	3.1-5	1100		OOK/PPM/BPSK	No	
Wentzloff & Chandrakasan (2007)	90	3.1-5	47	-	PPM w/ DB-BPSK	N/A	1
Lee & Chandrakasan (2007)	90	3.1-5	-	2500	PPM	No	1
Crepaldi et al. (2010)	90	3.6-4.3	249	1450	OOK	No	
Joo et al. (2010)	130	3.1-5	3300		BPM-BPSK	YES	0
(Zheng et al., 2010)	180	3.5-4.5	920	5300	OOK/BPSK	YES	
This work	90	3.1-5	90	90	OOK	Yes	5

Table 2. Comparison with previous published work

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6. References

Adler, R. (1973). A study of locking phenomena in oscillators, *Proceedings of the IEEE* 61(10): 1380 – 1385.

Bulzacchelli, J., Meghelli, M., Rylov, S., Rhee, W., Rylyakov, A., Ainspan, H., Parker, B., Beakes, M., Chung, A., Beukema, T., Pepeljugoski, P., Shan, L., Kwark, Y., Gowda, S. & Friedman, D. (2006). A 10-gb/s 5-tap dfe/4-tap ffe transceiver in 90-nm cmos technology, *IEEE J. Solid-State Circuits* 41(12): 2885 –2900.

Chiang, P., Woracheewan, S., Hu, C., Guo, L., Khanna, R., Nejedlo, J. & Liu, H. (2010). Short-range, wireless interconnect within a computing chassis: Design challenges, *Design Test of Computers, IEEE* 27(4): 32 –43.

Crepaldi, M., Li, C., Dronson, K., Fernandes, J. & Kinget, P. (2010). An ultra-low-power interference-robust ir-uwb transceiver chipset using self-synchronizing ook modulation, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 226 –227.

First Report and Order (n.d.). FCC, 2002.

Hu, C., Chiang, P., Hu, K., Liu, H., Khanna, R. & Nejedlo, J. (2010). A 90nm-cmos, 500mbps, fully-integrated ir-uwb transceiver using pulse injection-locking for receiver phase synchronization, *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 201 –204.

Hu, C., Redfield, S., Liu, H., Khanna, R., Nejedlo, J. & Chiang, P. (2009). Transmitter equalization for multipath interference cancellation in impulse radio ultra-wideband(ir-uwb) transceivers, *VLSI Design, Automation and Test, 2009. VLSI-DAT '09. International Symposium on*, pp. 307 –310.

Hu, K., Jiang, T., Wang, J., O'Mahony, F. & Chiang, P. Y. (2009). A 0.6mw/gbps, 6.4 -8.0gbps serial link receiver using local injection-locked ring oscillators in 90nm cmos, *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 46 –47.

Jayaraman, K., Khan, Q., Chi, B., Beattie, W., Wang, Z. & Chiang, P. (2010). A self-healing 2.4ghz lna with on-chip s11/s21 measurement/calibration for in-situ pvt compensation, *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, pp. 311 –314.

Joo, S., Chen, W.-H., Choi, T.-Y., Oh, M.-K., Park, J.-H., Kim, J.-Y. & Jung, B. (2010). A fully integrated 802.15.4a ir-uwb transceiver in 0.13μm cmos with digital rrc synthesis, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 228 –229.

Lachartre, D., Denis, B., Morche, D., Ouvry, L., Pezzin, M., Piaget, B., Prouvee, J. & Vincent, P. (2009). A 1.1nj/b 802.15.4a-compliant fully integrated uwb transceiver in 0.13μm cmos, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 312 –313,313a.

Lathi, B. (n.d.). *Modern Digital and Analog Communication Systems*, Oxford University Press, 3rd edition, New York.

Lee, F. & Chandrakasan, A. (2007). A 2.5nj/b 0.65v 3-to-5ghz subbanded uwb receiver in 90nm cmos, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 116 –590.

Lee, J. & Wang, H. (2009). Study of subharmonically injection-locked plls, *Solid-State Circuits, IEEE Journal of* 44(5): 1539 –1553.

Lee, J., Wang, H., Chen, W.-T. & Lee, Y.-P. (2009). Subharmonically injection-locked plls for ultra-low-noise clock generation, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 92 –93,93a.

Lee, M.-J., Dally, W. & Chiang, P. (2000). A 90 mw 4 gb/s equalized i/o circuit with input offset cancellation, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 252 –253, 463.

O'Donnell, I. & Brodersen, R. (2006). A 2.3mw baseband impulse-uwb transceiver front-end in cmos, *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 200–201.

Razavi, B. (2004). A study of injection locking and pulling in oscillators, *Solid-State Circuits, IEEE Journal of* 39(9): 1415 – 1424.

Schinkel, D., Mensink, E., Kiumperink, E., van Tuijl, E. & Nauta, B. (2007). A double-tail latch-type voltage sense amplifier with 18ps setup+hold time, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 314 –605.

UWB Channel Modeling Contribution from CEA-LETI and STMicroelectronics (n.d.). J. Keignart, N. Daniele, and J.B. Pierrot, Nov 2002 [Online].

Van Helleputte, N. & Gielen, G. (2009). A 70 pj/pulse analog front-end in 130 nm cmos for uwb impulse radio receivers, *IEEE J. Solid-State Circuits* 44(7): 1862 –1871.

Verhelst, M., Van Helleputte, N., Gielen, G. & Dehaene, W. (2009). A reconfigurable, 0.13μm cmos 110pj/pulse, fully integrated ir-uwb receiver for communication and sub-cm ranging, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 250 –251,251a.

Wentzloff, D. (2007). *Pulse-Based Ultra-Wideband Transmitters for Digital Communication*, PhD thesis, MIT.

Wentzloff, D. & Chandrakasan, A. (2007). A 47pj/pulse 3.1-to-5ghz all-digital uwb transmitter in 90nm cmos, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 118 –591.

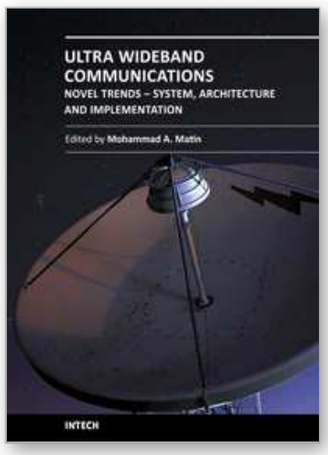
Zheng, Y., Annamalai Arasu, M., Wong, K.-W., The, Y. J., Suan, A., Tran, D. D., Yeoh, W. G. & Kwong, D.-L. (2008). A 0.18μm cmos 802.15.4a uwb transceiver for communication and localization, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 118 –600.

Zheng, Y., Diao, S.-X., Ang, C.-W., Gao, Y., Choong, F.-C., Chen, Z., Liu, X., Wang, Y.-S., Yuan, X.-J. & Heng, C. (2010). A 0.92/5.3nj/b uwb impulse radio soc for communication and localization, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 230 –231.

Zheng, Y., Zhang, Y. & Tong, Y. (2006). A novel wireless interconnect technology using impulse radio for interchip communications, *Microwave Theory and Techniques, IEEE Transactions on* 54(4): 1912 – 1920.

Zhou, L., Chen, Z., Wang, C.-C., Tzeng, F., Jain, V. & Heydari, P. (2009). A 2gbps rf-correlation-based impulse-radio uwb transceiver front-end in 130nm cmos, *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 65 –68.

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