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# Graphene Transistors and RF Applications

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## 1. Introduction

Graphene is an atomically thin but stable layer form of hexagonal carbon and has attracted a lot of attention in the research community over the last few years because of its unique electronic properties [Geim & Novoselov, 2007; Guisinger and Arnold, 2010]. Graphene exhibits the highest carrier mobility:  $>100,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  at room temperature [Morozov et al., 2008]. This is not only  $\sim 100$  times greater than that of Si, but about 10 times greater than state-of-the-art semiconductors lattice-matched to InP, currently regarded the best high-speed materials. The saturation velocity ( $v_{\text{sat}}$ ) of graphene has not been determined clearly yet, but it is estimated to be  $\sim 5$  times greater than that for Si MOSFETs [Akturk and Goldsman, 2008]. With expected large on-state current density and transconductance per gate capacitance compared to Si, graphene has the potential to offer excellent switching characteristics (capacitance/on-state current) and short-circuit current gain cut-off frequency. Although it is too early to predict, graphene FETs could potentially be processed in a manner compatible with Si CMOS with desirable integration density for system-on-chip applications. While there are numerous challenges (including proper bandgap engineering) to be overcome for graphene to become a mature technology, this material offers unique device and circuit applications including ambipolar RF electronics [Moon et al., 2009].

## 2. Epitaxial graphene synthesis

Several epitaxial graphene synthesis approaches have been reported on the wafer-scale, including a Si sublimation method out of SiC substrates [Berger et al., 2004 & 2006], metal catalyst-based CVD growth [Sutter, 2008] and direct carbon deposition in MBE.

## 3. Epitaxial graphene transistors

Epitaxial graphene FETs on the wafer-scale are in early stages of development, although several key device parameters have been demonstrated. For example, epitaxial graphene RF FETs have been demonstrated in a top-gated layout with the highest ever on-state current density of  $3 \text{ A/mm}$  [Moon et al., 2009 #2]. In addition, the extrinsic speed performance ( $f_t/f_{\text{max}}$  of  $5 \text{ GHz}/14 \text{ GHz}$ ) is reported with a  $2 \text{ }\mu\text{m}$  gate length [Moon et al., 2009 #2]. On the other hand, the current-voltage characteristics are quasi-linear with weak saturation behaviors, yielding low transconductance ( $g_m$ ) per capacitance (i.e.,  $<140 \text{ mS/mm}$  at  $3.4 \text{ fF}/\mu\text{m}^2$ ) and poor voltage gain ( $g_m/G_{\text{ds}}$ ). Also, the  $I_{\text{on}}/I_{\text{off}}$  ratio was  $\sim 4$  with field-effect mobility below 200

$\text{cm}^2/\text{Vs}$ . While graphene field-effect mobility as high as  $5400 \text{ cm}^2/\text{Vs}$  for electron has been demonstrated [Wu et al., 2008], it was achieved using six to seven layers of epitaxial graphene on C-face SiC substrates, resulting in an  $I_{\text{on}}/I_{\text{off}}$  ratio of  $<2$ . In the case of graphene FETs fabricated on the Si-face of SiC substrates, field-effect mobility has been limited to below  $1200 \text{ cm}^2/\text{Vs}$ , but with an improved  $I_{\text{on}}/I_{\text{off}}$  ratio of  $\sim 10$  [Kedzierski et al., 2008].

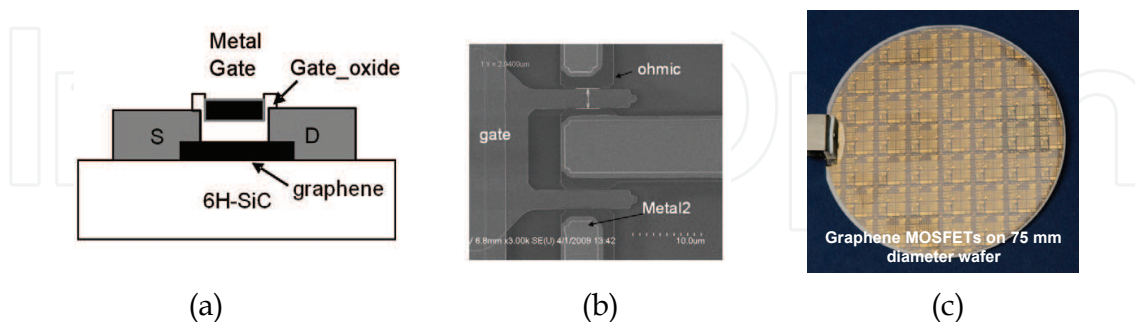


Fig. 1. (a) A schematic of the top-gated graphene FET. (b) A SEM photograph of  $2f \times 4 \mu\text{m}$  graphene FET. (c) A photograph of 75 mm graphene wafer.

In this section, we present top-gated graphene n-FETs and p-FETs from epitaxial graphene layers, where *excellent I-V saturation behaviors were observed in epitaxial graphene FETs with a record peak extrinsic transconductance of  $600 \text{ mS/mm}$  [Moon et al., 2010].* Also, the effective mobility and field-effect mobility versus  $E_{\text{eff}}$  were characterized and compared with Hall mobility. The epitaxial graphene layers were grown on Si-face 6H-SiC substrates on 50-mm wafers via Si sublimation [Gaskill et al., 2009]. The sheet electron carrier density of the epitaxial graphene layer was typically  $8.8 \times 10^{12} \text{ cm}^{-2}$  at room temperature and had electron mobility of  $\sim 1192 \text{ cm}^2/\text{Vs}$ , characterized by non-contact Hall Leighton 1600. The number of epitaxial graphene layers (nGL) was found to be one layer on the SiC terraces and two layers on the step edges over the entire 50-mm wafer as characterized by Raman analysis and transmission electron microscopy analysis.

Graphene FETs were fabricated using Ti/Pt/Au source and drain metal deposition and lift-off process. The non-alloyed ohmic metal yielded the contact resistivity of  $10^{-6} - 10^{-7} \Omega\cdot\text{cm}^2$  [Moon et al., 2009 #2]. The metal gates were processed via the Ti/Pt/Au metal deposition and lift-off process on top of a 35-nm-thick  $\text{SiO}_2$  gate dielectric layer deposited by electron beam evaporation. The gate leakage current was in the range of  $\sim \text{nA}/\mu\text{m}^2$  or less, which is negligible in the device characterization presented here.

Figure 1 (a)-(c) shows the graphene FET processed in a layout, where the gate metal is aligned with respect to the ohmic metals in an under lap layout with a gate-to-source/drain separation of  $<100 \text{ nm}$  to minimize the access resistance over a source-drain spacing ( $L_{\text{sd}}$ ) of  $3 \mu\text{m}$ . The source access resistance was  $<0.2 \Omega\cdot\text{mm}$  via the standard end-point measurements on transfer length method (TLM) structures. A graphene channel width of  $4 \mu\text{m}$  was defined by  $\text{O}_2$  plasma etching.

Figure 2 (a)-(b) shows measured room temperature, common-source, current-voltage characteristics of a two-gatefinger and  $4\text{-}\mu\text{m}$ -wide n-channel graphene FET (denoted as  $2f \times 4 \mu\text{m}$ ), in which excellent drain current saturation was observed. The source-to-drain voltage ( $V_{\text{ds}}$ ) increased to  $3 \text{ V}$ , where the gate-to-source ( $V_{\text{gs}}$ ) voltage was stepped from  $3 \text{ V}$  (top-curve) in steps of  $-0.5 \text{ V}$ . At  $V_{\text{ds}} = 1 \text{ V}$ , on-state current at  $V_{\text{gs}} = 3 \text{ V}$  was  $0.59 \text{ A/mm}$ . The off-state current was  $0.047 \text{ A/mm}$  at  $V_{\text{gs}} = -1 \text{ V}$ , yielding  $I_{\text{on}}/I_{\text{off}}$  ratio of 12.5. At  $V_{\text{ds}} = 0.5 \text{ V}$ , the  $I_{\text{on}}/I_{\text{off}}$  ratio increased to 19 with the on-state current of  $0.31 \text{ A/mm}$ . At  $V_{\text{ds}} = 3 \text{ V}$ , the on-state current at  $V_{\text{gs}} = 3 \text{ V}$  was measured as high as  $1.65 \text{ A/mm}$ . The on-resistance was  $1.6 \Omega\cdot\text{mm}$ .

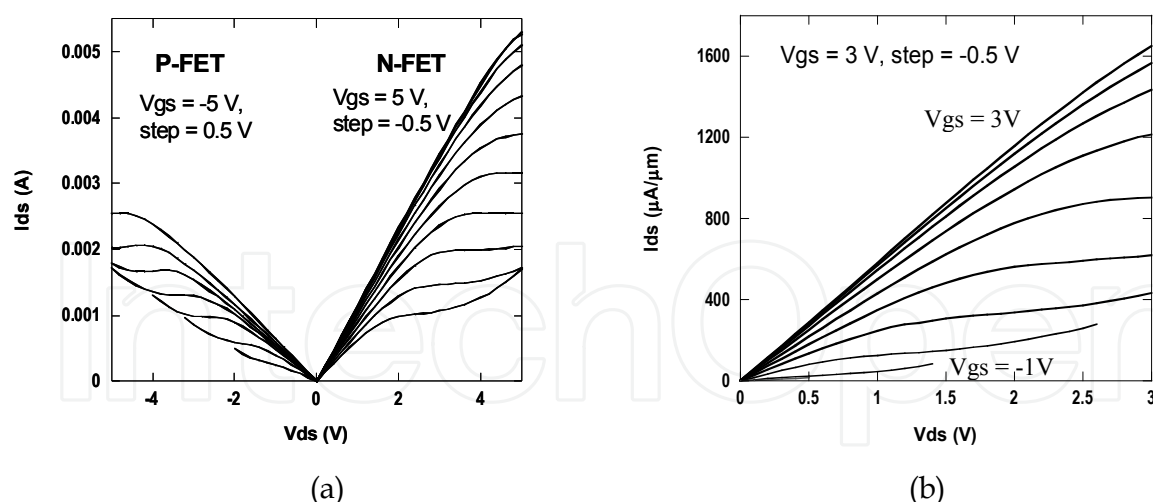


Fig. 2. (a) Measured common-source current-voltage characteristics of  $1f \times 4 \mu\text{m}$  graphene FET. (b) Both p-channel and n-channel graphene MOSFET operations.

Figure 3 shows measured transconductance ( $g_m$ ) of a  $2f \times 4 \mu\text{m}$  graphene FET at different  $V_{ds}$ , stepping from 1.05 to 3.05 V with a step of 0.5 V. The inset shows measured transfer curves. At  $V_{ds} = 3.05$  V, the  $I_{ds}$  reached up to 1.1 A/mm at  $V_{gs} = 3$  V. The ambipolar behavior was observed clearly at  $V_{ds} > 2$  V, while the ambipolar behavior is not well-developed with a relatively flat region observed at low  $V_{ds}$  such as  $V_{ds} = 1.05$  V. The peak extrinsic  $g_m$  of 600 mS/mm was measured at  $V_{ds} = 3.05$  V, which is the highest ever, amongst epitaxial graphene FETs. The observed negative transconductance is due to a conversion of n-channel to p-channel. The effective mobility,  $\mu_{eff}$ , was extracted using a formula:  $\mu_{eff} = (L/W) \cdot I_{ds} / [C_{ox} \cdot (V_{gs} - V_T) \cdot V_{ds}]$ . The  $C_{ox}$  is gate\_oxide capacitance,  $\epsilon_0 \cdot \epsilon_{ox} / t_{ox}$ , where  $\epsilon_0$  and  $\epsilon_{ox}$  are permittivity of the free space and gate\_oxide layer, respectively. Gate\_oxide capacitance is measured using a metal-gate\_oxide-metal (MOM) capacitor array with OPEN and SHORT calibration standards. The geometric scaling of the MOM capacitors is verified to eliminate fringe capacitances. The geometric oxide capacitances were measured at 1 fF/ $\mu\text{m}^2$  or 1.7 fF/ $\mu\text{m}^2$  from the two different wafers. The dielectric constant of the deposited  $\text{SiO}_2$  films was determined to be 3.9, which is close to that of  $\text{SiO}_2$ . The field-effect mobility,  $\mu_{FE}$ , defined by  $\mu_{FE} = (L/W) \cdot g_m / (C_{ox} \cdot V_{ds})$ , was obtained from the transconductance ( $g_m$ ) at  $V_{ds} = 50$  mV. So, there is no ambiguity in  $\mu_{FE}$  associated with the  $V_T$  unlike the case of  $\mu_{eff}$ . The effective electric field is estimated using  $E_{eff} = Q_{Gr} / (\epsilon_0 \cdot \epsilon_{ox})$ , where  $Q_{Gr}$  is the total charge in the graphene channel.

Figure 4 shows extracted  $\mu_{eff}$  and  $\mu_{FE}$  of graphene n-FETs versus the effective electric field,  $E_{eff}$ . In comparison, the universal and field-effect mobility of Si n-MOSFETs [Takagi et al., 1994] and strained Si n-MOSFETs on SiGe-on-oxide [Cheng et al., 2001] are shown. While both the  $\mu_{eff}$  and  $\mu_{FE}$  of the graphene n-FETs depend on  $E_{eff}$ , both values were higher than 1000  $\text{cm}^2/\text{Vs}$  over a wide range of the effective electric field up to 1.6 MV/cm. The peak field-effect mobility values ranged from 3200  $\text{cm}^2/\text{Vs}$  to 6000  $\text{cm}^2/\text{Vs}$ . A record field-effect mobility of 6000  $\text{cm}^2/\text{Vs}$  was obtained at an effective electric field of 0.27 MV/cm. The measured field-effect mobility of graphene n-FETs was at least seven times higher than that of ITRS Si n-MOSFETs and  $\sim 80$  times higher than ultra-thin-body SOI n-MOSFETs. The peak field-effect mobility of graphene p-FETs was also determined to be 3200  $\text{cm}^2/\text{Vs}$  at an effective electric field of 0.2 MV/cm.

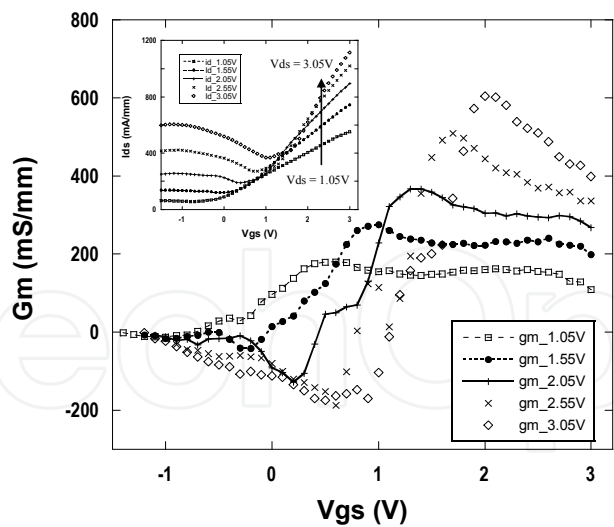


Fig. 3. Measured small-signal transconductance of 1f x 4 μm n-channel graphene FET at different Vds , from 1.05 V to 3.05 V in steps of 0.5 V. Peak extrinsic transconductance is as high as 600 mS/mm at Vds = 3.05 V. The inset shows measured transfer curves from 1.05 V to 3.05 V in steps of 0.5 V.

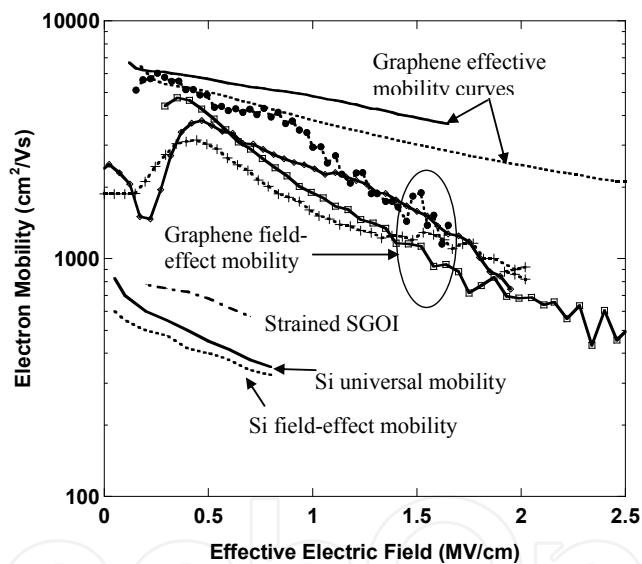


Fig. 4. Measured effective carrier mobility and field-effect mobility of graphene n-FETs compared with those of Si n-MOSFET and strained Si on SGOI MOSFET.

4. Wafer-scale graphene-on-Si transistors

Graphene synthesis directly on silicon substrates is highly attractive because graphene wafers can be scaled-up significantly larger than commercially available (4,6)H-SiC substrates; this technique is being evaluated either via a direct carbon deposition [Hackley et al., 2009] or via a growth of template layer such as 3C-SiC [Suemitsu et al., 2009]. Utilizing a 3C-SiC(111) template grown on Si(110), epitaxial graphene-on-Si FETs are reported with Ion of >0.03 μA/μm at Vds = 1V in a top-gated layout [Kang et al., 2009]. The very low Ion was attributed to a high sheet resistance of 129 kΩ/sq. Ambipolar current-voltage characteristics, unique to the graphene, were not clearly demonstrated.



In this section, we present top-gated graphene-on-Si FETs utilizing 3C-SiC(111) templates grown on 75 mm Si(111) substrates. The ambipolar characteristics were observed clearly for the first time, with Dirac points close to zero gate voltage. The  $I_{\text{on}}$  of  $225 \mu\text{A}/\mu\text{m}$  was demonstrated, which is the highest for epitaxial graphene-on-Si FETs.

Figure 5 shows a schematic of top-gated and self-aligned, graphene-on-Si FETs with a SEM photograph of a 2 gatefinger graphene FET. These graphene-on-Si FETs were processed in a layout with a source-drain spacing ( $L_{\text{sd}}$ ) of 1 or 3  $\mu\text{m}$ ; the gate metal is aligned with respect to the pre-defined ohmic metals in an under lap layout with a gate-to-source/drain separation of  $<100 \text{ nm}$ . Graphene channel widths varied from 6  $\mu\text{m}$ , 12  $\mu\text{m}$ , and 25  $\mu\text{m}$ , which were defined by  $\text{O}_2$  plasma etching. Ohmic metals were fabricated with Ti/Pt/Au source and drain metal deposition and lift-off process. The non-alloyed ohmic metal yielded a contact resistance of  $2.5 \Omega\cdot\text{mm}$  and a contact resistivity of  $\sim 10^{-5} \Omega\cdot\text{cm}^2$  using the transmission line method (TLM). The contact resistivity was higher than that of  $\sim 10^{-7} \Omega\cdot\text{cm}^2$  from graphene-on-SiC FETs [6]. The metal gates were processed with Ti/Pt/Au metal deposition and lift-off process on top of a 35-nm-thick  $\text{SiO}_2$  gate dielectric layer deposited by electron beam evaporation. Figure 5(c) shows measured transfer curves of 25- $\mu\text{m}$ -wide graphene-on-Si FETs with  $L_{\text{sd}} = 3 \mu\text{m}$  at a fixed  $V_{\text{ds}} = 2 \text{ V}$ . The ambipolar behaviors were observed clearly with Dirac points closed to zero gate voltage. An  $I_{\text{on}}$  of  $80\text{--}100 \mu\text{A}/\mu\text{m}$  was obtained at  $V_{\text{gs}} = 3 \text{ V}$ .

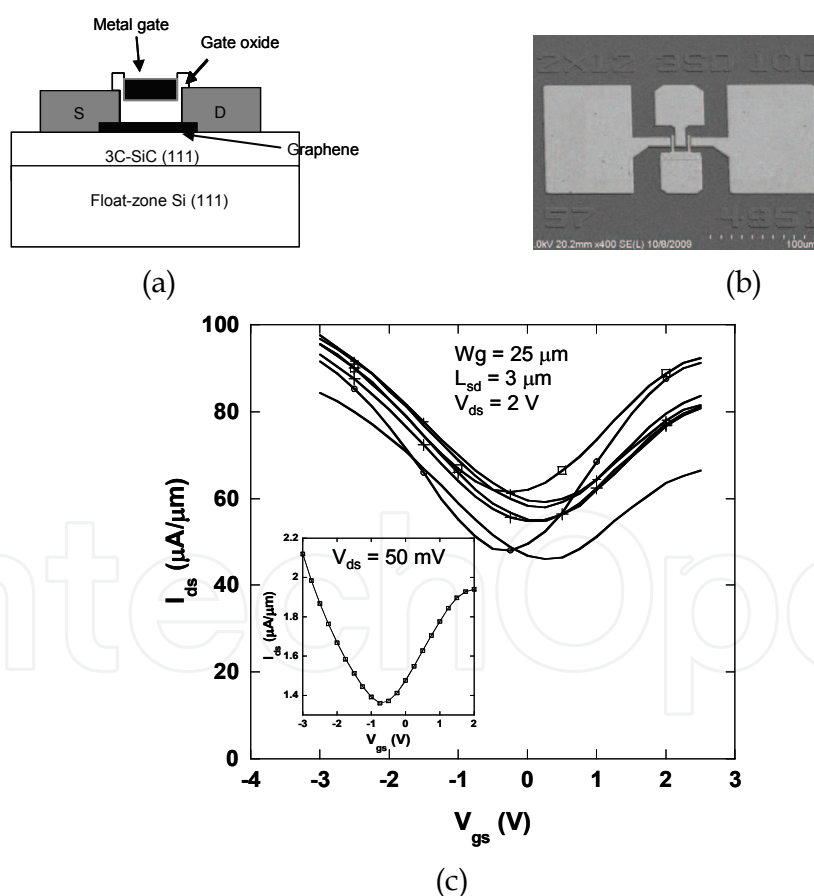


Fig. 5. (a) A schematic of the top-gated graphene FET. (b) A SEM photograph of two-gatefinger and 12- $\mu\text{m}$ -wide graphene FET (denoted as 2f x 12  $\mu\text{m}$ ). (c) Measured transfer curve of 1f x 25  $\mu\text{m}$  epitaxial graphene-on-Si FETs at  $V_{\text{ds}} = 2 \text{ V}$  with ambipolar behaviors. The  $L_{\text{sd}}$  was 3  $\mu\text{m}$ . The inset shows measured transfer curve at  $V_{\text{ds}} = 50 \text{ mV}$ .

5. RF Applications

Figure 6(a) shows measured  $|H_{21}|$  and unilateral gain (U) of the  $2 \times 12 \mu\text{m}$  graphene FETs at  $V_{ds} = 5 \text{ V}$  with source-drain spacing ( $L_{ds}$ ) of  $3 \mu\text{m}$ . The extrinsic  $f_T$  and  $f_{max}$  are 2.7 GHz and 3.4 GHz, respectively. Figure 6(b) shows measured plots of magnitude of  $H_{21}$  ( $|H_{21}|$ ) and unilateral gain (U) of the  $2 \times 12 \mu\text{m}$  graphene FETs with source-drain spacing ( $L_{ds}$ ) of  $1 \mu\text{m}$ . The S-parameters were measured at  $V_{ds} = 5 \text{ V}$  and  $V_{gs} = -2.5 \text{ V}$ . An extrinsic cut-off frequency ( $f_T$ ) of 4.1 GHz was extracted, yielding an extrinsic  $f_T \cdot L_g$  of  $8.2 \text{ GHz} \cdot \mu\text{m}$ . The extrinsic  $g_m$  was 195 mS/mm. A maximum oscillation frequency ( $f_{max}$ ) of 11.5 GHz was extracted from the unilateral gain (U) with a slope of -20 dB/decade. Figure 7 shows a plot of extrinsic  $f_T$  and  $f_{max}$  measured from both of the graphene FETs. For graphene FET #1, the extrinsic  $g_m$  improved to 148 mS/mm at  $V_{ds} = 9 \text{ V}$ , yielding the extrinsic  $f_T$  and  $f_{max}$  of 4.4 GHz and 6 GHz, respectively. For graphene FET #2, the  $f_T$  and  $f_{max}$  were 4.2 GHz and 14 GHz, respectively, at  $V_{ds} = 7 \text{ V}$ . With a source access resistance of  $1.9 \Omega \cdot \text{mm}$ , the intrinsic  $g_m$  becomes 205 mS/mm. This yields an intrinsic  $f_T$  of 5 GHz with an intrinsic  $f_T \cdot L_g$  of  $10 \text{ GHz} \cdot \mu\text{m}$ , which is slightly better than  $8.9 \text{ GHz} \cdot \mu\text{m}$  from the bulk Si NMOS. At present, the RF performance of graphene FETs is not close to what had been predicted by the intrinsic saturation velocity of the graphene channel,  $4\text{-}5 \times 10^7 \text{ cm/sec}$ . The  $f_T \cdot L_g$  product of graphene FETs is expected to improve as the quality of the epitaxial graphene layer and transistor fabrication processing improve with reduced parasitic charging delay, such as  $(R_s + R_d) \cdot C_{gd}$  [Moon et al., 2008]. The unique ambipolar nature of graphene FETs can benefit various RF circuit applications, such as frequency multipliers, mixers and high-speed radiometers. The future success of the RF circuit applications depends on vertical and lateral scaling of graphene MOSFETs to minimize parasitics and improve gate modulation efficiency in the channel.

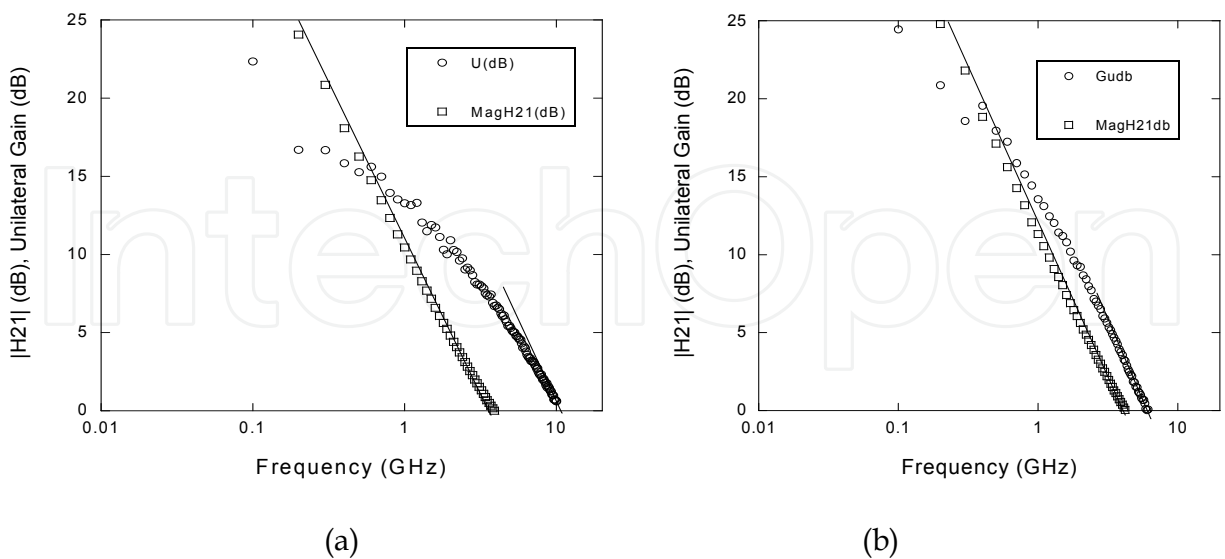


Fig. 6. Measured  $|H_{21}|$  and unilateral gain (U) are shown as a function of frequencies at  $V_{ds} = 5 \text{ V}$  and  $V_{gs} = -2.5 \text{ V}$  of  $2 \times 12 \mu\text{m}$  graphene MOSFETs with (a)  $L_{ds} = 3 \mu\text{m}$  and (b)  $L_{ds} = 1 \mu\text{m}$ .

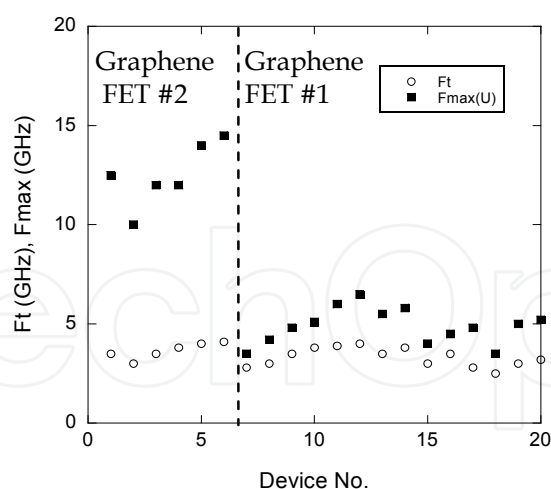


Fig. 7. A plot of measured extrinsic  $f_T$  and  $f_{max}$  of the graphene FETs is shown. The gate length is 2  $\mu\text{m}$ . The highest  $f_T$  and  $f_{max}$  are 4.1 GHz and 14 GHz, respectively.

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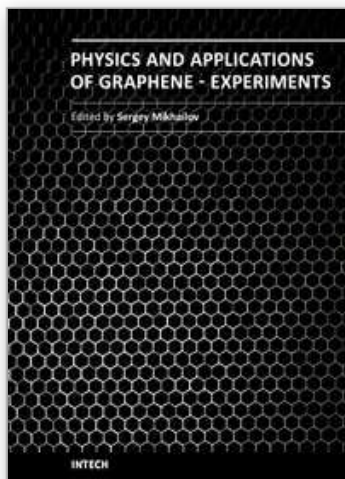
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## **Physics and Applications of Graphene - Experiments**

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The Stone Age, the Bronze Age, the Iron Age... Every global epoch in the history of the mankind is characterized by materials used in it. In 2004 a new era in material science was opened: the era of graphene or, more generally, of two-dimensional materials. Graphene is the strongest and the most stretchable known material, it has the record thermal conductivity and the very high mobility of charge carriers. It demonstrates many interesting fundamental physical effects and promises a lot of applications, among which are conductive ink, terahertz transistors, ultrafast photodetectors and bendable touch screens. In 2010 Andre Geim and Konstantin Novoselov were awarded the Nobel Prize in Physics "for groundbreaking experiments regarding the two-dimensional material graphene". The two volumes *Physics and Applications of Graphene - Experiments* and *Physics and Applications of Graphene - Theory* contain a collection of research articles reporting on different aspects of experimental and theoretical studies of this new material.

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