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Design of CMOS Integrated Q-enhanced RF Filters for Multi-Band/Mode Wireless Applications

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Section I: Wideband reconfigurable CMOS Gm-C filter for wireless applications

1. Introduction

Recent developments in portable applications and systems have lead to a significant in wireless standards. Therefore, cost efficiency of CMOS technology implementation has been greatly enhanced with the emergence of multi-mode wireless applications. Now multi-mode/multi-band receivers are designed based on the scheme of reuse^{[1]-[3]}. They avoid using multiple chipsets and can be made tunable which makes them more efficient in term of area and power consumptions. In a flexible receiver front-end, analog baseband filtering is a key task as it is used to select the required information under desired channel bandwidth. A large tuning range of the band-pass filter should be required for various wireless applications.

To meet different specifications for the desired channel in multimode receivers, there has been a tremendous amount of research [1-6] effort aimed at improving the performance of integrated reconfigurable continuous-time (CT) filters in recent years. However, due to the open-loop operation nature, Gm-C filters generally use operational transconductance amplifier (OTA) driving a capacitor load at the cost of moderate linearity, sensitivity to parasitics. Moreover, the major disadvantage of OTA is the large distortion caused by the nonlinear behavior of the transistors involved. To enhance the linearity of the OTA and avoid potential stability problems, an approach to linear Gm-C integrators with inherent CMFB is developed based on the techniques of the cross-coupled differential pairs and source degeneration with passive resistors. In Section 2, the high linear transconductor Gm is presented. The design of the Chebyshev bandpass filter is discussed, as such the simulated results of the bandpass filter are given in Section 3. The conclusion is given in Section 4.

2. The linearized techniques of transconductors

The transconductor in CMOS process is required for wideband reconfigurable Gm-C filter. Thus, the following section discusses the reported basic linearity technique in CMOS

process. The transconductor linearity techniques can be broadly classified into three types: (a) source degeneration (b) cross coupling (c) active biasing.

2.1 Source degeneration

Figure 1 shows circuit implementation of the source degeneration technology. The feedback equivalent resistance R (or $M3, M4$) is called source degeneration resistor, and differential pair $M1, M2$ and source degeneration resistors consist of the structure of source degeneration. The output current of the structure is related to the input voltage by the following equation

$$I_O = I_{D1} - I_{D2} = (V_d - I_O R) \sqrt{2KI_{SS}} \sqrt{1 - \frac{K(V_d - I_O R)^2}{2I_{SS}}} \quad (2.1)$$

Where $K = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L}$, I_{SS} is tail current source of the transconductor as shown in Figure 1, and the nonlinearity term of (2.2) is $V_d - I_O R$.

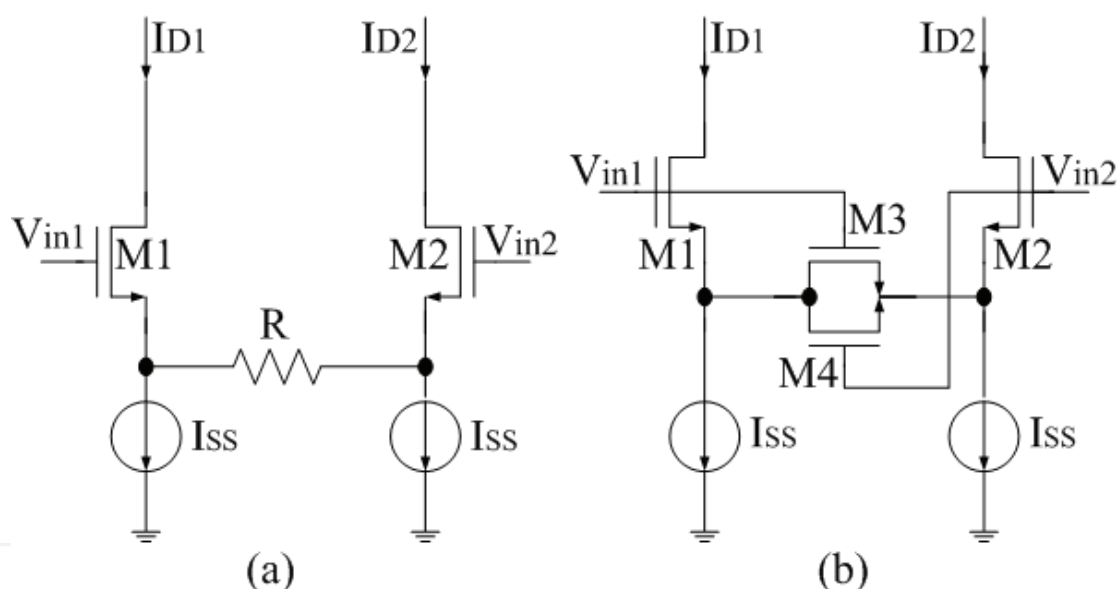


Fig. 1. The typical source-degeneration structure of transconductor

The transconductance G_m of source-degeneration structure can be about expressed as

$$G_m \approx \frac{g_m}{1 + g_m R} \quad (2.2)$$

When the resistance is much greater than $1/g_m$, the transconductance $G_m \approx 1/R$. However, this is traded-off with the noise and power consumption. In CMOS process, high quality passive resistance is achieved difficultly.

2.2 Cross coupling

A simple differential pair can cancel out the even order harmonics of distortion of transconductor output current. The remaining odd order harmonics can be cancelled out by

two cross-coupling differential pairs with the same distortion but with different gm values. The circuit is shown in Figure 2.

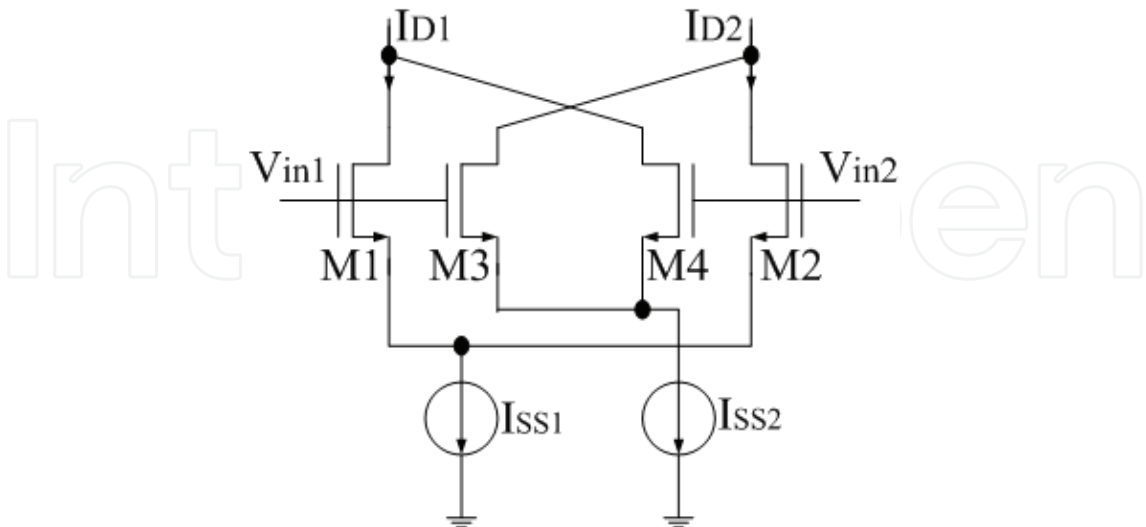


Fig. 2. The transconductor with differential cross-coupled pairs

The 3rd order harmonic is the main concern since it is now the most significant distortion. From Eq. (2-3), the 3rd order harmonic distortion (HD3) of output current can be obtained as:

$$HD_3 = \frac{K^{3/2}}{2\sqrt{2}I_{SS}} V_d^3 \tag{2.3}$$

Since HD3 depends on the ratio of $K^{3/2}$ and $I_{SS}^{1/2}$ only, the distortion can be cancelled by connecting two differential pairs M1, M2 in parallel with M3, M4 as shown in Figure 2. The transconductor parameter $K_{3,4}$ and $K_{1,2}$ are related to I_{SS2} and I_{SS1} as follows:

$$\left(\frac{K_{3,4}}{K_{1,2}}\right)^3 = \left(\frac{(W/L)_{3,4}}{(W/L)_{1,2}}\right)^3 = \frac{I_{SS2}}{I_{SS1}} \tag{2.4}$$

The corresponding effective gm is then given by:

$$g_{meff} = g_{m1,2} \left[1 - \left(\frac{K_{3,4}}{K_{1,2}}\right)^2\right] I = g_{m1,2} \left[1 - \left(\frac{I_{SS2}}{I_{SS1}}\right)^{2/3}\right] I \tag{2.5}$$

According to equation (2.5), when $I_{SS2} \ll I_{SS1}$, the transconductance is approximated as linearity. But the noise performance is worse than that of a simple differential pair because 2 differential pairs are connected. However, the noise is not doubled because $K_{3,4} < K_{1,2}$.

2.3 Active biasing

The idea of active biasing is to make the biasing current compensate for the non-linear term:

$$I_{SS} = I_{DC} + \frac{KV_d^2}{2} \tag{2.6}$$

Where I_{DC} is the DC bias current, and V_d is input differential signal. Now the bias I_{SS} supplies I_{DC} when $V_d = 0$ for the static bias. When there is a signal, an additional bias current $KV_d/2$ will compensate for the drop of the gm. This can be verified by inserting the new I_{SS} into Eq. (2.7):

$$I_{D1} + I_{D2} = 2K(V_{gs} - V_{th})^2 \quad (2.7)$$

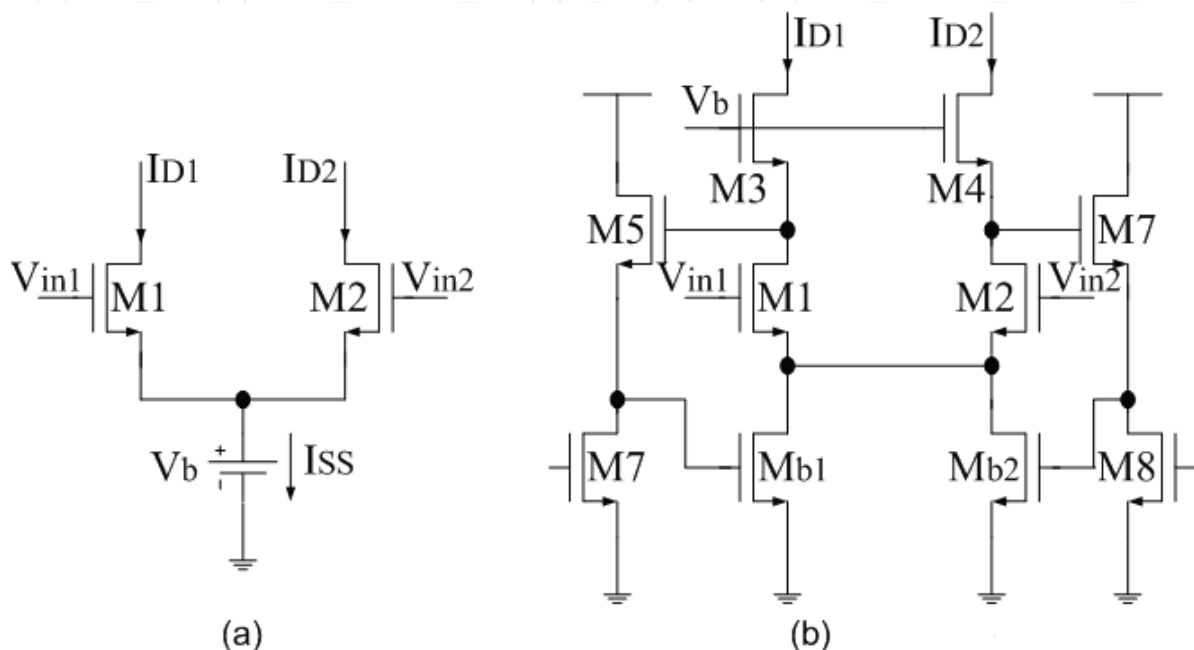


Fig. 3. The transconductor with active-biasing differential pair

In this design, all transistors are matched except M5-M8. For this cascode circuit, when there is an input signal, the same amplitude appears at the drains of M1 and M2 because the loading is $1/gm_{3,4}$ and $gm_{3,4}=gm_{1,2}$. The capacitance at that node and the loss of the level shifter M5-M8 are ignored. Both gates of M_{b1} and M_{b2} sense the differential voltage. Because the drains of M_{b1} and M_{b2} are connected together, a bias current is obtained as in Eqs. (2-26). The required active biasing is then established. But in the common-mode sense, now the conductance of M_{b1} and M_{b2} increases in phase with the input signal. This is a kind of feed-forward and thus causes a boost-up of the common-mode gain. As a result, CMRR drops and common-mode instability will be resulted.

2.4 The design of high linear transconductor

The OTA is based on the Gilbert multiplier, which uses the two cross-coupled differential pairs (M1 - M2, M3-M4) as the input stage to reduce the nonlinearities as shown in Figure 6. Thank to mismatching of passive resistor in CMOS process, active source-degeneration resistor M_{R1} and M_{R2} is perfect choice. For this OTA structure, all transistors operate in the saturation region except for the transistors M_{R1} and M_{R2} . The MOS transistor is approximated as

$$\frac{1}{R_{eq}} \approx K_R(V_R - V_{th} - V_{CMS}) \quad (2.8)$$

Where K_R is relative to MOS process parameter, $V_{R1, 2}$ is control voltage of source degeneration resistor, and V_{CMS} is common-mode voltage of tail current source. The output current of the transconductance is

$$\begin{aligned} I_O &= I_{O1} - I_{O2} = (I_{d1} - I_{d3}) - (I_{d2} - I_{d4}) = (I_{d1} + I_{d4}) - (I_{d2} + I_{d3}) \\ &= \sqrt{2K_{DC1}} V_d \sqrt{1 - \left(\frac{V_d}{2V_{dsat1}} \right)^2} - \sqrt{2K_{DC2}} V_d \sqrt{1 - \left(\frac{V_d}{2V_{dsat2}} \right)^2} \end{aligned} \quad (2.9)$$

Where V_d is input differential voltage, I_{DC1} , I_{DC2} is drain terminal current M_{b1} - M_{b4} respectively. V_{dsat1} , V_{dsat2} is source-drain overdrive voltage M_{b1} - M_{b4} respectively. Expanding (2.9) in the Taylor series and considering the first three terms only, the even terms for differential is neglected, and (2.10) becomes

$$I_O = I_{O1} - I_{O2} \approx (g_{m1} - g_{m2})V_d - \frac{1}{8} \left(\frac{g_{m1}}{V_{dsat1}^2} - \frac{g_{m2}}{V_{dsat2}^2} \right) V_d^3 \quad (2.10)$$

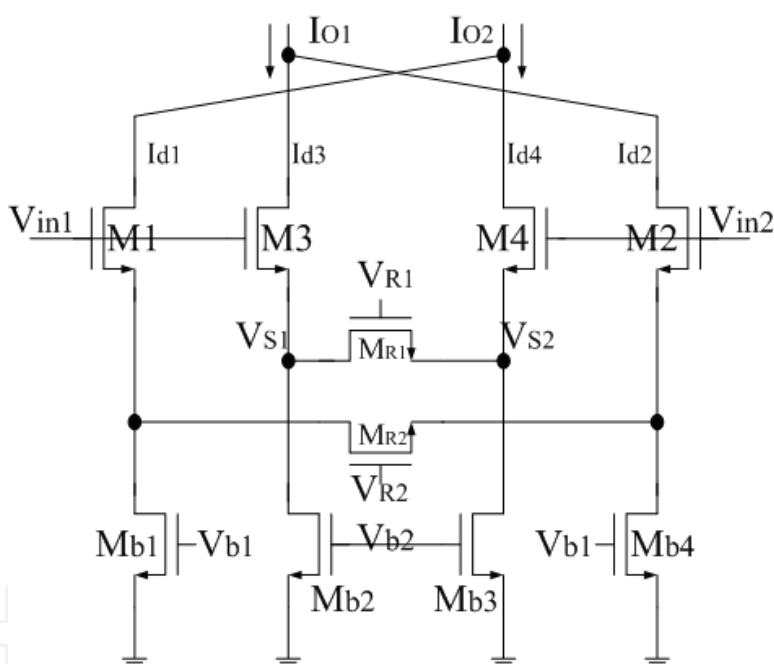


Fig. 4. The Gilbert OTA with source degeneration

Taking into account the mobility degradation, equation (2.10) is expressed as

$$\begin{aligned} I_O &= I_{O1} - I_{O2} \approx \left(\frac{g_{m1}}{1 + g_{m1}R'_1} - \frac{g_{m2}}{1 + g_{m2}R'_2} \right) V_d \\ &\quad - \frac{1}{8} \left(\frac{g_{m1}}{V_{dsat1}^2 (1 + g_{m1}R'_1)^3} - \frac{g_{m2}}{V_{dsat2}^2 (1 + g_{m2}R'_2)^3} \right) V_d^3 \end{aligned} \quad (2.11)$$

where $R'_1 = R_1 + R_{\theta1}$, $R'_2 = R_2 + R_{\theta2}$, $R_{\theta1}$, $R_{\theta2}$ are source series resistance of the mobility degradation, $R_{\theta} = \frac{2\theta}{K}$, and θ is the mobility reduction coefficient.

In equation (2.11), if the nonlinearity third-order term satisfies

$$\frac{g_{m1}}{V_{dsat1}^2(1+g_{m1}R_1')^3} - \frac{g_{m2}}{V_{dsat2}^2(1+g_{m2}R_2')^3} = 0 \tag{2.12}$$

Then the transconductance is expressed as

$$G_m = \frac{g_{m1}}{1+g_{m1}R_1'} - \frac{g_{m2}}{1+g_{m2}R_2'} \tag{2.13}$$

If the condition $R \gg 1/g_m$ is satisfied, the transconductance can be obtained by

$$G_m \approx \frac{1}{R_1'} - \frac{1}{R_2'} \tag{2.14}$$

Figure 5 is overall structure of the high linear transconductor. Figure 6 shows the simulation of step response of the transconductance. When the dc common-mode voltage is about 1.67V, the transient-time response is less than 60ns, and the variation of common-mode voltage is less than 15mV. We use 5pF as the loading capacitance to verify the AC response of the transconductor. The bandwidth of unit gain is about 98MHz, and the phase margin is about 76 degree as shown in Figure 7.

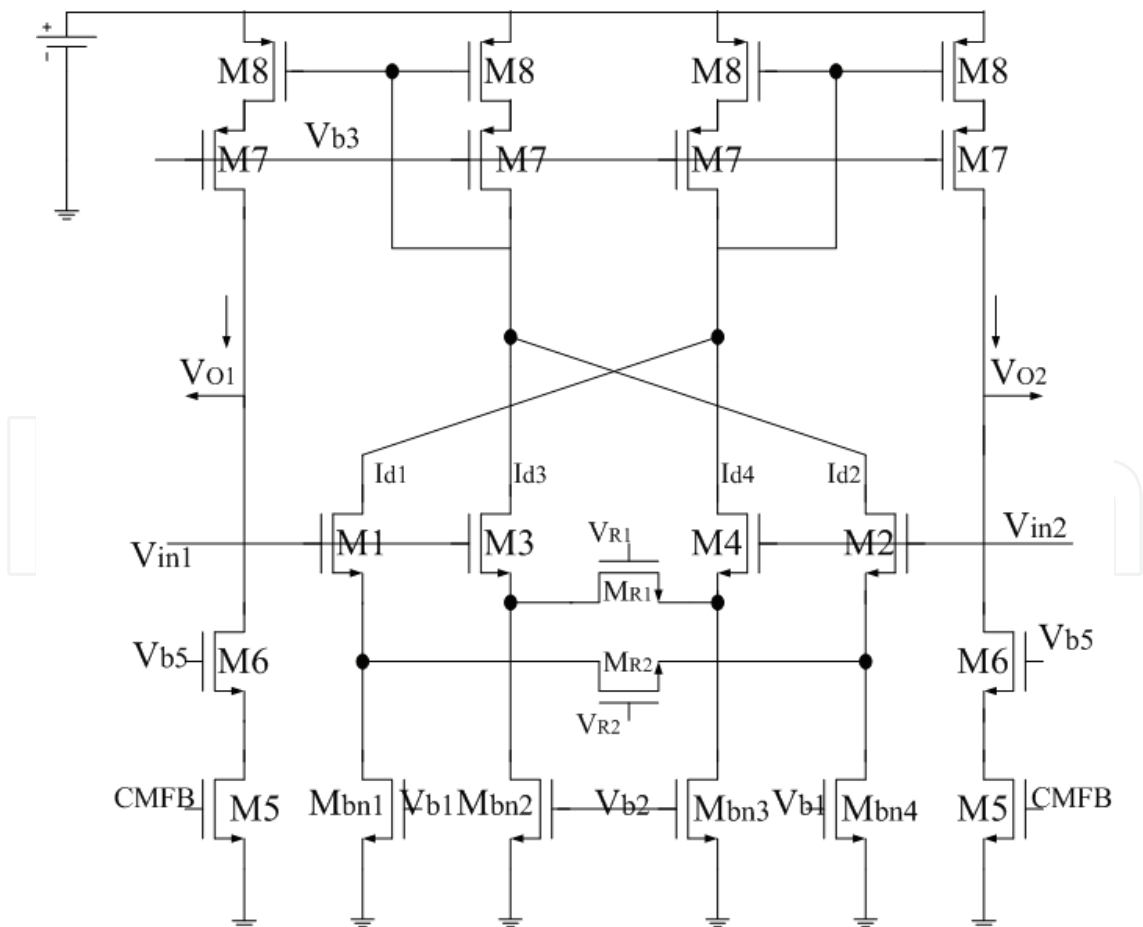


Fig. 5. The overall structure of high linear transconductor

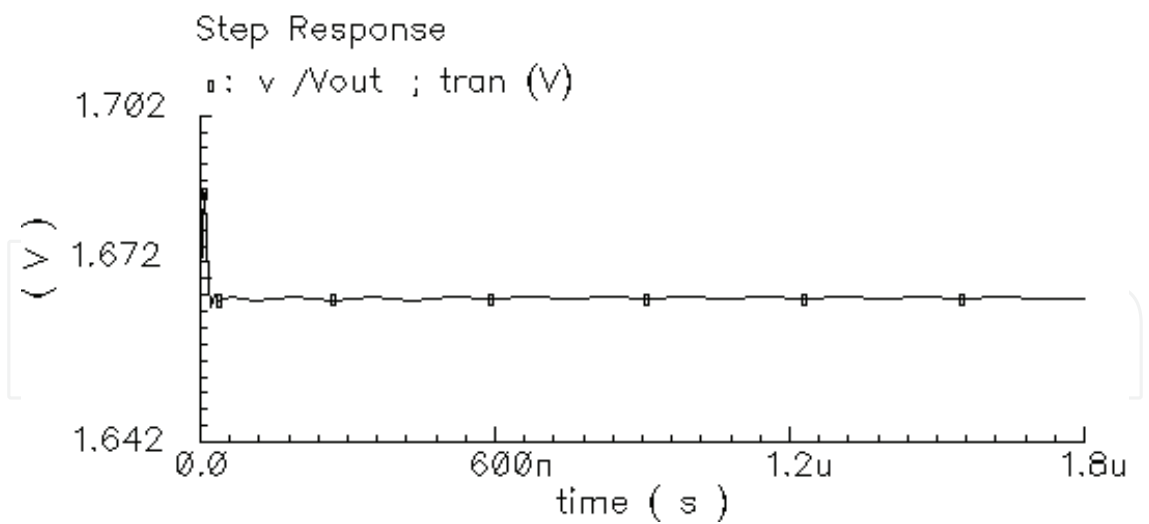


Fig. 6. Step response of the proposed transconductor

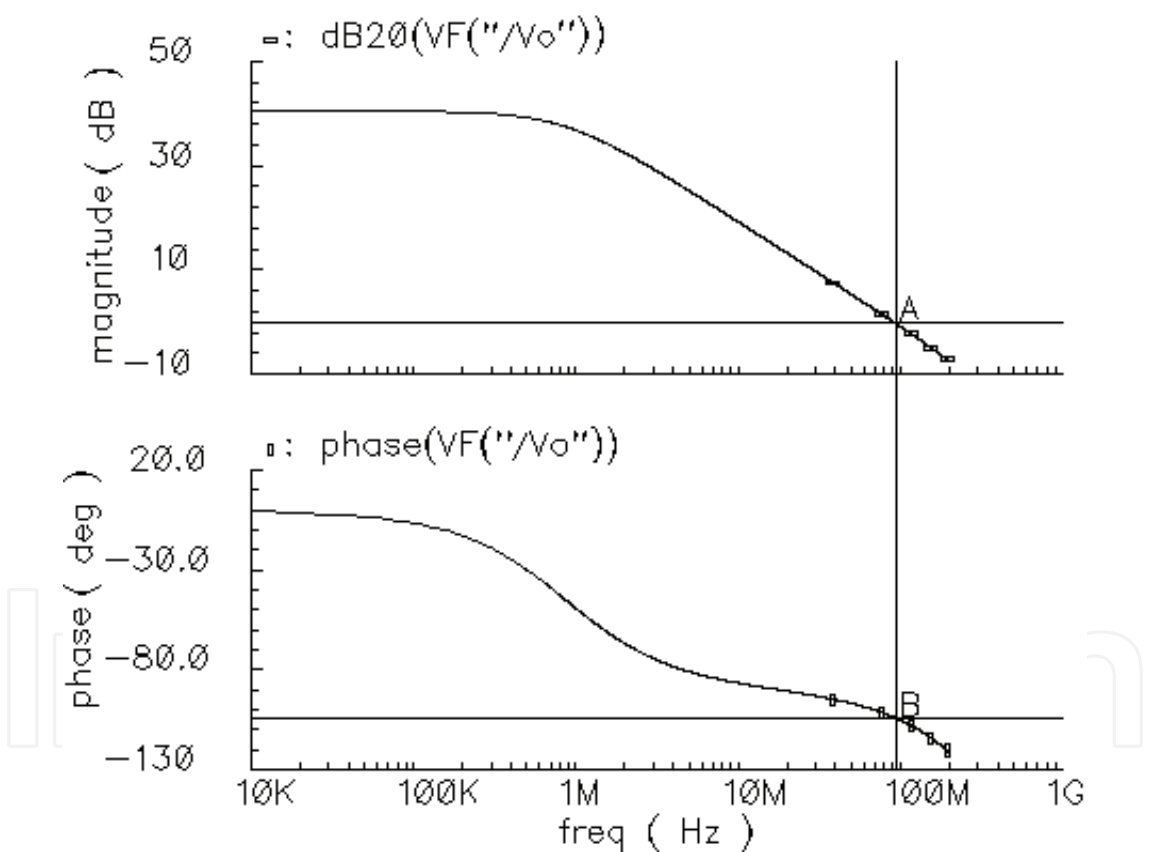


Fig. 7. The response of amplitude and phase for the transconductor

Figure 8 shows the simulated G_m plot with the input voltage. The linear range of the proposed active degenerative resistance (ADR) G_m of cross-couple differential pair is about $\pm 1V$. The linear range is higher than the other G_m of differential cross-coupled pair without ADR and differential pair with ADR (source degeneration structure as shown in Figure 2). When the operating frequency is 4MHz, the third-order intermodulation IM3 is -72dB as shown in Figure 9.

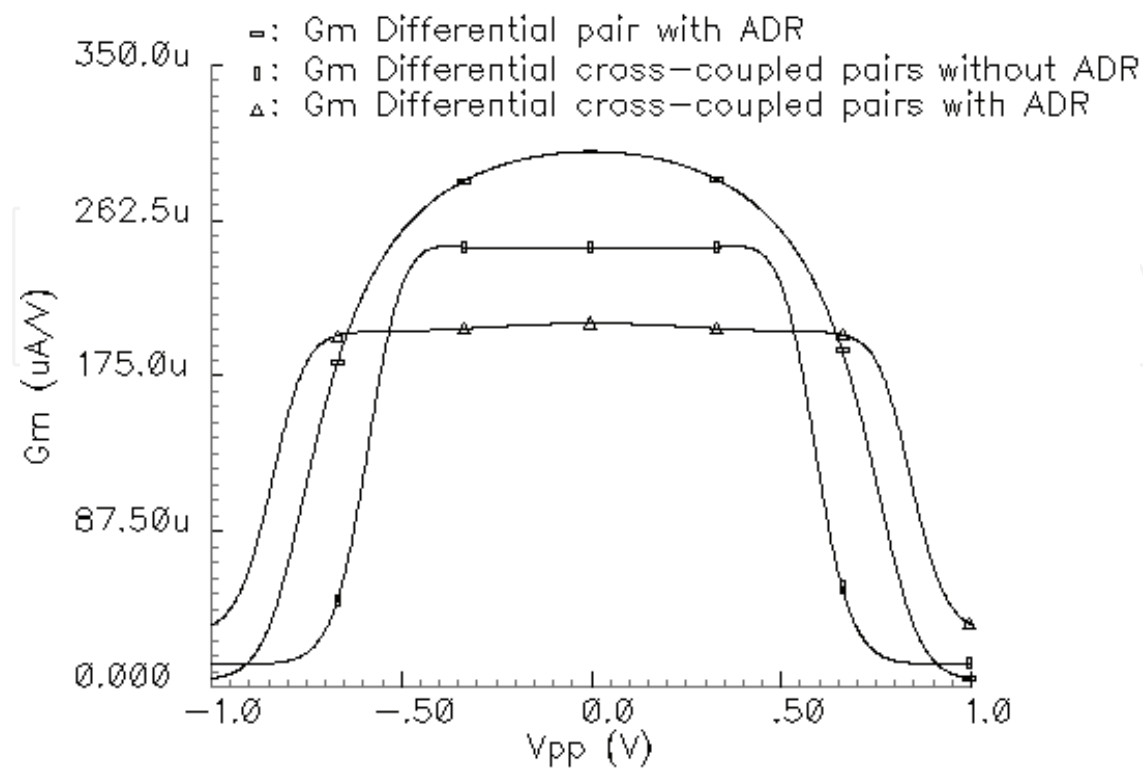


Fig. 8. Simulation of linearity for the three differential linearized transconductor

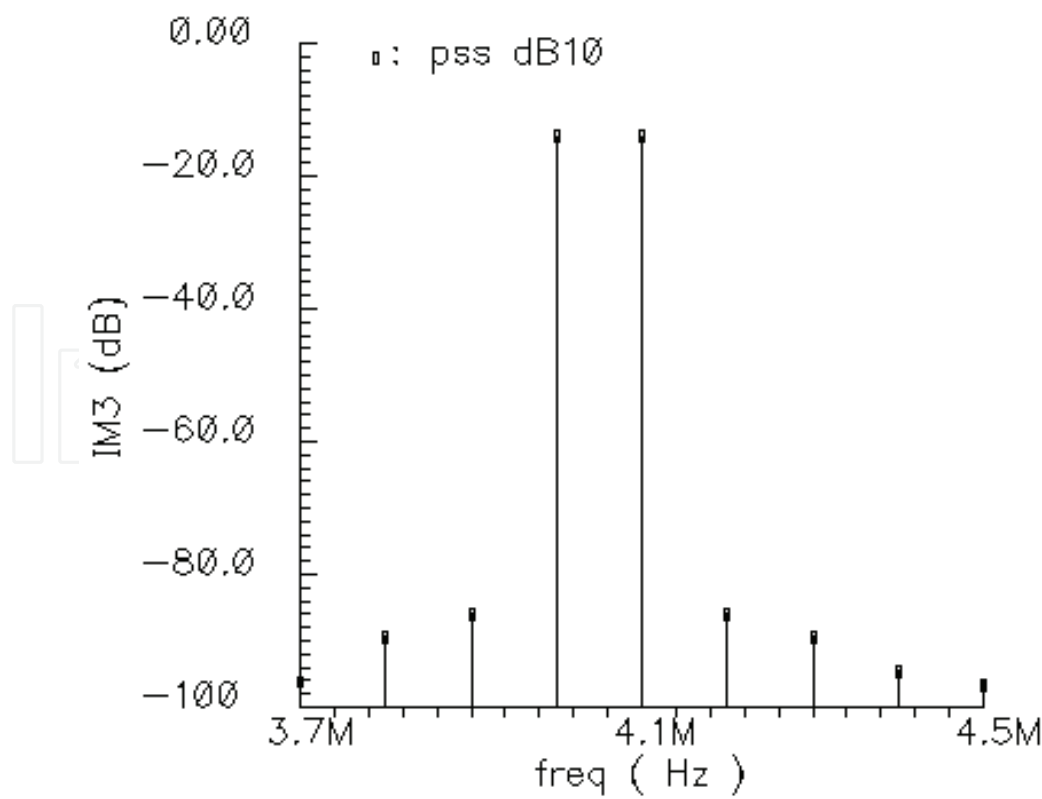


Fig. 9. Response of third-order intermodulation distortion of the OTA at 4MHz

3. Circuit design of Gm-C filter

Using the proposed high linear OTA, a six-order Chebyshev bandpass filter is designed. To obtain a passband frequency with minimal sensitivities to individual component values, the filter topology is derived from a doubly terminated passive RLC lowpass prototype as shown in Figure 10. The associated signal flow graph (SFG), shown in Figure 11 is obtained by writing down the state equations for six reactive components. Notice that the SFG contains only integrators and summers. The bandpass filter topology is derived by applying the well-known lowpass to bandpass transformation

$$S_L = \frac{s^2 + \omega_0^2}{s\omega_c}$$

(2.15)

Where S_L is the normalized lowpass Laplace variable, ω_0 is the center frequency, and ω_c is the bandwidth of the bandpass filter to be designed.

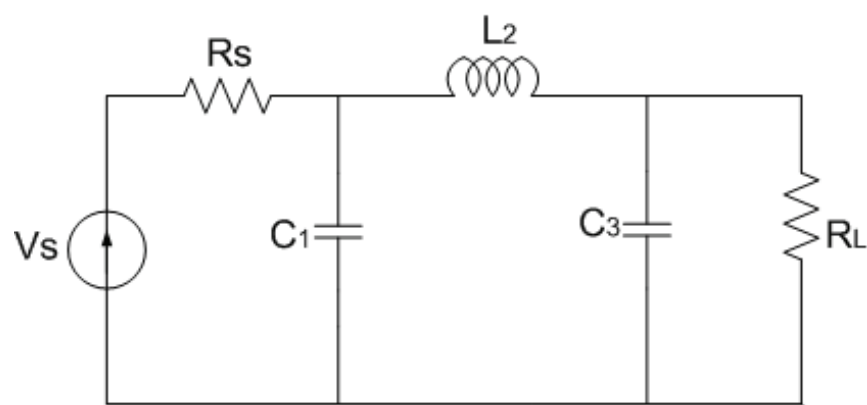


Fig. 10. The passive RLC lowpass prototype of low-pass filter

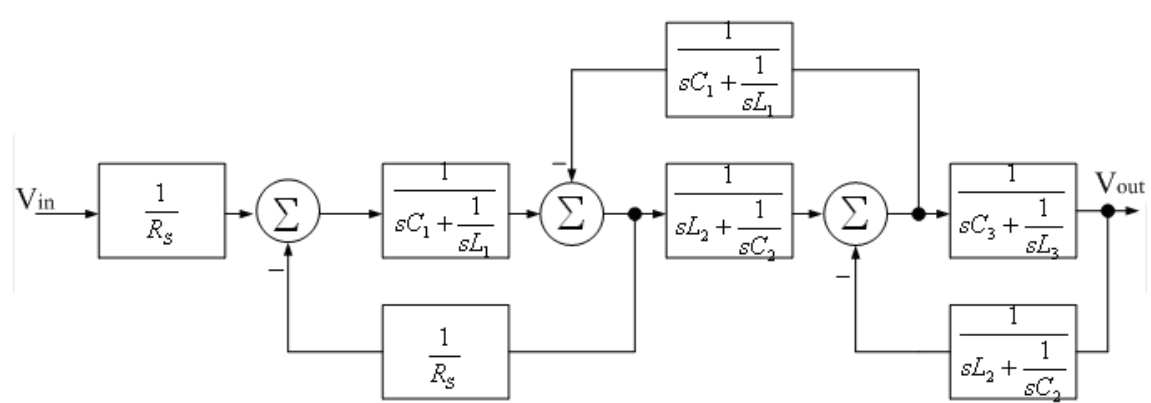


Fig. 11. The signal flow of the transfer function from passive low-pass filter to bandpass filter

The design method is based on component substitution. A ground inductor produces two transconductors and one capacitor, while a floating inductor need four transconductors and one capacitor as shown in Figure 12(a),(b). Figure 12(c) shows the use of a differential transconductor connected as a pseudo-resistor. The bandpass filter topology is obtained by replacing six integrators with six coupled resonators.

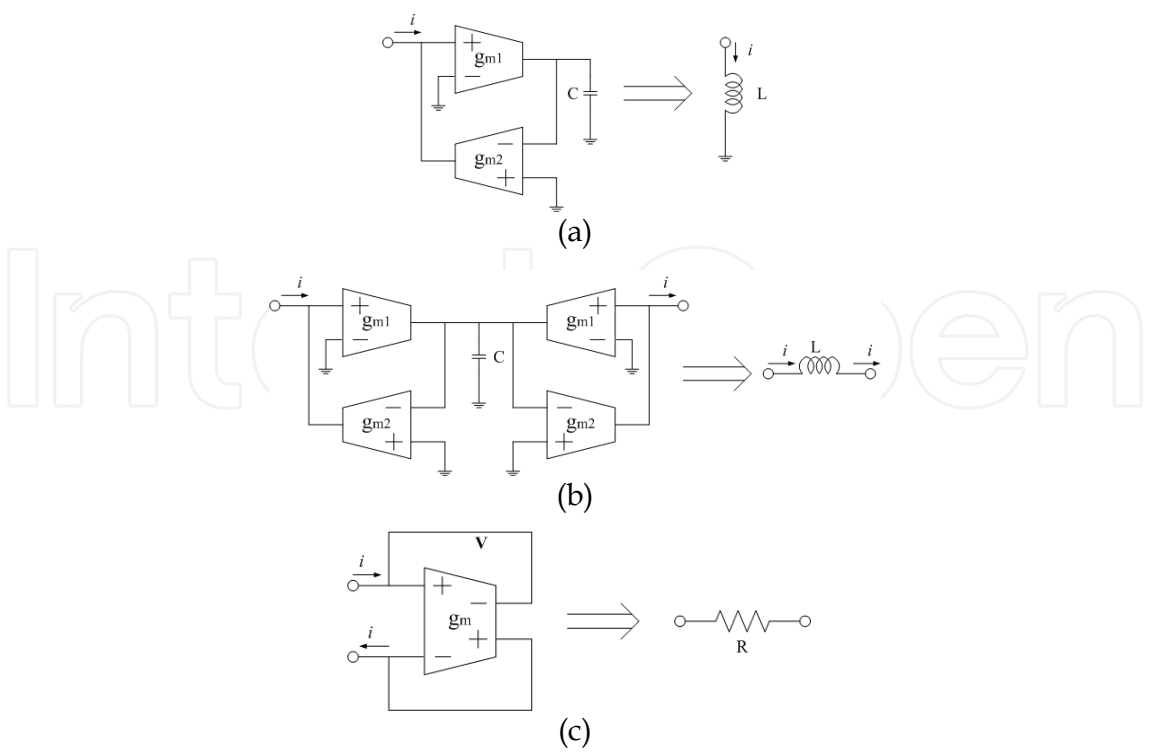


Fig. 12. Methods of passive component substitution

The complete filter is shown in Figure 13. The resonator is composed of two Gm-C integrators with feedback loop.

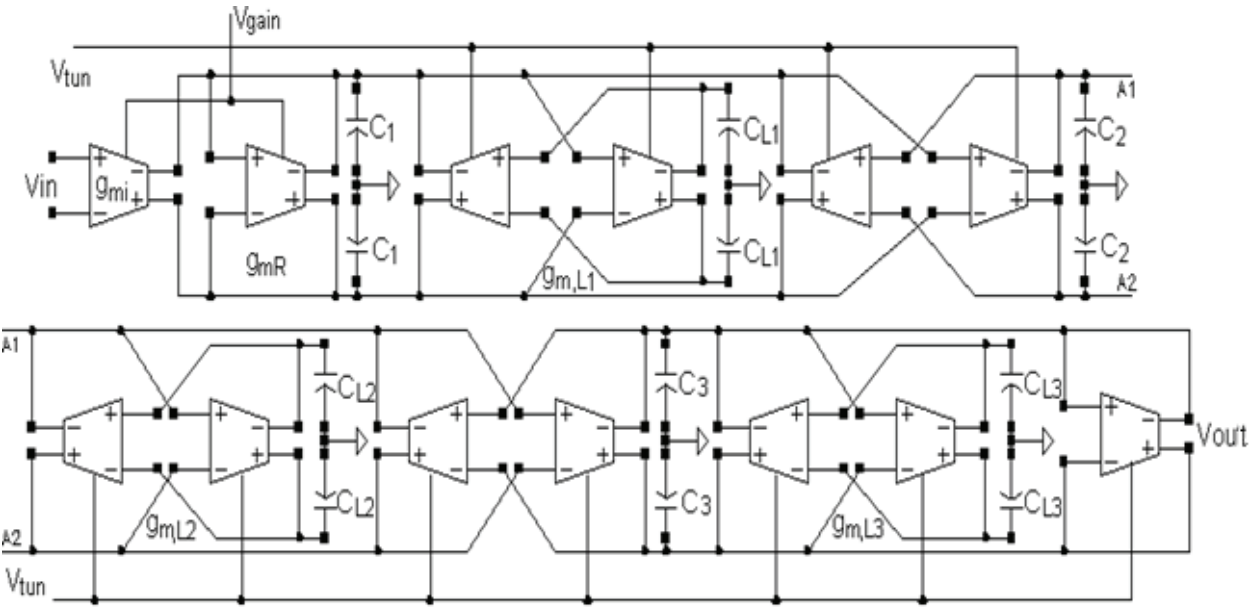


Fig. 13. The sixth-order Chebyshev OTA-C bandpass filter

The proposed filter is simulated with Cadence's Spectre softwares using TSMC 0.25um standard CMOS process models. Simulation results in Figure 14 and Figure 15. Figure 13 shows the AC tuning-Q response of the filter when the tuning center frequency is about 2MHz. The center frequency tuning range is about 0.5MHz to 10MHz as shown in Figure 14.

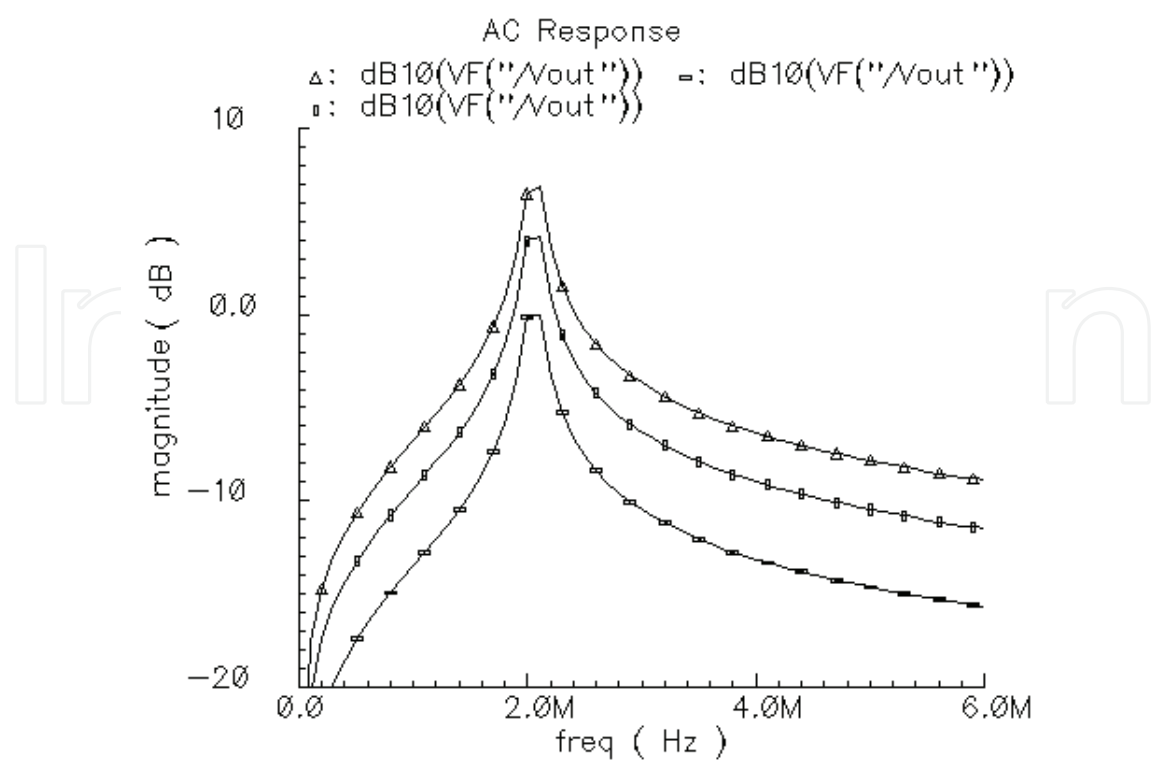


Fig. 14. The tuning-Q response of the Gm-C bandpass filter at $f_c \approx 2\text{MHz}$

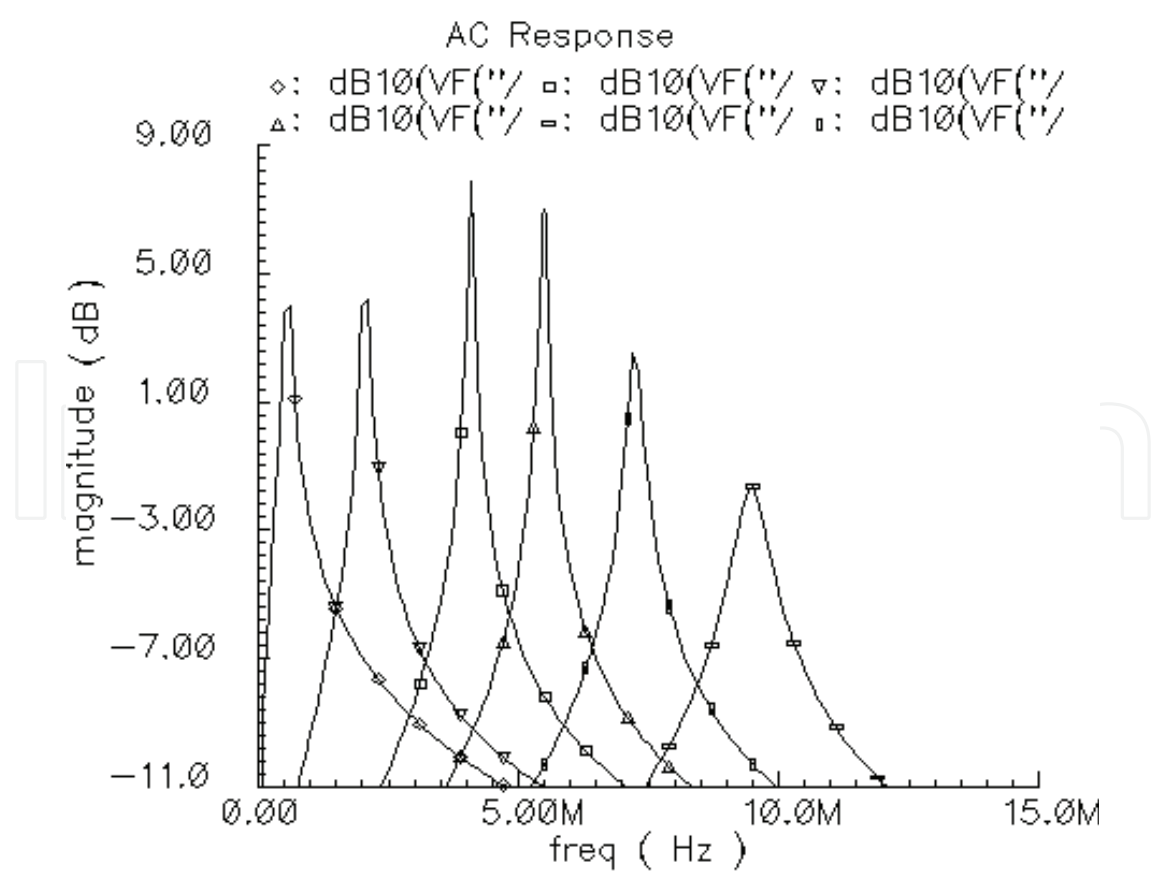


Fig. 15. Tuning center frequency of the OTA-C bandpass filter

4. Conclusion

A full CMOS six-order Gm-C Chebyshev filter based on passive LC-ladder synthesis is designed in TSMC standard 0.25 μ m CMOS process, which uses a highly linear operational transconductance amplifier (OTA) based on cross-coupled differential pairs with source-degeneration structure, which exhibits a wide product of gain-bandwidth, and high linearity. The simulated results show the center frequency tuning range of the filter is from about 0.5MHz to 10MHz and the maximum quality factor of 150 at the center frequency 4.3MHz. The filter is suitable for multi-band wireless applications.

5. References

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Section II: A RF LC Q-enhanced CMOS filter for wireless receivers

1. Introduction

Despite decades of research in developing “single-chip” radio transceivers, most designs continue to rely on off-chip components for RF bandpass filtering. Implementing these filters on-chip remains nearly as challenging today due to problems in meeting system requirements. Recent advances in silicon-on-chip IC processes targeted at RF designs, however, offer the possibility of producing on-chip filters in the coming years using Q-enhancement techniques.

CMOS technology is an attractive solution due to the low cost, high-level integration. One of prevalent off-chip component required in wireless receiver circuits is RF bandpass filter, usually realized with a surface acoustic wave (SAW) or ceramic device. If on-chip high frequency filters with acceptable electrical characteristics can be realized, this would eliminate or reduce the need for these currently required off-chip filters. This implementation of integrated filters could lead to complete communications system design solutions on monolithic chip that would decrease the complexity, reduce the size, lower the power and cost of wireless transceiver circuits. However, the use of on-chip RF bandpass filters in commercial radio transceivers has been limited so far by inferior performance relative to system requirements. Such requirements include: narrow bandwidths, high linearity, low insertion and noise figure, and the need for low-power consumption in

wireless system of aerospace applications. This fact has made the acceptance of on-chip designs much more difficult than it would be if the system specifications were more relaxed, pushing radio designers to embrace modified, and generally problematic, radio architectures such as the direct-conversion, or zero-IF schemes. If on-chip bandpass filters are accepted into commercial products, they must at least compete with the performance of products designed around these architectures.

In this section, we outline the alternatives for building on-chip bandpass filters practical considerations in section 2. The design of the integrated on-chip 1.8V 2.14GHz Q-enhanced LC filter using silicon CMOS process is presented in section 3. The simulated results of the filter presented are provided in section 4. Finally in section 5, conclusion is drawn.

2. Filter technology

A wide range of technologies exists for implementing RF bandpass filters, as illustrated in Figure 16.

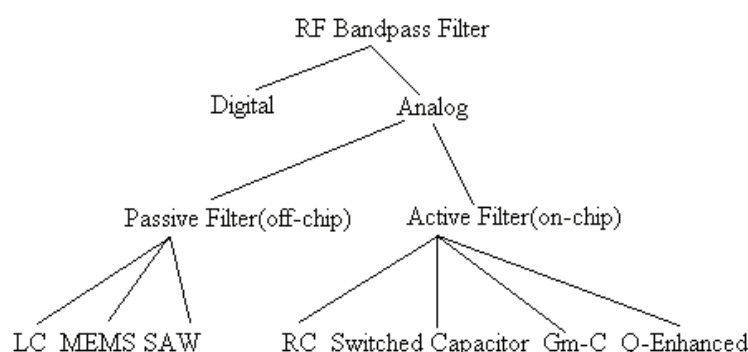


Fig. 16. Taxonomy of RF bandpass filter implementations

In theory, digital filters could implement any filter desired, and achieve true “software-radio” realizations. However, their applications are still generally limited to baseband frequency due to problems with power consumption and noise at high frequencies. To illustrate these problems, bounds on power consumption were developed in based on CV^2f considerations, because the scale of the digital filter has at least thousands of transistors and each of the transistors is considered as source of the noise. If the digital filter is operated at RF band, the power consumption and noise of the filter is large enough to beyond imagination.

Currently, however, on-chip RF bandpass filtering remains an analog endeavor. Here, the choices involve passive or active designs, each with several implementation possibilities including LC, and fully active architectures. In these active architectures, RC filter and switched capacitor filter isn’t suited for high frequencies application. Although Gm-C filter can be operated at high frequencies, it poses its own drawbacks, namely, large power consumption and high noise contribution. A promising solution is to implement a active LC filter using on-chip passive elements with loss compensation circuitry to improve the effective quality factor [1, 3-7, 10].

3. Q-enhanced filter design

3.1 On-chip spiral inductor

The design and characterization of on-chip inductors is central to the implementation of high performance Q-enhanced LC filters. In a typical two-metal silicon IC process, these

inductors are fabricated using planar spiral geometries as illustrated in Fig. 17. Top layer metallization usually provides the lowest resistivity and capacitance to the underlying substrate and is therefore used for the spiral turns, while the lower metallization layer is used for connection to the spiral center.

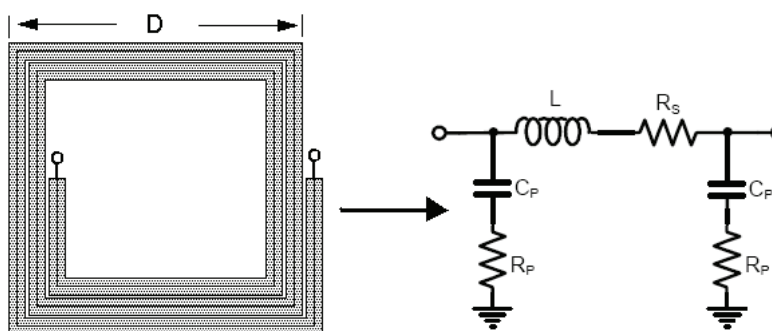


Fig. 17. Top view of an on-chip spiral inductor and its electrical model

In practice, electrical characteristics of the integrated inductor are generally frequency dependent and are more precisely described with a lumped-element model of greater complexity. A commonly used square-spiral IC layout and a more accurate electrical model for the inductor, the π -model, are shown in Figure 2. In this model, R_s represents the resistive losses in the metal traces of the inductor, any contact losses, and losses attributable to eddy currents in the substrate. Note that the top branch of Figure 2, which is composed of series resistor R_s , along with the inductance L represents the simplified series resistance model for the inductor shown in Figure 2. The substrate capacitance is modeled by C_p , and R_p represents loss caused by substrate conductance. With the help of a patterned ground shield, the electric field from the lossy substrate [3][10]. Thus, the only dominant loss due to the serious resistance R_s , and to cancel it, it is necessary to implement a loss compensation mechanism that effectively introduces a negative resistance of the same magnitude in series with R_s .

3.2 Q enhancement

A primary method for increasing the Q of non-ideal on-chip resonators is through the use of active devices to create negative resistance. Although methods that include phase-shifted current feedback via coupled inductors [21] have been investigated, the direct use of active devices as negative resistors is the prevalent Q enhancement technique. Single-ended negative resistance methods have been documented [23-25], while the more common differential method using a cross-coupled transistor pair is presented in Figure 18. The voltage to current ratio indicates the effective negative resistance at the terminals of the cross-coupled MOSFET shown in the figure and is described by

$$R = -\frac{2}{g_{mQ}} \quad (2.16)$$

It is clear from Figure 18 and Equation (2.16) that the effective negative resistance can be adjusted by changing the bias source, I_Q , and thereby the transconductance, g_{mQ} , of the differential pair MQ1, MQ2. This facilitates electronic tuning of this loss-canceling mechanism.

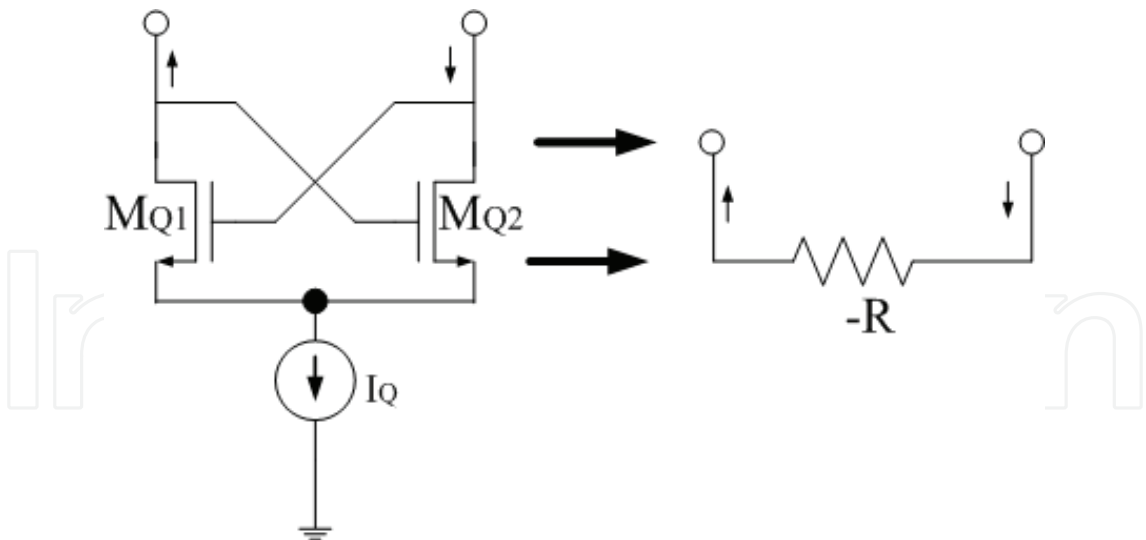


Fig. 18. Cross-coupled MOSFET negative transconductance

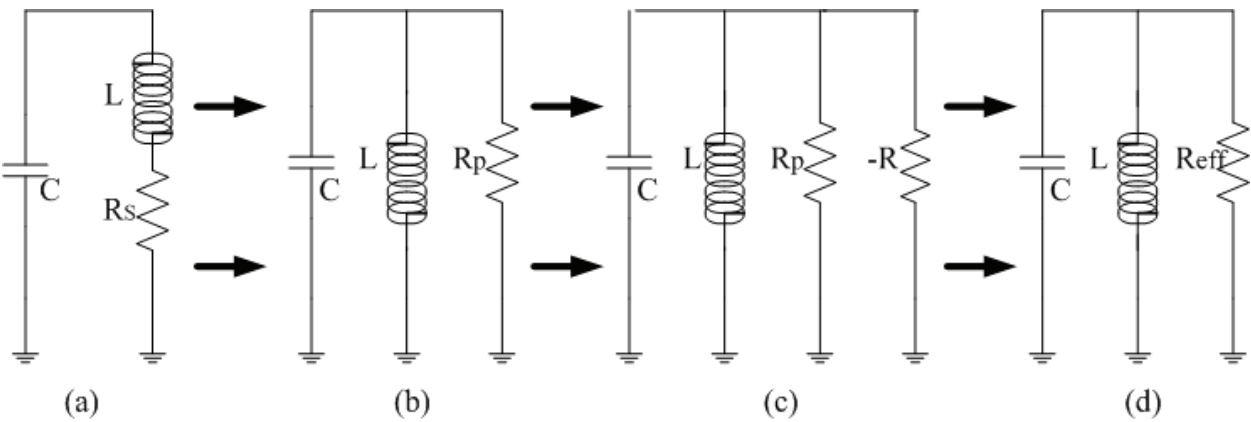


Fig. 19. Q-enhanced LC circuit

The concept of Q-enhancement for an LC tank circuit with parallel-connected negative resistance is illustrated in Figure 18-19, with the series resistance inductor model utilized to simplify the analysis. We assume for now that a lossy inductor and a capacitor can be simplistically modeled as shown in Figure 19(a), in which R_s represent the losses in the inductor. We can compensate the losses by connecting negative resistor in parallel with the LC tank as shown in Figure 19(c). In this approach, the negative resistance has been implemented negative resistance $-R$ as shown in Figure 17 to cancel the loss represented by R_p . The effective parallel resistance R_{eff} and the effective quality factor Q_{enh} of the LC resonator as shown in Figure 19(d) is given by

$$R_{eff} = R_p \parallel \frac{-1}{g_m} = \frac{1}{1 - g_m R_p} R_p$$

(2.17)

and

$$Q_{enh} = \frac{R_{eq}}{X_L} = \frac{1}{1 - g_m R_p} Q_0$$

(2.18)

Where Q_0 is the self-tuning quality factor of the circuit as illustrated in Figure 19(a). It should be noted that as $g_m R_p$ continues to increase and approaches the unit, the value of Q_{enh} is infinite and the circuit (theoretically and practically) become an oscillator.

The prototype circuit of the second-order RF Q-enhanced bandpass filter based on the above negative-resistance techniques is shown in figure 20. Common-source transistor M1 and M2 are employed for the input buffer stage. They are large devices and biased to have low-input impedance and small distortion. Two pair of PMOS transistors M_C are varactors which are used to tune the center frequency of the filter and also adjust the quality factor of the filter through DC voltage V_{con} . The PMOS M_C capacitors are operated in depletion and inversion regions within the tuning range. The negative-resistance circuit can be realized by cross-coupled differential pair M_{Q1} and M_{Q2} . The negative resistance is $-2/g_m$ if we assume that the two transistors have the same size. As such, the negative resistance can be adjusted by current source I_Q .

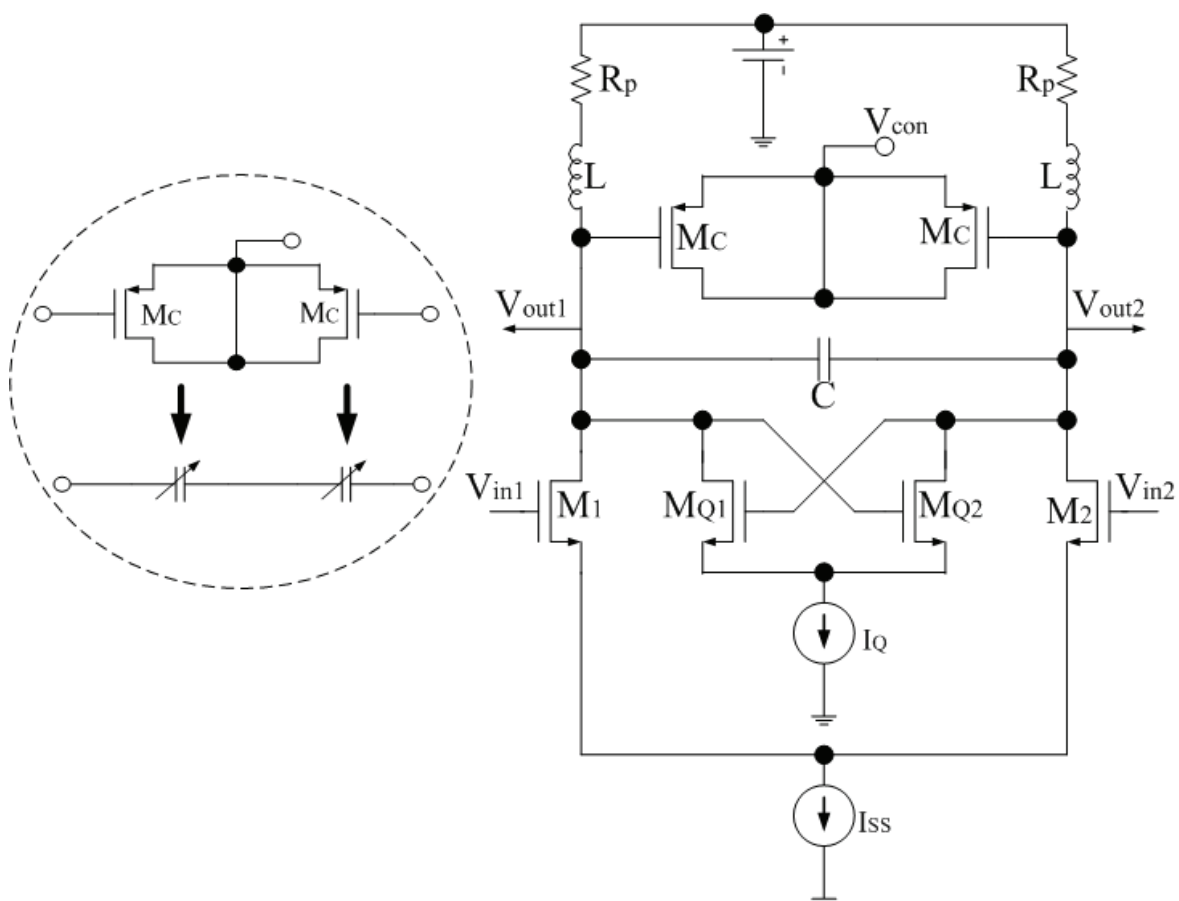


Fig. 20. A 2nd Q-enhanced on-chip LC bandpass filter

The transfer function, quality factor Q , and center frequency ω_0 of the biquad Q-enhanced filter can be expressed as

$$H(s) = \frac{\frac{g_{m,in}}{C_{tot}}(s + \frac{R_p}{L})}{s^2 + (\frac{R_p}{L} - \frac{g_{mQ}}{C_{tot}})s + \frac{1}{LC_{tot}}(1 - g_{mQ}R_p)} \quad (2.19)$$

$$Q = \frac{R_p C_{tot}}{\sqrt{LC_{tot}}(1 - g_{mQ} R_p)} \quad (2.20)$$

$$\omega_0 = \frac{1}{\sqrt{LC_{tot}}} \quad (2.21)$$

Where $C_{tot} = C + 2C_{gmc} + 2C_{gm,in} + 2C_{gmQ}$, C_{gmc} is the parasitic capacitance of transistor M_c , $C_{gm,in}$ is the parasitic capacitance of input buffer M_1 , M_2 , C_{gmQ} is the parasitic capacitance of transistor M_{Q1} , M_{Q2} . $g_{m,in}$ and g_{mQ} are the transconductance values of the input buffer M_1 , M_2 and Q-enhanced cross-coupled differential pair M_{Q1} and M_{Q2} , respectively.

To facilitate a theoretical noise analysis of the circuit, an appropriate noise model for the MOSFET and passive components is required. For noise modeling, passive L and C components will be considered noiseless. The accepted expression is used for passive resistors and transistors. As shown in Figure 19, the mean square noise contributions of each component at the center frequency are given by

$$NF = 1 + \frac{8kT\gamma(g_{mQ} + g_{m\Diamond,in}) + 8kTR_p}{4kTR_S g_{m,in\Diamond}^2} \quad (2.22)$$

4. Simulation results

To verify the design of the Q-enhanced RF bandpass filter, the filter was simulated with TSMC 0.18 μ m CMOS technology. At the same time, in order to test the circuit, the external wideband transformers are employed to serve as the impedance matching. The quality factor Q, gain S_{21} , and noise performance is simulated with Cadence Spectre tools as shown in Figure 21-23. The input reflection coefficient S_{11} is about -23dB when the center frequency is about 2.14GHz and bandwidth is about 36MHz in Figure 24. The effect of Q-tuning controls on the filter's response is shown in Figure 21 when the bias current I_Q and I_{SS} is from 200 μ A to 500 μ A. The maximal value of the quality factor for the filter can be attained 60. Noise figure is about 15dB at center frequency of 2.14GHz in Figure 22. Figure 23 shows the gain of the filter at center frequency of 2.14GHz and $Q=60$, S_{21} is about 15dB. The linearity performance of the filter for $f_c=2.14$ GHz and input power -60dBm is tested by IIP3 as shown in Figure 25. Two-tone signal at 2.14 and 2.144GHz is presented at the filter input through an RF power combiner, the input power at the filter input is -30dBm, which is small (the amplitude of the input voltage is about equals to 7mV) when the input load is 50 Ω . The third-order intercept point (IP3) is about -7.63dBm with SpectreRF PSS tools. The input noise floor is also measured by Cadence tools and the RMS value N_{out} is measured to be about -90.5dBm. Thus, the spurious-free dynamic range (SFDR)[2] can be calculated as

$$SFDR = \frac{2}{3}(IIP3 - N_{out}) \approx 56dB \quad (2.23)$$

The relation between the dynamic range and the quality factor of the filter is simulated as shown in Figure 26 for the center frequency of 2.14GHz. The simulation in Figure 25 shows that the dynamic range is lower when the Q is increased. The main reason for the

degradation in the dynamic range is quality factor and the output noise voltage is increased, it leads to deteriorating the linearity of the filter. The performance of the filter is summarized in Table 1.

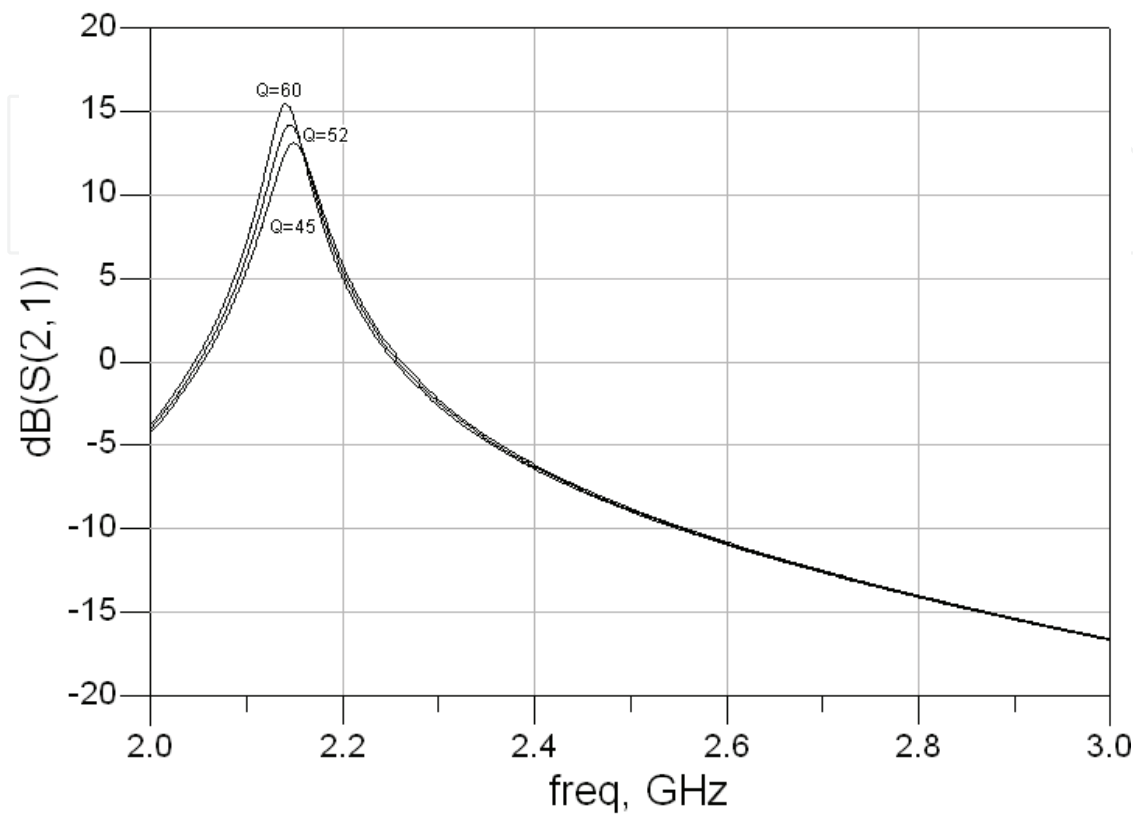


Fig. 21. Quality factor tuning of the RF LC Q-enhanced filter

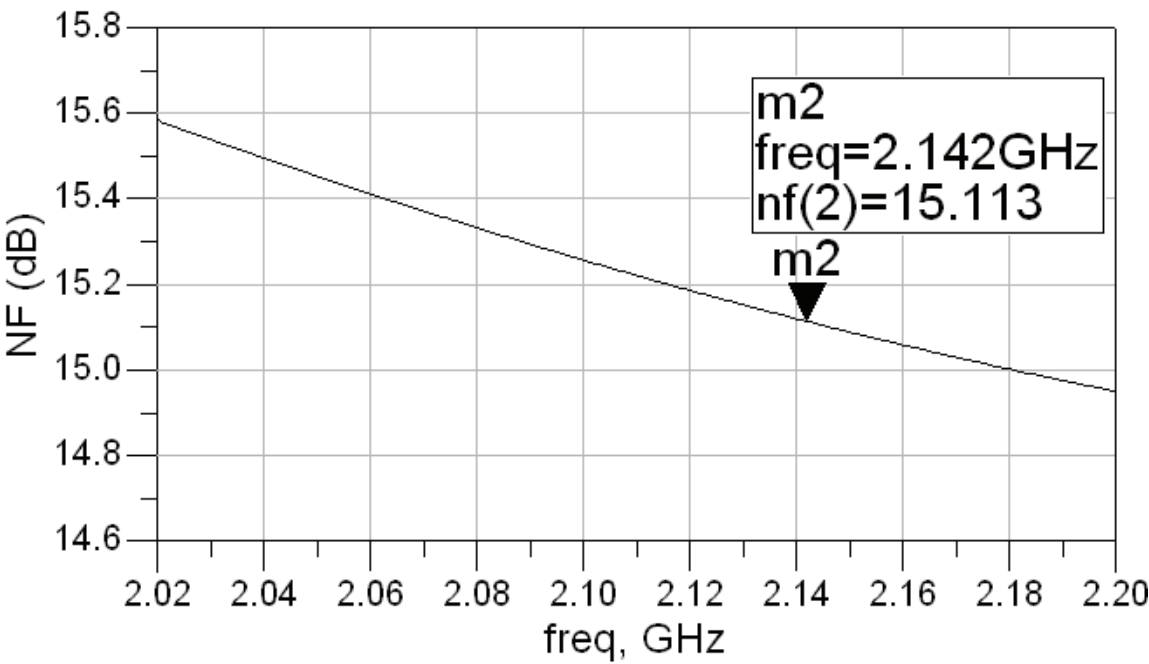


Fig. 22. Noise figure of the RF LC Q-enhanced filter

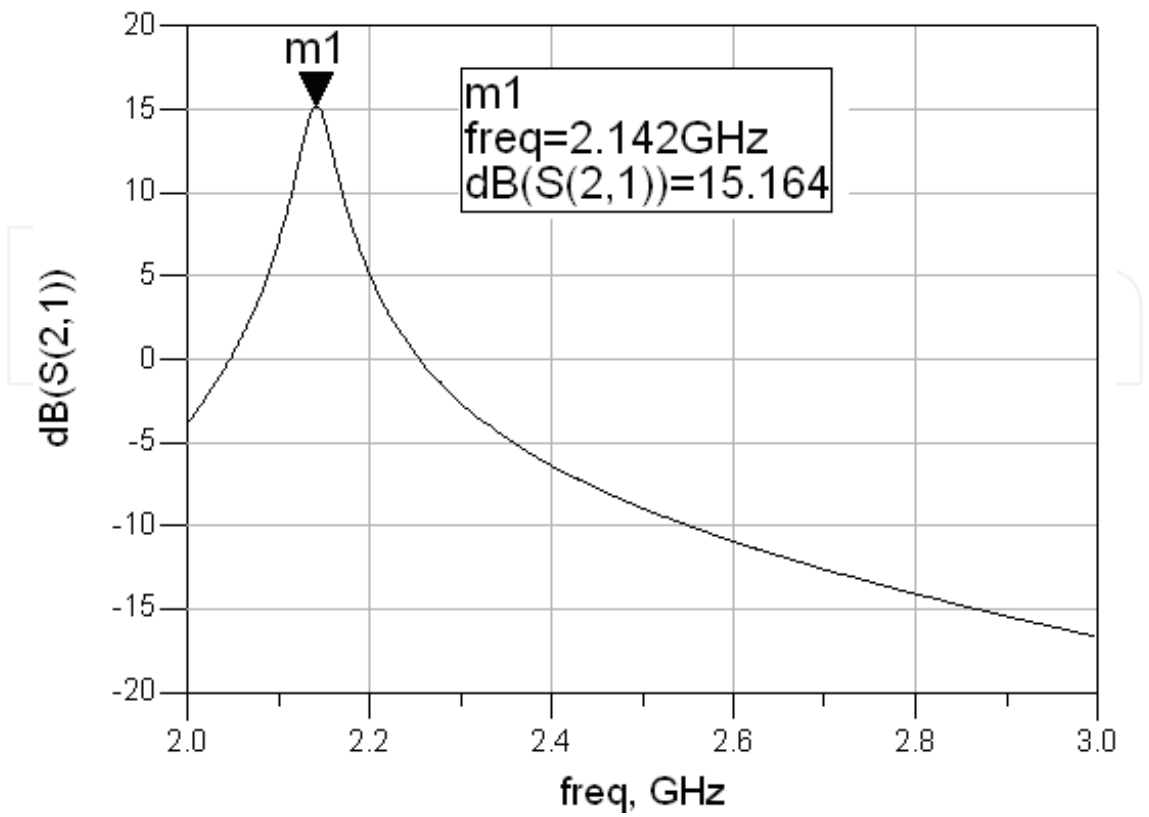


Fig. 23. S21 response of the RF LC Q-enhanced filter

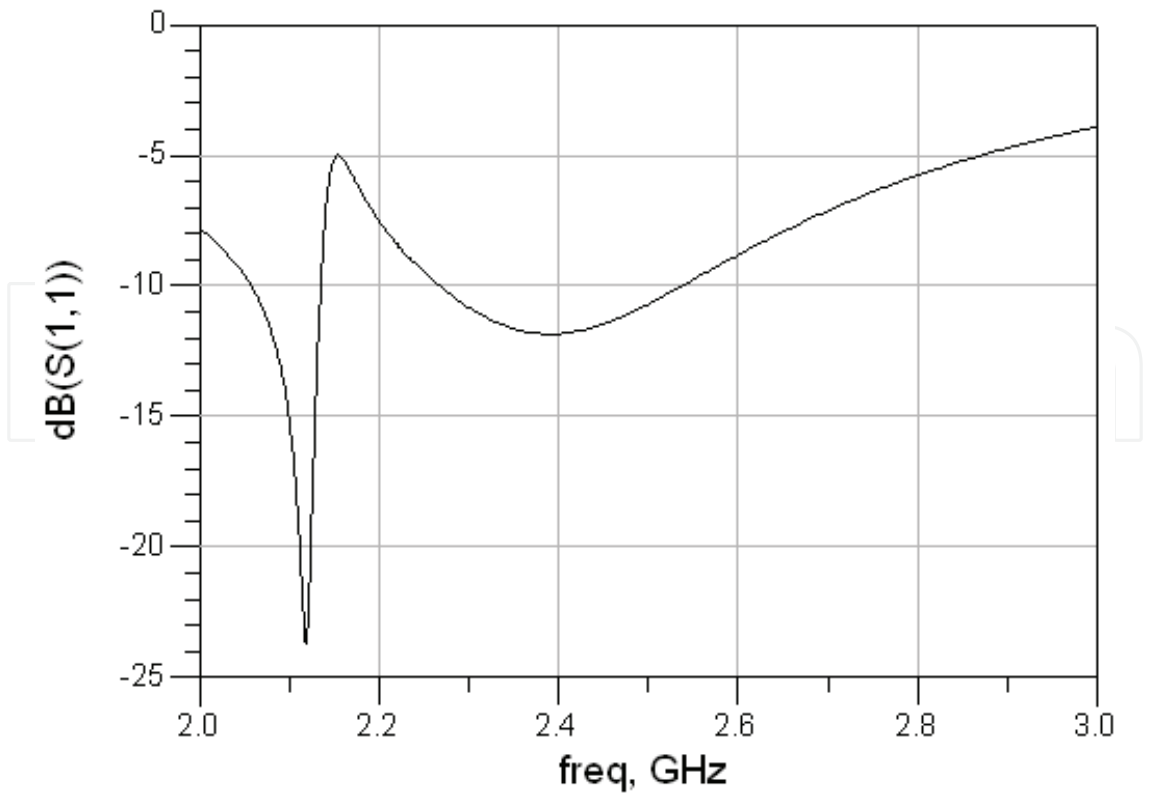


Fig. 24. Input reflected loss response S11 of the RF filter

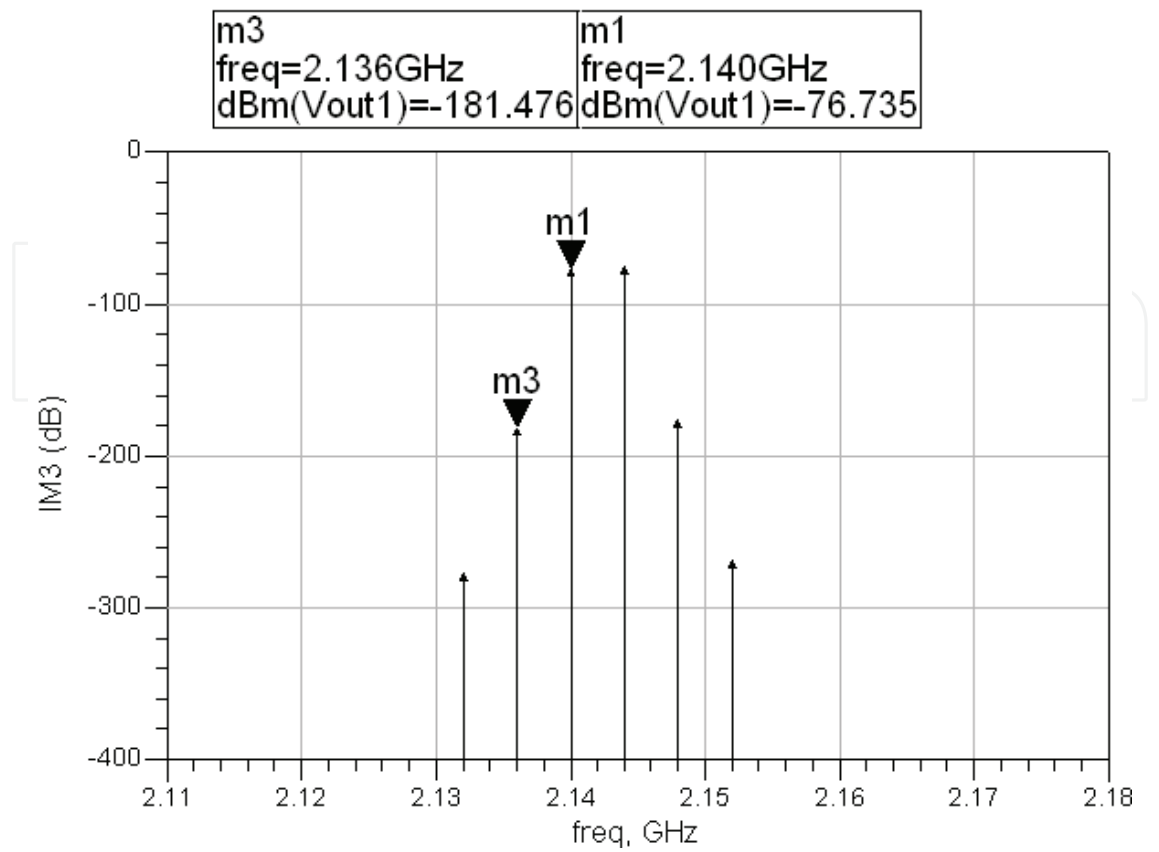


Fig. 25. The 3rd order intercept point response of the RF filter

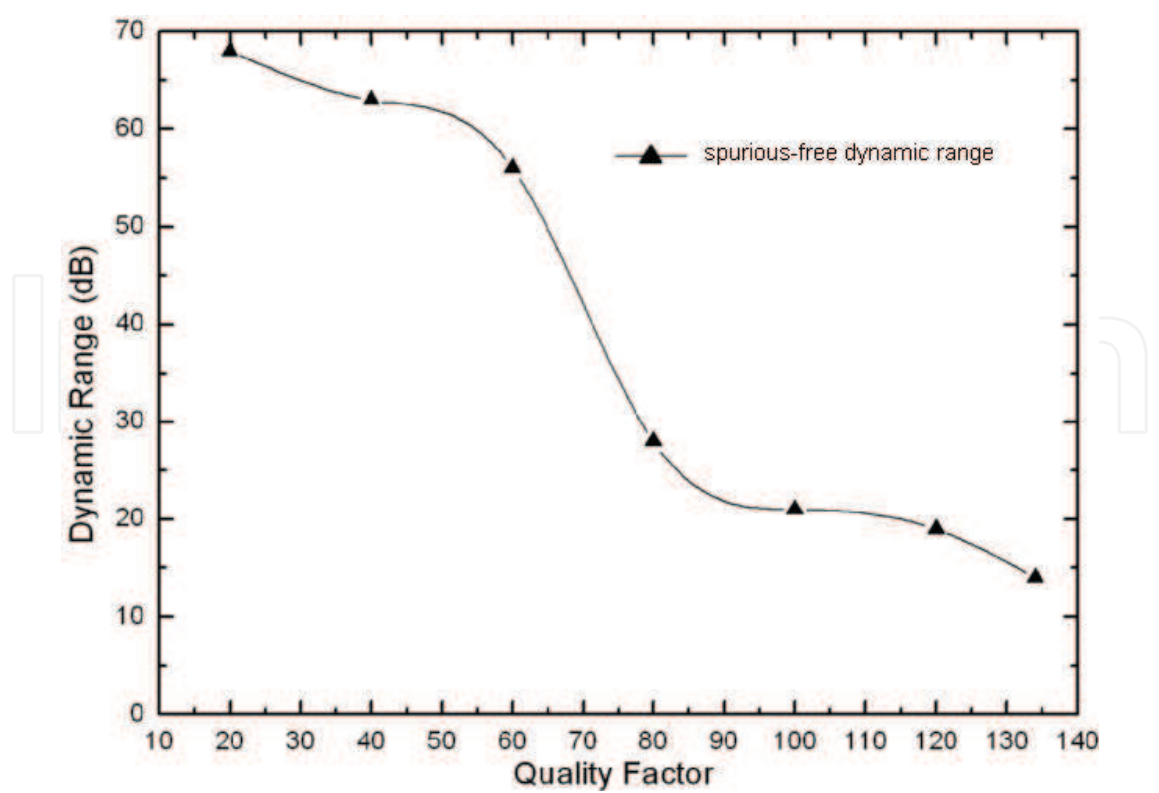


Fig. 26. The related curve of the dynamic range and quality factor

Performance Parameters	[11]	[12]	This work
Technology	0.25μm CMOS	0.5-Si-SOI	0.18μm CMOS
Center frequency	2.14GHz	2.5GHz	2.142GHz
3-dB Bandwidth	60MHz	70MHz	36MHz
Maximum Gain in passband	0dB	14dB	15dB
Noise Figure	19dB	6dB	15dB
Supply voltage	2.5V	3V	1.8V
DC consumption	17.5mW	15mW	15mW

Table 1. The performance comparison of RF active integrated LC filter

Table 1 shows the comparison for published CMOS, and bipolar RF integrated bandpass filters in the literature. The comparison table demonstrates that the proposed RF filter has lower power-supply, the highest selectivity, and the largest gain.

5. Conclusion

A 2.14GHz CMOS fully integrated second-order Q-enhanced LC bandpass filter with tunable center frequency is presented. The filter uses a resonator built with spiral inductors and inversion-mode MOS capacitors which provide frequency tuning. The simulated results are shown that the filtering Q and gain can be attained 60 and at 2.14GHz, and the spurious-free dynamic range (SFDR) is about 56dB with Q=60 and power consumption is about 15mW. The presented filter is suitable for S-band wireless applications.

6. References

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Section III: A fully integrated CMOS active bandpass filter for multi-band RF front-ends

1. Introduction

Now, the fast-growing market in wireless communications has led to the development of multi-standard mobile -terminals [1-3]. This creates a strong interest toward the highly integrated RF transceivers in a compact and low-cost way. So, it is becoming more and more attractive to have a single chip of the complete CMOS multi-band transceiver in the industrial, scientific, and medical (ISM) bands. However, the integrated high-performance filters working at RF frequency still remain the one of the most difficult parts in the integrated RF front-ends. The existence of large interference, spurious tones, unwanted image and carrier frequencies, as well as their harmonics in the wireless communication environment demands the use of RF filters with high selectivity in the RF front-ends as shown in Figure 27.

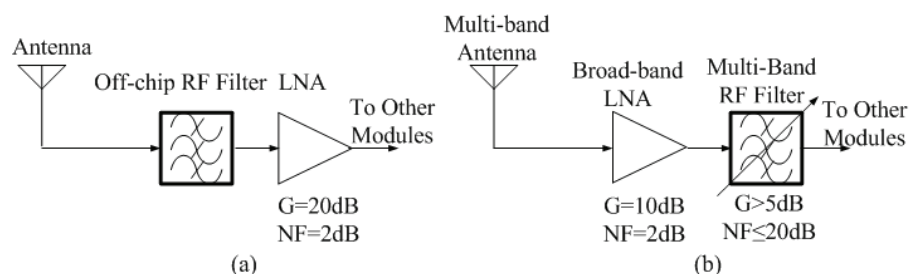


Fig. 27. Multi-Band RF front-end designs

In fact, in current gigahertz-range transceivers, the bulky and expensive off-chip bandpass filters [2] are still required to handle the existence of large out-of-band interference as shown in Figure 1(a). Furthermore, it increases the size, power consumption, and cost of multi-standard transceivers significantly by adding different copies of discrete filters for different bands. Great efforts have been made to use an on-chip tunable Q-enhanced filter to replace such off-chip preselect filter.

To this extent, recent researches on integrated filter design have fallen into the active-LC category [5]-[11]. Filters of this category are built around on-chip spiral inductors and capacitors used as LC resonant tanks, whereas an important cause for the limited integration of RF filters is the low quality factor of monolithic spiral inductors. These inductors are inherently lossy due to ohmic losses in the metal traces and due to substrate resistance and eddy currents. This problem has been addressed by using various methods such as patterned ground shields and geometry improvements, but the Q factor of integrated inductors is still generally limited to a value less than 20 [12] in standard RF CMOS process.

For multi-band RF front-end designs, a suitable on-chip tunable filter is available, but the tunable nature of the on-chip passive inductors is hard.

Compared with the passive inductors, the RF bandpass filter using active inductors can not only achieve wide frequency tuning range and high quality factor, but also occupy the small chip areas. However, it also pays for the higher noise and the worse linearity. In commercial designs as shown in Fig. 1 (a), an LNA combined with a 3dB insertion loss discrete filter typically achieves a net 5dB noise figure, 17dB gain, and 1dB input compression point about -17dBm if the input P1dB of LNA is about -20dBm, while consuming 15mW [4]. If the filter using active inductors is located in the RF front-end as shown in Fig. 1(b), and the input P1dB of LNA is about 20dBm, the proposed RF filter and the LNA can achieve a net less than 4dB, and a net more than or equal to -20dBm input compression point with 15dB gain, so the proposed RF filter combined with other RF modules will satisfy the performance of the moderate noise figure and linearity of RF system requirements such as Bluetooth, 802.11b and so on.

The section is organized as follows. Section 2 presents the novel Q-enhanced active inductor topology, as well as the analysis of the noise figure linearity and stability. Section 3 describes the RF bandpass filter based on the active inductors and the measured results of the filter are demonstrated. Finally, conclusion is given in section 4.

2. Circuit principle

2.1 Proposed active inductor

An often-used way for making active inductors is through the combination of a gyrator and capacitor, but designing high-Q active inductors at GHz with opamps or standard transconductance-C techniques is very difficult due to relatively significant power consumption and noise. The active inductor based on the principle of gyration, consisting of minimum-count transistors can be operated at GHz easily because f_T of single transistor is so high as hundreds of GHz. A class of active inductors have been proposed by researchers [14][19][20] in Figure 27. A common feature of these active inductor topologies is that they all employ some kind of shunt feedback to emulate the inductive impedance in Figure 28.

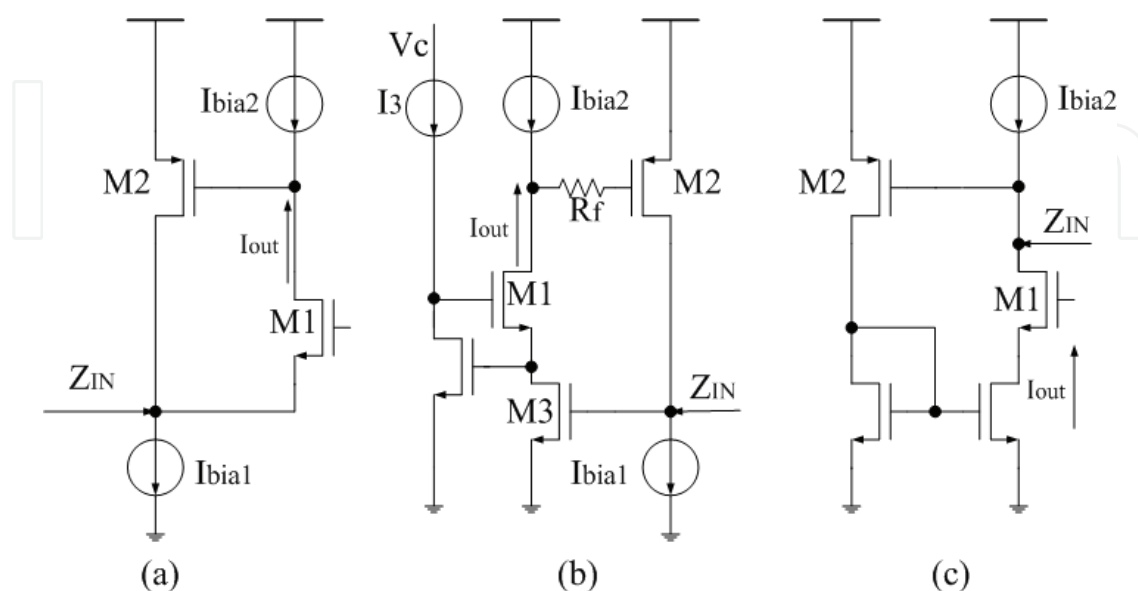


Fig. 28. The proposed CMOS active inductor topology

Intuitively, the circuits can be explained as follows: the input signal at the source of M2 will generate a current $g_{m2}V_i$ at the drain of M2, this current will be integrated on the gate-source capacitance C_{gs1} . The voltage at the gate of M1 will then generate the input current, thus generating the inductive loading effect. Compared with the active inductor proposed in Figure 28(a) and improved (b) or (c), we found the active inductor in Fig. 28(a) has some advantages over the active inductor in Figure 28(b) or (c). As can be seen from the circuit figure, the minimum voltage for the active inductor itself is only $\max(V_{gs1}+V_{ds1}+V_{in}, V_{gs2}+V_{ds2}+V_{gs1}+V_{in})$. Therefore, the circuit in Fig 28(a) is better than the circuit in (b) or (c), and it has two transistors contributing noise directly to the input. In our design, the current-reused active inductor based on (a) is chosen.

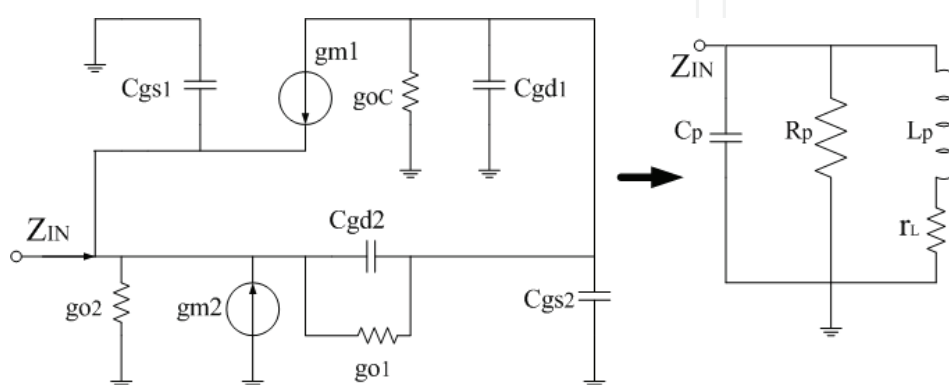


Fig. 29. The small-signal equivalent circuit of the proposed active inductor

A conceptual illustration of the proposed active inductor is shown in Figure 27. A more detailed small-signal representation of Figure 28(a) is shown in Figure 29, where g_O is the drain-source conductance and g_{OC} represents the loading effect of the nonideal biasing current source Z_{load} . The impedance of Z_{in} can be expressed as

$$Z_{in} \equiv \frac{V_{in}}{I_{in}} = R_p // C_p // Z_L \quad (2.24)$$

where the inductive impedance of Z_{in} is

$$Z_L = \frac{g_{oc} + g_{o1} + s(C_{gs2} + C_{gd2} + C_{gd1})}{g_{m1}g_{m2} + [g_{m2} - g_{m1} + g_{oc} + s(C_{gs2} + C_{gd1})](g_{o2} + sC_{gd2})} \quad (2.25)$$

The small-signal analysis of the circuit in Figure 28(a) shows that Z_{in} is a parallel RLC resonant tank with the following values:

$$R_p = \frac{1}{g_{o2}} // \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}} \quad C_p = C_{gs1} \quad L_p \approx \frac{C_{gs2}}{g_{m1}g_{m2}} \quad r_L \approx \frac{g_{oc} + g_{o1}}{g_{m1}g_{m2}} \quad (2.26)$$

where r_L is the intrinsic resistor of the active inductor. The self-resonant frequency ω_0 and intrinsic quality-factor of the inductor is

$$\omega_0 \approx \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} = \sqrt{\omega_{t1}\omega_{t2}} \quad (2.27)$$

and

$$Q_0 = \frac{R_p}{\omega_0 L_p} \approx \sqrt{\frac{g_{m2} C_{gs1}}{g_{m1} C_{gs2}}} \quad (2.28)$$

where ω_{t1} and ω_{t2} are the unity-gain frequency of M1 and M2, respectively.

2.2 Noise analysis

Unlike the passive inductor where the damping resistor r_L is the main noise contributor, the noise in active inductor originates from the thermal noise of MOS transistor channel [14], [15]. By referring to the transistor noise sources to the terminals of the active inductor in Figure 28(a), the noise figure of the circuit will be computed considering, for simplicity, only three main noise sources, i.e., the thermal noise of the two transistors (M1 and M2) and the noise of the load impedance R_p (i.e. $\frac{1}{g_o} || Z_{load}$). where $\overline{v_{n1}^2} = 4kT\gamma\Delta f / g_{m1}$, and

$\overline{i_{n2}^2} = 4kT\gamma\Delta f g_{m2}$, kT is Boltzmann's constant times temperature in Kelvin, and γ is chosen empirically to match the observed thermal noise behavior of a given fabrication process. Computing the transfer functions from all noise sources to the output node, the following expression for the NF (at the resonance frequency) can be obtained

$$NF = 1 + \frac{\gamma}{g_{m1} R_S} + \gamma g_{m2} R_S + \frac{(1 + g_{m1} R_S)^2}{g_{m1}^2 R_S \cdot R_p} \quad (2.29)$$

Where R_S is the source impedance. The second term in the right-hand side of (6) represents the noise contributed by transistor M1 and it has the same expression as for a common-gate amplifier. However, in this case, due to the feedback in the gyrator, g_{m1} can be made larger than $1/R_S$ while still ensuring matching conditions. The third term represents the noise introduced by the feedback transistor M2. Consistently with the intuition, transistor M2 injects noise directly at the input, and its transconductance has to be small to have a low noise. The fourth term in the equation represents the noise contributed by the load. If $g_{m1} R_S \gg 1$, this term becomes approximately equal to R_S/R_p . Notice that increasing R_p (i.e., increasing the quality factor of the resonant load) reduces the noise contributed by the load but also the noise of M2, since it results in a reduction of g_{m2} .

2.3 Nonlinear distortion

As shown in Fig. 27, the distortion is mainly influenced by two factors: the additional current path provided by M2 and the effect of negative feedback on both the gate-source voltage swing across M1 and its DC bias point. The analytical expression for the circuit input P1dB can be found from Sansen's theory [13]. Considering the transistor in strong inversion, the input P1dB for the circuit as a function of the transconductance of transistors becomes

$$V_{in,1dB} = 2 \sqrt{\frac{0.244 V_{in}^2}{1 - 2 g_{m1} g_{m2} R_S R_p}} \cdot (1 + g_{m1} g_{m2} R_S R_p)^2 \quad (2.30)$$

Where V_{in} is the input voltage, and the loop gain of the circuit is given by $g_{m1} g_{m2} R_S R_p$. According to (2.30), the distortion of the circuit can cancel completely for specific values of

the loop gain. This causes the large difficulty to maintain over a wide range of transistor variables.

2.4 Q-enhanced technique and stability analysis

Since the basic concept in the Q-enhanced LC filter is to use lossy LC tank, it is necessary to implement a loss compensation to boost the filter quality factor incorporating negative-conductance. Negative conductance g_{mF} realizes the required negative resistance to compensate for the loss in the tank. The effective quality factor [6] of the filter at the resonant frequency can be shown to be

$$Q_{en} = \frac{Q_0}{1 - g_{mF} R_p} \quad (2.31)$$

Where Q_0 is the base quality factor of the LC tank, which is dominated by the equivalent inductor. Theoretically it can be set as high as desired with appropriate g_{mF} . Indeed, the filter core can be tuned to oscillate if negative transconductance is sufficiently large, i.e., greater than $1/R_p$.

Additionally, the main problem is that the use of shunt feedback by M2 to compensate the loss resistance of the active inductor can result in potential instability depending on the filter terminating impedances yet. In order to make sure that the circuit is stable, the poles of the circuit must be in the left half-plane [16], [17]. In this condition, according to (1), using closed-loop analysis, the circuit will be stable provided that

$$g_{m1} < \frac{(C_{gs2} + C_{gd1})g_{o2}}{C_{gd2}} + g_{m2} + g_{oc} \quad (2.32)$$

Simultaneously it must be ensured that the magnitude of the input reflection coefficient is less than unity i.e. $|S_{11}| < 1$. Due to the stability problem, we should determine the reasonable transconductance g_{m1} and g_{m2} in order that the trade-offs between noise, Q enhancement and stability will satisfy the requirements of the communication systems.

3. Design of the RF filter and its measured results

3.1 Circuit design

The complete prototype circuit of the proposed second-order RF bandpass filter based on the active inductor topology is shown in Figure 30. This circuit consists of three different stages, including two differential high Q-enhancement active inductors, negative impedance and buffers. Common-drain transistors M11, M13 and M12, M14 are employed for the output buffer stages. This common drain configuration can offer to minimize the loading effect and output impedance matching.

M1, M3, M5 and M2, M4, M6 construct LC-resonant circuit which is made up of the active inductor respectively. Note that the transistor M5 and M6 are respectively used to amplify the signal of shunt feedback in the active inductor topology in order to boost the impedance of active inductors. M7, M8 and M9, M10 consisting of unbalanced cross-coupled pairs are employed not only to produce negative resistance for canceling the inductor loss, but also increase linearity of the filter when the signal is large. The transistors and capacitors are sized to optimize gain in the passband, noise figure, and linearity. Transistors M1, M2 have a length/width ratio of $2\mu\text{m}/0.18\mu\text{m}$, M3, M4 have $4\mu\text{m}/0.18\mu\text{m}$, M5, M6 have

20um/0.18um, and M7, M8 have 0.4um/0.2um and M9, M10 have 0.3um/0.18um. For the output buffers, transistors M11, M12 have a length/width ratio of 3um/0.18um, and M13, M14 have 2um/0.18um. The input capacitance is about 120ff. The DC bias current I_{Q1} and I_{Q2} can be used to tune the Q of the active inductors and the transconductance of the cross-coupled pairs. V_b and V_c are bias voltages which are used for DC operating state of the filter. The DC bias currents I_{bia1} and/or I_{bia2} can be adjusted to tune the center frequency of the circuit and also change the Q of the inductance in Fig. 3.

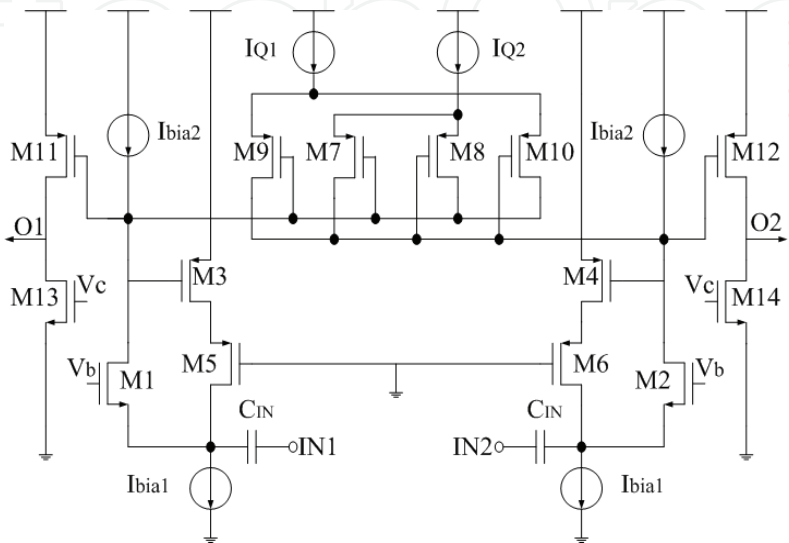


Fig. 30. The fully Q-enhancement bandpass filter

3.2 Measured results

The circuit is fabricated in 0.18-um UMC-HJTC CMOS process through the educational service. The die photograph of the fabricated circuit is shown in Figure 31. To ensure the fully differential operation, a symmetrical layout is used for the design. The total chip area is 0.7×0.75mm² including the pads, where the active area occupies only 0.15×0.2mm².

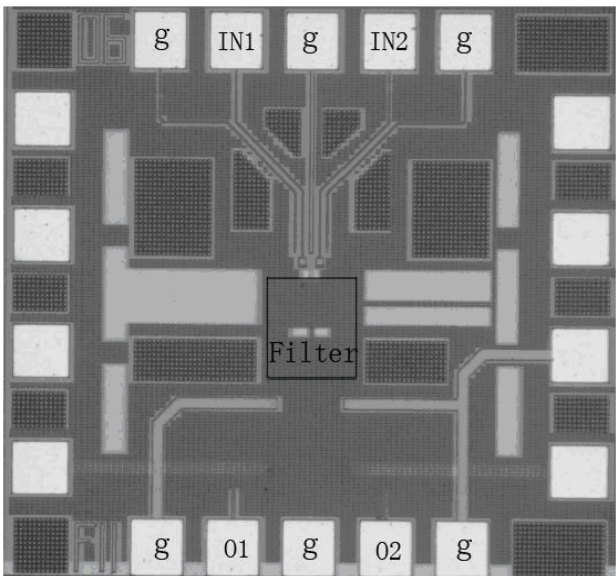


Fig. 31. Photomicrograph of the Q-enhanced RF bandpass filter

The two-port S-parameter measurements were made with the vector network analyzer Agilent E8363B. Noise measurements were made with a spectrum analyzer equipped with power measurement software and a noise source. The 1-dB compression point measurements were made with a spectrum analyzer and a power meter. The measured RF bandpass filter forward transmission response, S_{21} , is shown in Figure 32, Figure 33 and Figure 34, respectively. Figure 32 shows the passband center frequency is 1.92GHz and 3-dB bandwidth is about 28MHz. The maximum gain in the passband is about 11.64dB and the input return loss, S_{11} is -14.67dB in Figure 32. In Figure 33, the center frequency is about 2.44GHz and 3-dB bandwidth is about 60MHz. The maximum gain in the passband is about 5.99dB. Moreover, the S_{21} at about center frequency 3.82GHz is about 12dB and return loss S_{11} is about -29dB as shown in Figure 34.

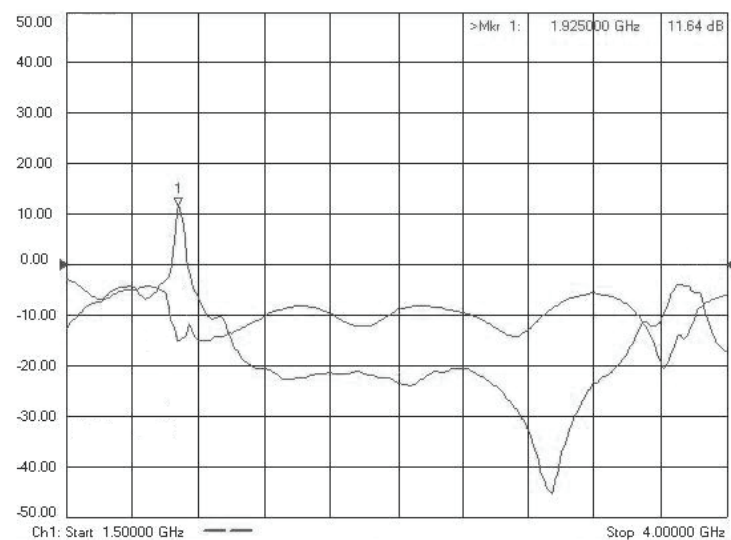


Fig. 32. Measured bandpass filter insertion loss S_{21} and return loss S_{11} at center frequency about 1.92GHz

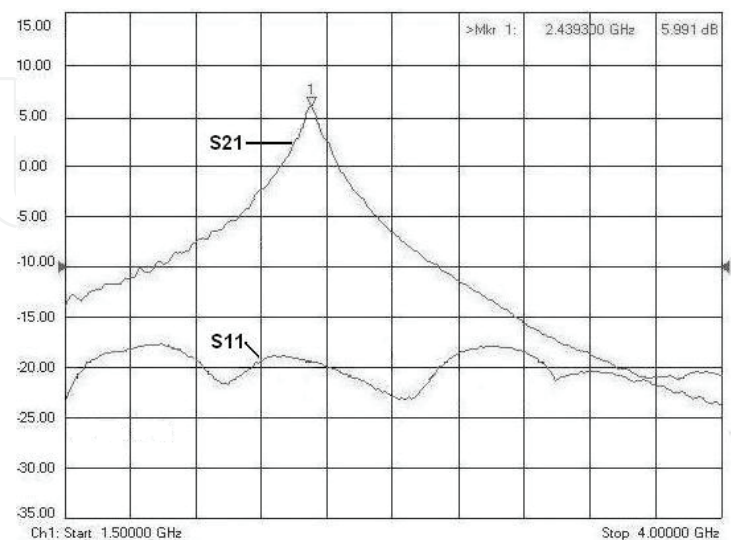


Fig. 33. Measured bandpass filter insertion loss S_{21} and return loss S_{11} at center frequency about 2.44GHz

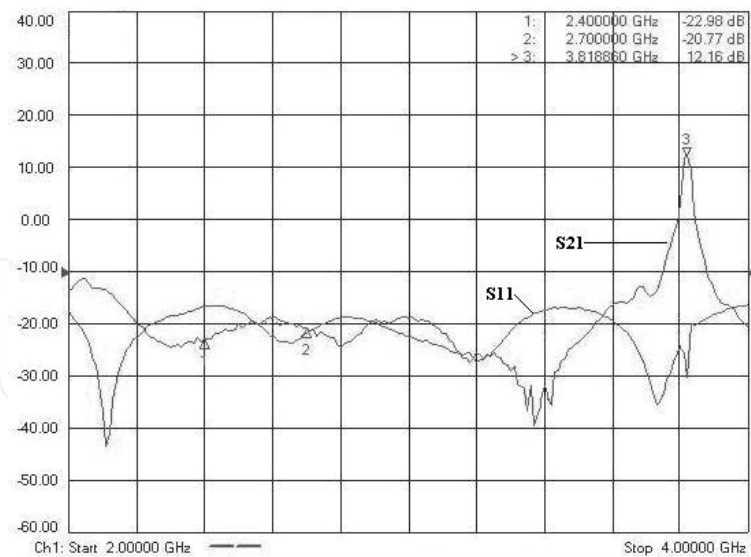


Fig. 34. Measured bandpass filter insertion loss S21 and return loss S11 at the center frequency about 3.82GHz

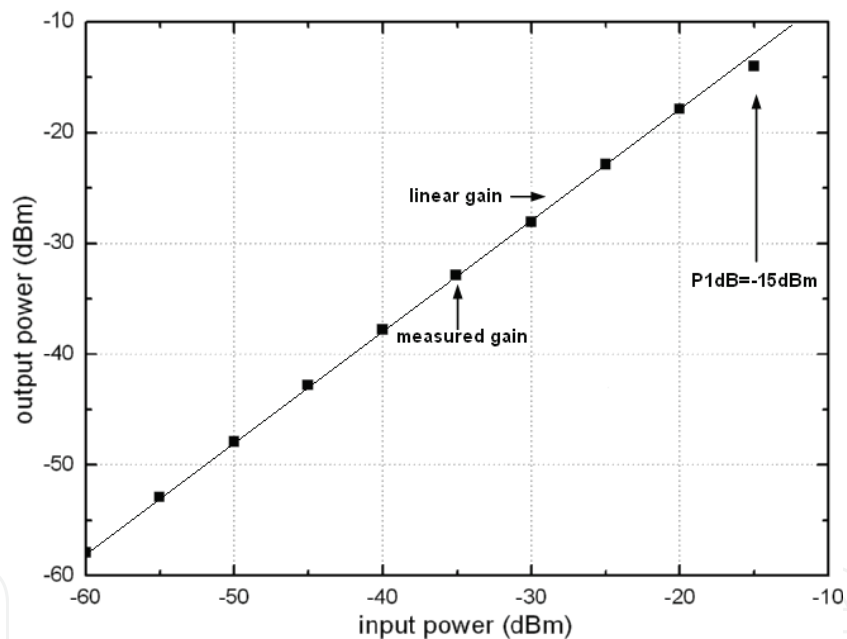


Fig. 35. P1dB measurement at center frequency about 2.44GHz

A measurement to the input 1dB compression point of the circuit can be obtained by sweeping the input power to the tank and measuring the output power. As the input power is increased, the input impedance presented by the Q-enhanced active inductor tanks begins to drop due to nonlinear effects, which can be observed when the output power no longer depends on the input power in a linear fashion as shown in Figure 35. The measured bandpass filter P1dB input power compression point is -15dBm at the center frequency about 2.44GHz passband. The noise figure of 18dB was also measured by disconnecting the input signal. The RF filter has wide-tuning range from the center frequency about 1.92GHz to 3.82GHz when the DC voltage sources of the controlled bias currents I_{bia1} and/or I_{bia2} are adjusted from 0.5 to 1.5V or vice versa. The noise figure evaluated in each band gives the

following results: 15dB for center frequency 1.92GHz, 18dB for center frequency about 2.44GHz, 20dB for center frequency about 3.82GHz. Furthermore, 1-dB compress point is about -17dBm, -15dBm, -18dBm respectively.

Ref.	[8]	[9]	[10]	[11]	This work
Process	0.25um-CMOS	0.5-Si-SOI	0.18um-CMOS	0.18um-CMOS	0.18um-CMOS
Die area	3.5mm ²	2.5mm ²	2.25mm ²	0.81mm ²	0.53mm ²
N-orders	6	2	3	4	2
f_{center}	2.14GHz	2.5GHz	2.36GHz	2.03GHz	2.44GHz
-3dB Bandwidth	60MHz	70MHz	60MHz	130MHz	60MHz
Tuning range	-	250MHz	-	60.9MHz	1900MHz
Noise figure	19dB	6dB	18 dB	15 dB	18 dB
Mid-band gain	0dB	14dB	-1.8dB	0dB	6dB
Supply voltage	2.5V	3V	1.8V	1.8V	1.8V
FOM	72	82	78	77	81

Table 2. Comparison of the RF bandpass filters Performance

The summary of the measured performance and the comparisons of the performance among the fabricated RF filters in CMOS and other process is given in Table 2. A figure of merit [18] (FOM) which allows comparison between other RF filters in silicon is given as

$$FOM = \frac{N \cdot P_{1dBW} \cdot f_{center} \cdot Q_{filter}}{P_{DC} \cdot NF} \tag{2.33}$$

where N is the number of poles, P_{1dBW} is the inband 1-dB compression point in Watt, f_{center} is the center frequency, Q_{filter} is the ratio of the center frequency and the 3-dB bandwidth, P_{DC} is the DC power dissipation in Watt, and NF is the noise figure (not in dB). It has shown from Table II that the filter presented in this work achieves a good FOM with higher quality factor and gain in the passband, and the tuning range is the largest, and the chip area is the smallest.

4. Conclusion

The design and implementation of tunable RF bandpass filter in 0.18um CMOS process have been introduced and verified, which demonstrate that the RF bandpass filter can achieve

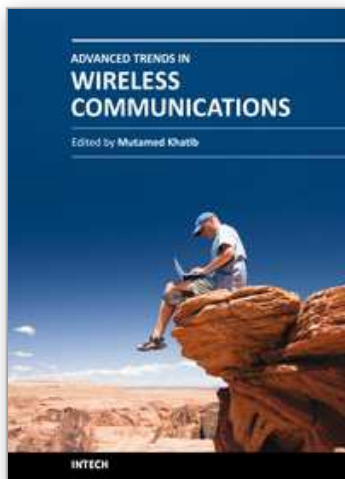
high quality factor and large tuning range from 1.92GHz to 3.82GHz. Although the noise and linearity of the proposed active inductors are inferior to passive ones, the smallest chip area, and the largest tenability make them apply to the multi-band on-chip wireless systems in future.

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