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Analog Design Issues for Mixed-Signal CMOS Integrated Circuits

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1. Introduction

Today, due to the continuous miniaturization of electronic components, a single integrated circuit (IC) contains many transistors and interconnections very close each other, and this causes an increased number of unwanted interactions. Crosstalk is one of the main difficulties to face. In a mixed-signal System-on-Chip (SoC), i.e., when analog and digital circuits are integrated on the same silicon chip, performance limitations come mainly from the analog section which interfaces the digital processing core with the external world. In such ICs, the digital switching activity may affect the analog section.

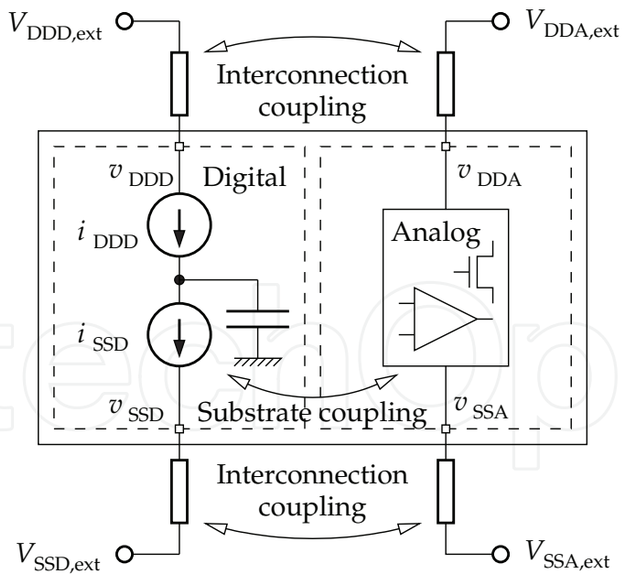

Fig. 1. Schematic diagram of a mixed-signal IC; in the digital section only the switching currents i_{DDD} and i_{SSD} are modeled.

Fig. 1 illustrates a simplified scheme of digital/analog interactions: the switching currents drawn from the voltage supplies (i_{DDD} and i_{SSD}) cause a voltage drop across the interconnection impedances, and the on-chip supply voltages (v_{DDD} and v_{SSD}) differ from

the external voltages. Voltage fluctuations may propagate to the analog part of the chip, either trough interconnection cross-capacitances and mutual inductances, or through the common substrate of the silicon chip. This interaction, acting as a "digital noise" superimposed to analog signals, is often the limiting factor affecting the overall system performance.
For this reason, the optimum "mixed-signal" design can be very different from the optimum stand-alone design. The analog designer must choose the optimum circuit architecture considering robustness and crosstalk immunity.
The objective of this chapter is to provide some guidelines for the design of analog blocks suitable for mixed analog-digital integrated circuits. Three different design levels will be considered.

- Modeling: the model must be as simple as possible; the designer has to consider everything is important and to neglect the details that do not contribute to a remarkable improvement, in order to obtain valuable results at a reasonable complexity level.
- Architectural design: the switching noise generated by digital circuits should be as low as possible; analog structures should be insensitive to digital noise.
- Physical design: layout design must be optimized for the fabrication technology, to ensure a proper isolation between digital and analog sections, and to achieve a correct biasing of substrate and well areas.

2. Modeling

The choice of the optimum circuit architecture with respect to robustness and crosstalk immunity requires the analysis of noise generation, noise propagation, and effects on sensitive parts of the system. Hence, a correct design methodology should account for digital switching noise from early stages of the design process, in order to evaluate different architectural choices. To this end, analysis tools are required to evaluate current consumption during logic transition, in order to understand the propagation path towards analog blocks, and to design suitable protection structures.
Switching noise effects depend on total currents drawn from the positive and the negative supplies of the digital circuit. Therefore, the calculation of the current consumption of each single logic gate is a too much detailed information, with would require a huge computational effort for simulation at circuit level. For this reason, a viable method should provide only aggregate information.
Although logic transitions are a completely deterministic phenomenon, their effects are complex. Noise effects depend on the values of currents and of their time derivatives, and on propagation mechanisms, which in turn are related to both on-chip and off-chip interconnections and on substrate parasitics (Donnay & Gielen, 2003). Then, for a large integrated system, logic transitions can be considered as a cognitively stochastic process, due to the huge number of logic blocks. For these reasons, a statistical distribution can model the overall switching current of a large digital circuit, using only few global parameters. The amplitude distribution and the power spectral density of the digital noise can be obtained from a theoretical analysis.
For simplicity, let us consider a combinational network, made up with identical logic cells, each of them driving equal capacitive loads. A simplified model of digital switching current can be obtained under the following hypotheses.

1. *Independence of logic transitions:* the transition activity of a logic gate is independent of transitions of other gates. Although this statement is not true, as the output of a logic

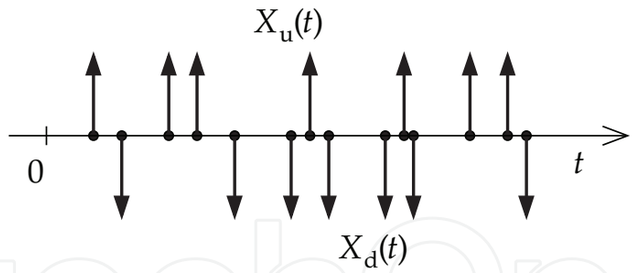

Fig. 2. Switching instants of logic gates modeled as two trains of Dirac impulses.

gate drives other cells, in a large system the huge number of logic gates makes each of them dependent only on a very small number of neighboring cells. Therefore, each logic transition is independent of almost all other transitions.

2. *Input switching instants uniformly distributed in time:* the transition activity of logic cells occur at random instants with uniform distribution over time.
3. *Logic gates with equal delay:* all logic transitions require the same time, therefore all current pulses have the same finite time duration t_p.
4. *Logic gates with equal current consumption:* the current consumption due to switching activity is equal for all logic cells.

Under the above assumptions, the digital switching noise is described by a shot noise process. The instants when logic gates start switching can be considered as Poisson points.
Given a time interval of duration t, we define the random variable $n(t)$ as the number of transitions of signals within the considered time interval. The probability to have exactly $n = k$ events is given by:

$$\Pr[n(t) = k] = e^{-\lambda t}\frac{(\lambda t)^k}{k!} \quad \text{for } k = 0, 1, 2, \ldots \tag{1}$$

The number of Poisson points in an interval of length t is a Poisson distributed random variable, and the parameter λ is the density of the points (Papoulis & Pillai, 2002).
Each logic transition can be described as a Dirac impulse, as shown in Fig. 2. Therefore, two trains of impulses taken at random instants are the stochastic processes $X_u(t)$ and $X_d(t)$ which represent the transitions of logic gates from 0 to 1 and from 1 to 0, respectively. Each of the processes can be written as:

$$X(t) = \sum_i \delta(t - t_i). \tag{2}$$

Under the assumptions mentioned above, the convolution between the train of impulses and the current drawn by the single logic gate gives the total current drawn by the whole digital circuit:

$$I(t) = h(t) * X(t) = \sum_i h(t - t_i), \tag{3}$$

where $h(t)$ is the impulse response, representing the current of a single gate in one logic transition.
This process, known as shot noise, is based on the statistical independence of the events (Papoulis & Pillai, 2002), which are, in our case, the transitions of logic gates. If the impulse density λ is uniform over time, the process is stationary. Fig. 3 illustrates an example of a stationary shot noise process.

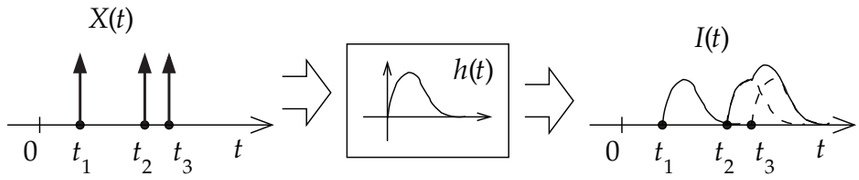

Fig. 3. Switching current as a shot noise process.

2.1 Amplitude and frequency distribution of switching noise

The amplitude distribution of the total current drawn by the digital circuit is represented by the probability density function (p.d.f.) of the stochastic process $I(t)$, which can be calculated from the p.d.f. of the single current pulse $f_H(i)$.

At an arbitrary time instant t_1, the total current $I(t_1)$ is a random variable, whose p.d.f. depends on both the number of Poisson impulses falling in the interval $[t_1 - t_\mathrm{p}, t_1]$ (i.e., the number of logic gates which have not yet completed the logic transition), and the p.d.f. of the single current pulse $f_H(i)$ (Boselli et al., 2010):

$$\begin{aligned} f(i) &= \delta(i)\Pr[n=0] + f_H(i)\Pr[n=1] + f_H(i) * f_H(i)\Pr[n=2] + \ldots + \\ &+ \underbrace{f_H(i) * f_H(i) * \ldots * f_H(i)}_{k \text{ factors}} \Pr[n=k] + \ldots = \\ &= \sum_{k=0}^{\infty} f_k(i)\Pr[n=k], \end{aligned} \tag{4}$$

where

$$\begin{aligned} f_0(i) &= \delta(i), \\ f_1(i) &= f_H(i), \\ f_2(i) &= f_H(i) * f_H(i), \\ f_k(i) &= \underbrace{f_H(i) * f_H(i) * \ldots * f_H(i)}_{k \text{ factors}}. \end{aligned}$$

By using the Poisson probability (1) in (4), we obtain:

$$f(i) = \sum_{k=0}^{\infty} f_k(i) e^{-\lambda t_\mathrm{p}} \frac{(\lambda t_\mathrm{p})^k}{k!}. \tag{5}$$

If $\lambda t_\mathrm{p} < 1$, i.e. the duration of current pulses is small compared to the average interval between Poisson impulses, then we have a low-density shot noise, and the p.d.f. of the total current can be obtained by adding just a few terms of the series (5), since the general term vanishes quickly as k increases. If $\lambda t_\mathrm{p} > 1$, then we have a high-density shot noise, and the p.d.f. of the total current tends to be gaussian.

The frequency distribution of the switching current $I(t)$ is given by its power spectral density (p.s.d.) $S_I(f)$, which can be calculated as (Papoulis & Pillai, 2002):

$$S_I(f) = S_X(f) \cdot |H(f)|^2 = \lambda^2 \delta(f) \cdot |H(f)|^2 + \lambda \cdot |H(f)|^2, \tag{6}$$

where $S_X(f) = \lambda^2 \delta(f) + \lambda$ is the power spectral density of the process $X(t)$ and $H(f)$ is the Fourier transform of the impulse response $h(t)$. As the Dirac's impulse $\delta(f)$ is zero for all

$f \neq 0$, the term $\delta(f)|H(f)|^2$ in (6) can be replaced with $\delta(f)H^2(0) = \delta(f)Q^2$, where Q is the charge transferred during the complete switching of a single logic gate:

$$Q = H(0) = \int_{-\infty}^{+\infty} h(t)dt. \tag{7}$$

Therefore, the power spectral density $S_I(f)$ of the stochastic process $I(t)$ is:

$$S_I(f) = \lambda^2 Q^2 \delta(f) + \lambda \cdot |H(f)|^2, \tag{8}$$

and the normalized power P_I of the switching current $I(t)$ is:

$$P_I = \int_{-\infty}^{+\infty} S_I(f)df = \lambda^2 Q^2 + \lambda \int_{-\infty}^{+\infty} |H(f)|^2 df. \tag{9}$$

In (9), the term $\lambda^2 Q^2$ is the dc component of the digital switching power (λQ is the average value of the current drawn from the supply voltage), while the term $\lambda \int_{-\infty}^{+\infty} |H(f)|^2 df$ is the ac component of the switching power. The rightmost term in (9) can be simplified by using Parseval's theorem, thus obtaining:

$$P_I = \lambda^2 Q^2 + \lambda \int_{-\infty}^{+\infty} h^2(t)dt. \tag{10}$$

For any impulse response $h(t)$, the normalized power P_I can be written as:

$$P_I = \lambda^2 Q^2 + \alpha \frac{\lambda}{t_\mathrm{p}} Q^2, \tag{11}$$

where α is a "pulse shape" factor, which depends on the single current pulse waveform in time domain, and t_p is the switching time of logic gates (Boselli et al., 2010).

2.2 Current pulses with different duration, amplitude, and time density

Although equations (4) to (11) were derived starting from restrictive assumptions, the theory can be extended to digital systems made of logic cells with different switching time, different switching currents, and switching activity variable over time.

Let us start considering different switching times. For simplicity, let us assume that the combinational circuit is made of two types of logic cells, labeled "A" and "B". In more detail, gates of type "A" are characterized by the digital switching current $i_A(t)$, which can be described as a shot noise with time density λ_A and impulse response $h_A(t)$, and gates of type "B" are characterized by the digital switching current $i_B(t)$, with time density λ_B and impulse response $h_B(t)$. The total current drawn by the whole circuit is:

$$i(t) = i_A(t) + i_B(t), \tag{12}$$

which is the sum of two shot noise processes. The amplitude distribution $f(i)$ of the total current $i(t)$ is:

$$f(i) = f_A(i) * f_B(i), \tag{13}$$

where $f_A(i)$ and $f_B(i)$ can be calculated separately using (5).

The power spectral density $S_{II}(f)$ is given by the sum of the p.s.d. of the single processes and their cross-spectra:

$$S_{II}(f) = S_{AA}(f) + S_{BB}(f) + S_{AB}(f) + S_{BA}(f). \tag{14}$$

The cross-spectra $S_{AB}(f)$ and $S_{BA}(f)$ can be obtained by taking the Fourier transforms of the cross-correlations $R_{AB}(\tau)$ and $R_{BA}(\tau)$, which are constant:

$$R_{AB}(\tau) = R_{BA}(\tau) = \lambda_A \lambda_B Q_A Q_B. \tag{15}$$

Therefore, the cross-spectra $S_{AB}(f)$ and $S_{BA}(f)$ have a single component at $f = 0$:

$$S_{AB}(f) = S_{BA}(f) = \lambda_A \lambda_B Q_A Q_B \delta(f). \tag{16}$$

By using (8) and (16) in (14), we obtain:

$$S_{II}(f) = (\lambda_A Q_A + \lambda_B Q_B)^2 \delta(f) + \lambda_A \cdot |H_A(f)|^2 + \lambda_B \cdot |H_B(f)|^2. \tag{17}$$

Therefore, at $f = 0$ the power spectrum component is given by the square of the sum of dc current; while at any frequency $f \neq 0$, the power spectral density is given by the sum of the power spectral densities of all shot noise components.

Current pulses having different peak amplitudes can be described by considering Poisson impulses with different intensities, proportional to the current drawn by logic gates. The mathematical model is a generalized Poisson process (Papoulis & Pillai, 2002), given by:

$$X^G(t) = \sum_i c_i \delta(t - t_i), \tag{18}$$

where c_i is a random variable representing the amplitude of Poisson impulses, with mean μ_c and standard deviation σ_c. The autocorrelation $R_X^G(\tau)$ is (Papoulis & Pillai, 2002):

$$R_X^G(\tau) = \mu_c^2 \lambda^2 + (\mu_c^2 + \sigma_c^2) \cdot \lambda \delta(\tau), \tag{19}$$

and the power spectral density $S_X^G(f)$ is given by the Fourier transform:

$$S_X^G(f) = \mathcal{F}(R_X^G(\tau)) = \mu_c^2 \lambda^2 \delta(f) + (\mu_c^2 + \sigma_c^2) \cdot \lambda. \tag{20}$$

The current consumption $I^G(t)$ due to switching activity of logic gates with different current intensities can be calculated by filtering the process $X^G(t)$ through the linear, time-invariant system $h(t)$. The power spectral density $S_I^G(f)$ is:

$$S_I^G(f) = S_X^G(f) \cdot |H(f)|^2 = \lambda^2 Q_{\text{avg}}^2 \delta(f) + \lambda(1 + \sigma_c^2) \cdot |H(f)|^2, \tag{21}$$

where Q_{avg} represents the average charge transferred during the switching transitions (assuming $\mu_c = 1$).

Finally, let us consider a non-uniform distribution of logic switching activity over time. In this situation, the switching noise can be described by a non-stationary stochastic process. In a sequential network driven by a master clock, we can assume that the time density of logic transitions is periodic, and therefore we have a cyclostationary shot noise. Although the p.s.d. cannot be defined for a non-stationary process, it is possible to define a "mean energy spectrum" which has frequency components similar to (8), plus discrete frequency components at the master clock frequency and its harmonics.

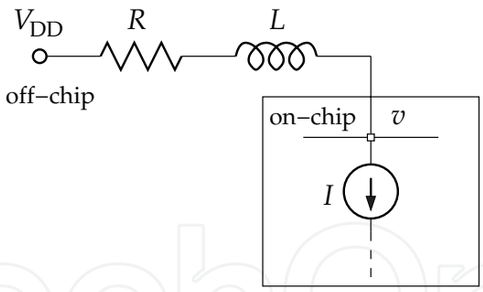

Fig. 4. Equivalent circuit for bondwires.

2.3 Effects of parasitics on on-chip supply voltages

Digital switching noise propagates from the digital to the analog section through both interconnections and substrate. Therefore, realistic models of interconnections (including package, bonding and on-chip parasitics) and substrate must be adopted for simulations. Such models are inherently technology dependent. The model of couplings through package interconnections strongly depends on the package. Therefore, the designer should use the correct model of the production package. For the same reason, the use of different package types for prototyping is not recommended, as parasitic effects can be very different. Substrate models can also be very different. We can distinguish two major categories of substrates: heavily-doped bulk with epitaxial layer, and lightly-doped substrate. The heavily-doped bulk has a very low resistance and can be considered as a single node. Therefore, any disturbance injected into the bulk propagates into the whole chip, irrespective of the distance. On the other hand, the lightly-doped substrate is resistive, and the substrate resistance attenuates the injected disturbance. Some fabrication technologies allow to insert a buried n-well, that can be used for shielding purposes. Such differences must be considered during the design of the chip. Moreover, the same circuit integrated in different technologies can behave in a very different way from the point of view of robustness to crosstalk. Indeed, effects of substrate parasitics put a severe limit on design portability. The results obtained in previous subsection can be used to calculate the on-chip noise voltage is due both to digital switching currents and to parasitic elements.

Let us start considering the simplified circuit shown in Fig. 4, where the current generator models the digital switching noise source, and bondwire parasitics are modeled as series inductance L and resistance R. The bondwire impedance Z is:

$$Z = R + sL = R + j2\pi fL. \tag{22}$$

The on-chip power supply v is affected by a noise voltage having the power spectral density:

$$S_V(f) = S_I(f) \cdot |Z|^2 = \lambda^2 Q^2 R^2 \delta(f) + \lambda R^2 \cdot |H(f)|^2 + \lambda (2\pi)^2 L^2 f^2 \cdot |H(f)|^2. \tag{23}$$

The normalized power P_V of the switching noise affecting the on-chip voltage supply v is:

$$P_V = \int_{-\infty}^{+\infty} S_V(f) df = \lambda^2 Q^2 R^2 + \lambda R^2 \int_{-\infty}^{+\infty} h^2(t) dt + \lambda L^2 \int_{-\infty}^{+\infty} h'^2(t) dt, \tag{24}$$

where we have used Parseval's theorem for both $h(t)$ and its time derivative $h'(t)$. The first two terms in (24), $\lambda^2 Q^2 R^2$ and $\lambda R^2 \int_{-\infty}^{+\infty} h^2(t) dt$, are the dc and ac components due to the voltage drop across the parasitic resistance R. The last term, $\lambda L^2 \int_{-\infty}^{+\infty} h'^2(t) dt$, is the ac

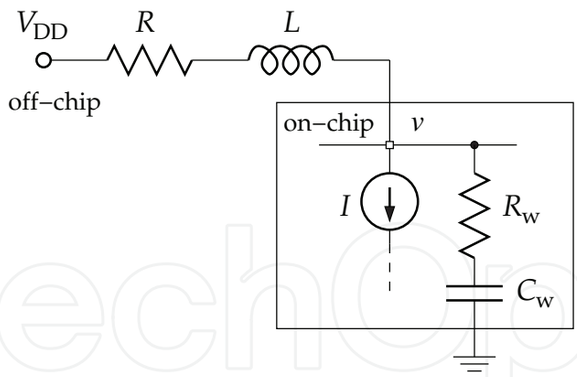

Fig. 5. Equivalent circuit for calculation of bondwire and substrate parasitic effects.

component due to the parasitic inductance L. By comparing the voltage spectral density and power in (23) and (24) with the current spectral density and power in (8) and (9), we can observe that the noise voltage terms due to the parasitic resistance R are similar to the noise current terms, since the resistance R gives a proportional relationship between current and voltage. On the other hand, the last term in (23) and (24) accounts for the inductive voltage drop $Lh'(t)$. Therefore, spectral characteristics of noise voltage are dependent on both the impulse response $h(t)$ and its time derivative $h'(t)$. The rms value of the on-chip noise voltage is given by:

$$v_{\text{rms}} = \sqrt{P_V} = \sqrt{\lambda^2 Q^2 R^2 + \lambda R^2 \int_{-\infty}^{+\infty} h^2(t)dt + \lambda L^2 \int_{-\infty}^{+\infty} h'^2(t)dt}. \tag{25}$$

Now we suppose that, besides bondwire parasitic inductance L and resistance R, the n-well and p-substrate are providing an additional ac path from on-chip supply towards ground, modeled by the resistance R_w and the capacitance C_w, as shown in Fig. 5. The overall impedance Z is:

$$Z = \frac{R + s(L + RR_wC_w) + s^2LR_wC_w}{1 + s(R + R_w)C_w + s^2LC_w}. \tag{26}$$

Since the impedance formula (26) has a second-order denominator, oscillations may arise in the circuit in the underdamped case, i.e., when

$$R + R_w < 2\sqrt{\frac{L}{C_w}}. \tag{27}$$

If the values of parasitics satisfy (27), then the current pulses due to digital switching make the on-chip voltage supply to oscillate, giving rise to the well known "VDD bounce". The lower the ratio $(R + R_w)/\sqrt{\frac{L}{C_w}}$, the longer the duration of the bouncing.

2.4 Interconnection parasitics

An accurate model of interactions between analog and digital parts of an integrated circuit must account for off-chip parasitics. In particular, package and wire bonding parasitics may give a remarkable contribution to propagation of switching noise. Indeed, in addition to the parasitic elements of a single interconnection, an accurate model should consider also capacitances and mutual inductances between adjacent wires, as shown in Fig. 6 (Boselli

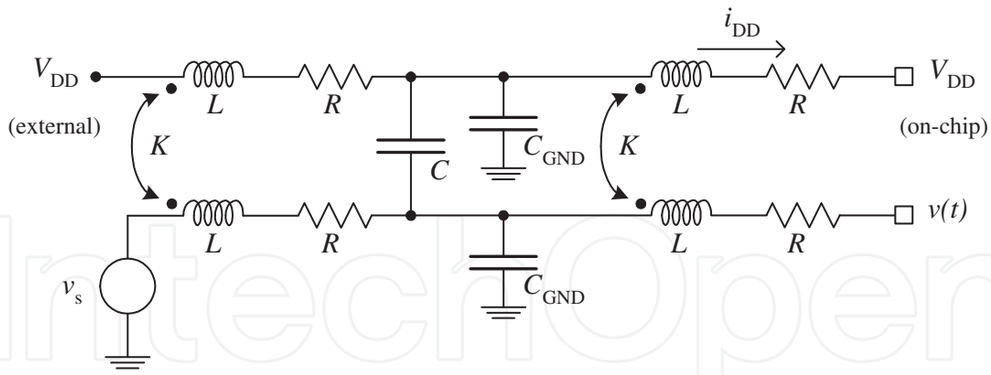

Fig. 6. Equivalent circuit of bonding and package parasitics between two adjacent wires.

et al., 2007). In this model, each wire has series inductance and resistance, capacitance to ground, and both capacitive and inductive couplings towards the other wires. The switching current i_{DD} affects both the on chip voltage supply and the signals coupled either through cross-capacitances (C) or through mutual inductances (K). Coupling between neighboring wires must be carefully considered, since it contributes to disturbance propagation from digital supplies to analog supplies, even without galvanic connection.
The parameters R, L, C, and K in Fig. 6 strongly depends on the package. Therefore, the designer should use the correct model of production package. Moreover, the use of different package types for prototyping is not recommended, as parasitic effects can be very different (Ferragina et al., 2010).

3. Architectural design

A careful evaluation of digital switching noise effects should allow the designer to select a robust architecture for the analog blocks and to choose digital structures which generate less switching noise as possible.
To reduce digital switching noise, transition activity of logic gates must be low, and load capacitance must be minimized. To this end, a partitioning of logic circuitry into different clock domains can reduce both the total capacitance and the switching activity, provided that each part of the circuit is driven by the minimum clock frequency required for correct operation.
The analog designer should use robust structures, insensitive to noise (Bonomi et al., 2006). Fully-differential structures are useful to this end, since injected disturbances behave as common-mode signals and are rejected. Moreover, on-chip decoupling capacitances help in reducing digital switching noise, as they provide a low impedance path for high frequency disturbance.
As an example, let us consider the voltage reference generator shown in Fig. 7. It is based on a band-gap voltage reference and it provides the voltages used as references in a 3-bit flash analog-to-digital converter (ADC). V_{BG} is the band-gap voltage reference; $V_1, V_2, \ldots, V_7$ are the voltage references of the flash ADC; V_{bias} is used to bias the operational amplifiers. The band-gap reference voltage is not affected by switching noise. Indeed, the circuit exhibits a low impedance to V_{SSA}; moreover, the reference output node is capacitively coupled by C_{BG} to V_{SSA}. For these reasons, the output voltage is kept at a constant value $V_{BG} = 1.22$ V (with respect to the V_{SSA} supply). On the other hand, the resistive string voltages $V_1, V_2, \ldots, V_7$ are

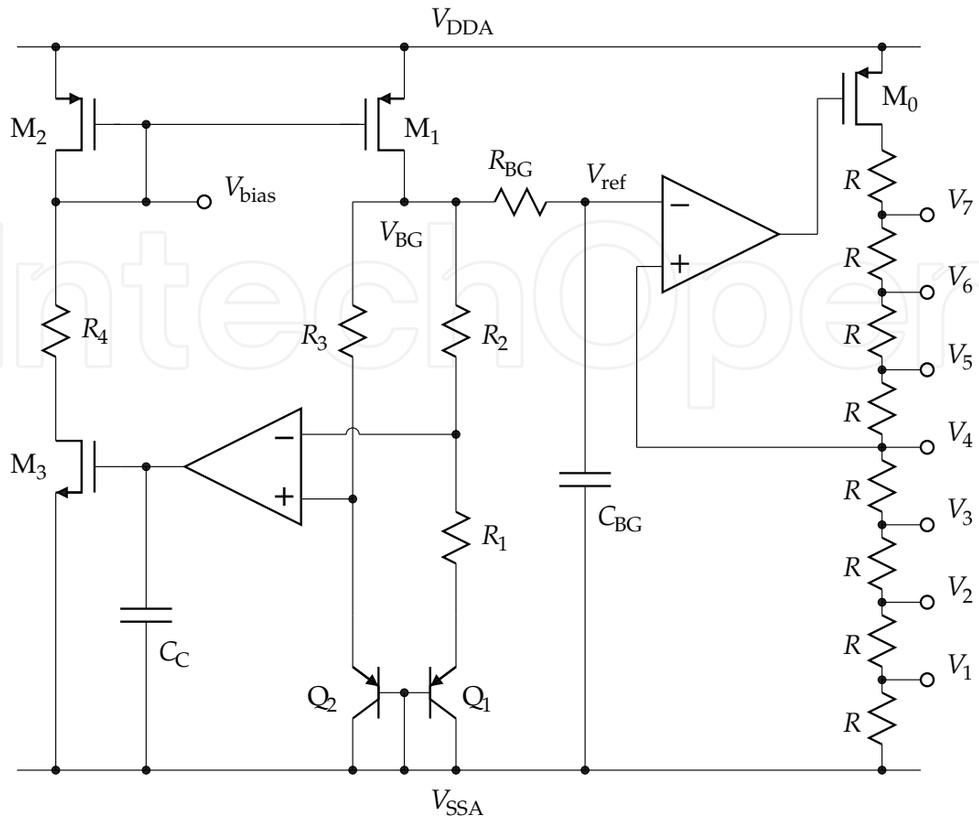

Fig. 7. Schematic diagram of the analog voltage reference.

affected by the digital switching noise superimposed to V_{DDA}, which is injected through the MOS transistor M_0.

To understand the effect of the switching noise on the whole ADC, let us consider the analog-to-digital conversion stage in Fig. 8, which is part of a pipeline converter (Rodríguez-Vázquez et al., 2003). The input voltage V_{in} is stored into a sample-and-hold circuit (S&H). A flash ADC converts the input voltage, by comparing it with each of the reference voltages and by decoding comparator outputs to obtain a binary N-bit codeword, which corresponds to the "segment" of the input range where V_{in} lies in. The 7 comparators divide the range in 8 segments, which are coded with 3 bits. The binary code is converted again into the corresponding (lower) reference voltage by a digital-to-analog converter (DAC), and the difference between the input voltage and the voltage corresponding to the N-bit code is amplified to obtain the output voltage V_{out}, which is passed to the next pipeline stage. By cascading pipeline stages, it is possible to achieve a high resolution ADC.

However, it is worth pointing out that a pipeline ADC is a "mixed-signal" circuit, where partial results from first stages must be digitally decoded and stored until the last pipeline stage has completed its operation. To operate correctly, the pipeline converter must be driven by a two-phase clock generator made up of digital gates. The clock generator acts as digital noise source, which affects the voltage references of the ADC and DAC. If the clock frequency is $f_{ck} = 100$ MHz, with rise and fall times $t_r = t_f = 100$ ps, then, according with the model presented in Sect. 2, the digital switching noise has a power spectral density with the following characteristics: it depends on the shape of the single current pulse, it becomes negligible for

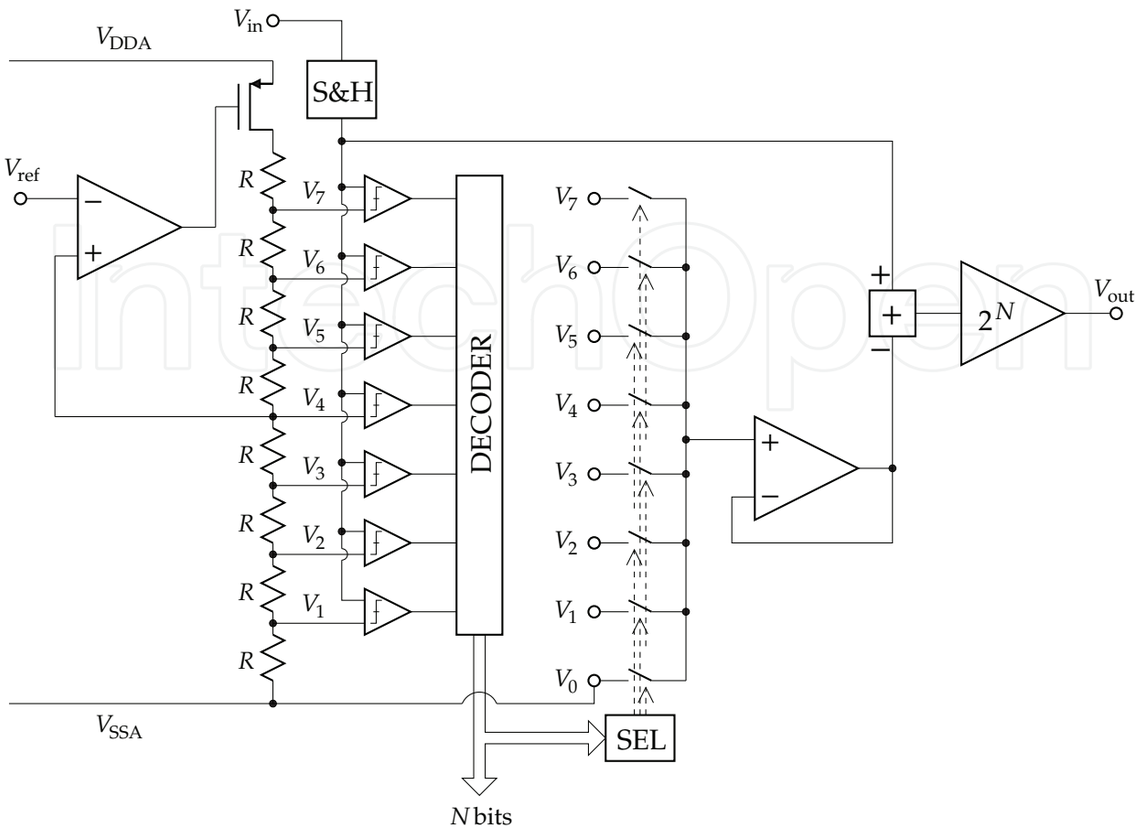

Fig. 8. Schematic diagram of one stage of a pipeline ADC, with the resistor string for reference voltage generation.

frequencies $f > 2/t_r = 20$ GHz, and it exhibits peaks at multiples of $f_{ck} = 100$ MHz (Boselli et al., 2010). The switching noise propagation through substrate and interconnections leads to fluctuations in the voltage references. Although both converters share the same voltage reference levels, ADC and DAC operations occur at different time instants. Therefore, a fluctuation of the voltages leads to an additional error, which is amplified and transferred to the next stage, thus limiting the effective number of bits.

To improve the robustness of the ADC to the digital switching noise, it is necessary to improve the power supply rejection ratio in the frequency range where digital switching noise is generated. This can be achieved by modifying the voltage reference generator, as illustrated in Fig. 9. A first improvement consists in the use of an NMOS transistor (M_0), instead of the PMOS transistor in Fig. 7. The NMOS transistor in common drain configuration increases the impedance towards the positive supply, thus improving disturbance rejection. Moreover, the addition of an on-chip decoupling capacitance (C_{dec}) between analog supplies further reduces voltage fluctuations, as noise peaks on reference voltages are inversely proportional to C_{dec} (Boselli et al., 2007).

As a further example, we consider the effects of disturbances coming from the digital section on a fully-differential voltage-controlled oscillator (VCO). The schematic diagram of the VCO is illustrated in Fig. 10 (Liao et al., 2003). To reduce the effects of digital disturbance, the VCO has a fully-differential structure and the output signal is differential: $v_1 - v_2$. Since

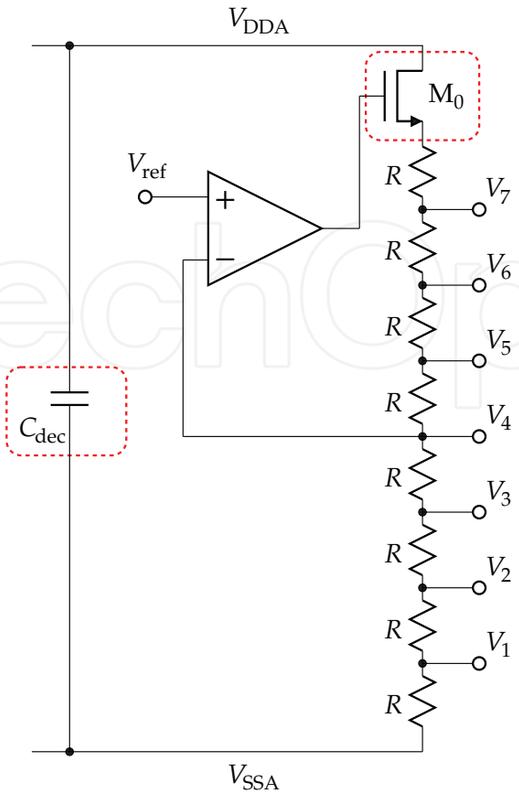

Fig. 9. Schematic diagram of the improved voltage reference generator.

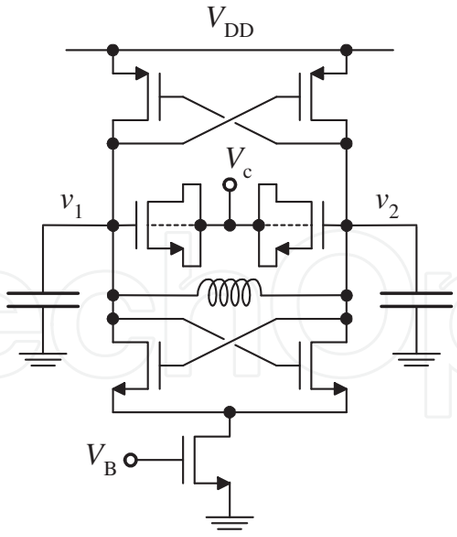

Fig. 10. Schematic diagram of the VCO.

the digital switching noise is a common mode signal, the differential output should not be affected, provided that the differential structure is perfectly matched.

Fig. 11 shows a lumped model of on-chip parasitics affecting the control voltage of the VCO (Trucco et al., 2004). The model accounts for capacitances between wires and substrate

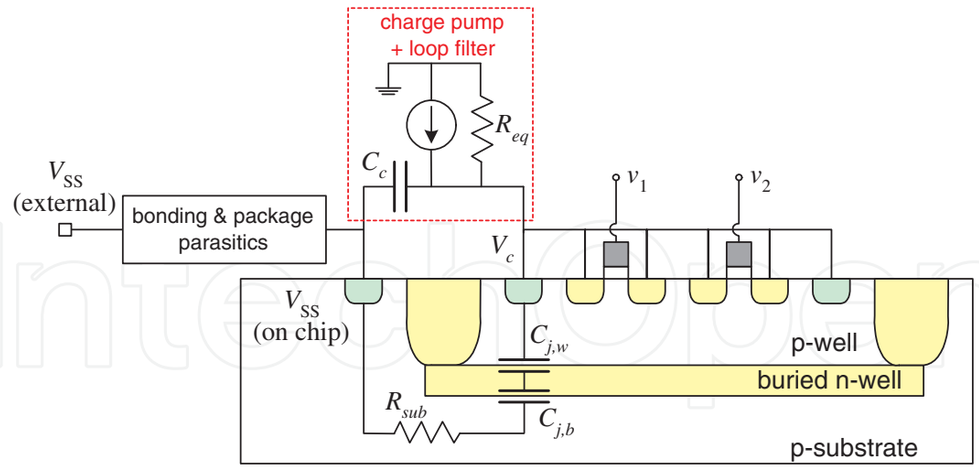

Fig. 11. Model for propagation of digital noise to the VCO through interconnections and substrate.

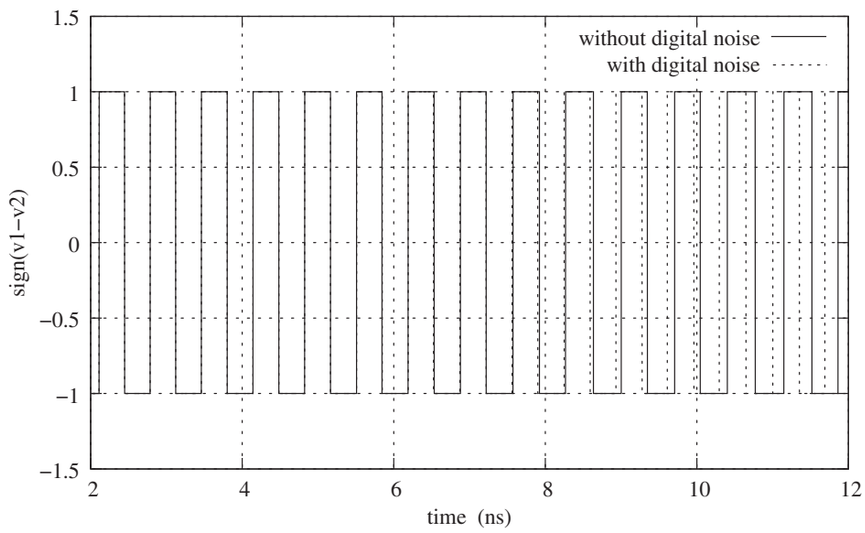

Fig. 12. Differential VCO output.

(C_c), substrate resistance (R_{sub}), well-to-well capacitance ($C_{j,w}$) and well-to-bulk capacitance ($C_{j,b}$). Although the VCO structure is differential, the control voltage V_c is a single-ended signal. Therefore, it is affected by switching noise, which propagates through interconnection parasitics and through the substrate. Simulation result shown in Fig. 12 confirm this conclusion. More details can be found in (Soens et al., 2006; Trucco et al., 2004).

4. Physical design

The IC layout must be designed to isolate the analog sensitive parts from the digital noise injecting structures.

In principle, it is possible to shield both digital and analog structures, to reduce the amount of injected noise. However, the designer must keep in mind that the best isolation strategy depends on the fabrication technology and on the package. Moreover, it is worth pointing out that in the frequency range of digital switching noise there is no integrated structure

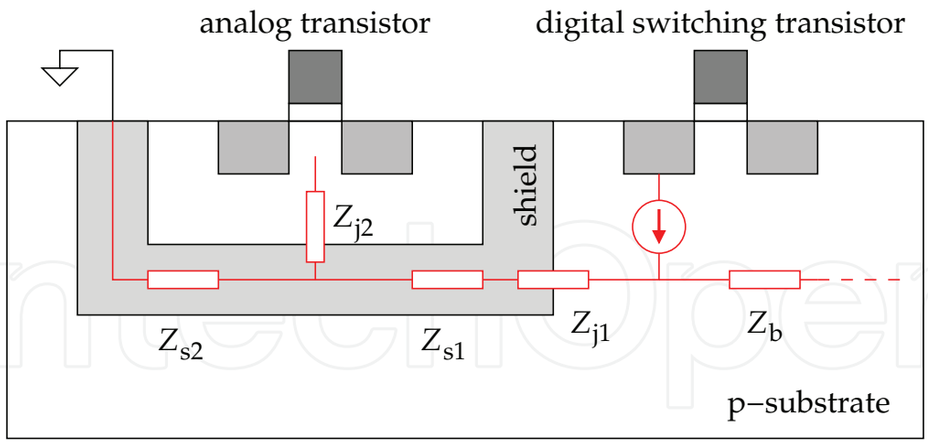

Fig. 13. Simplified cross-section of a shielding layer inserted between analog and digital parts, with equivalent impedances.

which operates either as an ideal short circuit, or as an ideal open circuit. In other words, any integrated geometry has an electrical impedance, whose value is neither zero nor infinity. Therefore, any shielding technique must be carefully evaluated, as it depends on the frequency of both signals and disturbances and on the disturbance paths from digital to analog devices. These paths can vary, due to both the fabrication technology and the frequency range of signals. A shield is obtained inserting one or more layers with different impedance, to collect noise current and to prevent disturbance from reaching sensitive devices (Jenkins, 2004). An example is triple-well shielding, where a buried n-well is used to separate the local p-wells from the p-substrate. Fig. 13 shows a triple well shielding placed around an analog MOS transistor. The shield exhibits a capacitive impedance Z_{j1} towards the p-substrate, and has a non zero resistivity, modeled with lumped resistances Z_{s1} and Z_{s2}. For an NMOS device, the impedance Z_{j2} is capacitive (due to the reverse biased junction between the p-well and the buried n-well). For this reason, triple-well shielding can be an effective technique, provided the frequency range is not too large. Fig. 14 shows a qualitative plot of the impedance of the disturbance path as a function of the frequency. On the contrary, for PMOS transistors, triple-well shielding can be harmful, as the impedance Z_{j2} is mainly resistive (Rossi et al., 2003). Shielding is less effective in heavily doped substrates, as the low resistivity of the bulk propagate disturbance across the whole chip (Liberali, 2002).

In lightly doped substrates, guard rings provide effective isolation, as disturbance paths are near to the silicon surface. Guard rings around noise sources provide a low resistance path to ground for the noise; therefore, they help minimizing the amount of noise injected into the substrate. Again, efficiency of guard rings depends on the frequency range of injected noise and on package inductance.

The relative position of analog and digital cells with respect to each other on the same die is an important issue to consider. In lightly-doped substrates, physical separation helps in reducing crosstalk.

On-chip interconnections can provide additional paths for injected disturbance. In a careful design, the voltage supplies of the analog and of the digital sections must be completely separated, and also pad rings and ESD protections should have their separate supplies.

Packaging affects performance and reliability in mixed-signal integrated circuits. One of the most common used assembling technology is chip-in-package. When using this assembling

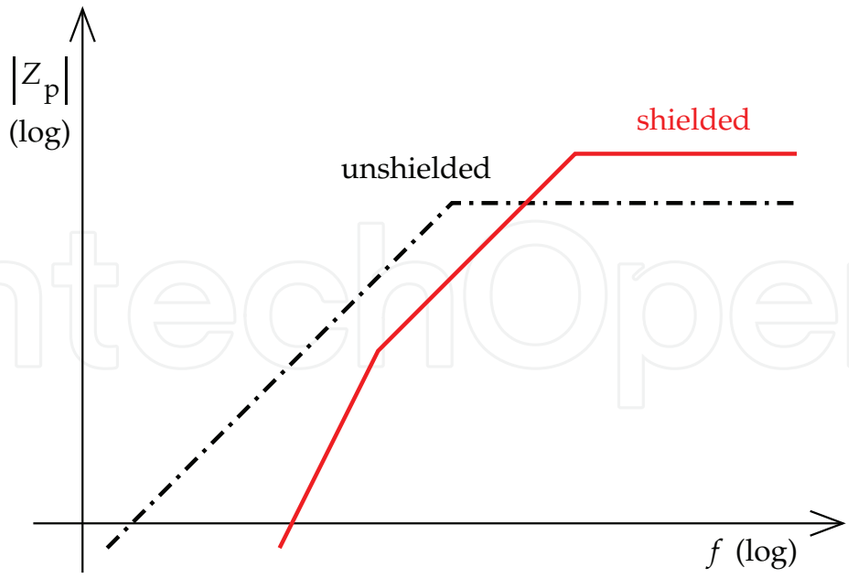

Fig. 14. Qualitative plot of the impedance from the digital noise source to the sensitive analog device.

technique, the designer should account for both bondwires and package parasitics. When the digital part operates at high speed, inductive effects are a major source of performance degradation. Multiple bonding helps in achieving a further reduction of parasitic equivalent bondwire inductances (Ferragina et al., 2010). An assembling technology without bondwires (flip-chip mounting) has even better noise immunity, due to reduced parasitic elements, and must be considered for high-performance mixed-signal integrated systems. However, it is worth noting that interconnection parasitics due to the circuit board remain unchanged.
Finally, special post-processing techniques for 3-D insulation of parts of the chip can be helpful for critical applications, at the expense of additional wafer cost (Chong & Xie, 2008).

5. Conclusion

This chapter has presented some aspects of digital noise in mixed-signal CMOS ICs.
Digital switching noise can be modeled as a stochastic process. By considering switching activity of logic gates as a random process, with transition instants randomly distributed in time, digital switching currents can be modeled as shot noise processes, and small signal analysis techniques can be applied to evaluate their impact on analog structures.
As a general rule, crosstalk between digital and analog sections increases with size reduction and with clock frequency. Design techniques for crosstalk reduction are essential for high-performance integrated systems. Differential structures and on-chip decoupling capacitances can be helpful in reducing disturbance, thus improving crosstalk immunity. A correct design approach should be based on a top-down methodology, including a crosstalk analysis from early design stages, to improve the robustness and to reduce the risk of failure.
Physical design is also very important, since noise propagation depends on fabrication and assembling technologies. Therefore, rules for the "best" mixed-signal design are technology-dependent, and, in general, design portability is not guaranteed with respect to crosstalk robustness.

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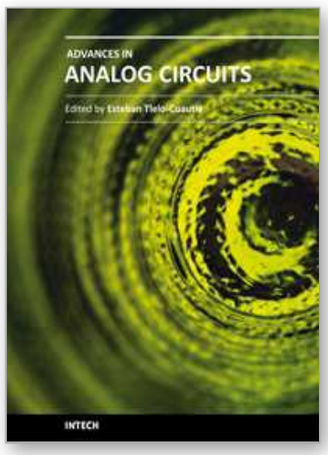

Advances in Analog Circuits

Edited by Prof. Esteban Tlelo-Cuautle

ISBN 978-953-307-323-1
Hard cover, 368 pages
Publisher InTech
Published online 02, February, 2011
Published in print edition February, 2011

This book highlights key design issues and challenges to guarantee the development of successful applications of analog circuits. Researchers around the world share acquired experience and insights to develop advances in analog circuit design, modeling and simulation. The key contributions of the sixteen chapters focus on recent advances in analog circuits to accomplish academic or industrial target specifications.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Gabriella Trucco and Valentino Liberali (2011). Analog Design Issues for Mixed-Signal CMOS Integrated Circuits, Advances in Analog Circuits, Prof. Esteban Tlelo-Cuautle (Ed.), ISBN: 978-953-307-323-1, InTech, Available from: http://www.intechopen.com/books/advances-in-analog-circuits/analog-design-issues-for-mixed-signal-cmos-integrated-circuits

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