3

New Port Modeling and Local Biasing of Analog Circuits

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1. Introduction

In today's high-speed technology, analog and mixed signal integrated circuit technology has an important and decisive place in communication and signal processing. In particular with CMOS technology rapidly embracing the field, analog circuit design has become more challenging than ever [1–8]. Other developments in the technology such as lower supply voltages, low-power consumption, performance complexity, and high transistor counts have substantially increased the demand for new design methodologies and techniques.

A major difficulty in dealing with analog circuits is the DC biasing – getting desirable operating points with quick convergence; and the problem is getting worse with the advancement of the technology which is due to increase in size and circuit complexity. The analysis may even lead to multiple DC operating points, or instability in the operating points caused by positive feedbacks [9, 10]. In SPICE circuit simulator [3, 4], for examples, methods such as Newton-Raphson iteration techniques are employed to deal with nonlinearities; the major difficulty sometime is to get the circuit to converge within a limited number of iterations. Schemes such as adding minimum conductance (GMIN), shunt resistors, changing the tolerance values for the results, and supply stepping are typically adopted in the simulator to make the convergence possible.

There are several causes for these problems. A major difficulty arises from the fact that, in traditional methods, an analog circuit is usually analyzed and simulated as a whole – with the linear and nonlinear components all together. Usually a poor selection of initial conditions or adopting large and unregulated steps of iterations cause instability or it may even cause the circuit to diverge. Another difficulty can result from a fixed circuit topology with fixed DC supplies throughout the biasing procedure. With such a pre-setting conditions the operating points are naturally found through long and timely iterations. All this adds up to the design burden and timely process. We need a more guided design procedure; a procedure that helps a designer to go through a top-down and piece-by-piece design strategy.

The objective in this chapter is to introduce such a guided design procedure for biasing. The purpose is to use a "divide and concur" strategy for a better handling the case. This strategy separates linear and nonlinear portions of an analog circuit, and takes more control of the nonlinear portions. This separation of portions (components) within the circuit is accomplished by introducing a new port modeling that nullifies the ports of nonlinear

devices. This in turn leads to a new biasing technique for nonlinear components. The result is to replace the regular DC supplies with alternative supplies that are directly attached to the nonlinear devices. It is shown that a unique and very powerful additivity property takes charge in performing this component biasing operation. Another useful property using this strategy is the removal of nonlinearity in the biasing design. This is done because being locally biased the nonlinear components can be replaced with their linear models operating at those Q-points; hence making the biasing design of the circuit entirely linear. However, one major drawback that exists in using local biasing is the sheer number of DC supplies needed in local biasing. There are source transformations methods that help to reduce these supplies and possibly end up with the regular circuit supplies. As discussed in the next chapter, one direct and simple technique is introduced that removes the distributed local biasing sources all together and replaces them with the regular supplies, such as V_{DD} or V_{CC}, in a single step. Finally, because the proposed strategy offers a complete isolation of individual nonlinear devices (transistors), it makes it possible to modify, adjust and tune the circuit locally without disturbing the rest of the circuit.

Another important outcome of this methodology is that it provides an ability to control and reduce power consumption in a circuit. It is shown that by local biasing nonlinear devices we actually reduce the DC power to its minimum – just enough to get the devices biased. In other words, by locally biasing we are totally cutting off the DC power from entering the linear elements in the circuit.

1.1 Thevenin and Norton equivalent circuits

Thevenin and Norton equivalent circuits, also known as Thevenin and Norton models, are two known conventional models that explain terminal behavior of linear circuits. They are crucial for circuit analysis, replacing a terminal port with a source and an impedance [11]. Both Thevenin and Norton models are very useful circuit simplification techniques that are often used in order to concentrate only on the terminal behavior of certain linear portion of a circuit that normally supplies power or signal to the rest of the circuit. In general, both models are used in different circuit analysis and applications such as, in source transformation, DC analysis, Transform (frequency or phasor and s-domain) analysis [1, 6]. Here we limit our discussion to DC analysis only. Figure 1(a) represents a two terminal linear resistive circuit, N, with both independent and internally-dependent sources; and Figs. 1(b) and (c) are the Thevenin and Norton models of N, respectively. Where, V_{Th} represents the open-circuit voltage and I_N is the short-circuit port current in the original circuit. For R_{eq}, we can either remove all independent sources from the circuit and calculate the port resistance, or alternatively get R_{eq} from Eq.(1).

$$R_{eq} = \frac{V_{Th}}{I_N} \tag{1}$$

Example 1: Figure 2(a) shows a simplified small signal equivalent circuit of a single stage BJT amplifier with the virtual biasing supplies included. The Thevenin model for the amplifier looking from the output port is given in Fig. 2(b). Figure 2(c) shows the port's characteristic curve (line), indicating the circuit linearity. The figure also shows how we can move from the Thevenin model, specified by point T(2.5V, 0), to the Norton model, given as point N(0, 1.25mA) on the characteristic line.

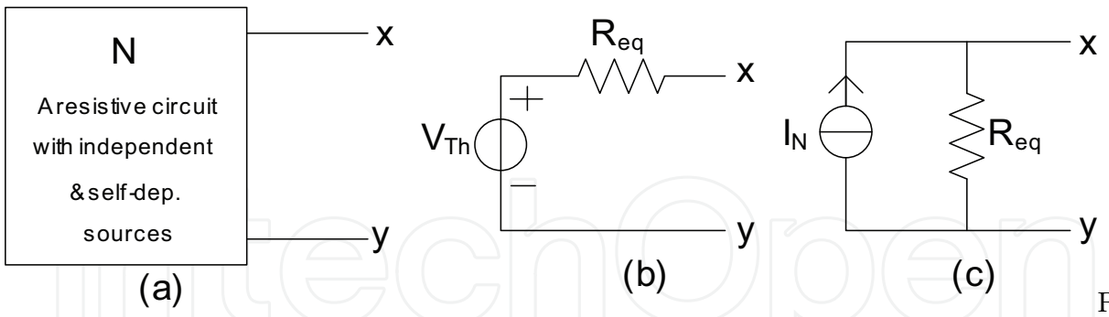

Fig. 1. (a) A two terminal linear resistive circuit; (b) Thevenin, and (c) Norton equivalent circuit.

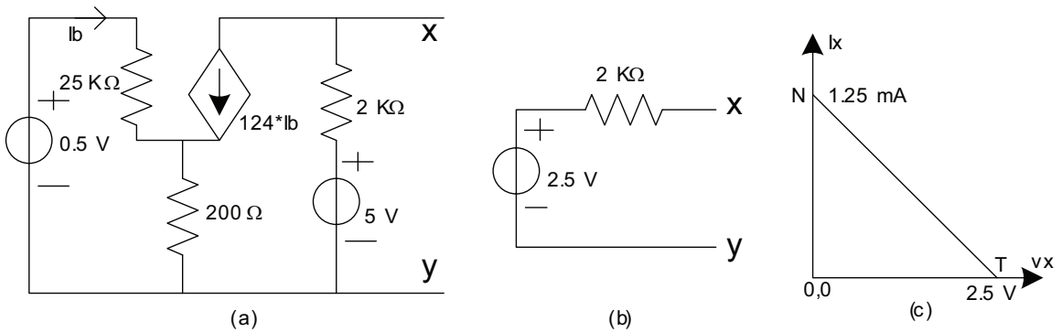

Fig. 2. (a) A simplified small signal equivalent circuit of a single stage BJT amplifier; (b) the Thevenin equivalent circuit; (c) the port's characteristic curve, indicating the linearity.

However, despite their simplicity, there is a rigidity involved in port representation by either the Thevenin or Norton equivalent circuits. As indicated in Fig. 2(c), Thevenin or Norton model occupy only one point on the characteristic line, where the line meets one of the axis. This characteristic line also serves as a load line in some biasing situations, where it identifies the port's operating point (Q-point) when the two characteristic curves from both sides of the port cross. The limitation for Thevenin or Norton model is that it represents only the "sourcing" network with no information given about the "target" network, unless the two are connected and the analysis is done with the combined circuit. This of course fits with most circuit applications where all we need is a simplified two terminal linear circuit that gets connected with the target circuit for the rest of the process; but again, we perform the analysis only when the two are combined. The circuit complexity created this way may not be so evident for a single port connection, but for multiple ports the complexity may get quite significant. There are other cases where circuits in both sides of a port need to get engaged in some (sources or components) exchanges; hence a more dynamic port modeling may be needed. Examples can be found in source transformation, noise-source modeling, and power transport cases. Port nullification is another example that uses *Hybrid modeling*, as discussed next.

2. Hybrid equivalent circuit

A Hybrid equivalent circuit, or simply an H~-model, of a two-terminal network is a generalized version of Thevenin or Norton equivalent circuit; for resistive circuits it consists

of a voltage source, a current source and an equivalent resistance, R_{eq}, which is identical th that in the Thevenin or Norton model. Apparently here one source, V_H or I_H, can be selected arbitrarily and the other source is found through Eq(2).

$$I_H = I_N - \frac{V_H}{R_{eq}} \quad \text{or} \quad V_H = V_{Th} - I_H R_{eq} \tag{2}$$

Note that, like the Thevenin or Norton models, here only two measurements are needed to get all H~-model parameters. For example, for a selective value of I_H and two measurements of V_{Th} and I_N, Eqs. (1) and (2) can be used to obtain R_{eq} and V_H for the model. Now, consider two networks N_1 and N_2 connected through port j(V_j, I_j), as shown in Fig. 3. There are two types of H~-models for the linear two terminal network N_1. Type 1 H~-model is shown in Fig. 4(a). To find this model first open circuite the port where $I_j = 0$. By referring to Fig. 4(a) and considering Eq.(2) we get

$$V_j = V_H + I_H R_{eq} = V_{Th} \tag{3}$$

Next, short circuit the port terminals to get $V_j = 0$, and find

$$I_j = I_H + V_H / R_{eq} = I_N \tag{4}$$

In Type 2 H~-model, however, the sources remain the same as in Type 1, but instead of calculating the equivalent resistance R_{eq} we let N_1 remain unaltered except all its DC power supplies are removed, as shown in Fig. 4(b). The term "*DC power removed*" means that all

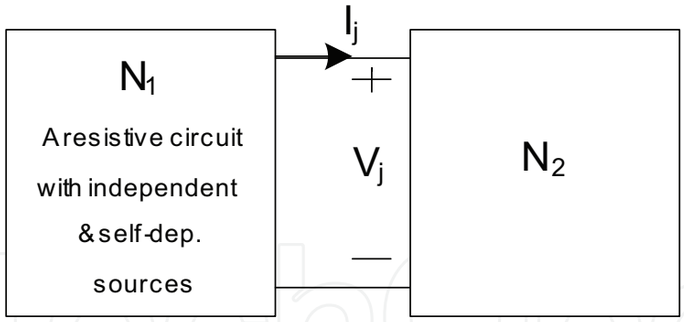

Fig. 3. Two networks N_1 and N_2 connected through a port j(V_j, I_j).

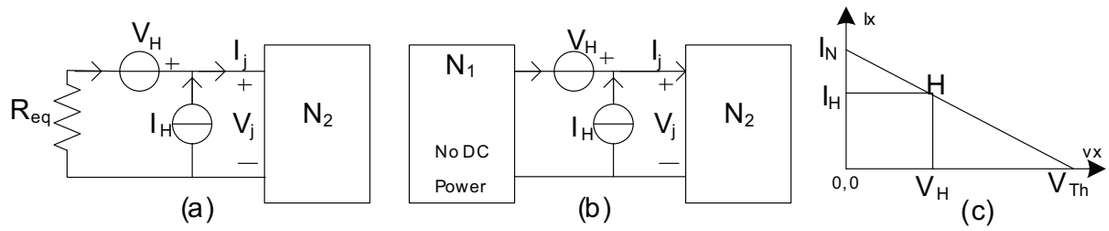

Fig. 4. A two-terminal Hybrid equivalent circuit for N_1; (a) Type 1 representation; (b) Type 2 representation; (c) the location on the port's characteristic curve.

independent DC supplies are removed from N_1, including charges on the capacitors and currents through the inductors. Type 2 H~-model is useful in a number of applications, such as moving the DC sources in a circuit to its port terminals without disturbing the internal structure (topology) of the network.

Note that, because of having two sources instead of one, an H~-model represents an axis of freedom that acts as a tool in dynamic modeling of a port. As indicated in Fig. 4(c), an H~-model covers a full and continuous range of equivalent circuits for a two-terminal network. It is evident from Eq. (2) and Fig. 4(c) that both the Thevenin and Norton models are two special cases of an H~-model.

Example 2: Figure 5(a) shows the same circuit given in Example 1 (Fig. 2(a)), except this time the x-y port is connected to a load R_L. Here we would like to have: i) an H~-model for the two terminal circuit, on the left of x-y, so that the power consumption on both sides of the port are equal; and ii) modify the H~-model in part i) so that the power consumption in the two terminal circuit (the left of x-y) becomes zero.

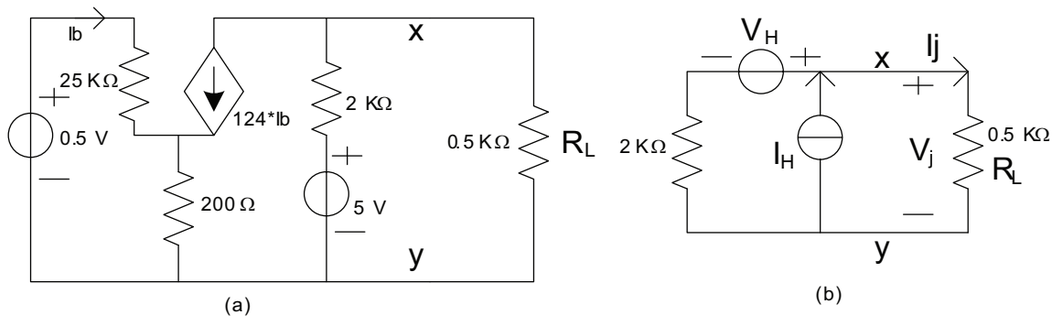

Fig. 5. (a) A simplified small signal equivalent circuit of a single stage BJT amplifier with load; (b) an H~-model of the amplifier.

Solution: We first find an H~-model representation for the two-terminal circuit as depicted in Fig. 5(b), with the source values, V_H and I_H, unspecified. Second, to make the power consumption on both sides of port j equal we need to have

$$R_L I_j^2 = R_{eq}(I_H - I_j)^2$$

By using Eq.(2), and knowing that V_{Th} = 2.5V and R_{eq} = 2KΩ we get $I_j = 1\ mA$, $I_H = 1.5\ mA$, $V_H = -0.5\ V$, and the power consumed for each side is $W_j = 0.5\ mW$.

For part ii), because the situation for the load R_L is not changed we still have $I_j = 1\ mA$, $V_j = 0.5\ V$, and $W_j = 0.5\ mW$. Now, to make the power consumption to the left of X – Y zero we must have $R_{eq}(I_H - I_j)^2 = 0$; or simply $I_H = I_j = 1\ mA$, and as a result $V_H = V_j = 0.5\ V$. This concludes the solution with the fact that in the part ii) the total power consumption is reduced to half, i.e., from 1.0 mW to 0.5 mW.

2.1 Universality

Universality is an important property of an H~-model. H~-models can be accurately applied to all possible cases of linear two-terminal networks, regardless of the port impedances; whereas both Thevenin and Norton equivalent circuits lose their sensitivity in some specific

cases where port impedances take extreme low or extreme high values. For example, consider measuring the Thevenin (open circuit) voltage of a two terminal network N_1 that has the equivalent resistance of R_{eq} = 2 MΩ. Suppose the measuring voltmeter has the input impedance of R_M = 20 MΩ and the measured open circuit voltage displayed is V_M = 3V. Apparently selecting $V_{Th} = V_M$ = 3V as the Thevenin voltage for the port carries an error of 10%. Whereas, an H~-model with $V_H = V_M$ = 3V and $I_H = I_M$ = 136nA represents an exact H~-model for the port. Note that there is no need for any extra measurement to find I_M, because we can simply get it from $I_M = V_M/R_M$.

3. Input-referred noise using hybrid models

H~-model representation can be very helpful in noise analysis, particularly in the input-referred noise calculations [12]. It simplifies and produces uniformity in noise analysis by using only one noise model for all possible cases, dealing with different values of the source impedance R_S and the amplifier input impedance R_{in}.

Let us consider an amplifier with a gain factor of G and input impedance R_{in}, shown in Fig. 6(a). Because noise is more conveniently measurable at the output port of a circuit we can represent the output noise of the amplifier in its *power spectrum density,* denoted by $V^2_{o,n}(f)$ in V^2/Hz. However, to specify a measured output noise we need to have a frequency band. For simplicity, suppose the measurement frequency bandwidth is $B = f_H - f_L$ Hz; where f_H and f_L are the high and low frequency of the spectrum, respectively. With relatively constant (within -3 dB) gain factor within the bandwidth the measured output noise can be found as:

$$V^2_{o,n,rms} = B V^2_{o,n}(f) \tag{5}$$

On the other hand, depending on the type of input signal to the amplifier, the gain factor G can be considered as a voltage gain A or as a trans-impedance R_M depaeding on the input voltage or current representation, respectively. Next, to calculate the input-referred noise of the amplifier[1] we need to attenuate the output noise by the gain factor G to bring it into the input loop of the amplifier. The question is how this input-referred noise must be represented when transferred into the input loop: as a voltage source, a current source, or in combination of the two? It of course depends on the values of the two parameters: the source impedance R_S and the amplifier input impedance R_{in} [12]. Note that our objective here is to find the input-referred noise of the amplifier that corresponds to the measured noise at the open circuit output port. Hence, the assumption is that the thermal noises associated with R_S, R_{in} and the amplifier output impedance, among others are all included in the process, and there is no need to separately calculate and add up to the input-referred noise. However, exception might arise for a case where the source input impedance is not included in the output noise measurement. In such a case, because of linearity, the thermal noise of R_S must be added to the input-referred noise to get the final response. In our analysis, however, we assume the inclusive case, i.e., the entire amplifier noise, including that of R_S, is all measured at the amplifier output port.

[1]Input-referred noise is a virtual input noise that creates $V_{o,n,rms}$ at the output, in case the amplifier is noise free.

3.2 Input-referred noise computation

We first consider the case where the input-referred noise is represented either as a voltage source or as a current source. The two choices are depicted in Figs. 6(b) and (c), and the values of the input-referred noises are expressed in Eqs. (6) and (7), respectively. To simplify this representation, again, we assume the thermal noise from R_S, as well as other noise components, to be included in $V_{i,n,rms}$ or $I_{i,n,rms}$.

$$V_{i,n,rms} = \frac{R_{in} + R_S}{AR_{in}} V_{o,n.rms} \tag{6}$$

$$I_{i,n,rms} = \frac{R_{in} + R_S}{AR_{in}R_S} V_{o,n.rms} \tag{7}$$

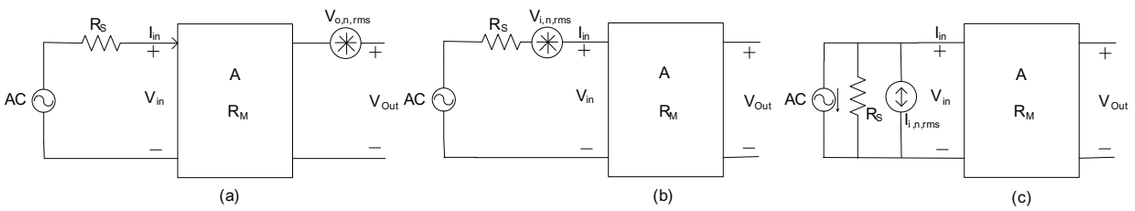

Fig. 6. (a) An amplifier with a gain factor of G (A or R_M), and input impedance R_{in}, and the measured output noise $V_{o,n.rms}$; (b) the input-referred noise as a voltage source; (c) the input-referred noise as a current source.

However, in a special case where R_S or R_{in} gets an extreme (low or high) value the situation may become different so that Eq.(6) or Eq.(7) may not produce the correct response as discussed below.

1. For a very low value of R_S the input-referred noise is represented by a voltage source (Fig. 6(b)) calculated by using Eq. (6) as

$$V_{i,n,rms} = \frac{V_{o,n.rms}}{A} \tag{8}$$

For the case when both R_S and R_{in} are very small we get the ratio $\alpha = R_S/R_{in}$ and from Eq. (6) we can get

$$V_{i,n,rms} = \frac{1+\alpha}{A} V_{o,n.rms} \tag{9}$$

2. For very high value of R_S the input-referred noise is represented by a current source (Fig. 6(c)) calculated by using Eq. (7) as

$$I_{i,n,rms} = \frac{V_{o,n.rms}}{AR_{in}} \tag{10}$$

For the case when R_{in} is very small the gain facto G can be represented by the trans-impedance R_M; the input-referred noise is obtained as

$$I_{i,n,rms} = \frac{V_{o,n.rms}}{R_M} \tag{11}$$

3. For the case when both R_S and R_{in} are very large and they approach infinity there is an ambiguity in the circuit and a rational solution cannot be pursued. This is because we are basically pushing current through an open circuit! However, for large but limited values of R_S and R_{in}, either Eqs. (6) or (7) can provide the input-referred noise. For example, we can use Eq. (9) to get $V_{i,n,rms}$.

3.2 Use of H~-models in noise computation

The problem with the foregoing procedure is that in each case we need to know the range of values of R_S and R_{in} in order to decide on the circuit topology; hence, decide on the right type of the input-referred noise source. This definitely makes the analysis rather impractical. It is only in an H~-model representation that all cases discussed above can be combined and integrated into one. An H~-model can simply provide a universal and accurate model for the noise calculation, regardless of the value of R_S or R_{in}. Figure 7 shows an H~-model representation of the input-referred noise for the selected amplifier. As shown, we can use both types of input-referred noise sources in Fig. 7 to calculate the output noise, as shown below.

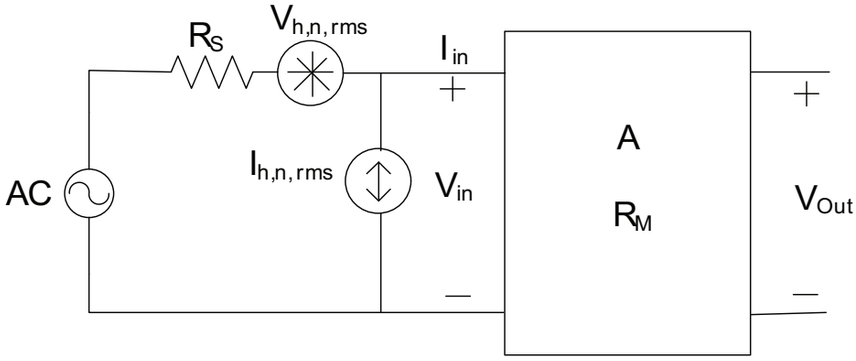

Fig. 7. Use of H~-modeling for computation of input-referred noise.

$$V_{o,n,rms}^2 = V_{h,n,rms}^2 \left(\frac{AR_{in}}{R_S + R_{in}}\right)^2 + I_{h,n,rms}^2 \left(\frac{AR_S R_{in}}{R_S + R_{in}}\right)^2 \tag{12}$$

Equation (12) can be written as

$$V_{Th,n}^2 = V_{h,n,rms}^2 + I_{h,n,rms}^2 R_S^2 \tag{13}$$

Where $V_{Th,n}$ is the Thevenin noise voltage at the input loop, and is given by

$$V_{Th,n} = V_{o,n,rms} \frac{R_S + R_{in}}{AR_{in}} \tag{14}$$

A comparison between Eq. (13) and Eq. (2) reveals that Eq. (13) is, indeed, the result of H~-modeling of the input-referred noise; except that the representation here is in terms of noise power rather than the noise voltage or current values.

$V_{h,n,rms}$ and $I_{h,n,rms}$ can be found using Eqs. (13) and (14) with $R_S = 0$ and $R_S = \infty$, respectively. This results in

$$V_{h,n,rms} = \frac{V_{o,n,rms|Rs=0}}{A} \text{ and } I_{h,n,rms} = \frac{V_{o,n,rms|Rs=\infty}}{AR_{in}} \tag{15}$$

Here $V_{o,n,rms|Rs=\infty}$ stand for the output noises obtained when the amplifier input port is open circuited; similarly, $V_{o,n,rms|Rs=0}$ stand for the output noises obtained when the amplifier input port is short circuited. We are now ready to show that for all the cases discussed earlier (with different values of R_S and R_{in}) the proposed H~-model can be exclusively used to calculate the input-referred noise. For example, for R_S = 0 we get from Eq. (13) that $V_{Th,n} = V_{h,n,rms} = V_{i,n,rms}$, and from Eq. (14) we get $V_{i,n,rms} = \frac{V_{o,n.rms}}{A}$ which is the same as Eq.(8). For R_S very large by combining Eqs. (13) and (14) we get $V_{Th,n} = V_{o,n,rms}\frac{R_S + R_{in}}{AR_{in}} = I_{h,n,rms}R_S = I_{i,n,rms}R_S$, which simply results in $I_{i,n,rms} = \frac{V_{o,n.rms}}{AR_{in}}$, which is the same as given in Eq. (10).

Example: 3 - Consider an amplifier with a voltage gain of A = 40 dB, source impedance R_S = 2 KΩ and the input impedance R_{in} = 8 KΩ. The output noise is measured for two cases of R_S and $R_S = \infty$ and for a bandwidth of 300 MHz. For R_S we measure $V_{o,n,rms|Rs=0}$ = 200 μV, and for $R_S = \infty$ we measure $V_{o,n,rms|Rs=\infty}$ = 400 μV. Calculate i) the hybrid noise voltage and current for the input-referred noise $V_{h,n,rms}$ and $I_{h,n,rms}$; ii) $V_{Th,n}$, iii) and the overall output noise $V_{o,n,rms}$.

Solution – The amplifier gain is A = 100 V/V. From Eq. (13) we get

$V_{h,n,rms}$ = 200/100 = 2 μV, and $I_{h,n,rms}$ = 400/(100*8) = 0.5 nA.

From Eq. (13) $V_{Th,n}^2$ = 4.0e-12 + 0.5e-18 * 4.0e+06 = 6.0e-12.

Which results in $V_{Th,n}$ = 2.45 μV.

Next, from Eq. (14) we get $V_{o,n,rms}$ = 2.45 * 100 * 8/10 = 200 μV.

4. Nullified Hybrid equivalent circuit

A Nullified Hybrid equivalent circuit, called H-model, is an especial case of an H~-model; where, the values of the voltage and current sources in the model are identical to the corresponding port voltage and current values. What this means is that the sources in an H-model are representing the biasing situation of the corresponding port. For example, take the case of Fig. 3, where the network N_1 provides the voltage V_j and the current Ij to bias the network N_2. The two models for this example are shown in Figs. 8(a) and 8(b). Note that Figs. 8(a) and 8(b) are identical to Figs. 4(a) and 4(b) except here the model-sources represent the port values. Note also from Fig. 8 that, as a result of H-modeling another port, k(V_k, I_k), is created across N_1, where both V_k and I_k are zero. Port k(V_k, I_k) is called a "null" port and the process of creating it is called "port nullification", as will be discussed shortly.

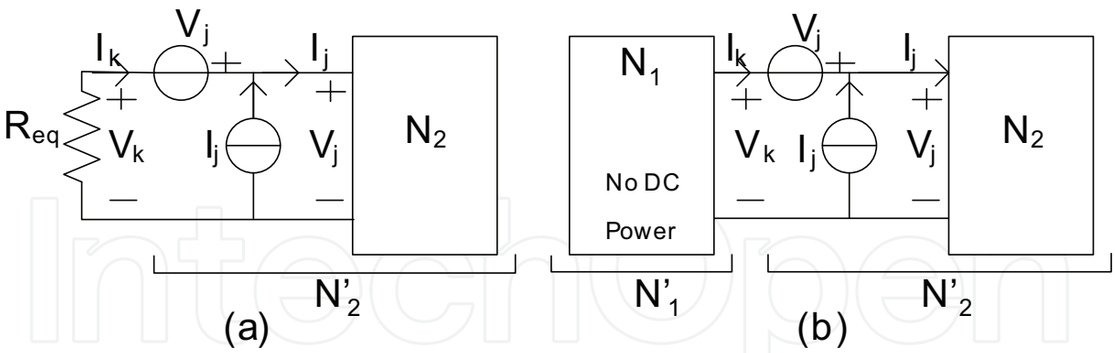

Fig. 8. An H-model for a two terminal N_1; (a) Type 1 representation; (b) Type 2 representation.

Theorem 1 introduces an important property of an H-model dealing with power distribution in a network [13]. It adds an extra dimension to the power analysis and power segmentation in a network.

Theorem 1: Consider a network N_2 connected to another network N_1 through a port $j(V_j, I_j)$, as in Fig. 3. Replacing N_1 with its Type 1 or Type 2 H-model reduces the power consumption in N'_1 to zero, while the power consumption in N_2 remains unchanged.

Proof: Consider the H~-model in Fig. 4(a) or 4(b). Both sources, I_H and V_H, provide power to networks N_1 and N_2. The power delivered to N_2 is fixed and it amounts to $P_2 = V_j * I_j$; whereas in Type 1 H~-model the power consumed for N_1 (Fig. 4(a)) is $P_1 = R_{eq}(I_H - I_j)^2$. Hence, the power P_1 in N_1 becomes zero if $I_H = I_j$ which also results in $V_H = V_j$. For Type 2 H-model however, notice from Fig. 8(b) that N'_1 has no DC supply to get power from, plus its port is also nullified. Therefore, all currents and voltages inside N'_1 must be zero, resulting in zero power consumption.

Port Nullification: Consider a network N_2 connected to another network N_1 through a port $j(V_j, I_j)$ as shown in Fig. 3. One way to *nullify* Port j is to augment the port from both sides (N_1 and N_2) by current sources I_j and voltage sources V_j as depicted in Fig 9. The result is the creation of another port $k(V_k, I_k)$ that, by definition, is a null port, i.e., both I_k and V_k are zero.

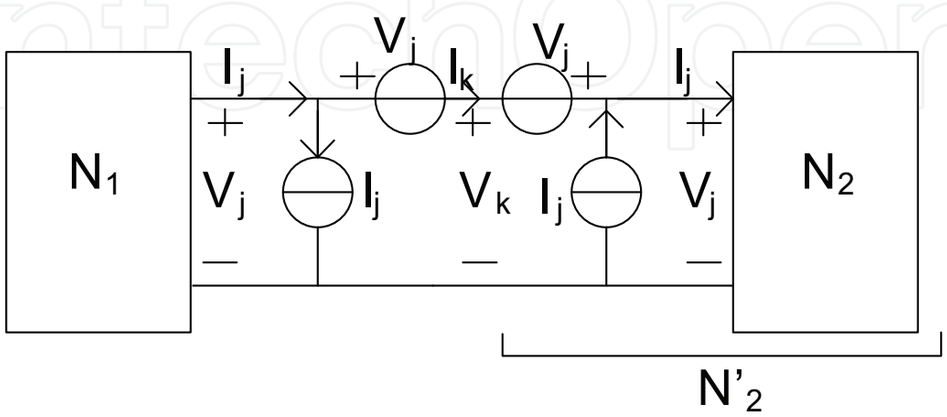

Fig. 9. A simple port nullification procedure with no change imposed on N_1 or N_2.

However, there is an alternative method to create a null port when two networks N_1 and N_2 are connected through a port j(V_j, I_j), shown in Fig. (3). Here we can simply replace N_1 with its H-model (Type 1 or Type 2) and create the null port k(v_k, i_k), as depicted in Fig. 8. Note that as a result of port nullification procedure, shown in Figs. 8 and 9, an extended network, N'_2, is created that contains N_2 plus the sources belonging to the H-model. Similarly, another network N'_1 is also created, on the left hand side, when the H-model loses its sources. As we can see it later, these extended networks are of particular importance in circuit biasing.

Note that the characteristic curves of ports j and k are identical except for shifts of v and i, coordinate axis, from the origin to the $Q_j(V_j, I_j)$ point. This makes the operating point $Q_j(V_j, I_j)$ to fall on the origin, creating a new operating point $Q_k(0, 0)$ for the port k, shown in Fig. 10. This simply means that, for any pair of networks, N_1 and N_2, connected through a port j it is always possible to nullify the port and change N_1 and N_2 to N'_1 and N'_2, where N'_1 and N'_2 are identical to N_1 and N_2, except the v and i coordinate axis are move to the port's operating point. This is stated in Property 1.

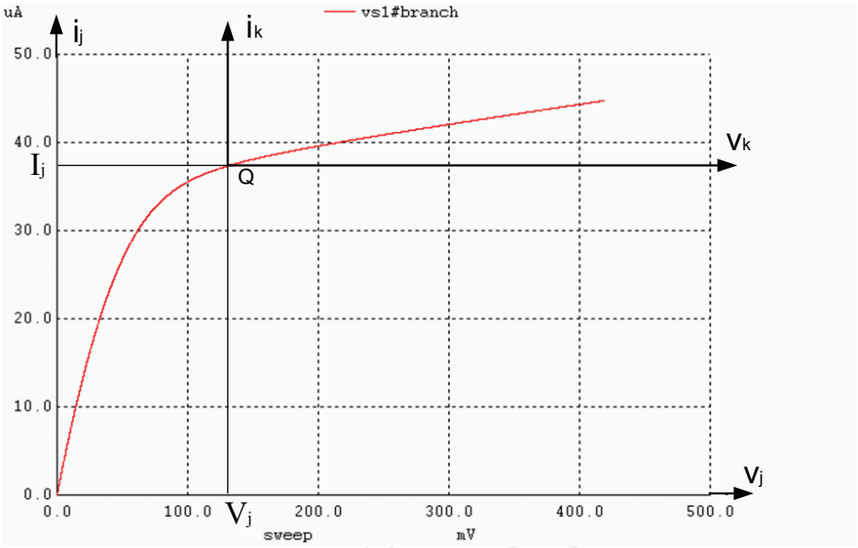

Fig. 10. The i-v coordinate axis moved from (0, 0) for the j port to a new position, $Q_j(V_j, I_j)$, for the k port.

Property 1: Consider two networks N_1 and N_2 connected through a port j, as in Fig.3. If port j is null then the i-v characteristic curve of the port, looking through either network, passes through the origin and the origin is the operating point of that port. In case port j is not null it is always possible to nullify the port to get the corresponding networks N'_1 and N'_2 with a null port k, as shown in Fig.8.

Example 4: Consider the circuit of Fig. 11(a), where two sections of a circuit are connected through a port j(V_j, I_j). Let the MOS diode be characterized by $i = K (V-1)^2$ mA for $V > 1$V, and let $K = 0.5$ mA/V^2. The analysis shows that port j is not a null port because $I_j = 1$ mA and $V_j = 3$ V. Next, we augment port j of N_2 by two current and voltage sources $I_j = 1$ and $V_j = 3$ V and then remove the supply sources of 5 V and 1 mA from N_1. As a result a new null port k(V_k, I_k) is created, as shown in Fig. 11(b). Note that although the i–v characteristic curve of port j (associated with both networks) does not pass through the origin that of port

k does (property 1). In addition the Q-point of port k is located at the origin, as expected. Note that i) the network N'_1, on the left hand side, is still linear, and ii) the new port k has an i–v characteristic curve that passes through the origin, and the origin is also the Q-point for the port. This simply means that the Thevenin equivalent circuit of N'_1, looking from port k, must be a resistance with no source attached to it.

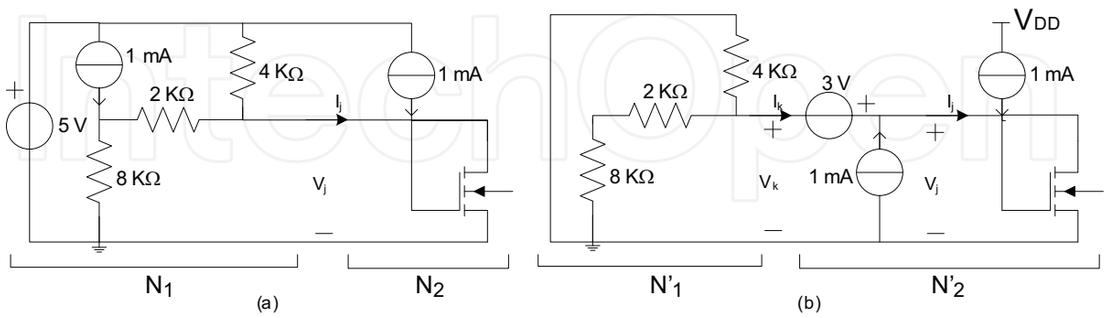

Fig. 11. (a) Example of two networks N_1 and N_2 separated by a port j; (b) creation of a null port k in an H-modeling representation.

5. H-modeling in multi-port networks

H-model is also capable of representing a multi-port network; and this representation is of Type 2, introduced in Section 4. Consider a linear network N_1 connected to another network N_2 through n-ports j(V_j, I_j), for j = 1, 2, …, and n, as shown in Fig. 12. Similar to a two terminal network, the Type 2 H-model representation of N_1 is obtained by removing all independent sources[2] from N_1, and instead augmenting the ports with voltage and current sources that match the corresponding port values, as depicted in Fig. 13.

Note that, similar to a single port network, the H-model procedure described above creates n null ports k(V_k, I_k), for k = 01, 02, …, and 0n. Also note from Fig.13 that, as a result of the H-modeling, two networks N'_1 and N'_2 are created that are connected together through n null ports. Property 2 is similar to Property 1 that holds for n-port networks.

Property 2: Consider two networks N_1 and N_2 connected through n ports j, for j = 1, 2, …, and n. Replace N_1 with its Type 2 H-model representation to create n null ports k, for k = 01, 02, …, and 0n, as shown in Fig.13. Then for any of n nullified port the i-v characteristic curve passes through the origin and the origin is the operating point of that port.

In another interpretation, Property 2 clearly states that port nullification through the H-modeling does not change the ports' i-v characteristic curves; it only moves the v and i coordinate axis so that the ports' operating points fall on the origins, for all n ports.

Similarly, Theorem 1 also applies to n-port networks, as stated in the following corollary.

Corollary 1: Consider a network N_1 connected to another network N_2 through n ports j(Vj, Ij), for j = 1, 2, …, and n. Replacing N_1 with its (Type 2) H-model reduces the power consumption in N'_1 to zero.

The proof of Corollary 1 is similar to that of Theorem 1 in that we only need to note that N'_1 has no source to get power from, and that all its n ports are nullified and cannot deliver power to N'_1. Corollary 1 has several applications in power analysis of analog circuits. One

[2] Again, N_1 does not have dependent source that is controlled from outside of N_1.

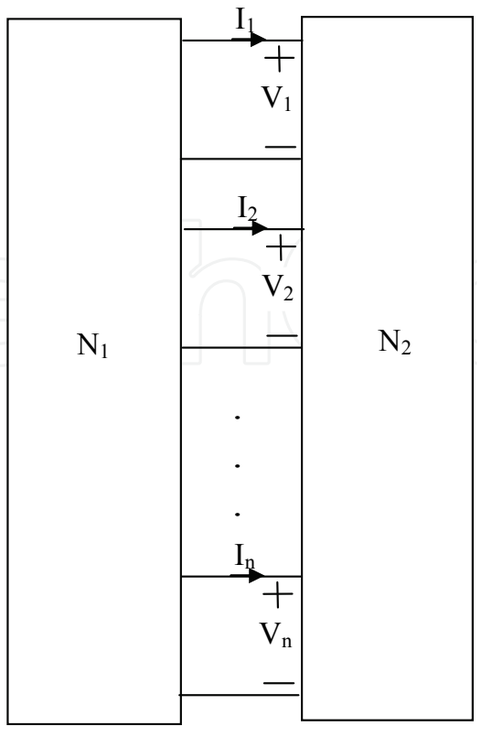

Fig. 12. Multi-port networks N_1 and N_2 connected through n ports.

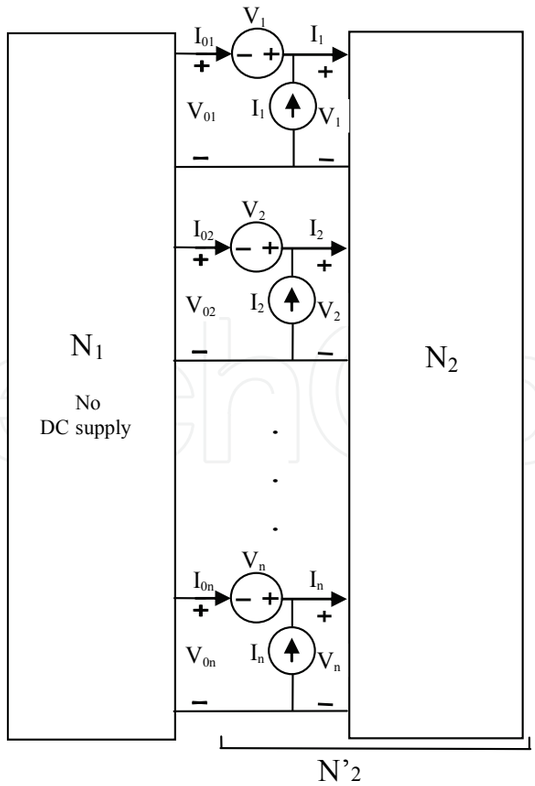

Fig. 13. H-model representation of the n-port network N_1.

application is to verify the power consumption in different parts of a network without disturbing the rest of the circuit. For instance, to calculate the power used in an amplifier core, minus the losses in the DC suppliers and the power supporting circuit elements, we can do as follows: replace the DC supply sections of the circuit with their H-models and then calculate the total power consumed in the circuit. This is equal to the power consumed in the amplifier core. This is in fact true for any type of power consumption including AC power. For example, to calculate the power consumed in a circuit alone, minus the input sources, we can represent the input sources by their H-models and calculate the total power in the circuit. Another important application of Corollary 1 is in low power designs of analog circuits. Here we can start designing a circuit, say an amplifier, with minimum DC power consumption, i.e., just enough to bias the transistors in the circuit. However, the circuit so obtained may not be very practical, after all. This is because there might be too many DC sources, known as "distributed supplies", being added to the circuit as a result of the H-modeling. Nevertheless, this is a good starting point for an efficient design for power consumption. The question asked is: how to remove the "distributed supplies" in the circuit and replace them with typical circuit supplies, but still keep the DC power consumption minimized? One simple solution to deal with the distributed supplies is to move them to their destination one at a time, having in mind to keep the power consumption minimized. This process definitely takes time and programming it may need a major effort. A more strait forward methodology for DC supply allocation in analog circuits has been recently developed [14] that makes this journey much simpler. The next chapter discusses this new methodology in more details.

5.1 Coupling capacitors in H-modeling

Another useful property of H-model is that from two sources used in the model only one souse provides power to the circuit and the other source is inactive (sitting idle with zero voltage or current). For example, in the H-modeling shown in Figs. 8 and 13 the current sources I_j provide power to N_2, but the voltage sources V_j are only to provide voltage drops necessary to create the null ports k, for k = 01, 02, …, and 0n, without delivering (or consuming) any power to the circuit. It is also possible to reverse the situation and have the voltage sources provide power and the current sources sitting inactive. Figure 14 shows such a modeling for a single port network that is identical to Fig. 8(b) except here the positions of the model-sources have been swapped. This is summarized in Property 3.

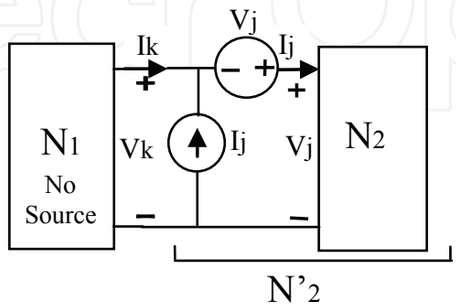

Fig. 14. An alternative H-modeling representation

Property 3: Consider two networks N_1 and N_2 connected together through one or multiple ports $j(V_j, I_j)$, for all j, as shown in Figs. 3 and 12. Next, replace N_1 with its H-model such as

those in Figs. 8, 13 and 14. Then there is only one active model-source, I_j or V_j, for each port delivering power to N_2 and the other model-source is inactive.

According to Property 3 only half of the sources used in H-models are active sources and the other half are inactive; they are there to establish the voltage or current requirement for the null ports. This brings up an alternative representation for an H-model. In this representation we can replace an inactive source with a storage element such as capacitor or inductor. Forexample, Figs. 8(b) and 13 are two circuit examples where the voltage sources are inactive. Apparently replacing these voltage sources with capacitors that are charged to the same voltages must satisfy the H-modeling: hence, making no changes in the voltages and currents within N_1 or N_2, as depicted in Fig. 15. In fact, these capacitors play similar roles as the coupling capacitors in ordinary amplifiers. Traditionally, coupling capacitors are used in amplifier designs to confine the DC power within the stages of the amplifier, or to block the DC from entering the input source or the load. The same role is played here; except here the choice is broader. In general a circuit can arbitrarily be partitioned into two blocks, N_1 and N_2 connected through n ports, where one block, say N_2, receives the DC power it needs to bias the (nonlinear) components and the other one does not need it. For example, take again the case of Fig. 13; assume N_2 is the collection of all the nonlinear components (transistors) and N_1 represents the rest of the circuit. This simply means that the DC supplies are limited to directly bias nonlinear components in N2 and nothing else. Figure 15 shows how the voltage sources in local biasing in Fig. 13 are replaced with coupling capacitors; and these capacitors are going to get charged at the beginning of the

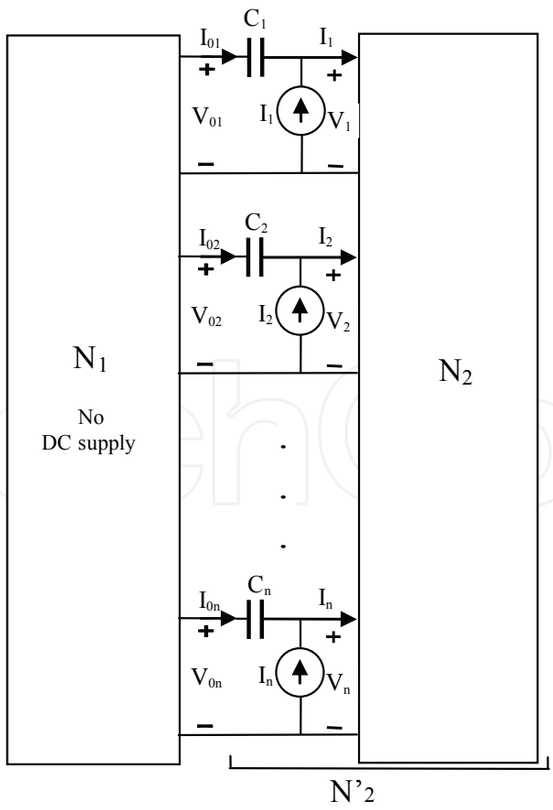

Fig. 15. H-model representation of an n-port network using coupling capacitors.

circuit operation, known as the transient response. It is during this period that the capacitors are charged to the same voltages as those voltage sources, V_j, provided that each capacitor has a (resistive) charging path, providing an RC time constant.

6. Component biasing

One of the applications of H-modeling, leading to port nullification, is in biasing of nonlinear components, individually or in clusters. This is known as *component biasing*. Take the case of Fig. 3 or Fig. 12 and assume N_2 consists of one or more nonlinear components connected to the rest of the circuit, N_1. This simply means that N_1 is biasing all the components accumulated in N_2, and it establishes operating points for the ports at $Q_j(V_j, I_j)$, for j = 1, 2, …, n. Now, compare Fig. 3 with Fig. 8(b), or Fig. 12 with Fig. 13; in both cases no change in the biasing of the components inside N_2 takes place i.e. the ports are still operating at $Q_j(V_j, I_j)$ points. The difference, however, is that in the former circuits (Figs. 3 and 12) the components in N_2 are globally biased through N_1, whereas in the later cases (Figs. 8(b) and 13) the ports are directly biased through the H-model sources, leaving N_1 with no DC supply. This brings us to introduce a new biasing scheme, known as *local biasing*. We can simply show that component biasing is the combination of local biasing applied to all ports of a nonlinear component (transistor). Next we introduce local biasing and its applications.

6.1 Local biasing

A port is locally biased if it is augmented with a voltage source and a current source so that they exactly provide the voltage and current the port needs to operate at its desired Q-point. Apparently the port receives its biasing power exclusively from one of those DC (voltage or current) supplies and that DC supply is fully dedicated to the port.

A component is individually biased (called *component biasing*) if all its ports are locally biased. Likewise, an m-port network consisting of multiple components is locally biased if all its ports are locally biased.

Property 4: A nullified port is locally biased.

The proof of Property 4 is quite evident because when a port is nullified the exchange of DC power through the port becomes zero and that is exactly what local biasing is all about. However, in local biasing the exchange of power between two sides of the nullified port is zero only at the designated operating point. The port behaves quite normal and like when it is globally biased, when a signal is applied to the port. In other words, local biasing only shifts the port's i-v coordinate axis to the operating point.

Local biasing Using Coupling Capacitors: As discussed in Section 5, coupling capacitors can be used in place of voltage sources in H-modeling, as shown in Fig. 15. Because of the identity between the two concepts the same rules apply to local biasing ports as well. Now we must realize that although both local biasing solutions (one with two sources and one with a current source and a coupling capacitance) serve the same purpose of confining the DC power within the nonlinear components, they do not perform identically; and they are not interchangeable in some cases. Here are the major differences between the two. As we discussed earlier, a locally biased port j with both sources being present create a null port k; and as long as k stays null it guaranties that port j operates at $Q_j(V_j, I_j)$, as shown in Figs. 8, 13, and 14. However, any new DC supply in the circuit that effects port k causes port j to shift from $Q_j(V_j, I_j)$ accordingly. Hence, local biasing, with both sources present, is transparent to any signal (DC and AC) in the circuit; the same it is in a normal biasing

situation. This, for example, helps in amplifier designs where the frequency band includes DC. However, this is not the case when coupling capacitors are used in local biasing. Once the port's operating point is established in the coupling capacitor case it remains unaltered, no matter how much DC supply we bring to the main circuit. In fact, here, it is the current source across the port that provides the biasing condition for the port and as long as it remains constant at I_j the operating point stays unaltered at $Q_j(V_j, I_j)$. That is why in a capacitor coupling case we lose the low frequency bandwidth to a non-zero value of f_L, depending on the RC time constants; C being the coupling capacitor. The following property is valid for both types of local biasing.

Property 5: Consider a linear circuit N connected to one or more nonlinear components through p ports. Suppose the DC supplies in N bias the p ports to their Q-points $Q_j(Vj, Ij)$, for j = 1, 2, …, and p. Now, if we remove all DC supplies from N and instead locally bias all p ports to their assigned operation points $Q_j(Vj, Ij)$ then we observe no change happening in the AC performance of the entire circuit, i.e., the gains, input and output impedances, frequency responses, and signal distortion remain unaltered. The exception is in the case when coupling capacitors are used. The later causes the low frequency response of the amplifier to change from DC to a higher frequency f_L.

The proof of Property 5 is quite evident. For the case of local biasing using two DC sources for each port, the sources are transparent to the AC signals and they can simply be removed for AC analysis (including DC signal). For the case of local biasing with coupling capacitors the capacitors bypass AC signals except for the frequencies below the low cut-off frequency f_L of the circuit.

Example 5: Consider designing a two stage BJT amplifier with feedback. The circuit structure (topology) is shown in Fig. 16, and the design specifications are given in Table I. The

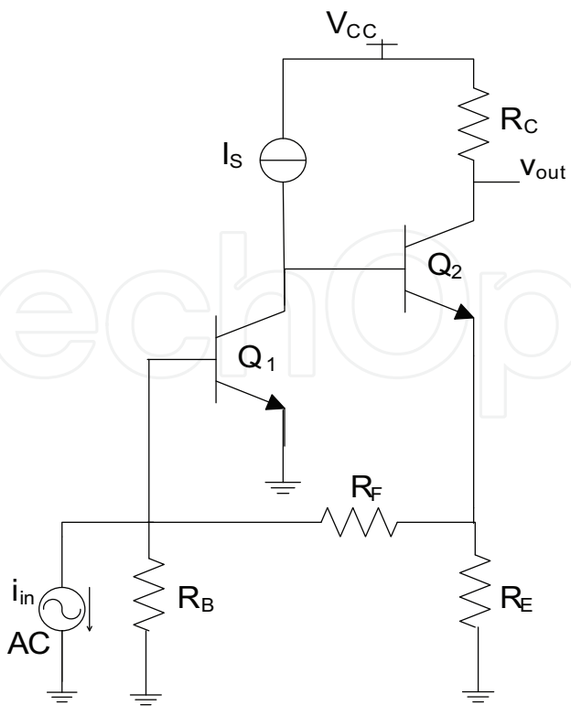

Fig. 16. A two stage BJT amplifier with feedback

A_v dB	A_i dB	R_{in} KΩ	R_{out} KΩ	f_L Hz	f_H KHz
44	46	1.2	65	30	300

Table I. The design specs for the amplifier

Transistors are two npn, 2N3904, and their selected operating points during the AC operation are listed in Table II. We first start with the AC performance design. This is done by replacing the transistors with their small signal linear models at the designated Q-points. Next, in a routine linear analysis, the circuit components are found so that the design meets the given criteria. Table III lists the resistor values resulting from the AC design.

Trans.	V_{BE} V	I_B μA	V_{CE} V	I_C mA
Q_1	0.57	0.32	1.5	0.025
Q_2	0.7	25.0	4.2	4.0

Table II. The selected operating points for the transistors in the amplifier

R_B KΩ	R_C KΩ	R_E Ω	R_F KΩ
100	1	200	40

Table III. the resistor values resulting from the AC design of the amplifier

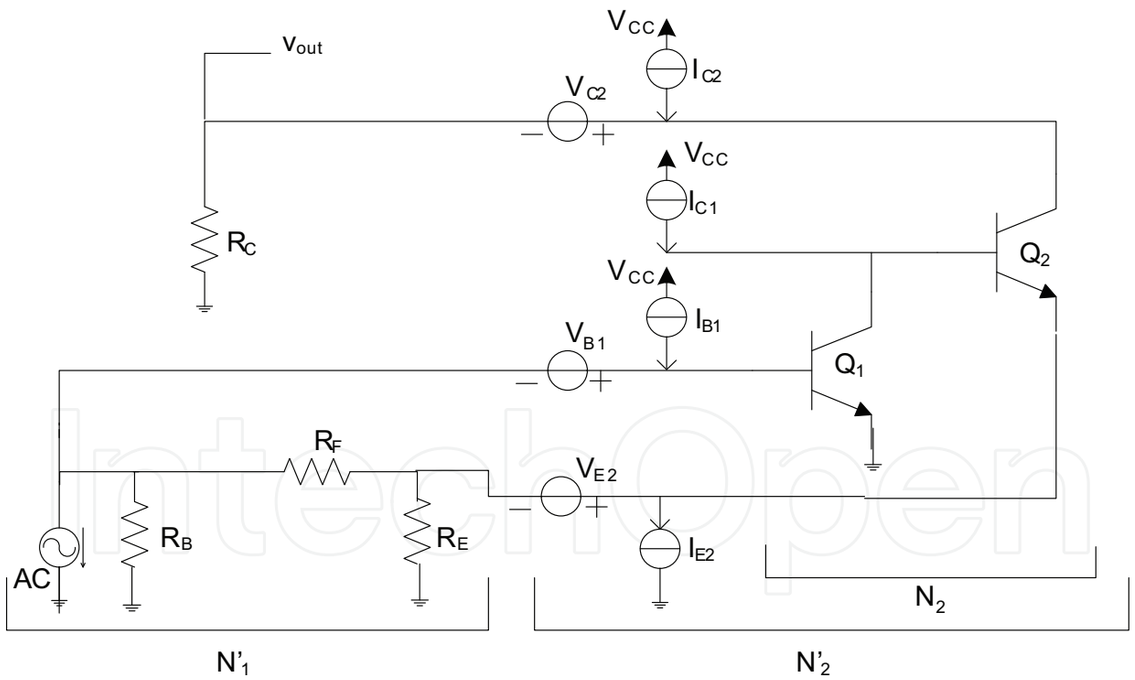

Fig. 17. Separation of linear and nonlinear sections in the two stage BJT amplifier using H-modeling

Our next step is to bias the transistors through local biasing. To do this we first separate the nonlinear components from the rest of the circuit. Next, we remove the unknown DC supplies (V_{DD} and I_S) from the circuit, and instead locally bias the transistors to their desired Q-points, as shown in Fig. 17. Notice how the circuit is partitioned into two sub-networks

N'_1 and N'_2; where N'_1consistes of the linear (resistive) components of the amplifier with zero DC power, and N'_2 contains the locally biased transistors. Our formal amplifier design is over by now and the circuit should work perfectly fine. However, there is still one practical problem left that must be taken care of; which is to reduce the number of DC supplies and possibly allocate only one or two normal DC voltage supplies at the designated locations. We leave this to the next chapter where the problem is tackled and a systematic solution for DC power management and supply allocation is provided for analog circuits. Instead, here we will continue to focus on local biasing. Because there is a low cut off frequency specified for this design we have a choice to use coupling capacitors for the local biasing. Figure 18(a) shows the amplifier locally biased with coupling capacitors. Note that the capacitor values are selected based on the low cutoff frequency response, f_L = 30 Hz, specified for the amplifier. Figure 18(b) shows the output voltage swing in full range with negligible distortion, and Fig. 18(c) shows the output frequency spectrum of the amplifier, which tightly meets the design criteria. Theoretically our design objective for this amplifier is accomplished at this point; however, one may argue about the practicality aspects of this design with four current sources distributed within the circuit. In case of integrated circuits this may be acceptable because the current sources can be replaced with active loads, current mirrors and current sinks. For our design, as a lumped amplifier circuit, this may create problems. One simple solution is to replace the current sources with resistors that provide the same DC currents to the devices. But the problem with these resistors is that when added to the circuit they may, to some extent, change the AC performances of the amplifier, such as the gains. In some cases the changes might be negligible. In tighter design however we can repeat the AC design; this time analyze the linear circuit with the resistors included.

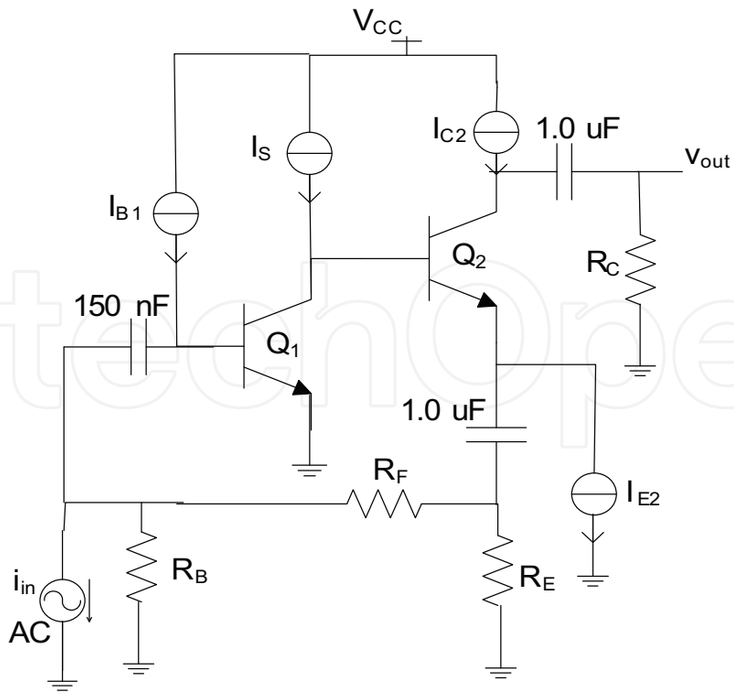

Fig. 18. (a) – The amplifier, locally biased with coupling capacitors substituted for the voltage sources.

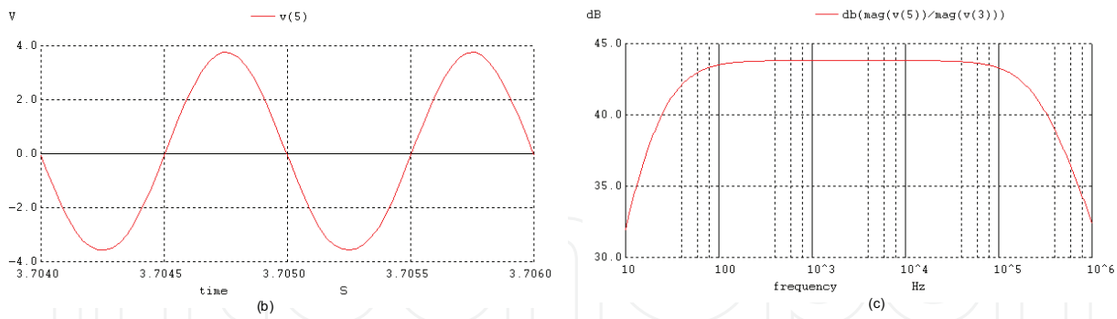

Fig. 18. (b) The output voltage swing of the amplifier; (c) the output frequency spectrum of the amplifier

6.2 Local biasing vs. normal biasing

Discussion - Note from Fig. 18(a) that, any change in the biasing resources, such as making changes in V_{CC} or in the DC current sources, shifts the operating points of the transistors; but the effect is negligible to the rest of the circuit. This is due to the coupling capacitors. For example, the feedback circuit (R_B, R_E and R_F), a very sensitive part of the amplifier, is not affected much by these changes. This is sometimes considered a serious deviation from the design purposes. For instance, suppose one of the purposes of the design is to provide feedback for the biasing to help to stabilize the transistor's operating points against shifts in the operating points during the amplifier operation. The purpose is definitely defeated by using this type of local biasing. This is because, in using local biasing the rest of the circuit becomes DC isolated except for the nonlinear block (N_2); hence, no DC power runs outside the block to make the feedback effective. In short, if negative feedback exists in the circuit to help stabilize the transistors biasing then local biasing with coupling capacitors does not help the situation and cuts off the feedback for DC. The good news is that we can do local biasing with a mixture of both methods. That is, we can leave the sensitive areas, which need DC feedback, with normal locally biasing, i.e. including voltage sources instead of coupling capacitor, and do the rest with the coupling capacitors. This way we are benefiting from both worlds, i.e. i) getting stability through the feedback, and ii) having the coupling capacitors to fix the operating regions when needed.

To summarize, we have introduced two types of local biasing for nonlinear components: one with both voltage and current sources present for each component, and one with coupling capacitors replacing the voltage courses. A third type is to use the mixture of both as appropriate. Here are some similarities and differences between the two types. For certain operating point assigned to a transistor in a circuit both types of local biasing provide voltage and current required to bias the transistor. In a way, this local biasing causes the v and i coordinate axis to move to the Q-point. The difference between the two types, however, is that in the coupling capacitor case the Q-point is fixed on the origin as long as the local biasing current stays fixed; whereas, in the former (with the voltage source) case the biasing behaves exactly like ordinary biasing except initially the Q-point is located at the origin, but it can move with adding extra DC sources to the circuit.

6.3 Local biasing of devices

Because local biasing deals with nonlinear devices, one way to efficiently analyze or design an analog circuit is to bias the transistors individually before placing them in the circuit. This allows the circuit to go directly for AC analysis. Within the three major semiconductor devices p-n junction diodes are one-port devices and can be locally biased. Bipolar-junction transistors are two-port devices, but they can also be modeled with two one-port devices in case Ebers-Moll or the transport large signal model [11, 16] is used to replace them. Figure 19 shows an npn and a pnp transistor locally biased with their symbolic representation also shown.

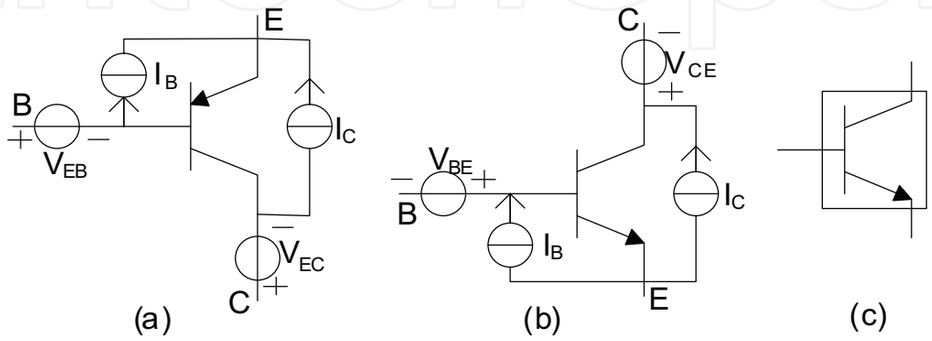

Fig. 19. Locally biased bipolar transistors; (a) an npn; (b) a pnp; and (c) the symbol for a locally biased BJT

MOS transistors, on the other hand, are considered three-port devices with only four sources needed to represent locally biasing of the device. This is because for the drain-source we need both I_D and V_{DS} sources to nullify the port; whereas for the gate-source and the substrate-source we only need V_{GS} and V_{BS} to nullify the ports, respectively. Figure 20 illustrates both an nMOS and a pMOS being locally biased; however, for simplicity purposes we may normally drop the substrate effect, V_{BS}, and consider the device as a two port (drain-source and gate-source) component.

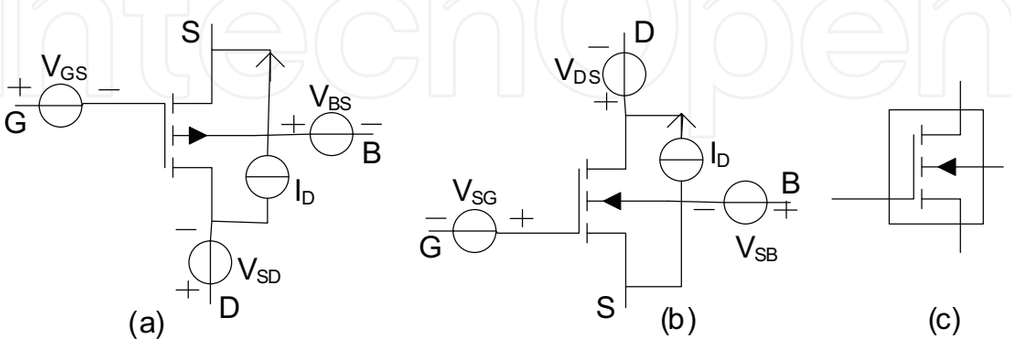

Fig. 20. Locally biased MOS transistors; (a) an NMOS transistor; (b) a PMOS transistor; and (c) the symbol for a locally biased transistor

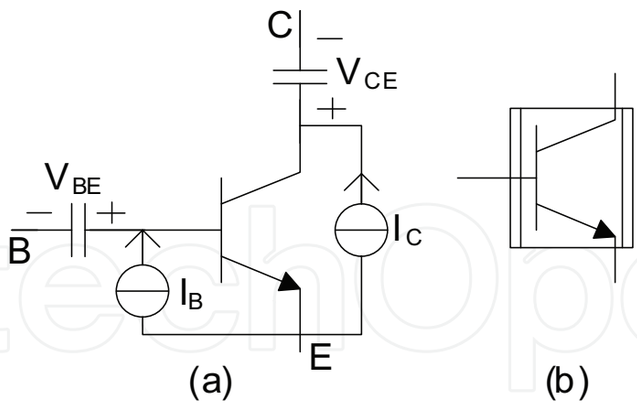

Fig. 21. (a) Locally biased bipolar transistor using coupling capacitors; and (b) the representing symbol

6.4 Source reduction in the local biased transistors

Coupling capacitors described earlier can also be used in device biasing to replace the voltage sources. Again, this is because only one of the two sources is needed to provide DC power to the port, and the other source is inactive. In case of an inactive voltage source we can replace it with a coupling capacitor. However, there are two related issues that must be addressed when coupling capacitors are used in amplifiers. First, a coupling capacitor must have a (resistive) path to DC supplies to get charged during the operation. Second, as we know, coupling capacitors have direct effect on the low frequency response of the amplifier; therefore, they must be selected so that the low frequency response criterion of the amplifier is not violated. Figure 21 is an example of coupling capacitor used in local biasing of a BJT.

Example 6: Figure 22(a) shows a single stage nMOS amplifier. To apply local biasing we remove all DC supplies from the circuit and locally bias the transistor. In this design the transistor is locally biased with capacitor coupling, shown in Fig. 22(b). However, the coupling capacitors need to be charged to the level needed for local biasing; hence, they need charging path. The capacitor C_{DS} has its charging path to the current source I_D, but the capacitor C_{GS} lacks such a path and we need to create one through an extra resistance R_F = 10MEGΩ. Although R_F is not part of the original amplifier, it is large enough to neglect its effect on the amplifier operations. The next step is to decide on the capacitors values. Each capacitor creates a pole (also zero) for the output transfer function, and for the correct frequency response the poles must lie below the low cutoff frequency of the amplifier, set at f_L = 100 Hz. We first assume C_{GS} = 0.5 nF and C_{DS} = 100 nF and compute the poles individually. For the gate capacitor, roughly speaking, we have

$$f_{GS} = \frac{1}{2\pi(R_F + R_G)C_{GS}} = \frac{1}{2\pi * 10.2e+06 * 0.5e-09} = 32\ Hz$$

And for the drain capacitor we get

$$f_{DS} = \frac{1}{2\pi R_D C_{DS}} = \frac{1}{2\pi * 30e+03 * 100e-09} = 53\ Hz$$

Both pole locations are below f_L = 100 Hz and hence are accepted for our design. This will conclude the design. The circuit of Fig. 22(b) is simulated by SPICE and the results for both, the transient response and the frequency response, are provided in Figs. 23 (a) and (b), respectively. Note from Fig. 23(a) that it takes about 4 msec for both C_{GD} and C_{DS} to charge to the level needed for local biasing. Also note that, since all biasing is accomplished by current sources we do not need to specify the DC supply value V_{DD}, unless certain voltage swing for the output waveform is needed.

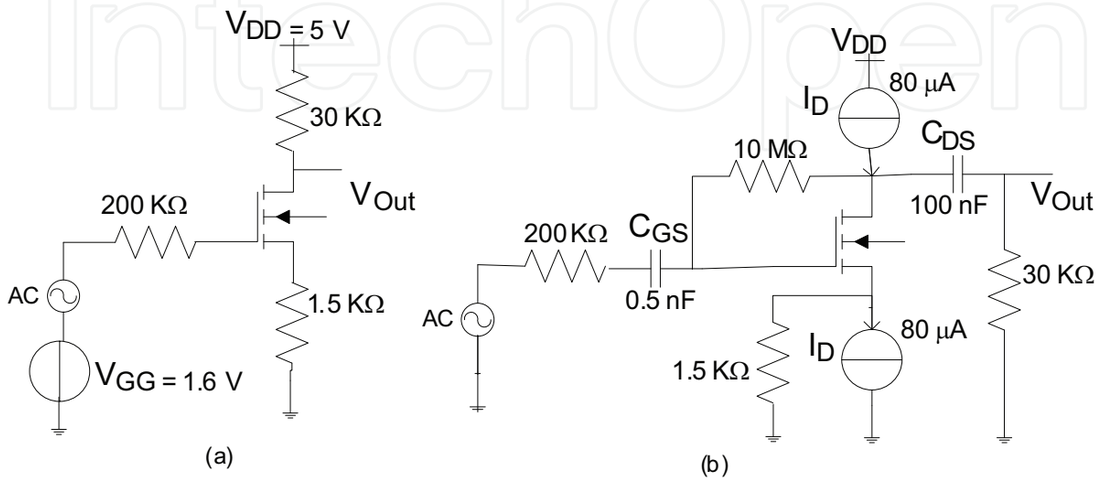

Fig. 22. (a) Single stage NMOS amplifier; and (b) locally biased transistor with coupling capacitors

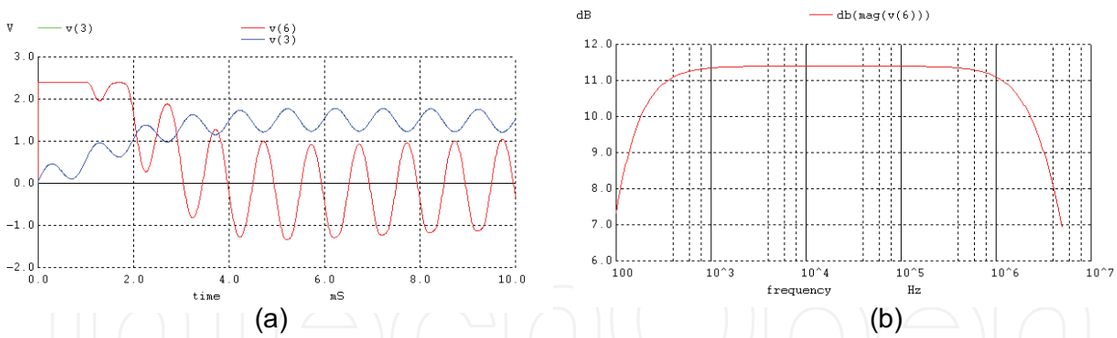

Fig. 23. The SPICE simulation results; (a) the transient waveforms; and (b) the amplifier frequency response

Before we leave our discussion about the coupling capacitors here we need to closely look at their effect on the AC operation of the circuit. As we add each capacitor to a circuit[3] we basically add one pole, and possibly one zero, to the transfer function; and in the case of large number of capacitors they may initiate circuit instability and oscillation. A rule of thumb that often applies here is that, if an amplifier has feedback and it exceeds more than two stages, the extra number of coupling capacitors for local biasing should be avoided.

[3] The assumption is that the capacitors are independent, i.e., they can arbitrarily assume any voltage across.

7. Additivity in local biasing

Additivity is a major property of linear circuits; it permits superposition as a convenient tool for breaking the circuit response to multiple stimuli into the sum of the circuit responses to individual stimulus, one at a time. As we know additivity does not apply to nonlinear circuits, but as we will prove, it works in circuits with nonlinear components provided that the circuit situation (response) is restored before applying the next stimulus (DC supplies). Theorem 2 describes the procedure for two terminal networks.

Theorem 2 – Additivity: Consider a network N_2 connected to another network N_1 through a port j(V, I), as shown in Fig. 24(a), and with its characteristic curve shown in Fig. 24(b). Let N_1 contain n DC supplies. Further, assume we are dealing with simple (non-multiple) operating points[4] in this case. Group the sources arbitrarily into p mutually exclusive groups[5]. Perform p number of biasing cycles to the circuit; each time applying only one group of supplies and remove the rest. Then, the final operating point of the port due to all n supplies can be determined by adding the (voltage and current) values associated with all p number of operating points in the p biasing cycles provided that the port is nullified (called partial local biasing) before the next operation is performed.

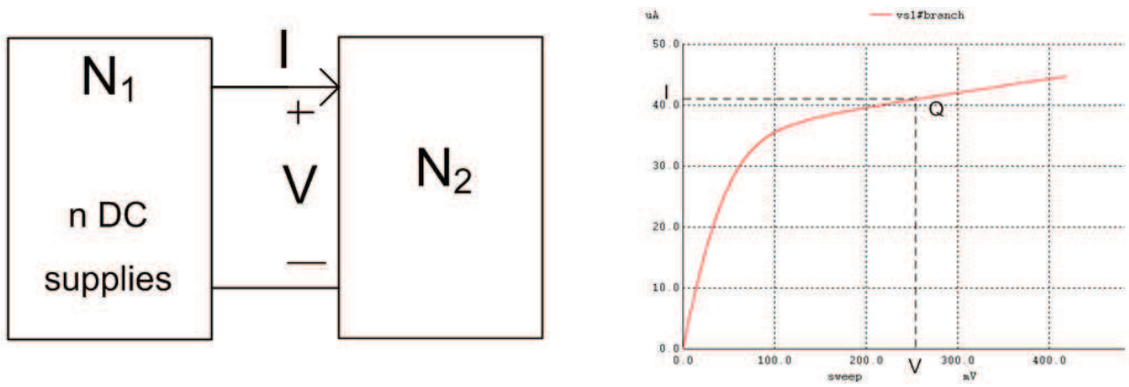

Fig. 24. (a) Two terminal networks connected; and (b) the port's operating point on the characteristic curve

Proof: Suppose a network N_1 with n DC supplies is connected to another network N_2 through a port j(V, I) (Fig. 20(a)), and suppose Q(V, I) is the operating point of the port looking to N_2, as shown in Fig. 20(b). Now, split n supplies into p groups of mutually exclusive supplies n_1, n_2, …, and n_p. First keep the group of n_1 supplies in N_1 and remove the rest (Fig. 25(a)). Suppose for this case the operating point moves to a new point, $Q_1(V_1, I_1)$, on the characteristic curve, as depicted in Fig. 25(d). Next do the followings: i) augment port $j_1(V_1, I_1)$ with current I_1 and voltage V_1 supplies, and ii) remove n_1 sources from N_1. This creates a nullified port $j_2(V_2, I_2)$ next to $j_1(V_1, I_1)$. Now we have completed a partial local biasing, which causes the v and i coordinate axis to move from (0, 0) to Q_1, and make it the

[4] In a case of multiple operating points we may end up with more than one operating point for a single set of supply sources.

[5] It is also permissible to have a supply used in more than one group. In this case the supply is partitioned and each part is exclusively used in one group.

new origin. Next, add the group of n_2 supplies to N_1, as shown in Fig. 25(b). This causes the operating point to move from Q_1 (the new origin) to $Q_2(V_2, I_2)$, as indicated in Fig. 25(d). Likewise, augment port j_2 with current I_2 and voltage V_2 supplies and then remove n_2 group of supplies from N_1 to create a nullified Port $j_3(V_3, I_3)$. Again, the last operation causes the v and i coordinate axis to move from Q_1 to the new location, Q_2, (Fig. 25(d)). Similarly, introduce n_3 group of supplies to N_1 (Fig. 25(c)) and move the operating point to a new point $Q_3(V_3, I_3)$ on the characteristic curve. Without loss of generality we can now assume that the sources in N_1 are exhausted at this point. Then Q_3 and Q must be the same point on the characteristic curve. This is because the process, just explained, is not different from applying all n supplies to the circuit in p steps of n_1, n_2, …, and n_p groups, but this time without removing any of them. This simply means that $V = V_1 + V_2 + V_3$, and $I = I_1 + I_2 + I_3$, as we can see in Fig. 25(d). This proves the theorem.

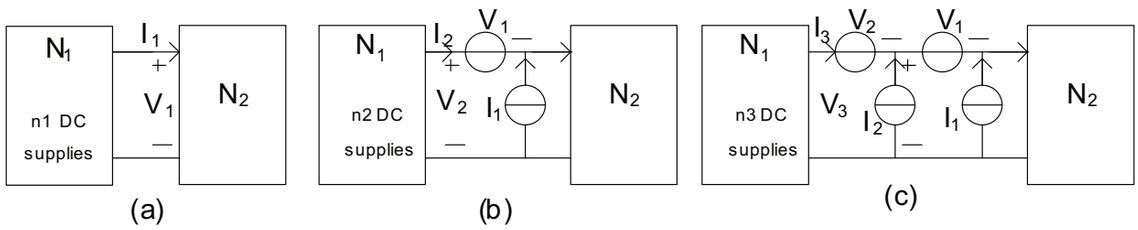

Fig. 25. The process of additivity in local biasing; (a) network with the first group of supplies; (b) and (c) Sequences of adding groups of supplies one at a time and accumulating the biasing results

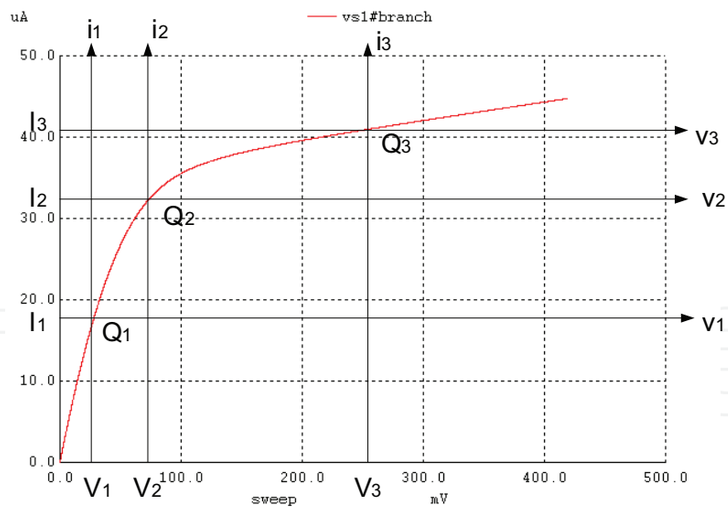

Fig. 25. (d) Progressive move of the operating point on the characteristic curve as the supplies are adding.

The method just described allows us to progressively bias a complex circuit in a step-by-step procedure. By using additivity property we can break down the DC supplies into p separate groups of supplies so that each time we only apply one group. At the end it is the sum of partial results that determines the final operating points of the transistors. This separation of multi-step biasing procedure, called *progressive biasing*, has only been possible by using local

biasing methodology. In a way, local biasing keeps (stores) the progression of the biasing status in the circuit in order to accumulate and direct the biasing to its destination. It can be thought of as a ladder procedure: in each step of the ladder one group of the circuit supplies are replaced with local biasing supplies so that the Q-points of the transistors stay unchanged on the characteristic curves, but all the coordinate axis move to the Q-points, making them new origins for the next step. This continues until the circuit supplies are exhausted. It is this additivity property that makes superposition, a valuable tool, available for nonlinear circuits. It is through this superposition that we can break down the complexity of biasing for large circuits and manage a smooth biasing convergence.

Another notable point regarding this step-by-step biasing procedure is that we can arrive at a final Q-point in a port from different directions, depending on the sequence of the supply groups we select to apply. And in these options we might be able to select the quickest one or the one that assures convergence. On the same line, following the procedure stated in Theorem 2 we might arrive at different Q-points when we approach from different directions. This is the case when we are dealing with multiple Q-points; and the described procedure can provide an alternative technique for searching for multiple operating points in a nonlinear circuit [9].

Although Theorem 2 is given for two terminal networks it can easily be extended to include multiple-port networks, as stated in Corollary 2.

Corollary 2: Consider a network N_2 connected to another network N_1 through m ports. Let N_1 contain n number of DC supplies used for biasing N_2. Further, assume all the operation points for the m ports are simple (non-multiple) Q-points. Next, group the sources arbitrarily into p mutually exclusive groups. It then follows that for each port the final operating point Q(V, I), due to all n DC supplies, can be found by adding the Q-point (voltage and current) values, $Q(V_j, I_j)$, for all p number of group of supplies, provided that the following condition holds:

The port is nullified by being locally biased after each group of supplies is applied; making the Q-point a new origin for the port's characteristic curve.

Hence we can write:

$$V = \sum_{j=1}^{p} V_j \quad and \quad I = \sum_{j=1}^{p} I_j \tag{16}$$

The proof of Corollary 2 is similar to that of Theorem 2 in the sense that in each sequence of applying a group of DC supplies to the circuit we can extend the procedure to include all m ports. However, we must remember that in each step the nullification of ports must be total and simultaneous. That is, for each application of a certain group of DC supplies we need to find the corresponding H-model of all m ports of N_1. This process does two things:

i. it generates m null ports -- one for each port --, and
ii. it finds the v and i values of the partial Q points for *all* ports at the same instance.

Again, we must emphasize that this additivity procedure is applied to circuits with simple operating points; where, for each port, any route taken ends up at a fixed location (Q-point) on the characteristic curve. For circuits with multiple Q-points the procedure works as well, except we may reach to different Q-points when we follow different sequences of supply groups.

This additivity property provides a new and remarkable methodology for the analysis and simulation of nonlinear circuit with multiple nonlinear components. Another unique feature

of the additivity property is that it provides a simple mechanism through which we can arbitrarily and gradually (ladder type) replace the normal supplies in an amplifier with supplies that locally bias the individual transistors. Conversely, in a design procedure, we can start with local biasing the transistors to get them to the desired Q-points; then move and combine the distributed supplies (by techniques such as source transformation) to merge into normal circuit supplies such as V_{DD}, V_{CC}.

Algorithm 1 provides a circuit analysis procedure based of the progressive biasing stated in Corollary 2.

Algorithm 1:

1. Given a nonlinear circuit, first identify all nonlinear devices and put them into one nonlinear network N_2 with m ports, $j(v_j, i_j)$, connected to the rest of the circuit as a linear network N_1.
2. Select a grouping scheme for the DC supplies and put them into an arbitrary sequence that best performs the biasing of m ports in N_2. The sequence selected should possibly guaranty a quick convergence. This is a crucial step and needs design experience to achieve a good result.
3. Keep the first group of supplies in N_1 and remove the rest. Assume this group of supplies makes N_2 to operate at Q_1 (V_1, I_1) on the characteristic curve (for simplicity the algorithm is given for one port but it is extendable to all m ports, as well). Next, augment the port with I_1 and V_1 sources for local biasing, and remove the first group of supplies from N_1. This will create a nullified port.
4. Include the second group of supplies into N_1 and remove the rest. This will cause the operating point to move from Q_1 (V_1, I_1) (now the origin) to Q_2 (V_2, I_2), which is the new operating point.
5. Continue with step 4 until all groups of supplies are sequentially applied.
6. The biasing of the transistors is complete and the entire circuit -- N_1 plus N_2 -- is ready for the application of the AC signals. The output signal, in this case, is only AC without being mixed with any DC component.

The following two examples are going through the progressive biasing procedure by using Algorithm 1.

Example 7: Figure 26(a) shows part of the circuit of the MC1553, a three stage BJT amplifier with feedback [11]. The circuit apparently works (biases) with a single supply of V_{CC} = 9V. To produce a progressive biasing for the amplifier we have spit the 9 volt supply into four separate unspecified supplies V_{BB}, V_{CC}, V_{DD}, and V_{EE}, shown in Fig. 26(b). Note that we have also replaced the transistors with their locally biased counterparts; where each transistor has its own voltage sources V_{BE} and V_{CE}, and current sources I_B and I_C used for the local biasing, as depicted in Fig. 19. Next, we are going to make three groups of supplies: (V_{CC} = 5V and V_{DD} = 9V), (V_{BB} = 7V and V_{EE} = 9V) and (V_{BB} = 2V and V_{CC} = 4V), and then apply Corollary 2 for a progressive biasing procedure. Table IV is the result of this biasing procedure. Column 2 in the table displays the biasing results (Q-points) of the transistors when the original circuit of Fig. 26(a) is used. Columns 3, 4 and 5 are the results of the progressive biasing sequentially applying the groups of supplies as indicated. As shown, column 5, which is the accumulation of all the three steps, is identical to column 2, as expected. Another interesting observation from Table IV is that, although the transistors may go into different modes of operations in the progressive biasing – such as saturation or cut off, for example – the results are coming out correctly at the end.

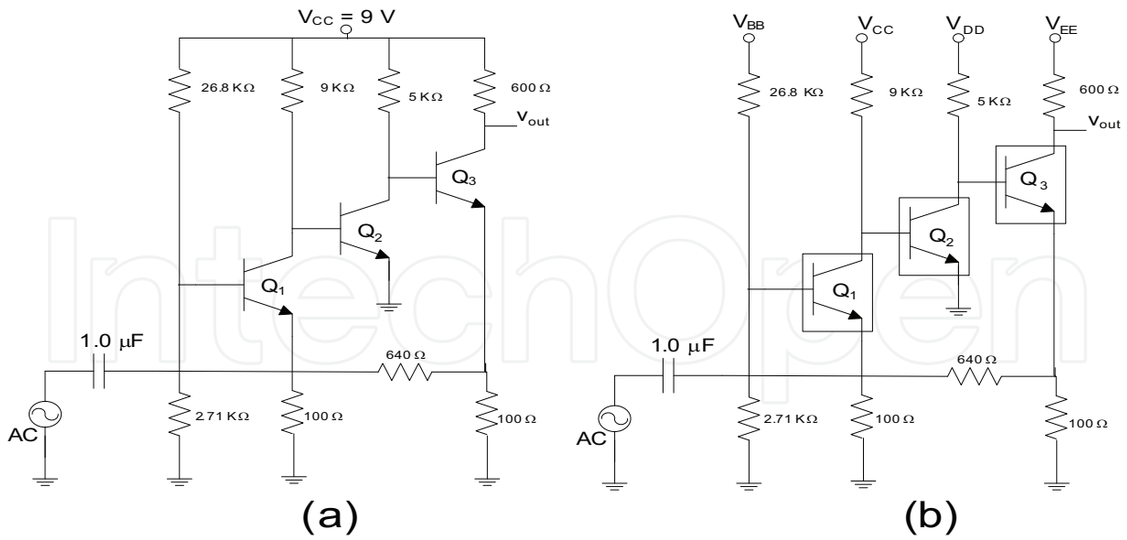

Fig. 26. (a) Part of the circuit of the MC1553, a three stage BJT amplifier with feedback; and (b) a progressive biasing of the amplifier using additivity property along with the local biasing.

Items	All four supplies 9V	V_{CC} = 5V V_{DD} = 9V	+ V_{BB} = 7V +V_{EE} = 9V	+ V_{BB} = 2V +V_{CC} = 4V
I_{B1}	6.97246e-06	-9.53064e-13	1.845914e-06	6.972464e-06
I_{B2}	1.08180e-05	4.782478e-04	2.838049e-04	1.081804e-05
I_{B3}	3.39962e-05	1.741652e-13	1.20893e-11	3.399617e-05
I_{C1}	9.13995e-04	1.662226e-12	1.950662e-04	9.139951e-04
I_{C2}	1.52165e-03	1.788923e-03	1.786860e-03	1.521652e-03
I_{C3}	5.64041e-03	-1.43753e-13	2.230231e-11	5.640411e-03
V_{BE1}	6.634702e-01	2.281979e-09	6.231302e-01	6.634702e-01
V_{CE1}	5.279963e-01	6.957695e-01	6.728130e-01	5.279964e-01
V_{BE2}	6.766817e-01	6.957695e-01	6.901600e-01	6.766817e-01
V_{CE2}	1.221757e+00	5.538356e-02	6.570034e-02	1.221757e+00
V_{BE3}	7.109050e-01	5.538356e-02	6.335615e-02	7.109050e-01
V_{CE3}	5.104901e+00	7.513105e-11	8.997656e+00	5.104902e+00

Table IV. the results of progressive biasing of the amplifier using additivity property with local biasing

Example 8 –BJT Circuit with multiple Operating Points: The circuit shown in Fig. 27 has multiple operating points, and for a similar circuit Goldgeisser and Green [9] have reported nine operating points. We originally simulate the circuit with all three external supplies, 12V, 10V and 2V simultaneously applied. When using WinSpice3 [4] it takes 163 iterations to converge to stable operating points for all transistors. In an effort to minimize the effect of other convergence factors both source stepping and the shunt convergence aids are disabled in this program – performed by enabling OPTIONS: ITL6=1 and MINCONVSHUNT=0. Table V shows the circuit node voltages obtained.

Next, we use local biasing methodology. First, we identify all four BJTs in the circuit and put them into a multi-port nonlinear block N_2. Next, we separate the DC supplies into two groups: i) the 12V and 10V supplies, and ii) the 2V supply. In step 1 we keep the 12V and 10V supplies in the circuit and remove the 2V supply, and simulate the circuit using Spice3 with applying the same conditions (OPTIONS) we did originally. Here we notice that the circuit converges fairly quickly into a set of operating points. In the second step we remove the supplies from the circuit and instead locally bias the transistors to the same operating points reached. Then we add the 2V supply to the circuit and simulate the circuit again. The circuit converges this time to a new set of operating points after a few more iterations. It is observed, as expected, that these new operating points are the same as those originally obtained, i.e., located at the same Q-points on the devices' characteristic cures.

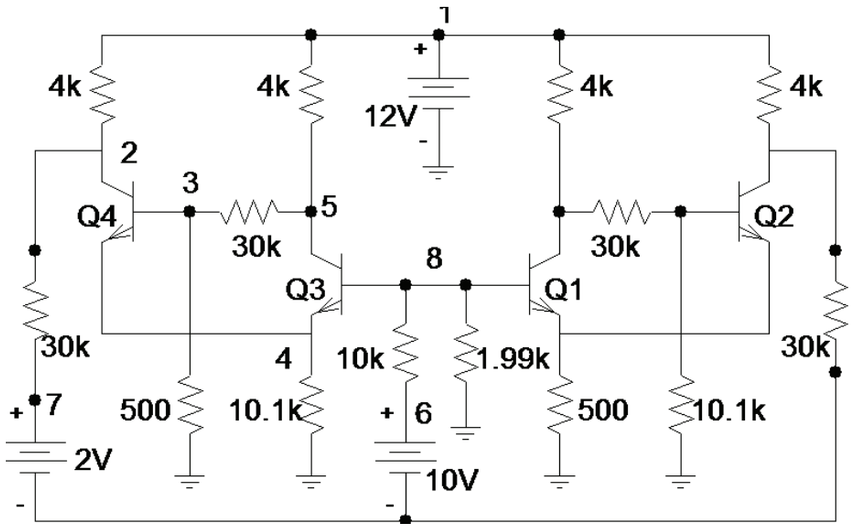

Fig. 27. A BJT circuit with multiple operational points

V(2)	V(3)	V(4)	V(5)	V(8)
10.425	0.171	0.5216	10.428	1.0967

Table V. The circuit node voltages for figure 27 external biasing

In comparing the two methods of biasing for this example, we notice that while 163 iterations was necessary for the biasing to converge in the original biasing scheme it only took 10 iterations for both steps in the local biasing scheme to converge. This is an outstanding achievement owing to the additivity property of local biasing, which is very essential in the analysis and simulation of complex circuits. One may argue that a similar power supply "stepping" is also provided in the conventional analog circuit simulators such as SPICE. However, the differences are quite evident. The proposed method gives choices to skilled designers to select their own DC supply grouping and the sequences they choose to apply. For example, in applying the local biasing scheme in this example if we apply the "2V" supply first and then the "12V and 10V" the number of iterations would substantially increase. The second, and the most important property of the new methodology is its additivity property; where the sequences of steps in biasing are "stored" in local biasing as it adds up to the final result (again, like stepping on a ladder).

Figure 28 depicts the circuit when it is locally biased, and as we notice the entire external DC supplies are removed leaving each transistor with its own biasing. Table VI provides the augmented voltage and current supplies used during the two steps of the local biasing. Note that the values in the column 5 are the sum of the corresponding values in the columns 3 and 4, which is due to the additivity property.

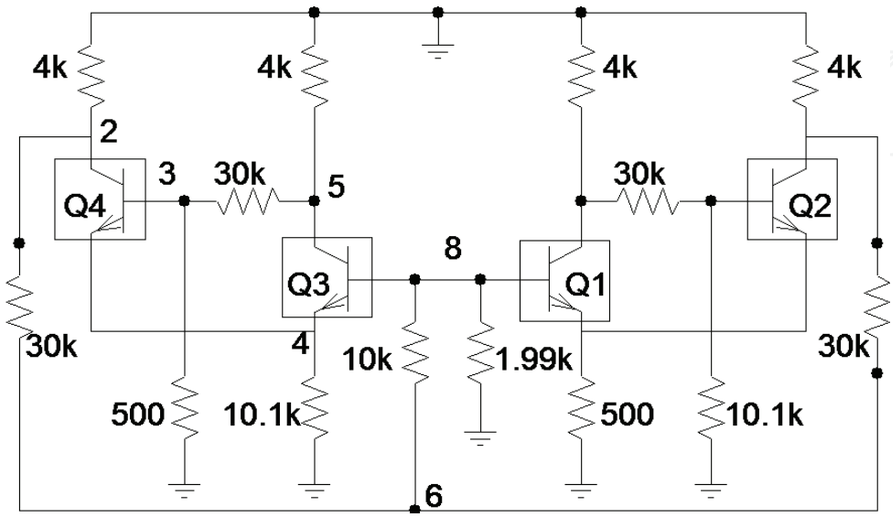

Fig. 28. The BJT circuit with locally biased transistors

BJT	BJT Ports	12V and 10V	2V	All Supplies
Q_1	V_{BE1}	0.667	-0871	-0.204
	V_{CE1}	4.17	5.35	9.52
	I_{B1}	1.18e-05	-1.18e-05	-1.61e-12
	I_{C1}	1.63e-03	-1.63e-03	1.24e-11
Q_2	V_{BE2}	0.437	0.248	0.685
	V_{CE2}	9.66	-9.61	5.16e-02
	I_{B2}	7.09e-09	9.79e-05	9.79e-05
	I_{C2}	2.48e-07	2.50e-03	2.50e-03
Q_3	V_{BE3}	0.589	-0.014	0.575
	V_{CE3}	9.40	0.51	9.91
	I_{B3}	8.80e-07	-3.27e-07	5.53e-07
	I_{C3}	8.80e-05	-3.69e-05	5.11e-05
Q_4	V_{BE4}	-0.728	0.377	-0.351
	V_{CE4}	9.58	0.32	9.90
	I_{B4}	-1.71e-12	1.09e-14	-1.70e-12
	I_{C4}	1.26e-11	3.46e-13	1.30e-11

Table VI. the voltage and current supplies used for local biasing

Progressive biasing, employed in the last two examples, has other applications in the analysis and design of analog circuits. One application in circuit design is in setting the

operating regions of the transistors based on the design specs. In this situation the transistors are initially locally biased to their assigned Q-points. What is then left to complete the DC circuit design portion is to move the generated local biasing sources to the locations designated for the circuit power supplies. The other application of local biasing is in circuit diagnosis and modification; where local treatments of a malfunctioning circuit can solve the problem rather then doing a complete redesign. Both applications are briefly explained next.

7.1 Using local biasing in circuits design

The methodology just described allows a circuit designer to locally bias the individual nonlinear devices in a circuit as desired; for the rest he/she will be dealing with the linear portion of the circuit. In other words, in this methodology the biasing become local and isolated from the rest of the circuit, while the AC signals remains global and not mixed with the biasing. This allows the designer to concentrate on the AC signal operations and design the circuit based on its best performance.

Another advantage in using local biasing for design purposes is the convenience it provides for the designer to play with the operating regions of individual transistors until he/she is satisfied. Whereas, in the traditional (global) biasing the DC and AC signals are mixed; making the design complex. In a way, by local biasing we are creating an orthogonality between AC and DC design and operation of circuits. Here, only the nonlinear devices are individually biased to meet the designated operating regions. Whereas, in the AC design the rest of the circuit contribute to the signal performance, with the small signal linear models of the devices included in the circuit.

In addition local biasing minimizes DC power consumptions in the circuit; hence by starting the circuit design with local biasing we in fact have started the design with minimum power. For any modification such as source transformations to another destination in the circuit we can monitor the power variations and go for optimal power as the design progresses.

Design Procedure: We are now ready to implement the proposed methodology in design stages. Algorithm 2 provides a stepwise procedure to design an analog circuit using the new methodology. Although given for an amplifier the procedure is equally applicable to any other analog circuit.

Algorithm 2:

1. To design an amplifier for a given topology and design specs first select the desired operating regions for the devices (diodes and transistors) so that the devices can best respond to the design specs. Locally bias the devices by augmenting current and voltage sources to each individual[6] device to meet the DC design specs.
2. Replace the locally biased devices with their small signal linear models and proceed designing the linear amplifier for its AC performance. It is important to note that as long as the linear models, representing the locally biased devices, are not altered the circuit topology, as well as the component values (including the W/L ratios in MOS transistors) can be changed for optimal performance of the amplifier.

[6] It is possible to combine multiple (transistor) devices in an m-port network and locally bias the m-port network instead.

3. After the AC performance design is completed satisfactorily go back and replace the linear models of the transistors with their corresponding locally biased devices. Theoretically, both DC and AC design of the amplifier is over by now, except for the existence of the distributed DC sources.
4. Use source transformation techniques combined with current sourcing and mirroring techniques to move and reduce the current and voltage sources used for the local biasing, in such a way that the result could end up with one or a few supplies -- V_{DD} and V_{SS} – in the circuit.

The following example provides the design of an amplifier using the proposed methodology described in Algorithm 2.

Example 9 –Three-stage CMOS Op-Amp: Consider designing a three-stage operational amplifier with circuit configuration shown in Fig. 29. For simplicity the current mirrors are substituted by ideal current sources. The transistors' biasing currents I_{D1} = 21.6 μA, I_{D2} = 21.6 μA, I_{D3} = 110 μA, and I_{D4} = 2.63 mA are provided as design specs; which are based on the power expectation for each amplifier stage. Also the design is targeted for a maximum output voltage swing of 7 V peak to peak. In addition, base on the design specs we expect to get about 5 mW of output power to the load.

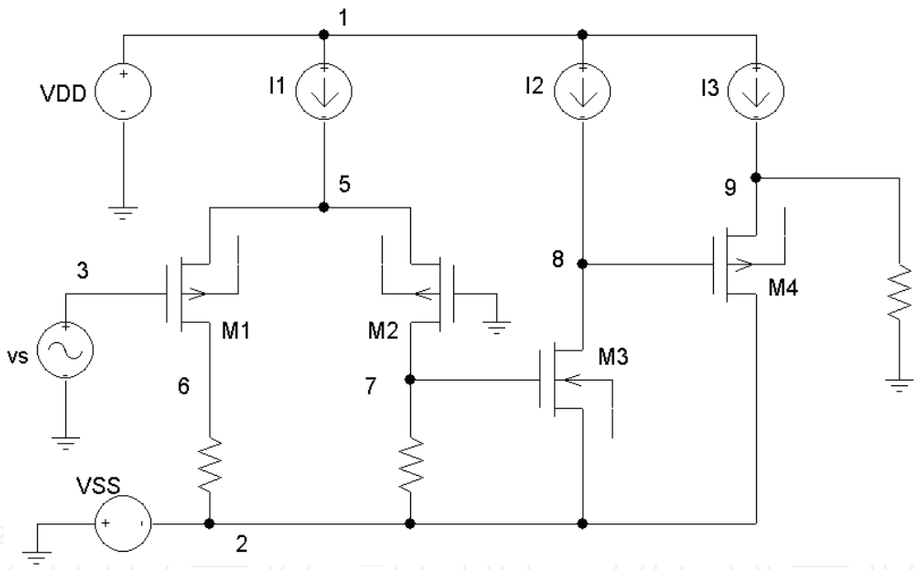

Fig. 29. Basic configuration for a three stage operational amplifier.

The next step in the design is to size the transistors. The channel lengths are assumed fixed for L = 2 μm; the transistor widths, based on the drain currents, are calculated and shown in Table VII. Now we locally bias the transistors so that the operating points are located far enough into the linear portion of the characteristic curves, in the saturation regions. It is reasonable to assume that the operating points of M_3 and M_4 to be two critical design specs. This is because M_3 and M_4 represent output stages and need to exhibit maximum voltage swings with high currents. The next step is to locally bias the transistors in the circuit and then remove all external DC supplies, as depicted in Fig.30. Table VII shows the biasing design specs for the transistors (see Fig.20).

Next, we can proceed with the design, taking the followings specs into consideration:

- For a maximum of 7 V peak to peak output voltage swing (M_4) we need the DC power supplies $V_{DD} = V_{SS} = 5$ V.
- The selection of the operating currents for the transistors is based on the power expectation for each stage. For example, in the buffer stage, the device current $I_{D4} = 2.63$ mA is selected to deliver about 5 mW power to the load. Likewise, given the current gain for the buffer stage $A_{I3} = 24$ A/A we can calculate the drain current for M_3 as $I_{D3} = 2.63 / 24 = 0.11$ mA.
- The selection of V_{GS} for M_4 is important in pushing the operating region of the buffer transistor far enough into the linear saturation region and to produce $V_{outp\text{-}p} = 7$ V without distortion.
- Other design parameters such as the resistor values are also calculated for the targeted performance of the amplifier. For this design we find $R_{M1} = 51$ KΩ, $R_{M2} = 51$ KΩ, and $R_{M4} = 4.5$ KΩ to best fit the specs.

Locally biasing Sources	W/L μm	V_{DS}	V_{GS}	V_{SB}	I_D
pMOS-1	15/2	-5.55	-1.65	-3.35	-21.6 μA
pMOS-2	15/2	-5.55	-1.65	-3.35	-21.6 μA
nMOS-3	30/2	2.71	1.10	0.00	110.0 μA
pMOS-4	500/2	-4.74	-2.03	-5.26	-2.63 mA

Table VII. Transistor Sizes and DC sources for local biasings of Transistors

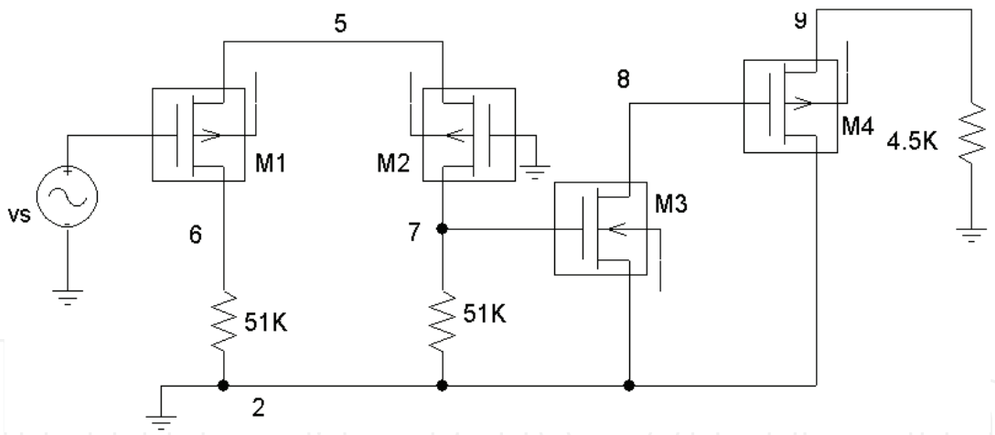

Fig. 30. The Op-Amp configuration with locally biased devices

The initial stage of the design of the amplifier including the component biasing is over now. In the next stage we need to replace the transistors with their small signal models to perform the performance design such as the gains, bandwidth, and so on. However, because our main intention at this point is the biasing design we ignore details on the performance design. Here we are allowed to modify the component values (except for the transistors' model values which are anchored by the local biasing) until the desired responses are obtained and the design criteria are met. Following the performance design we need to replace the linear transistor models with their locally biased transistors, as shown in Figure 30. Note that no external DC supply other than those included in the local biasing is needed to run the amplifier. Figure 31 shows the WinSpice3 simulation results for the amplifier with

the local biasing. Both the transient responses (the output signals before and after the buffer stage) and the frequency responses are provided. Note that all node signals in the transient responses lack any DC component, due to local biasing; hence no need for coupling capacitors or to stop offset voltages.

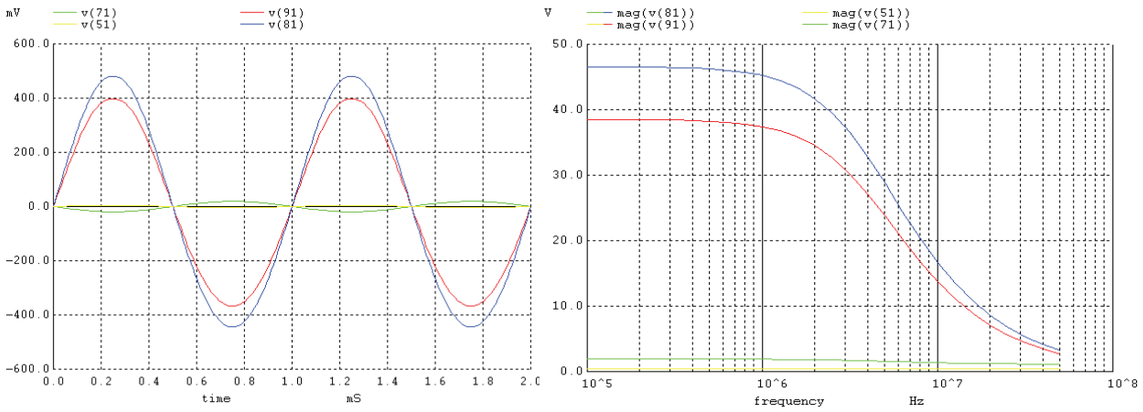

Fig. 31. The transient and frequency responses of the Op-Amp with locally biased configuration

Finally, for practical reasons we need to replace the local biasing supplies with limited external supplies located at the designated locations in the amplifier. Application of certain procedures (not explained here) has results in having three current sources I_1 = 43 μA, I_2 = 68 μA, and I_3 = 1.12 mA plus two voltage sources V_{DD} = 5 V and V_{SS} = 5 V, as originally shown in Fig. 29. These sources are replacing the local biasing sources in the amplifier.

7.2 Circuit diagnosis and partial local biasing

By partial local biasing (PLB) we mean to perform local biasing on a device (or a port) without disturbing any other part in the circuit, even without changing the regular DC supplies in the circuit. Hence, PLB allows a designer to diagnose an analog circuit and locally tune it by changing the biasing conditions of one or more components in the circuit without changing the operating points of other components. PLB is different from local biasing in which, local biasing makes the entire circuit DC-static (zero DC power) except for the locally biased devices; whereas in PLB the DC supplies remain intact within the circuit, except that the operating points of the ports, selected for modification, can be changed through PLB. This modification is done by augmenting those ports with a combination of voltage and current sources that have values equal to the differences between the old and the new Q-points of those ports.

PLB has two main properties; it is local and it is not destructive. It is local because it only affects the component under test. Second, because of the additivity property of local biasing and due to being local, PLB can be progressive in steps of one or more components at a time. For example, if in a circuit modification the biasing conditions of several components need to be changed, we can change one device at a time and look for the responses as we progress [15]. One application of PLB is in circuit diagnosis and repair. If the problem relates to a faulty transistor, for example, we can take it out and replace it with a new one. We can also

replace it with a different type of transistor, such as changing BJTs to MOS transistors, in a circuit. Another application of PLB is in partially testing a complex circuit looking for the troubled places. For example, consider the circuit in Fig. 32(a), where the MOS transistor M is malfunctioning because its output port is at Q(V, I), which is at the wrong place on the characteristic curve (Fig. 32(b)). To correct the situation we need to move the operating point to the right on the characteristic curve, positioning it at $Q_1(V+\delta V, I+\delta I)$, as indicated in Fig. 32(b). We use PLB by augmenting the transistor with one voltage and one current source that has values δV and δI, respectively. This causes the OP to move from Q to Q_1 without affecting the rest of the circuit, as depicted in Fig. 32(c). Later, we may need to move the sources, δV and δI, and integrate them with the rest of the DC supplies in the circuit by using techniques such as source transformations. Of course, we need to be careful in this source transformation so that the other operating points, for other transistors, are not disturbed.

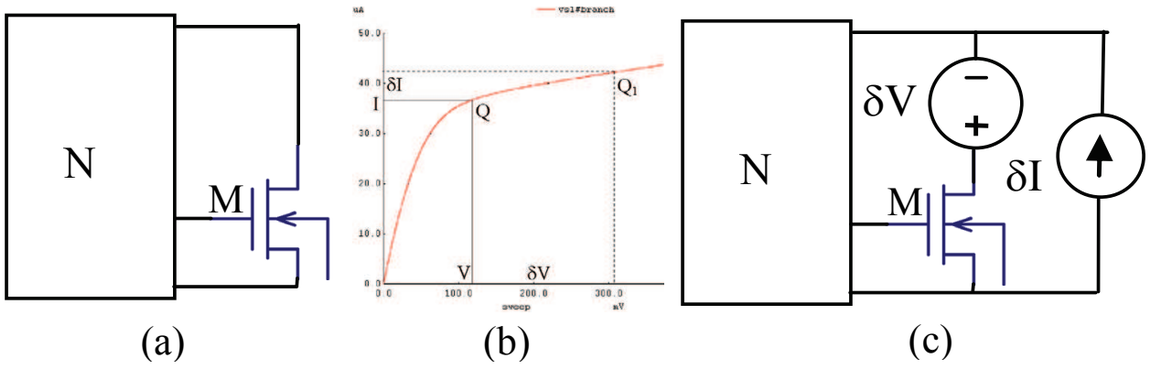

Fig. 32. Partial local biasing of an MOS in a circuit; (a) the original circuit with distorted output; (b) the device characteristic curve; and (c) .corrected operating point through partial local biasing.

The following example further explains the procedure.

Example 10: In this example we are considering a two stage MOS amplifier with feedback, as shown in Fig. 33. Initially both transistors, M_1 and M_2, are assumed identical with W/L = 50/5 μm. The amplifier works fine with this configuration without distortion. However, in an attempt to improve the output power of the amplifier we modify it by changing the size of M_2 from W/L = 50/5 to W/L = 100/5, doubling the transistor channel length. The change disturbs the biasing situation in the amplifier and distorts the output response, as shown in Fig. 34. Next we apply the PLB on M_2 to correct its biasing situation. It turns out that locally adding an extra current I_{D2} = 560 μA to the drain current of M_2 would correct its operating point. Both output waveforms, one before the biasing correction and one after, are shown in Fig. 34. Note that the gross distortion observed in the output waveform of the original amplifier has disappeared from the output waveform of the modified amplifier. We also notice a better gain for the second stage of the amplifier, which is mainly due to a better and flatter operating region created for M_2 transistor.

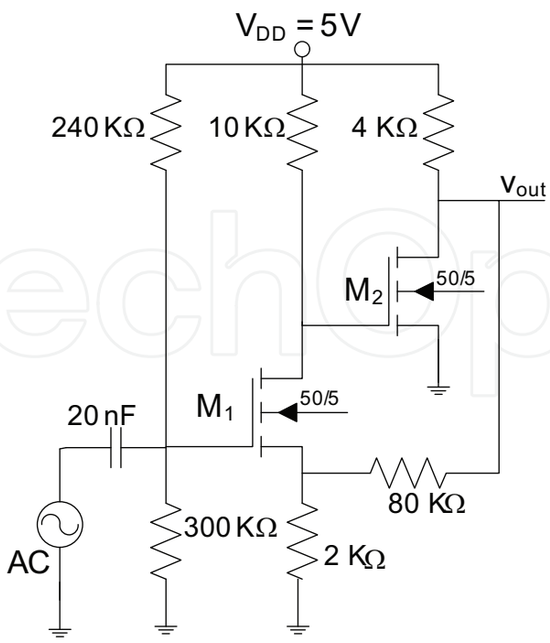

Fig. 33. Two stage MOS amplifier with feedback with the output distorted for W/L = 100/5

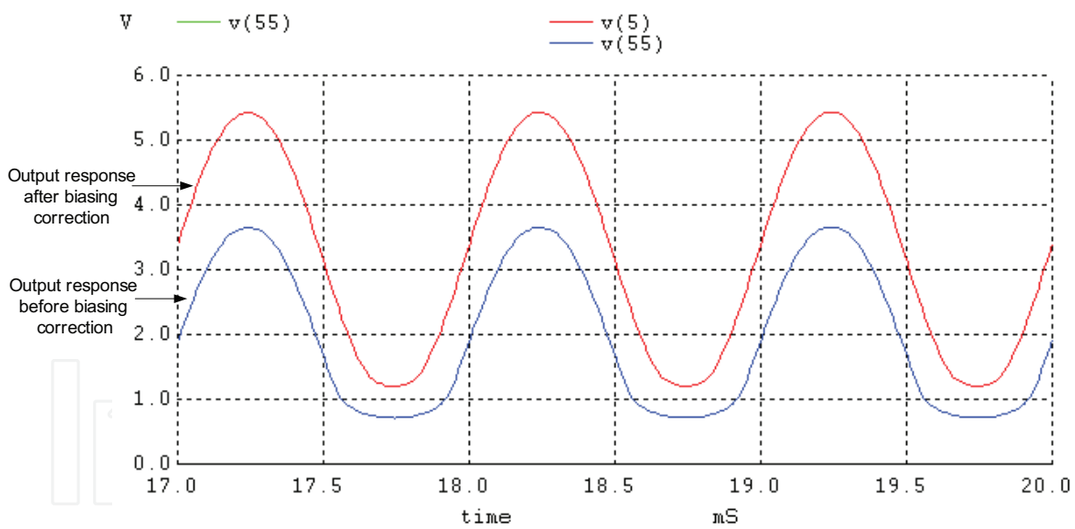

Fig. 34. The output response of the amplifier before and after bias correction.

8. Chapter summary

A new modeling technique, called H˜-modeling, is introduced for one and multiple port networks. It is shown that H˜-models are more dynamics compare to Thevenin or Norton equivalent circuits, and they have the ability to more accurately describe the port behavior. The properties of this model, particularly in calculating the input-referred noise, is discussed. A special type of H˜-model, called nullified H˜-model, or simply H-model, is also

introduced; and many properties of H-modeling including power management in the circuit is investigated. It is shown that H-models are not limited to single port networks but cover multi-ports, as well. A major property of H-modeling is in local biasing of transistors. It separates nonlinear components from the linear portion of the circuit for faster and more efficient circuit biasing. Here a designer can take advantage of H-modeling and bias individual transistors (or in combinations) with no need to perform the the normal circuit biasing. Because of the distributed supplies, created due to local biasing, the method is extended to include coupling capacitors for biasing purposes as well. The fact that local biasing helps to do a mixture of regular but progressive biasing in complex circuits is discussed. Here, local biasing keeps (stores) the status of partial biasing in any stage of a gradual and step-wise biasing procedure, i.e., it allows the global biasing to keep progression toward the completion of the biasing. Next, partial-local biasing is introduced, which helps to modify and locally correct the biasing of a circuit. This is important in debugging, modifying and repairing complex analog circuits.

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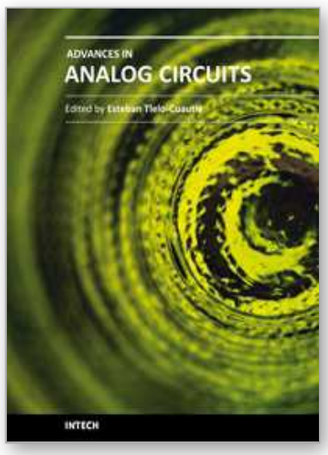

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This book highlights key design issues and challenges to guarantee the development of successful applications of analog circuits. Researchers around the world share acquired experience and insights to develop advances in analog circuit design, modeling and simulation. The key contributions of the sixteen chapters focus on recent advances in analog circuits to accomplish academic or industrial target specifications.

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