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DC/DC Step-Up Converters for Automotive Applications: a FPGA Based Approach

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1. Introduction

One emerging application of power electronics is the driving of piezoelectric actuators. These actuators can be used for different kinds of application. They are employed for micro and nano positioning tasks as well as hydraulic or pneumatic valves, where they replace magnetic control elements. Piezoelectric actuators have some specific advantages such as high resolution of the displacement, excellent dynamic properties and energy consumption near to zero for static or quasi static operations.

So, high performances, low emissions and less fuel consumption bring car designers to adopt new technologies in automotive systems. The use of piezoelectric actuators (used as injectors) allows less response time with respect to traditional magnetic actuators but requires high driving voltages in order to be driven in a smaller time. This is a big concern in automotive environment, where the battery voltage is still the main power source available.

A switching amplifier for reactive loads generally consists of two components. A unidirectional DC/DC converter with a small input power loads and large buffer capacitor and, a second bidirectional DC/DC converter that controls the energy exchanged between the buffer capacitor and the reactive load.

The requirements on the unidirectional DC/DC converter are few. It only needs to compensate the power losses of the two stages plus the energy dissipated in the actuator and the connected mechanical system. Second stage presents more problems, because it must be designed for full system power.

Conventional DC/DC boost converter is not the best solution in piezoelectric based applications where high step-up ratio and high efficiency power conversion is required.

The coupled inductor boost converter meets the demanding requirements of these applications, including high reliability, relative low cost, safe operation, minimal board space and high performance, therefore an excellent choice for interfacing the battery with the high voltage DC_{BUS} used for piezoelectric actuator system. An FPGA based controller allows interleaving two phases reducing both peak primary current and output current ripple. Moreover, a quasi constant frequency hysteretic current control technique reduces EMI interferences and ensures control loop stability. A soft start sequence permits to limit average input current and guarantees start-up phase in a short time.

In this chapter an FPGA based interleaved coupled inductor boost converter is presented for high step-up automotive applications.

Design and analysis of the proposed converter are reported. Finally experimental results are provided for verification of the proposed converter.

2. System specification and topology

Nowadays piezoelectric actuator allows less response time with respect to traditional magnetic actuator but requires high driving voltages.

In a traditional magnetic actuator the voltage applied is less than 100V, so a standard DC/DC Boost topology can be used to step up the 12V battery input voltage. Piezoelectric actuator require a high DCbus voltage to obtain high performances so high voltage step-up DC/DC converters are necessary to provide the interface between the standard energy storage component (battery) and the high voltage DCbus of the bidirectional converter used to drive the reactive load.

Fig.1 shows the typical power train of automotive piezoelectric actuator system.
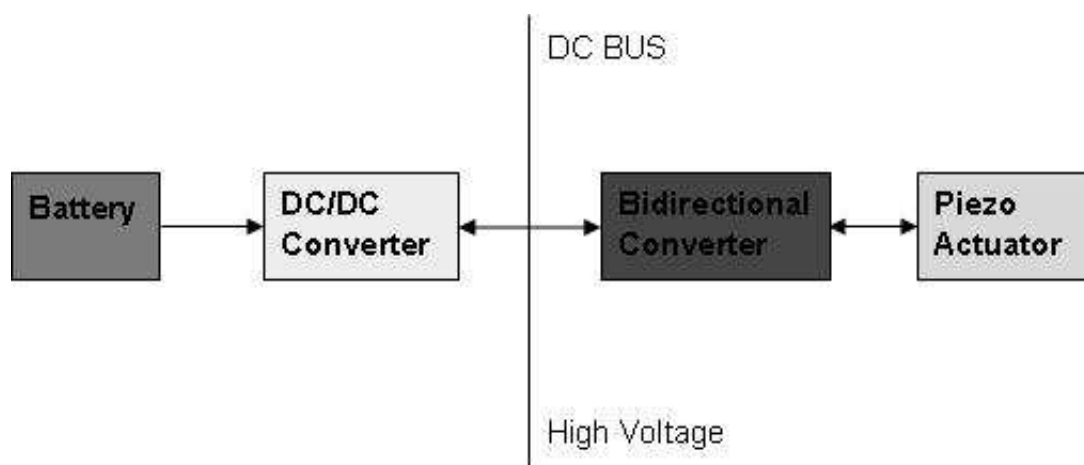

Fig. 1. Power solution for automotive piezoelectric actuators

So, the boost converter must be able to generate the a voltage up to 350V starting from a standard 9V-18V automotive range. If the input voltage is lower than this range, the system works in safe mode. Limit start up-time to reach the maximum output voltage is limited to 150ms and the maximum output power is 100W. The efficiency of the converter must be at least 85% under standard operating conditions.

In a conventional DC/DC Boost converter the duty ratio increases as the output to input voltage ratio increases. This class of DC/DC converter is not the best solution in piezoelectric based applications where a high step-up ratio (more than 20) and high efficiency power conversion is required.

Fig.2 shows a coupled inductor DC/DC boost converter topology: this converter is a good solution to the above problems since it reduces the required duty ratio for a given output to input voltage ratio in conjunction with a small voltage across the switch S (reducing switching losses).

The duty ratio and the switch voltage stress can be controlled by the N2/N1 turns ratio of the primary and secondary inductors (L1 and L2). Therefore, for high voltage step-up

applications, the coupled inductor boost converter can be more efficient than the conventional boost converter.

Moreover, for high power requirements and redundancy purposes, the coupled inductor boost converter can be easily interleaved to achieve high power, high reliability and efficient operation with reduced inductor and capacitor sizes. Various advantages of interleaving are well reported in the literature (Zhao & Lee, 2003).
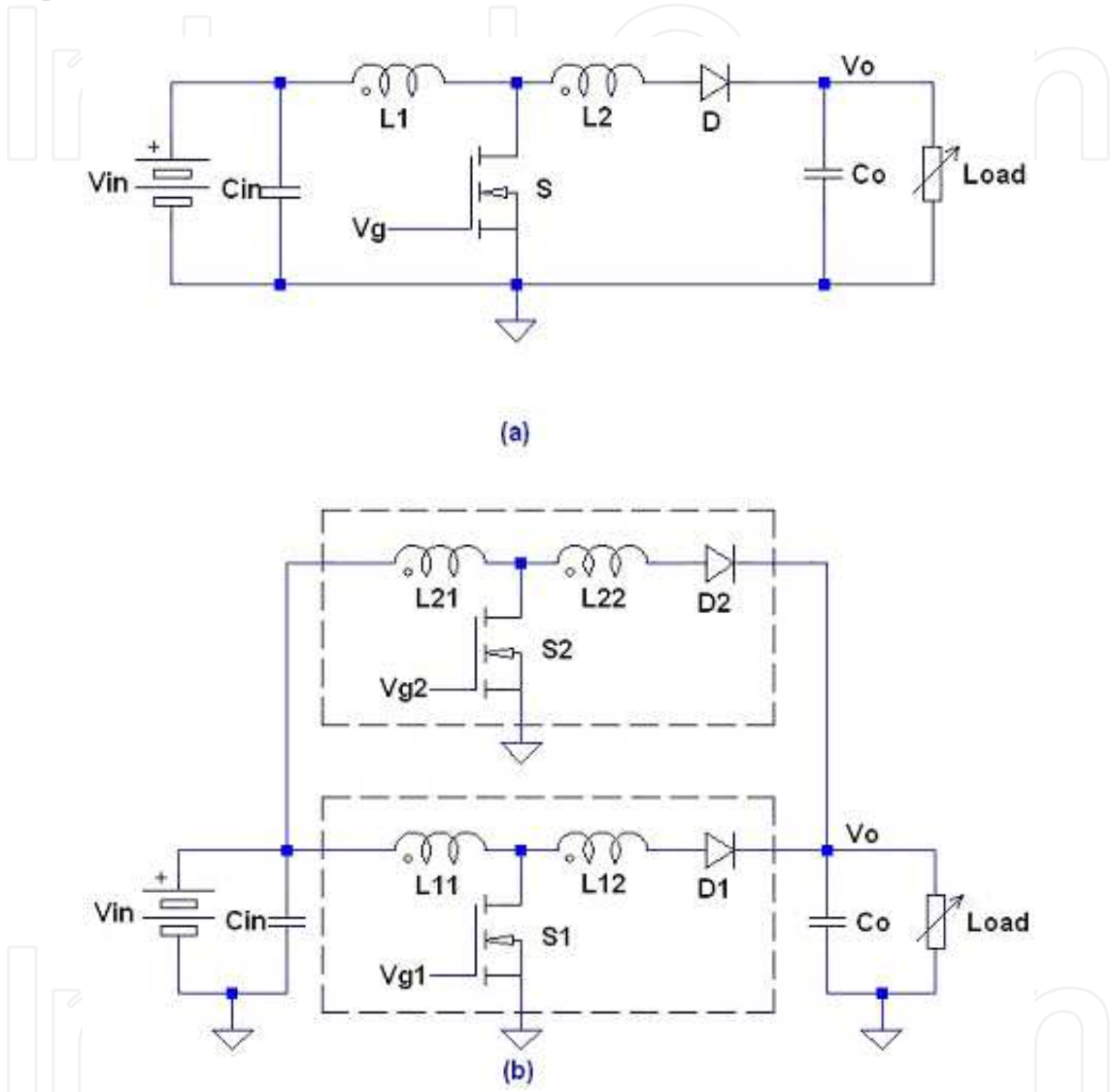

(a)

(b)

Fig. 2. (a) coupled inductor and (b) two phases interleaved coupled inductor boost converters

3. Design

Assuming the coupled inductor boost converter is in a continuous conduction mode (CCM) the steady state output voltage to input voltage ratio for an ideal converter can be obtained as:

$$\frac{V_o}{V_i} = \frac{(1 + kD)}{1 - D} \tag{1}$$

where Vi is the input voltage, Vo is the output voltage, D is the duty cycle of the converter and k is the secondary to primary inductor turns ratio. It can be seen from eq.1 that, for the same voltage gain, the duty cycle can be reduced by increasing turn ratio.

For high current or high power applications interleaving boost converter are well suited (Dwari & Parsa , 2007). In this approach a single coupled inductor boost converter cell (fig.2a) is treated as a phase of 'n' parallel connected phases (fig.2b). In order to operate at the same duty ratio a phase shift but of 2п/n radiant electrical angle must be considered. Under normal of full load condition each phase equally shares the total output load.

3.1 Switching frequency

In an interleaved system the number of cell (n) mainly depends on the step up voltage ratio and the maximum power demand of the load. In this work the nominal input voltage is taken as 12V and the range is the automotive standard 9V-18V.

With an output DCbus voltage of 350V, the voltage ratio is greater than 29. Referring to fig.3, using a secondary to primary inductor turn ratio (k) of 10 and incorporating the switch voltage and diode forward drop in the converter in equation 1, the duty cycle D is 0.72.

The expression of boundary inductance depends by load condition (eq.2) so, assuming minimum output power of 50W (half of total output power) the product Lf_{SW} must be greater than 0.767V/A.

$$Lf_{SW} = \frac{R_L D(1-D)^2}{2(1+k)(1+kD)} \tag{2}$$

Assuming a 5µH of primary inductance, the minimum switching frequency in order to satisfy the CCM condition is 153kHz, a quite high control frequency that requires a parallel implementation on a FPGA device with some control tricks to guarantee the control loop strategy.
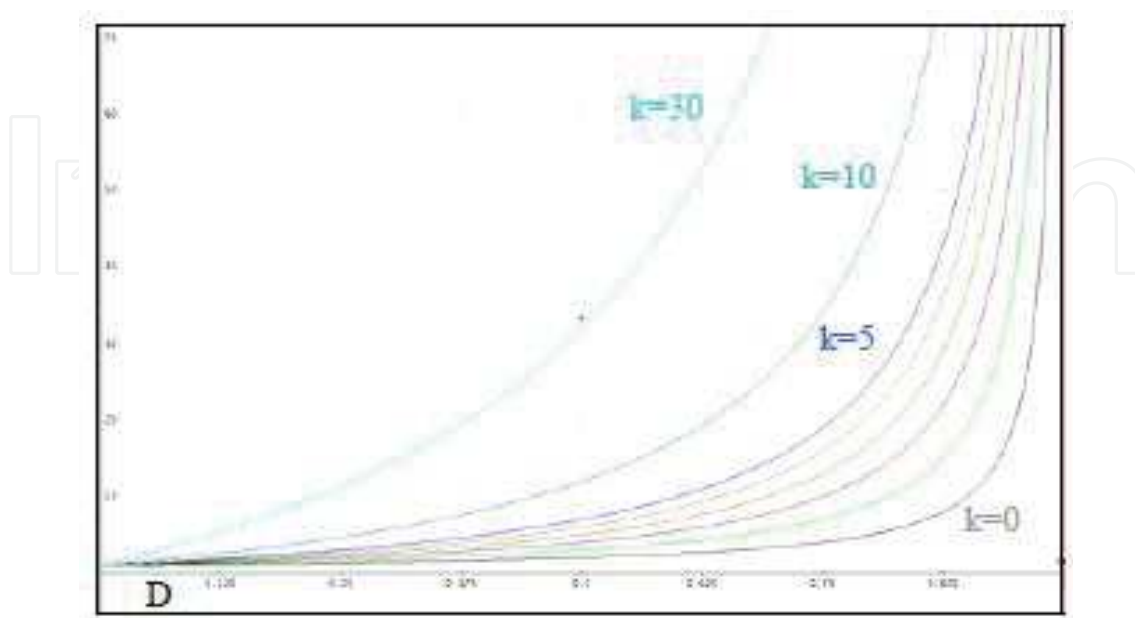

Fig. 3. Comparison among Vo/Vi as k fuction

3.2 Selection of power switch and freewheeling diode

The power switch is a high speed MOSFET in order to have fast rise and fall time and relatively low R_{DSon} that ensure less switching and conduction losses.

One of the main advantages of this topology respect to traditional Boost converter is that the maximum voltage on the MOSFET drain is limited by the turns ratio between primary and secondary inductors:

$$V_{D\max} = \frac{V_o - V_i}{1+N} = \frac{350V - 6V}{1+10} = 30.7V \tag{3}$$

where Vi is the input voltage, Vo is the output voltage and N is the inductors turns ratio.

The value in eq.3 is obtained considering the worst case, that is when the minimum input voltage occurs. To avoid over voltage MOSFET damaging the drain source voltage is chosen at least 1.5 times the V_{Dmax}.

The primary peak current value is determined by the duty cycle and the T_{on} period:

$$I_{pk1} = \frac{V_i D}{L_p f_{SW}} = \frac{6V\,0.84}{5uH\,200kHz} = 5A \tag{4}$$

The free-wheeling diode in Boost circuit plays a central role. When the switching transistor turns on, the diode should turn off immediately because otherwise the transistor will switch on into a full short circuit to the boosted output voltage close to 350V causing extreme over current and high dissipation.

Three different technologies could be used:

1. PiN
2. SiC Schottky Barrier Diodes
3. Fast Recovery Epitaxial Diode (FRED)

While Schottky and PiN diodes offer similar circuit functionality, their behavior is determined fundamentally different physical mechanisms. These differences directly impact the power dissipation associated with these devices.

Schottky Barrier Diodes (SBDs) offer a low junction voltage, low switching loss and high speed, but suffer from high on resistance.

When operated at high current density, PiN diodes offer significantly reduced on-resistance due to conductivity modulation, but suffer from high junction voltage and high switching loss.

The FRED diodes could be a good compromise between forward voltage, low peak reverse recovery currents with soft recovery. These diodes are characterized by a soft recovery behavior, showing even at very high di/dt (>800A/us) no tendency to "snap-off", but present higher leakage current than other diode. However the power loss caused by the leakage current is small compared to forward current and reverse recovery losses.

In this converter, the output diode should be able to support high voltage (higher than 350V) but a quite low average current (this is the average output current and so it is less than 0.3A).

3.3 Input filter capacitor

The input filter capacitor limits the supply ripple voltage. The less ripple voltage desired, the larger the capacitor, and the larger the surge current during the power up period. There are three major considerations when selecting a capacitor for this function:

- Capacitance value
- Voltage rating
- Ripple current rating

The value of the bulk capacitor can be found by:

$$C_{IN} \cong \frac{2P_{OUT}}{f_{SW}V_{RIPPLEpp}} = \frac{200W}{200kHz3V} = 330\mu F \tag{4}$$

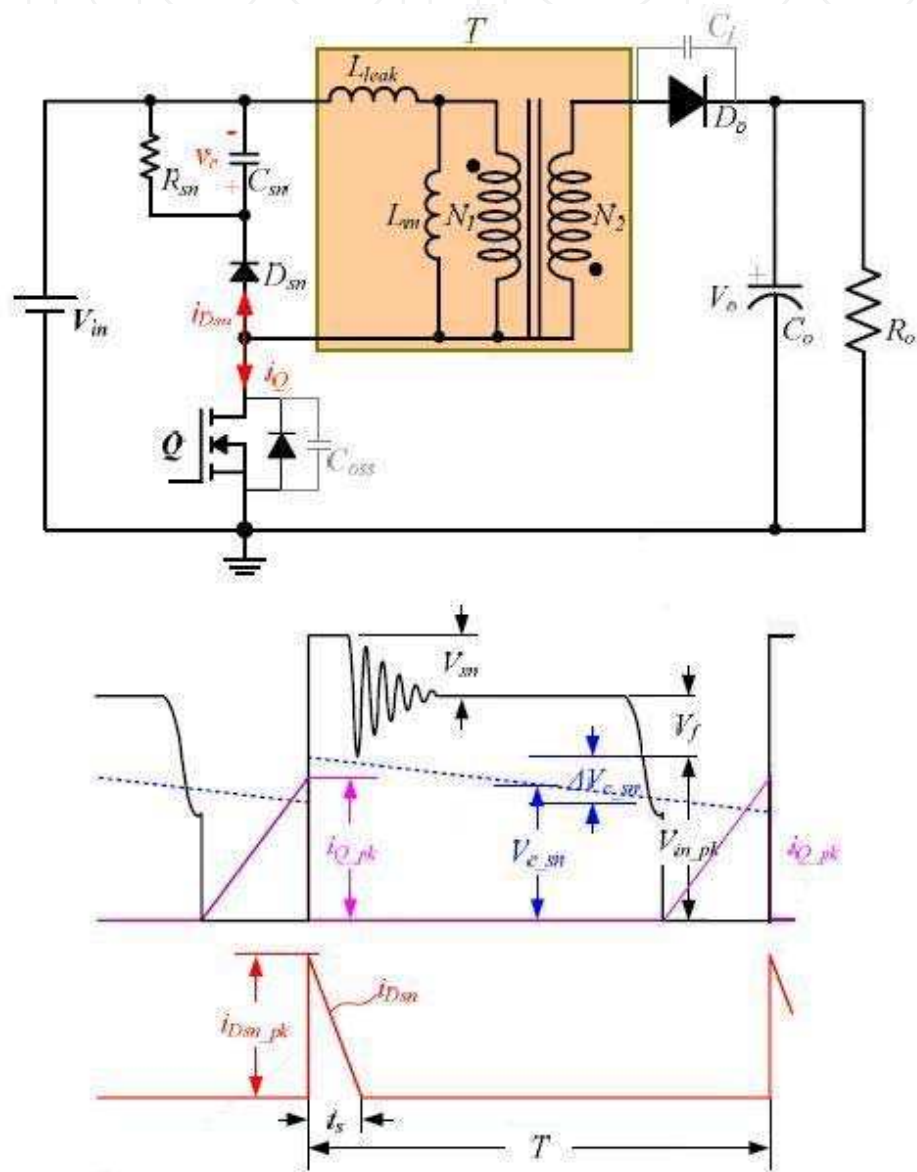We have placed three 100µF electrolytic capacitors and four 10µF ceramic in parallel.

Fig. 4. Snubber Circuit

3.4 Current sense

High side current sense amplifier has been used to monitor the primary input current across a shunt resistor. The sense voltage is amplified and shifted from the analog power supply to

a ground referred output. Considering 300uF as output capacitance, start up time is less than 150ms and low input voltage, the average input current in this phase is:

$$I_{INstart-up} = \frac{V_{OUT}}{V_{IN}} C_{OUT} \frac{V_{OUT}}{\delta t} = \frac{350V}{9V} 300\mu F \frac{350V}{150ms} = 27.2A \tag{5}$$

Assuming a peak current about 30A, to limit the voltage drop below 5% of nominal input voltage and therefore the power losses, the shunt resistor must have a value lower than 20mΩ. A four wire Kelvin terminals resistance is used to limit the parasitic resistance as well as series inductance. A high side, unipolar current shunt monitor IC has been mounted in order to correctly acquire and convert the shunt voltage with the analog voltage range of digital platform.

3.5 Snubber circuit design

In this type of converter, the resonance between L_{leak} and C_{oss} causes an excessively high voltage surge, that cause damage to the MOSFET during turn-off. This voltage surge must be suppressed and snubber circuit is therefore necessary to prevent MOSFET failures as shown in fig.4.

The clamping voltage by snubber is:

$$V_{sn} = V_f + L_{leak} \frac{\Delta i}{\Delta t} = V_f + L_{leak} \frac{I_{Dsnpk}}{t_s} \tag{6}$$

Therefore:

$$ts = \frac{L_{leak}I_{Dsnpk}}{V_{sn} - V_f} = \frac{L_{leak}I_{Dsnpk}}{1.5V_f} \tag{7}$$

The maximum power dissipation of the snubber circuit is determined by:

$$P_{sn} = \frac{1}{T} \int_0^{t_s} V_{sn} I_{Dsn}(t)dt = \frac{1}{2} L_{leak} I_{Dsnpk}^2 f_{SW} \tag{8}$$

The maximum power dissipation is:

$$P_{sn(max)} = \frac{1}{2} L_{leak} I_{Dsnpk}^2 f_{SW} = \frac{V_c^2}{R_{sn}} \tag{9}$$

Where:

$$V_c = V_{sn} = V_f + V_{Lr-} \tag{10}$$

Therefore, the resistance Rsn, is determined by:

$$R_{sn} = \frac{2V_c^2}{L_{leak}I_{Dsnpk}^2 f_{SW}} \tag{11}$$

The maximum ripple voltage of the snubber circuit is obtained by:

$$\Delta V_c = \frac{V_c}{C_{sn}R_{sn}f_{SW}} \tag{12}$$

The larger snubber capacitor results, the lower voltage ripple, but the power dissipation increases. Consequently, selecting the proper value is important. In general, it is reasonable to determine that the surge voltage of snubber circuit is 1.5 times of V_f and the ripple voltage is 25V. Thus, the snubber resistor and capacitor are determined by the following equations:

$$ID_{snpk} = \frac{V_iD}{L_Pf_{SW}} = 5A \tag{13}$$

$$V_{sur} = 1.5V_f = 1.5\frac{V_o - V_i}{1 + N} = 45V \tag{14}$$

$$t_s = \frac{L_{leak}I_{Dsnpk}}{1.5V_f} = \frac{0.1\mu H 5A}{45V} 11ns \tag{15}$$

$$R_{sn} = \frac{2V_c^2}{L_{leak}I_{Dsnpk}^2 f_{SW}} = \frac{2(45V^2)}{0.1\mu H(5A^2)150kHz} = 10.8k\Omega \tag{16}$$

$$C_{sn} = \frac{V_{sn}}{\Delta V_c R_{sn}f_{SW}} = \frac{30V + 45V}{25V 10.8k\Omega 150kHz} = 1.85nF \tag{17}$$

4. Control

The proposed DC/DC converter is controlled using a quasi constant frequency hysteretic current mode technique with current sharing and interleaving phases as inner loop in order to have symmetrical current partition between the switching phases. The outer control loop is based on a digital PI control law in order to stabilize the DC/DC output voltage.

Fig. 5 shows the schematic diagram of the proposed control technique.

The PWM signal obtained by feedback loop (from the hysteretic comparator) is acquired by the FPGA and processed to correctly control the two phases of the tapped boost.

To avoid sub-harmonic instability a variable frequency control is needed and to stabilize the switching frequency it is necessary to introduce a high speed period feedback loop. This is performed by an integral control law which, starting from the outer loop command, generates the variable hysteresis for the comparator.

Fig.6 shows a block diagram of a hysteretic control with frequency control loop.

There are several challenges to efficiently implement the proposed control technique with analog and discrete components. These challenges along with the FPGA implementation are related to:

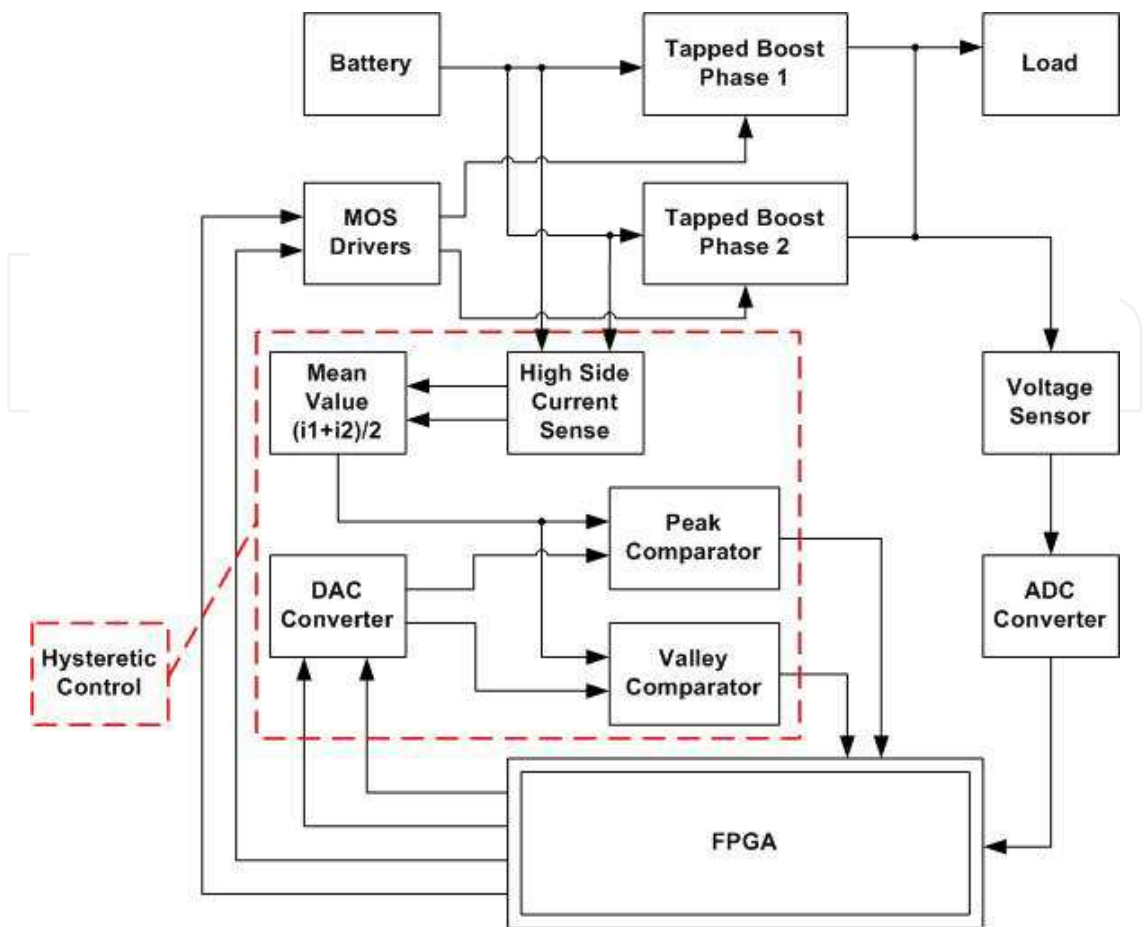- Current/voltage sharing and control
- Frequency feedback

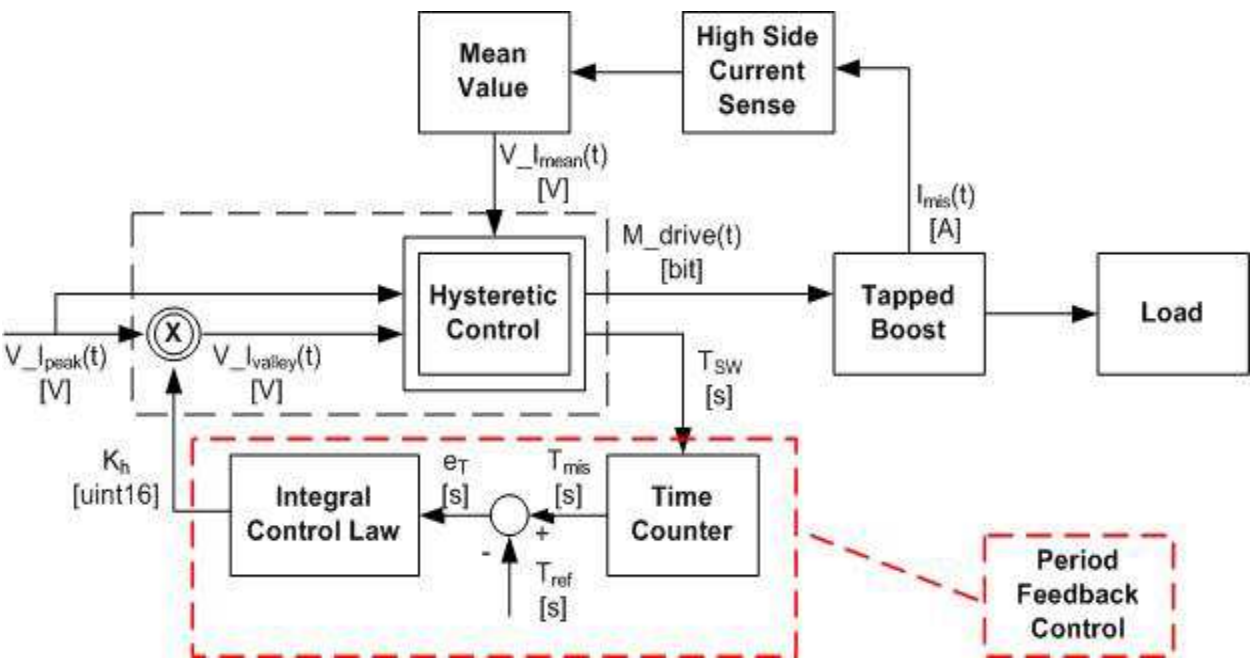Fig. 5. Schematic diagram of coupled inductor control technique

Fig. 6. Diagram of a quasi constant frequency hysteretic current control with a period feedback loop

4.1 Current sharing

It is really important to obtain an almost equally distributed current between the interleaved phases.

Unfortunately, components tolerances, connections differences from phase to phase, load conditions and other non idealities may cause the current distribution (sharing) to be unequal especially during large load transients.

Current sharing between the interleaved converters can be achieved by averaging current of each converter phase and compare the obtained value with command derived by the outer loop. Each phase is then turned on using two control strategies:

1. Sequence toggle mode where the ON signal is present only for one phase per cycle
2. Phase shift control technique where the two phases are shifted of half period

Current sharing functionality can be easily implemented using a fast FPGA.

In the first one the two control pulses (Cm1 and Cm2) are generated interleaved starting from the Cm PWM signal coming from hysteretic comparator (Fig 7a).

In the second control technique CM1 and Cm2 are shifted half period starting from the main control signal generated by the hysteretic comparator (Fig. 7b).
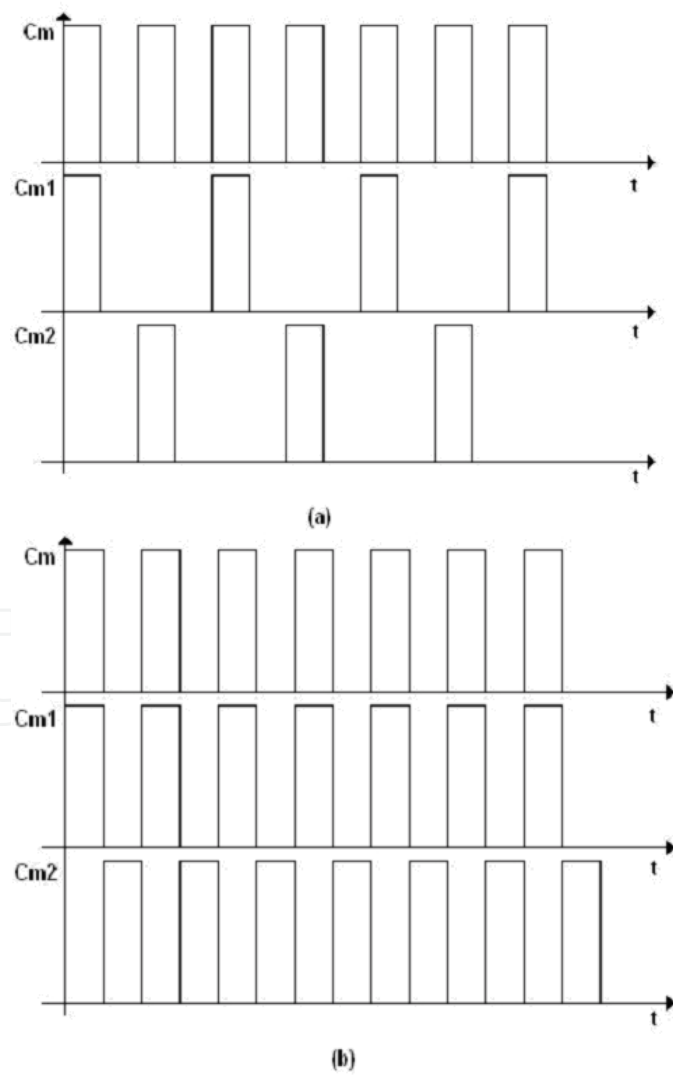

Fig. 7. Different control techniques: (a) toggle with the two phases (b) half period phase shift

The phase shift control technique has been implemented and tested but it presents some problems due to the inner frequency control.

4.2 Hysteretic current control circuit

Input current of each phase is sensed using a high side current sense amplifier with a very low shunt resistor value in order to reduce power losses. Sensed currents are decoupled, averaged, merged and included in the hysteretic current control.

Peak and valley current commands come from the digital outer voltage loop: peak value is the output of a PI control law while the valley one is obtained multiplying the command with a corrective factor derived by the frequency feedback loop.

Peak and valley comparator outputs are directly connected to the FPGA and are used to generate the two control signal applied to the switches.

4.3 Frequency feedback loop

The frequency feedback loop is implemented on FPGA in order to:
- Speed-up the computation of the control law
- Guarantee the modularity of the control law
- Generate a variable hysteretic width based on frequency measure (or period)

To minimize the number of analytical operations and to simplify the IP design on FPGA, we have implemented a switching period feedback loop.

This technique is based on switching period measured using a counter and comparator with a reference previously set (this is a variable of the proposed control). The difference is used as input of a regulator which generates a corrective factor on the nominal hysteretic width in order to stabilize the switching frequency.

The relation of corrective factor at the next step is:

$$k_h(i) = K_h(i-1) + K_i(T_{mis}(i) - T_{ref}$$ (18)

Where k_h is the corrective factor, K_i is the integral gain, i is the digital sampling period, T_{ref} and T_{mis} are the nominal switching period and the measured one.

The generated hysteretic width acts on the value of valley current, leaving the peak current unchanged.

4.4 Frequency feedback loop

Outer loop is a classic digital PI control law with anti-wind up algorithm. The output voltage is sensed and converted using a 12 bit resolution ADC and compared to the reference value on an FPGA IP. The error obtained is then transferred to a PI block that generates the command for the inner current control.

The right half plane zero (RHP) is present and its frequency depends of duty cycle, inductor value (smaller is better) and the load resistance, so at heavy loads its frequency is the lowest and the phase delay is the greatest; at light loads instead the RHP zero frequency is higher, and the converter is easier to control. The RPH zero frequency is obtained using:

$$\omega_{zero} = \frac{\dfrac{V_{OUT}^2}{P_{OUT}}(1-D)^2}{L_p(1+N)(1+ND)}$$ (18)

Common choice is to limit the bandwidth of the control feedback loop at about $1/5^{th}$ of the RHP zero frequency, which considering the worst case (100W at 350V with 12V as input voltage) is about 17kHz. The cross-over frequency is designed in order to stay under 3kHz.

5. Implementation

As previously explained, the control architecture is based on an inner loop that control and limit the average current of the two primary inductor currents, starting from a current reference obtained by an outer loop that maintains stable the DC bus voltage.
Control loops of Boost converter are illustrated in the following technological scheme (fig.8).
All the feedback loops are implemented as IP on FPGA operated at a 100MHz clock, mounted on a prototype board (EKU) completely designed by the Mechatronic Laboratory.
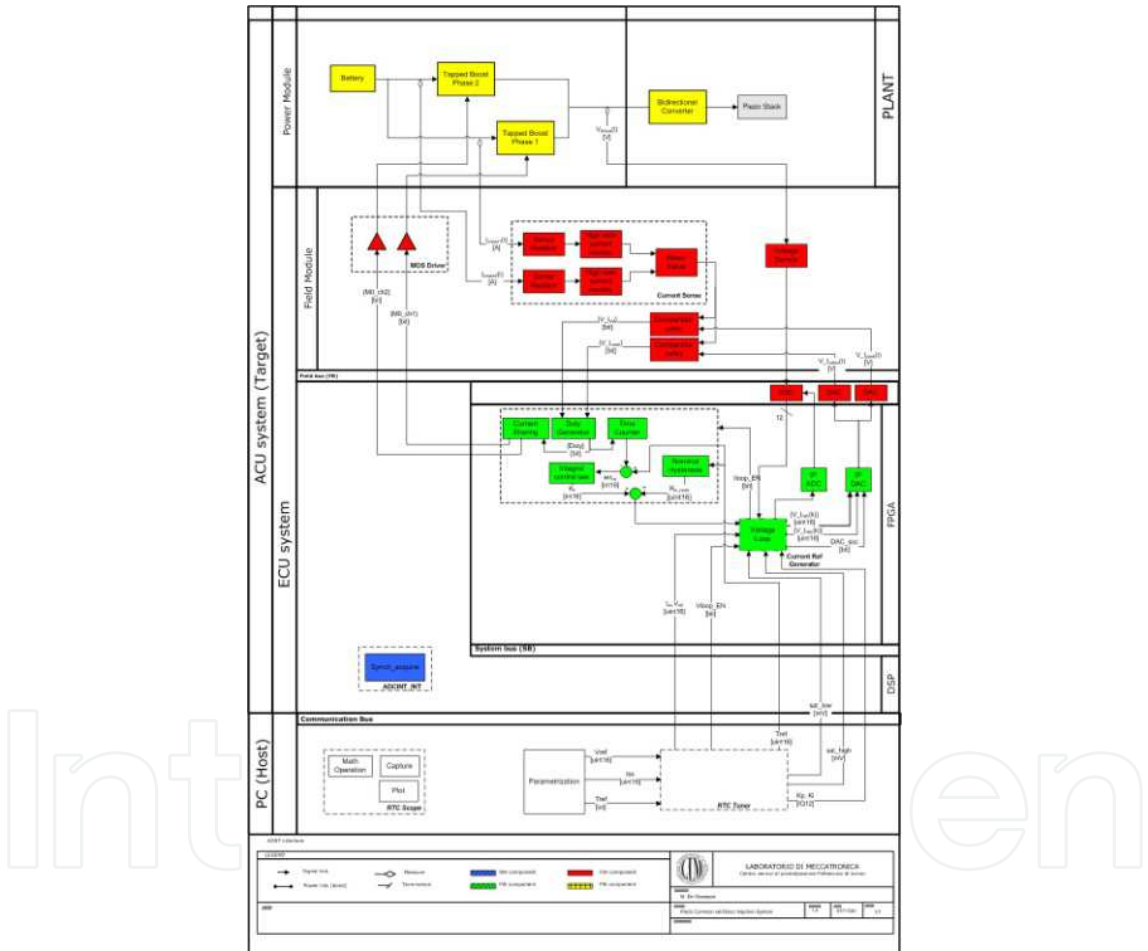
Fig. 8. Technological scheme of the Boost converter implemented

5.1 Current loop
The inner loop of the Boost section controls and limits the input current of each phase monitoring the voltage across the sense resistor connected in high side configuration using a current shunt monitor. The two amplifier's outputs are filtered and averaged in order to obtain a signal that drives the two comparators (peak and valley). With this control strategy the inductor currents ramp alternately between an upper limit and a lower limit.

Digital current control is based on two main blocks that are implemented as IP-core on FPGA:

- Duty Cycle Generator
- Current Sharing Algorithm

The Duty Cycle Generator, starting from peak and valley comparator outputs, controls the intrinsic behavior of an SR flip-flop, which turns the transistor of and on (considering one phase). A current sharing algorithm is added to equally subdivide the input current between the two phases: our strategy called sequence toggle mode, generates commands where only one phase is active at switching cycle; phase shift technique is also implemented but presents instability due to the inherent variable frequency during start up.

Peak and valley references are generated by DAC converters that are directly interfaced with the FPGA using a dedicated IP.

The hysteretic control maintains a controlled difference between the comparator's input and therefore variable frequency current loop. The introduction of a frequency feedback loop in this control leads to have variable hysteresis band but with the advantage of stabilizing the switching period.

5.2 Voltage loop

The outer loop maintains the output voltage stable around a reference value sent by engine control unit as a word parameter via CAN. Output voltage are sensed with a voltage monitor, converted by ADC and compared with digital reference in order to obtain an input to apply to the voltage loop block.

The tapped inductor open loop transfer function is:

$$\frac{V_o(s)}{d(s)} = \frac{V_o(k+1)\left(\dfrac{sL_p(1+k)(1+kD)}{R_L(1-D)^2} - 1\right)}{(D-1)(1+kD)\left(\dfrac{s^2L_pC(1+k)^2}{(D-1)^2} + \dfrac{s^2L_pC(1+k)^2}{R_L(D-1)^2} + 1\right)} \tag{19}$$

It is characterized by two poles, associated to LC output filter components, and one zero, determined by the ESR of output capacitor that for simplicity is neglected.

The two complex poles are placed at a lower frequency:

$$\omega_{poles} = \frac{(1-D)}{(1+k)\sqrt{L_pC}} \tag{20}$$

Additionally it presents a RHP zero. This is characteristic of boost and boost derived converters.

RHP zero determines a phase lag in loop gain of the voltage mode controlled boost converter forcing the maximum cross over frequency to be at most 1/5 RHP frequency. For this reason, a current mode is preferred, as the effect of RHP zero is mitigated.

RHP is a function of the duty cycle, load and inductance and causes an increase in loop gain while reducing the loop phase margin.

A common practice is to determine the worst case RHPZ frequency and set the loop unity gain frequency below one-third of the RHPZ.
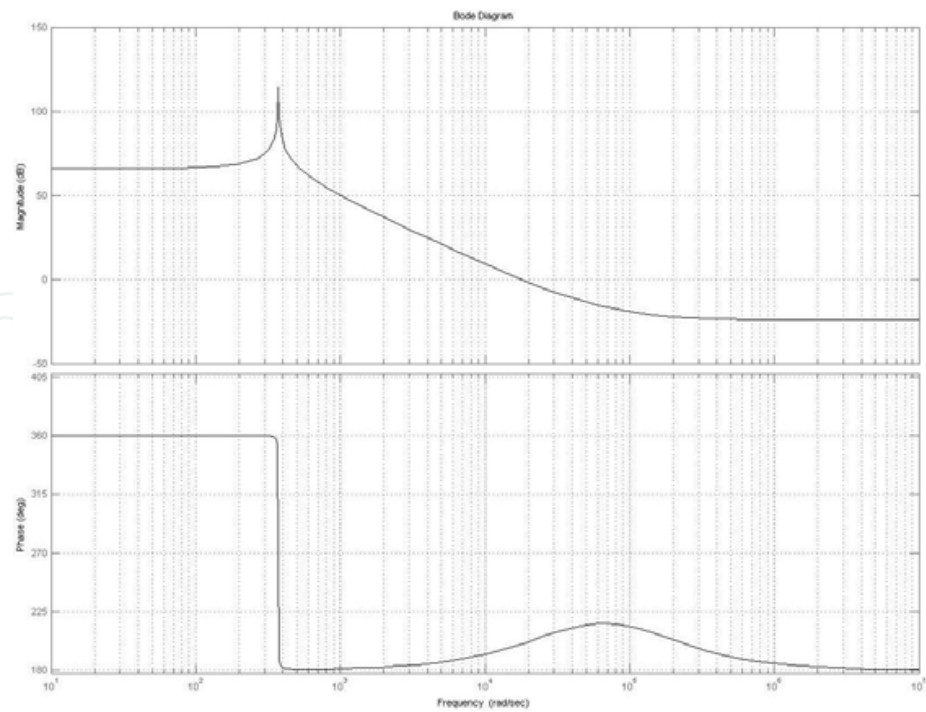
Fig. 9. Bode plot of Power Stage

Reducing the primary inductance increase the RHP zero location, therefore it may be possible to increase the close loop cross over frequency.

The Bode plot (Fig. 9) shows the frequency response of the power stage from the error amplifier output through to power stage output voltage. These approximated plots can be used to understand how to design the control/compensation circuitry.
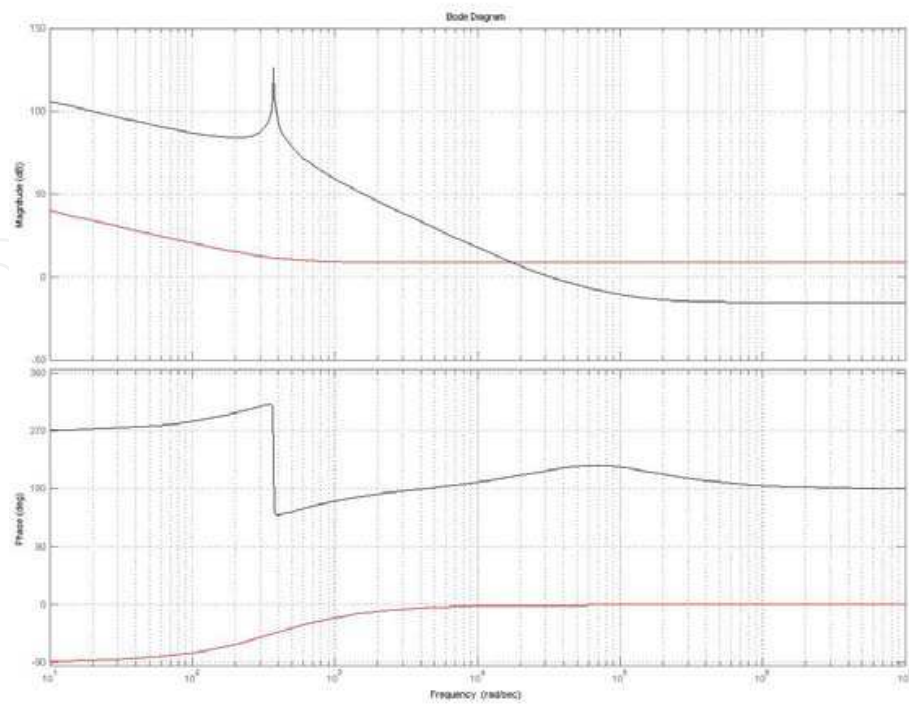

Fig. 10. Bode plot of Type I compensation network and the open loop TF

Type I compensation network is added to the control output TF in order to meet the static and dynamic performance requirements while maintaining stability.

This control gives one pole in the origin and one zero. The pole in the origin increase the DC gain to reduce the DC error in steady state. The zero is added at low frequency to obtain a at gain at mid frequency. Bode plot shows the effect of type I compensation. Fig. 10 shows the gain and phase of the overall system (power stage plus compensation). A cross-over frequency of 5kHz is achieved with a theoretical phase margin of 30°.

7. Experimental results

A 100W, 12V-to-350V step-up converter was completely designed and tested and the resulting power circuit components used are:

- Inductor: Coilcraft Flyback Transformer GA3459-BL with 5uH as primary inductance and 1:10 turns ratio
- Input capacitors: two 4.7uF ceramic and one 100uF electrolytic for high RMS current ripple
- Output capacitors: two 1uF plastic film and 150uF electrolytic
- MOSFETs: IRF1018 with 60V VDSS and 7.1mΩ of R_{DSON}
- Switching frequency: 200KHz

Operating duty cycle of the interleaved converter is 0.72. Figure 11 shows the prototype of the converter with the FPGA programmable device mounted on the above control board (a FPGA based ECU system developed at CSPP-LIM for fast prototyping applications).
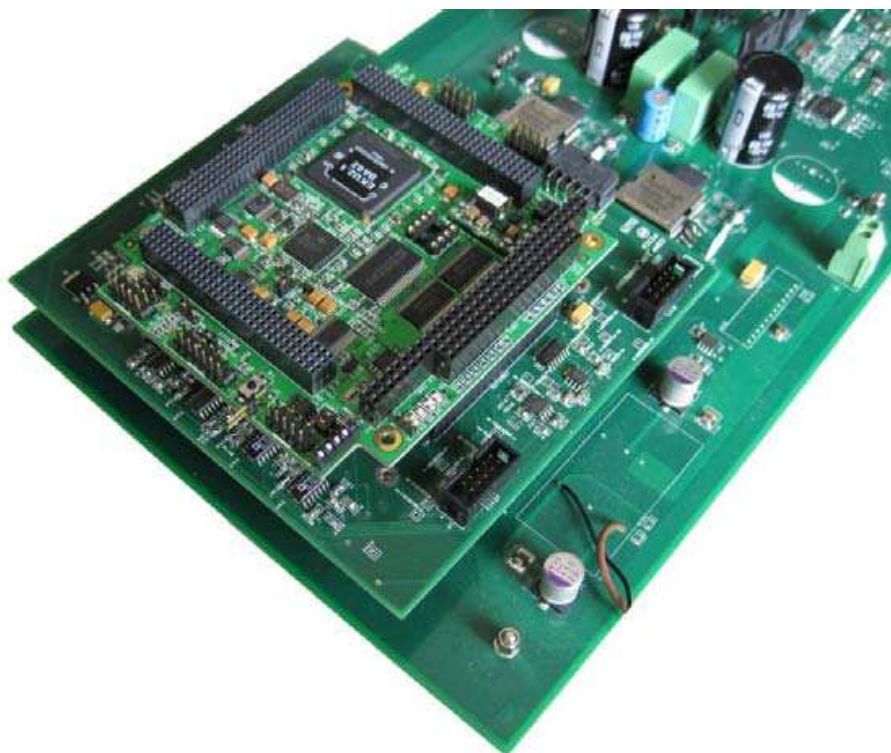

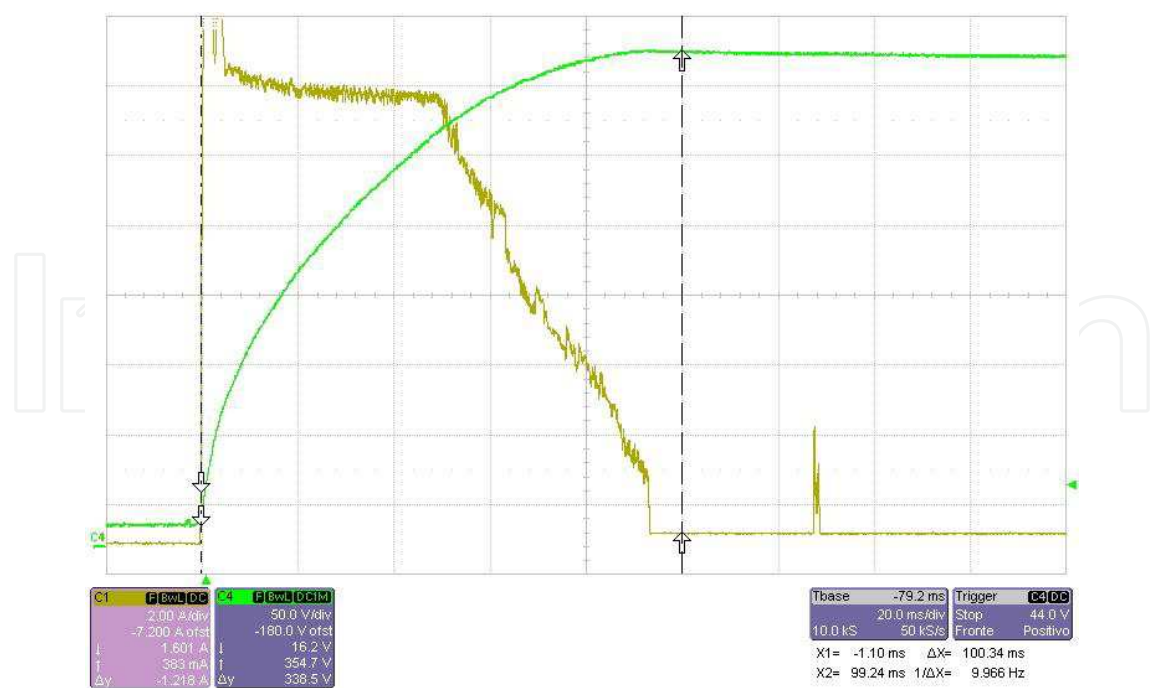Fig. 11. The experimental set-up of the proposed FPGA controlled DC/DC step-up converter

Fig. 12. DC/DC converter behavior during start-up sequence

Fig. 12 shows the output voltage (green) and output current (yellow) of the converter during start up sequence. During this time high primary inductor current in each phase is present as can be seen from the oscilloscope picture. The system goes in stable conditions in less than 100ms.
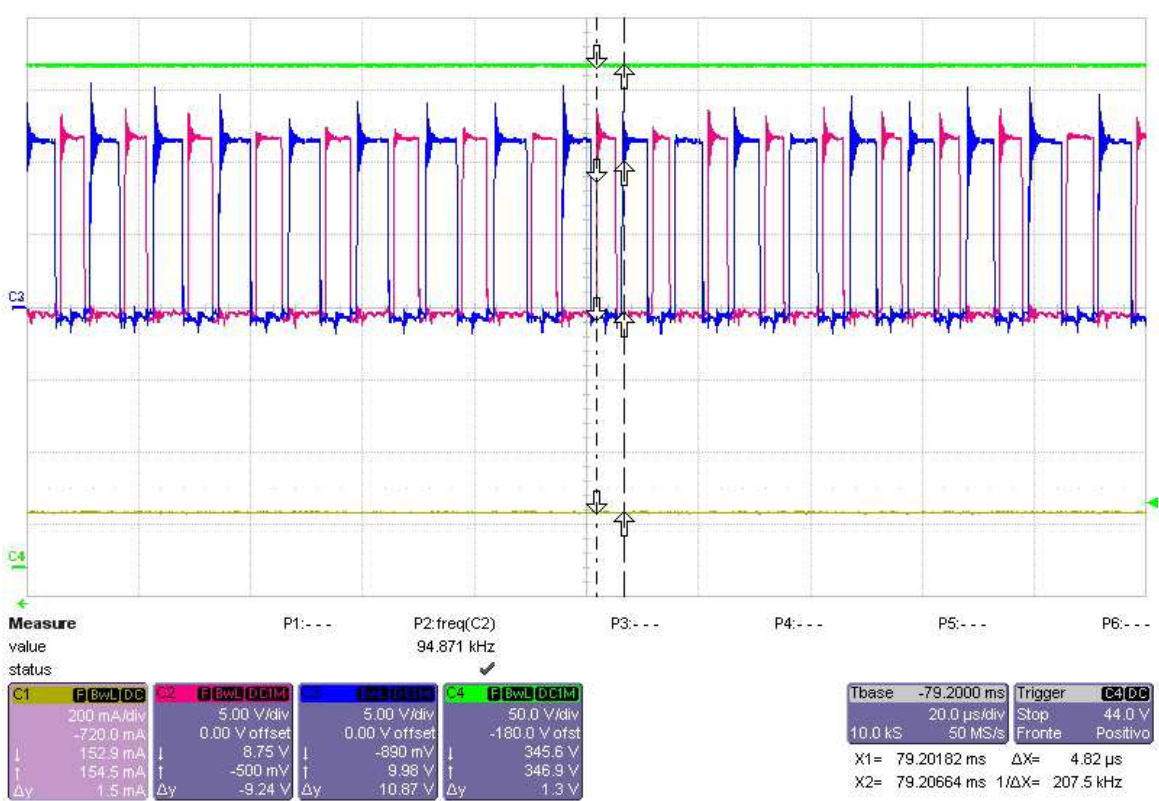

Fig. 13. Converter steady-state conditions

Fig. 13 shows the converter output voltage (green), output current (yellow) and *Cm1/Cm2* signals (blue/red) in steady-state conditions. It can be seen that the switching frequency is stabilized around 200kHz that represent the reference current period of frequency loop.
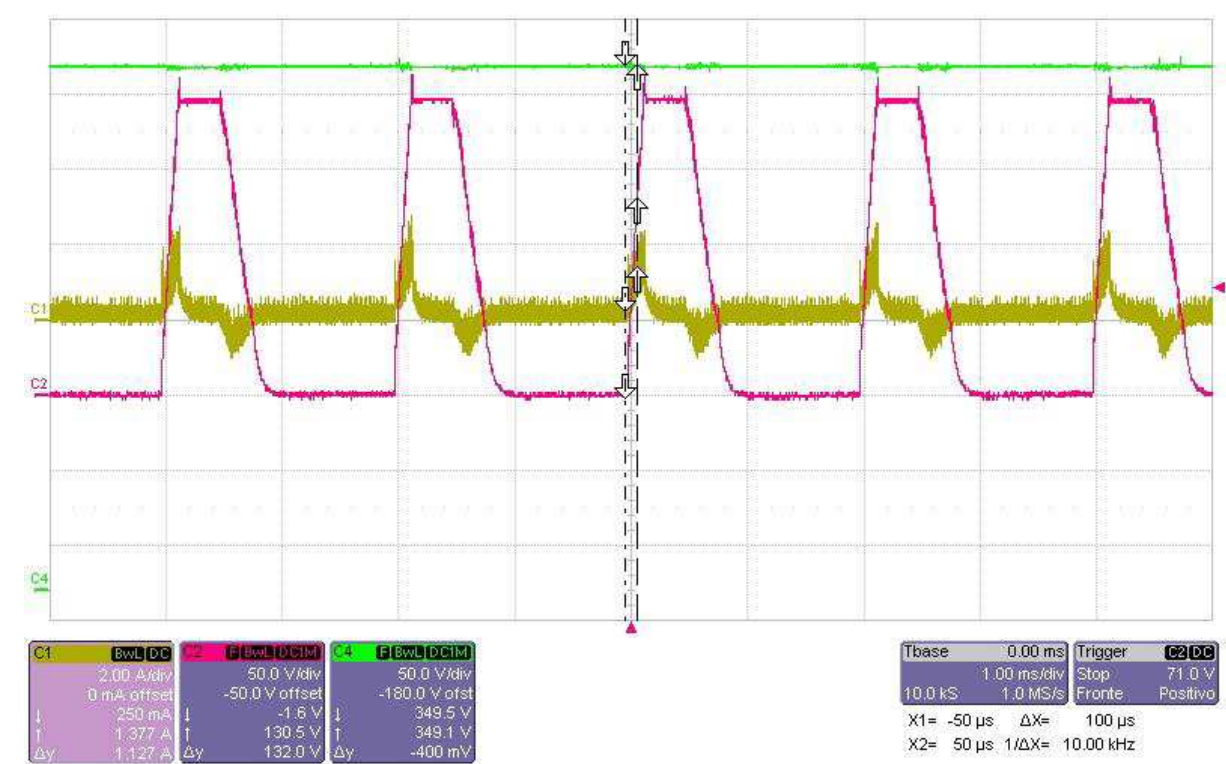
Fig. 14. Converter response under impulsive load test (10uF / 1.8Ω series RC load)

Fig. 14 shows converter output voltage (green), converter output current (yellow) and load voltage (red) during a impulsive load test (500Hz charge/discharge of a series 10uF / 1.8Ω RC load). It can be seen that the converter output voltage is very stable with a ripple less than 5V during 2A load driving transients.

7. Conclusion

In this chapter a new concept of FPGA controlled coupled inductor boost converter is presented as a good option to solve high boosting requirements in automotive applications. High power efficient converters with reduced size output filter can be obtained by interleaving and control these type of converters.

Using a quasi-constant frequency hysteretic current control it is possible to join the advantages of fixed and variable frequency control introducing a frequency feedback loop in a classic hysteretic CM control. Moreover, the FPGA implementation ensures good dynamic performances, reliability and high computational performances resulting in high efficiency overall characteristics.

The switching frequency is stabilized around 10% of nominal reference frequency: this allows the designer to easily estimate the switching losses and efficiently design the output EMI filter.

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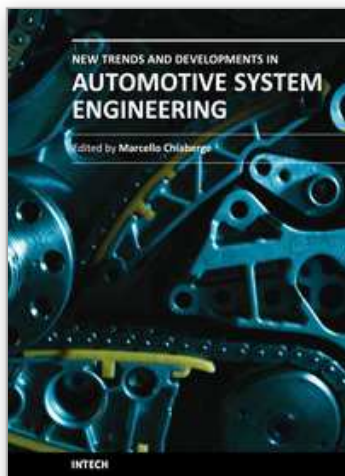
New Trends and Developments in Automotive System Engineering

Edited by Prof. Marcello Chiaberge

In the last few years the automobile design process is required to become more responsible and responsibly related to environmental needs. Basing the automotive design not only on the appearance, the visual appearance of the vehicle needs to be thought together and deeply integrated with the â€œpowerâ€ developed by the engine. The purpose of this book is to try to present the new technologies development scenario, and not to give any indication about the direction that should be given to the research in this complex and multi-disciplinary challenging field.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

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