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Readout System for Medium-Sized Experiments

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1. Introduction

In a vast area of fundamental nuclear/particle physics investigations are performed with relatively simple setups, encompassing up to few thousands of analog data sources. Multiplicity for events in such experiments is usually of the order of few tens. On the other hand, high precision studies require accumulating of large data samples and therefore the readout system must work reliably at trigger rates between one and a few tens of thousands per second, *without* any significant dead-time. To meet these requirements it is necessary to utilize a fast bus and/or protocol for the data transmission. In contrast to the present generation of high energy physics experiments, here the usage of complicated multiplexing schemes with specially developed chips and boards as well as many-level triggering and event-building techniques is rather disadvantageous.

This Chapter describes a readout system which fulfills all the needs of moderate-size experiments and possesses a number of attractive features which allow its easy modification for specific demands. Rather than utilizing possibilities of creating electronic boards tailored strictly to the needs of a particular application, the discussed implementation is based on modular electronics, which parts are still in possession of many laboratories all over the world. In (frequent) cases, when budget limitations do not allow to follow the path of a completely new design of dedicated custom-made boards, application of older electronic modules might be the only way to successfully perform the planned measurements. In the described system use is made of CAMAC based electronics, which turns out to provide data throughput sufficient for most demanding applications. In fact, when the readout is coupled to the front-end processor via VME-bus buffers, it does not feel any speed limits present in the traditional CAMAC-based systems.

The described modular electronic system is based on the standard FERA¹ configuration, which applications in physics experiments are numerous, see e.g. (Vander Molen et al. 1991; Gazes et al. 1993; Elfman et al. 1997; Hagemann et al. 1999; Okamura 2000; Davin et al. 2001; Karpukhin et al. 2003; Loudos et al. 2004). The full power of the FERA readout system is gained by introducing an additional custom CAMAC module. In spite of its relative simplicity, the module allows to avoid the bounds imposed by the FERA standard. This includes a possibility to prolong the FERA data-bus over many crates for large setups. Configurations of the experimental apparatus require a logical grouping of the signal sources into subsystems corresponding to particular sets of detectors (wire chambers,

¹ FERA (in full: Fast Encoding and Readout ADC) is a trademark of the LeCroy Corporation.

trigger hodoscopes, calorimeters etc.). Use of the custom FERA Extender/Tagger module allows to divide the readout system into sections matching the detector configuration and to drive each section by a separate (differing in width or shifted in time) gate signal. In each sub-system the data are sent over a dedicated bus (at the speed of 100 ns per data word) to a pair of alternatively active buffering memories. The coordination of the full system (controlling the event cycle, switching the memories, issuing DAQ requests) is performed by a single FERA Manager, which is equipped with a logic system for distributing and multiplexing of the synchronization signals. Improvements in the FERA sector have been proposed before – see e.g. (Ordine et al. 1997; Beausang et al. 2000) for descriptions of other custom-made control modules, with functionality similar to the FERA Manager or (Sugaya & Nomachi 1999) for an auxiliary VME sequencer module. It has also to be acknowledged that at present several additional FERA-line modules are commercially available, which would allow to achieve similar functionality as the Extender/Tagger. However, the discussed *Integrated Multi-Crate FERA* readout system was the first complete solution in which possibilities of application of various gates as well as tagging of events in several sub-systems were provided in a clean way.

In the following Sections, first a short description of the standard FERA system configuration and its limitations is presented. The FERA Extender/Tagger module is then introduced and its applications in constructing more elaborate FERA systems are described. Finally, the estimations of the full system performance for a typical configuration of a moderate-size experiment are given, followed by concluding remarks.

2. Standard FERA configuration

Fast increase of the experimental readout electronics complexity and size, confronted with the limited speed of the data transmission over the CAMAC DATAWAY, precipitated the introduction of faster busses. One of the solutions was the FERA system, in which data from the digitizing modules are passed over a dedicated ECL data bus with the handshake taking place on another special ECL control bus. The system initially consisted of the 4300B ADC's and the 4301 FERA Driver, which mediated the data transfer to the 4302 FERA Memories (LeCroy 1983). The system was later supplemented with a number of modules (3377 TDC, 4303 TFC, 3309 PFC, various logic modules: 34xx discriminators, 45xx ECLine Logic) and in particular with the global readout controller, the FERA Manager (Watzlawik et al. 1994). FERA compatible digitizing units were produced by several manufacturers (Silena 4418/x modules, Gan'elec 812F series; recently the FERA line of modules is followed by Cheesecote Mountain CAMAC (Sumner)).

This constant growth of the FERA family indicates clearly that the system possesses a number of attractive features. In addition to the wide variety of digitizing modules and the readout speed at 100 ns per a 16-bit word, the ability to buffer the fast-readout events in the memories enables derandomization of the event rate and reduction of the dead-time by multiplexing the buffers (one is being filled over the ECL data bus while the other is readout via CAMAC). The system control is done entirely by hardware, i.e. after initialization, the synchronization of the data transmission is performed by the Manager/Driver modules and external access to the accumulated data is limited to the Memory modules at the moment of the Manager's LAM (see below). In this way hardware changes within the system are virtually decoupled from the DAQ software, requiring only small changes in the initialization routines. One should note that the total readout speed of the system is limited

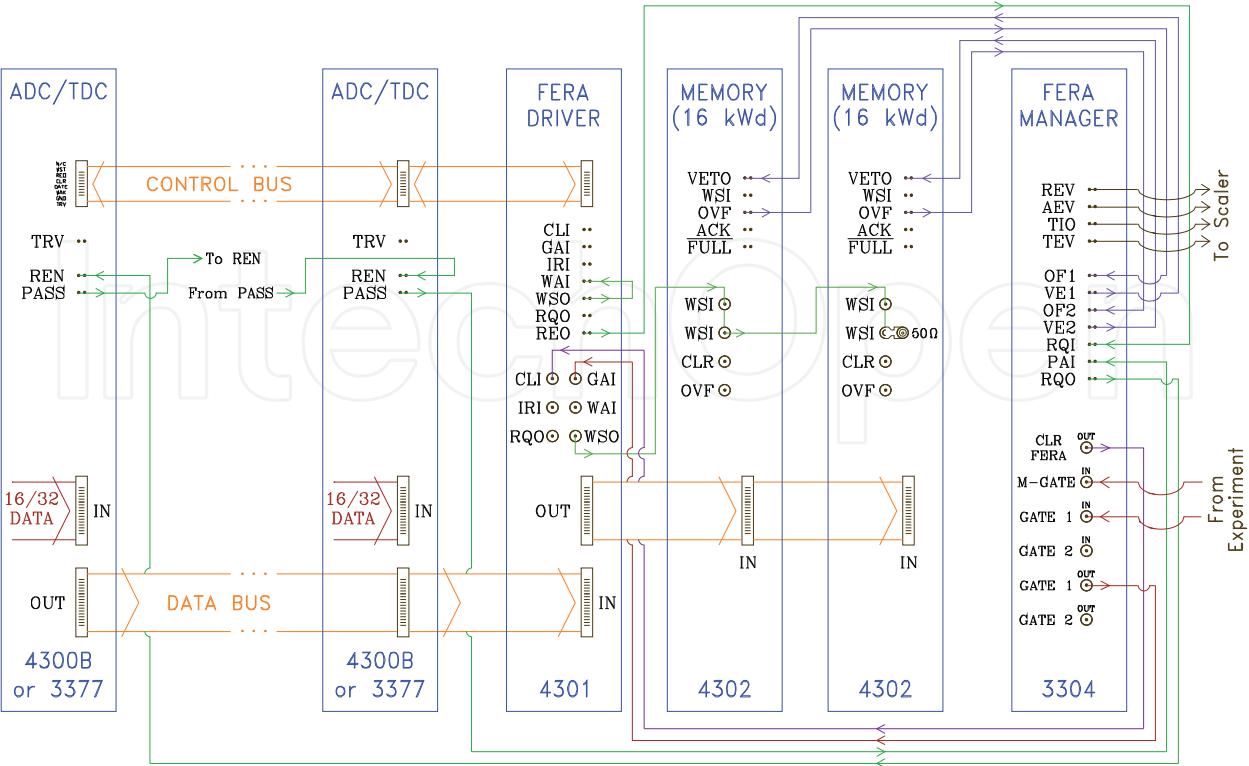


Fig. 1. Diagram of the standard FERA System interconnections.

by the CAMAC readout speed of the Memories. Therefore the overall rate capability can be further improved by replacing these by VME FERA Memories (LeCroy 1190 or CES 8170 modules).

In Fig. 1 the interconnections within the standard FERA system are presented. Several digitizing modules are chained in a readout series via the REN/PASS line and put on common control and data busses with the Driver, which converts the bussed single-ended ECL signals to true differential ones and mediates the data transfer into the Memories. Control over the memory switching and the event cycle as a whole is performed by the Manager.

2.1 FERA event cycle and handshake

A trigger signal from the experiment’s logic system is sent to the Manager as M-GATE and starts the event cycle. The GATE signal is then sent to the Driver and distributed to all digitizing modules (ADC’s and/or TDC’s) in the system. If the conversion in a given module results in a valid data, that module asserts the REQ line, signaling its request for readout. Logic OR of all these signals is transmitted via Driver to the Manager. The programmed delay in the 3304 module allows all digitizing units to get ready with all their conversion before the REN signal for the first ADC/TDC is issued. Obtaining REN, the module takes control over the busses and sends the data words, strobing the active Memory with the WST line. To obtain the highest possible data throughput the Driver generates the acknowledge signal directly, without waiting for the Memory ACK (what would result in a speed reduction by a factor of 2). After the first module has sent all its data it copies REN to PASS, which sets REN of the next manager. When the PASS signal of the last module in the chain is obtained by the Manager, the latter then generates a reset signal (CLR), distributed by the Driver to all modules. After approximately 2 μ s the Manager is ready to accept the next event.

One more important task of the Manager is the memory switching. At the beginning of the acquisition the first Memory is enabled while the second is VETO'ed by the Manager. When the overflow mark of the Memory (e.g. 14 kWords, set by side switch) is reached, the Manager receives the corresponding OVF signal, it allows the data transfer for the current event to finish and after obtaining PASS it swaps the VETO's, thus redirecting the flow of data to the second Memory. A LAM issued at that moment by the Manager interrupts the DAQ processor and causes the data from the filled Memory to be readout via CAMAC. After emptying of the 4302 module, the processor resets the corresponding flag in the Manager's register.

2.2 Standard FERA limitations

With all these favorable features the FERA system nonetheless contains in its original concept two inherent limitations which pose problems when trying to use it in more complex setups.

From the discussion of the circuitry shown in Fig. 1 those two restraints became obvious:

1. The system is designed to occupy a *single CAMAC crate* (LeCroy 1983), therefore severely limiting the maximum number of readout channels.
2. A *single GATE* signal is distributed to the whole system. This restriction could lead to two kinds of problems. The measuring system might contain various kinds of detectors, like e.g. plastic and crystal scintillators, which require the integration times (gate widths) to differ by at least an order of magnitude (in the chosen example ~ 50 ns and ≥ 500 ns, respectively). On the other hand, when the readout system contains both ADC and TDC modules, timing problems can arise when the same signal has to be used as the integration gate and common start or stop signal.

Easy solutions to the above problems are biased with serious shortcomings. Simple prolongation of the ECL busses over many crates could be accepted to solve the first problem if it concerns just a few more modules. If a significant enlargement of the system is needed the long busses will lead to signal distortion and eventually to failures in the data transmission. Of course this method does not address the single-gate problem.

Apparently employing *several* systems like the one depicted in Fig. 1 would solve both problems, however a serious deficiency of such application lies in a loss of event coherency. While different parts of the experimental apparatus send their digitized data in parallel to several Memories, one is not able subsequently to reconstruct the full events, i.e. to find out the correlation between information in the sub-systems.

3. FERA Extender/Tagger module

The above considerations specify firm guidelines for the desired solution, which should provide means for:

- Proper *prolongation* of the ECL data bus, possibly without limits.
- Easy *division* of the whole system into sub-systems, equipped with their own Memory pairs.
- Possibility to apply *common or separate gates* within each sub-system.
- Organizing the *data transfer* to the back-end computer in a convenient structure.

These demands are fulfilled by using a custom CAMAC module installed in an extended configuration of the FERA system, which shall be called "Full FERA System". Let us first concentrate on the characteristics of the module.

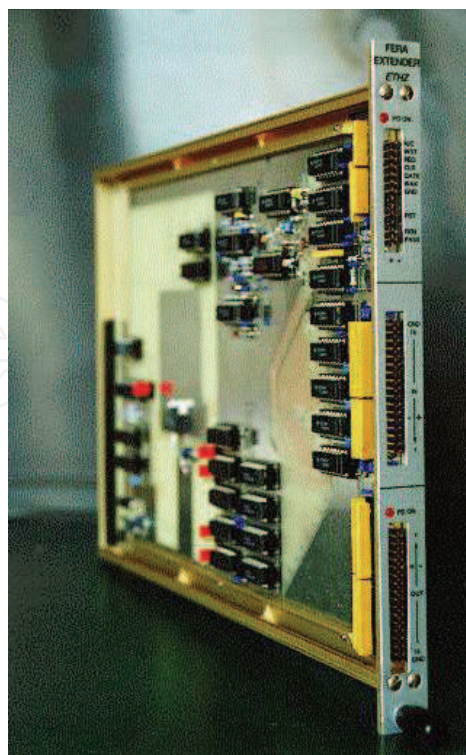


Fig. 2. FERA Extender/Tagger module.

The FERA Extender/Tagger module (see Fig. 2) was designed originally at the University of Bern². Additional modifications of the board to achieve the required functionality within the designed system configuration were introduced at ETH Zürich³. The description here is concentrated on the functions of the Extender within the FERA system, without going into a detailed discussion of its internal circuitry.

3.1 FERA Extender - “Separate Gates” system

When the module is used only as a data bus extender it remains a quasi-passive part of the system and does not participate in the FERA handshake. Its control bus and the REN/PASS connectors remain open. The module acts as a kind of data transmitter.

Such application of the module enables to split the ECL data bus into several independent, sequentially placed sections and allows therefore the distribution of the system over several CAMAC crates and to apply to each section an individual gate. It should be kept in mind that the gates are different in the sense of their widths and relative time shifts, they *must*, however, all be created out of the same original trigger (M-GATE) signal.

A schematic diagram of the Separate Gate system is shown in Fig. 3. Only the most relevant interconnections are shown, the other are analogous as in the standard configuration. No gate signals are indicated in the diagram - it is, however, obvious that each Driver can obtain (and in turn distribute) a GATE signal which can be unique for the given section. Some features of this configuration should be noted:

² Schemes and original design of the printed board were worked out by M. Hess, Laboratory of High Energy Physics, University of Bern, Switzerland.

³ The author holds the permission of unlimited duplication of the board, as well as can provide details on the original Extender modifications. Their electronic realization is designed by P. Eberhardt.

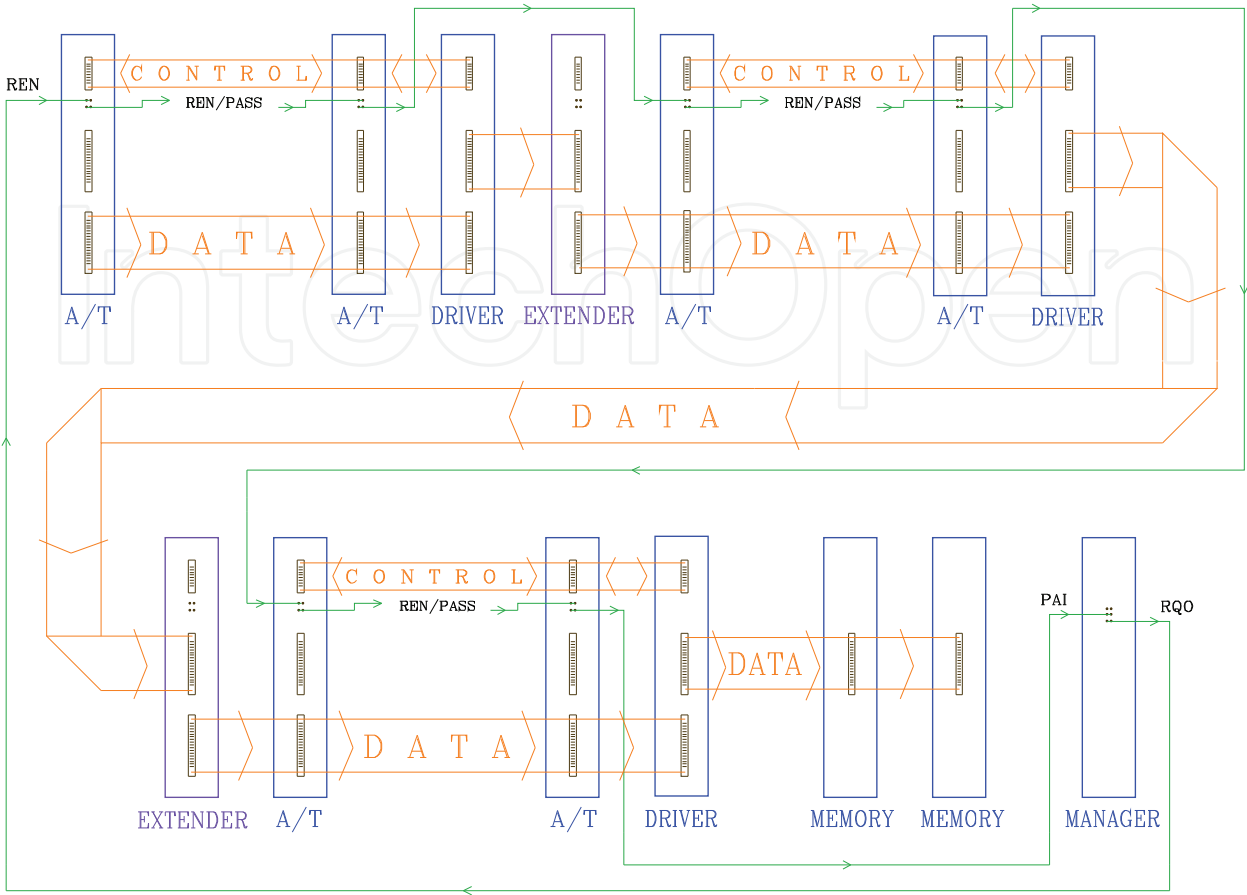


Fig. 3. Schematic diagram of an example of the Separate Gate system, employing the FERA Extender/Tagger as just the data bus extender. Only the REN/PASS chain and the ECL busses are shown.

- The Extender is always the *first module* in the FERA section. Each such section is associated with a Driver - the last module within it, which mediates the handshake, receives all the data and forwards them further to the Memories.
- The Extender *receives data* directly from the Driver of the preceding section.
- Each *Driver - Extender pair* acts effectively as a *repeater*, refreshing the data word as it passes along the bus from one section to another.
- Each digitizing module in every section in turn takes control over the whole bus and must be able to strobe the Memories to accept its data. Therefore the Memories must be *strobed* by the logic OR of all Drivers WSO signals.

The Separate Gates system allows the division of the whole readout front-end electronics into sections, corresponding logically to the configuration of the experimental detection elements. There remain, however, two shortcomings which require the ability to tag events:

1. All the data flow into a single pair of Memories. For experiments containing a really large number of channels that could lead to long event cycles. It might be desirable to split the data buffering into separate parallel sections.
2. While not all detection sub-systems always deliver valid conversions the data stored in the Memories could be biased with a certain ambiguity. Consider for simplicity only

two sections: finding in the data stream (from the Memory) a sequence of data from section 1 followed by data from section 2 will always result a priori in an uncertainty as to whether these data belong to one complete event or to a series of two not-complete ones, in which the section 2 and section 1 data were respectively missing. Use of an unique event marker is therefore necessary to resolve such problems.

3.2 FERA Tagger

The FERA Extender/Tagger module can act as an active unit, participating in the event cycle and the FERA handshake. In this mode it inserts an *event identification* word into the data stream, acting like any other FERA-compatible unit. To work as the event tagger the Extender/Tagger module must be connected to the control bus and into the readout (REN/PASS) chain.

The event mark supplied by the Tagger is simply the event number. The module contains a 16-bit counter, which can be reset at any suitable moment (via CAMAC command or – as it is in our Full FERA system– via the front panel input) to the initial value (0 or 1, selectable by an internal jumper). During each event cycle (see below) the counter content is transferred to the Memory (with its most-significant bit being 1 or 0, again selectable by an internal jumper) and incremented. It is probably most logical to place the Tagger as the first module in the sub-system and to treat the event tag word as a “super-header”, preceding the words (headers and conversions) of the digitizing modules.

The Tagger operates during the event cycle in a similar manner as the FERA ADC:

- It receives the GATE on the control bus . . .
- . . . *waits* a few μs - it emulates the conversion time in order to set the readout request signal not much earlier than the digitizing units. The delay can be adjusted by exchanging a socketed capacitor. In our application it is set to about 4 μs .
- Asserts REQ.
- After obtaining REN it *puts the counter* word on the data bus.
- At obtaining WAK it *increments* the counter and sets the PASS, transferring the bus control to the next module.

By equipping each parallel sub-system with a Tagger it becomes possible to recover the correlations between the information stored in them. Since the gate signal reaches all sub-systems (differing only in width and/or delay with respect to the Master-Gate), for a given event the Taggers will produce equal counter values in all of them, thus enabling an easy recombination of the event fragments into one full event.

4. Full FERA system

The last remark of the previous Section suggests an easy migration from the standard to the multi-system FERA configuration. The naive solution would consist of several copies of the standard configuration, each equipped with its own Tagger as the first module. Indeed, such a system would meet almost all requirements, in so far as its size, ability to apply separate gates and consistency in event tagging is concerned. However, this solution has one inherent *inconvenience*, connected with the fact that the event building is effectively performed in the back-end computer, after it receives all data from the FERA Memories.

A minor discomfort is posed by the fact of having many Managers in the system. The DAQ processor will have to react to several LAM's and, what is more important, perform slightly different actions at each of them.

To understand the other, really significant difficulty, consider an experiment in which in response to the trigger one sub-system receives some few tens of analog signals (e.g. calorimeter, energies and times in several elements) while in the other only very few parameters are digitized (e.g. single scintillator energy). The lengths (number of the header/data words) of the corresponding event fragments can easily differ by a factor of ten. Thus in the first system the data transfer will take place ten times more often. It is not difficult to handle these very asymmetric buffers in an off-line analysis, however in the on-line monitoring it will be necessary to temporarily store all these buffers until the one from the second sub-system is transmitted, as only then the full events can be reconstructed and sorted. Whereas it is not impossible to adopt such a scheme it would be certainly much easier to process the data coming to the back-end in a more symmetric structure.

4.1 Single manager control

The above considerations lead to the idea of applying a *general coordination* over all subsystems by a single Manager. The tasks it accomplishes can be summarized in the form of the basic features of the Full FERA system:

- Parallel FERA readout in sub-systems into the dedicated Memory pairs, encompassing in particular a proper coordination of the start and closing of the event cycle.
- Memory overflow in *any* sub-system is recognized by the Manager, which then redirects the data transfer in *all* of them into the complementary memory units and issues a single LAM. All the previously active Memories are readout by the DAQ processor via CAMAC while the complementary modules continue to accept data over the ECL bus.
- At any LAM the Taggers of all subsystems are reset. The event counting starts always from 1 in each block, enabling an easy correlation of event fragments.

It is obvious that in order to let the single Manager exert control over several sub-systems it is necessary to equip it with additional logic. Fig. 4 shows an example of the Full FERA system configuration (consisting of three sub-systems), with all the necessary interconnections. The FERA-compatible modules are shown as bigger rectangles while the small ones represent auxiliary logic units. The actions of the Manager can be divided into three groups:

1. Synchronization of Memory switching.

In order to perform this task the Manager must coordinate the VETO and OVF signals of all sub-systems; also the RESET signal for the Taggers is created as the logic OR of the VETO's. The functions of the corresponding part of the logic system are:

- Splitting the VE1 and VE2 output signals and distributing them to the appropriate VETO inputs of the Memories.
- OR'ing the parallel Memories' OFV outputs for the OF1 and OF2 inputs of the Manager.
- OR'ing the shaped (short) signals generated by the original veto levels of the Manager and splitting the OR for distribution to the RESET inputs of all Taggers.

2. Initiating parallel data readout.

The Manager should take care that the request coming from any sub-system does not result in enabling the readout before all the digitizing modules are ready with their conversions. The actions performed at this stage are:

- OR'ing all the Driver RQO signals for the Manager RQI input.

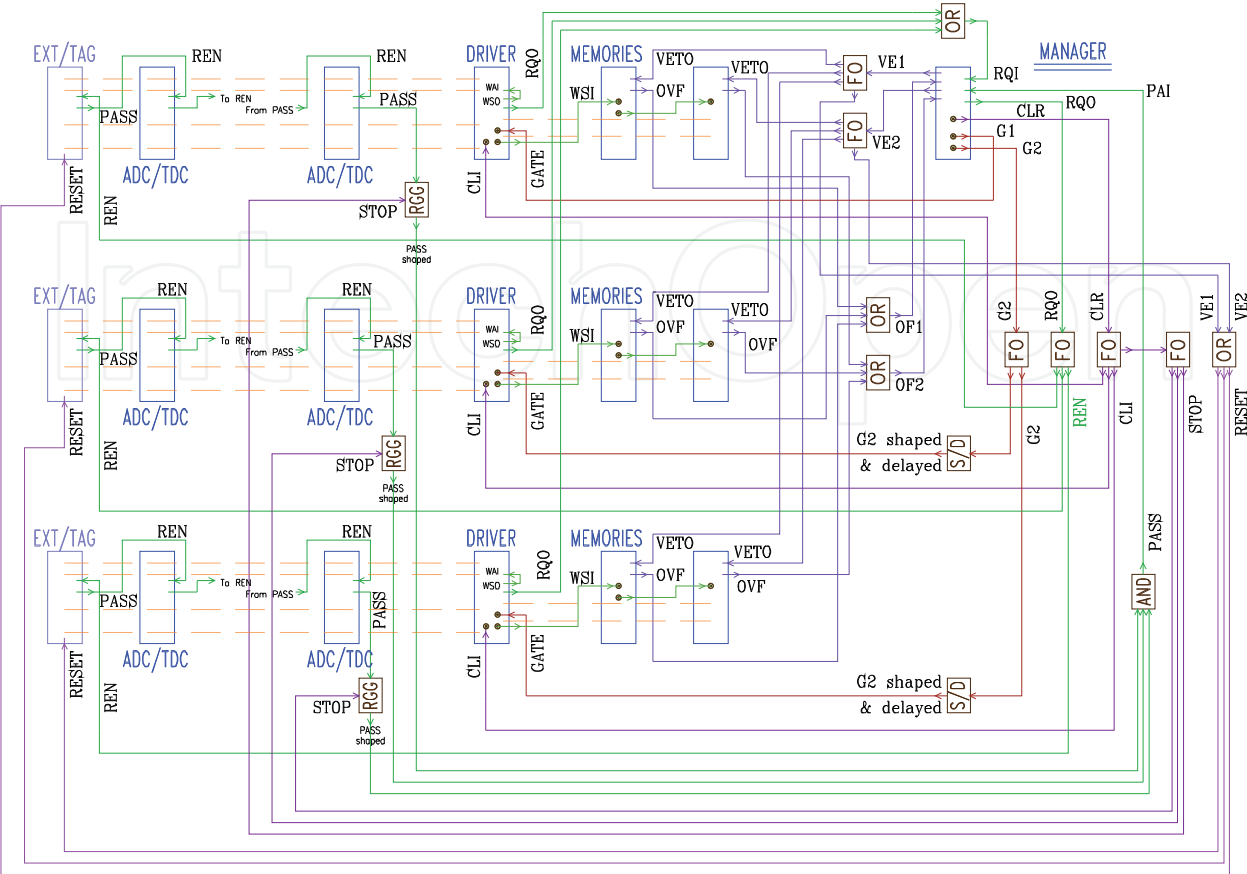


Fig. 4. Interconnections within the Full FERA system, consisting of three sub-systems. For a functional description see text. The sequence of signals relevant for the data transmission is shown in Fig. 5.

- Generating an internal delay in the Manager between obtaining the RQI pulse and setting the RQO output.
 - Splitting the RQO signal and distributing it as REN to all the first modules (Taggers) in each sub-system.
3. Correlating the readout termination.
- This task of the Manager is very critical for the data integrity. It must react to the PASS signals from all sub-systems in such a way that allows all the data to come to the appropriate Memories before the global clear is generated and before, at the proper moments, the Memories are swapped. The logic system must therefore:
- Stretch the last PASS signals to cover the possible readout time span for *all* subsystems.
 - Create the logic AND of all shaped PASS signals for the Manager PAI input.
 - Split CLR output of the Manager and distribute it to all Drivers (and in consequence to all the digitizing modules).
 - Use again the CLR to re-arm the stretchers in the PASS line – since the readout time span might be quite large (even a few tens of μs), in order to avoid some overlaps between events the generated readout gates must be terminated simultaneously with the whole system resetting.

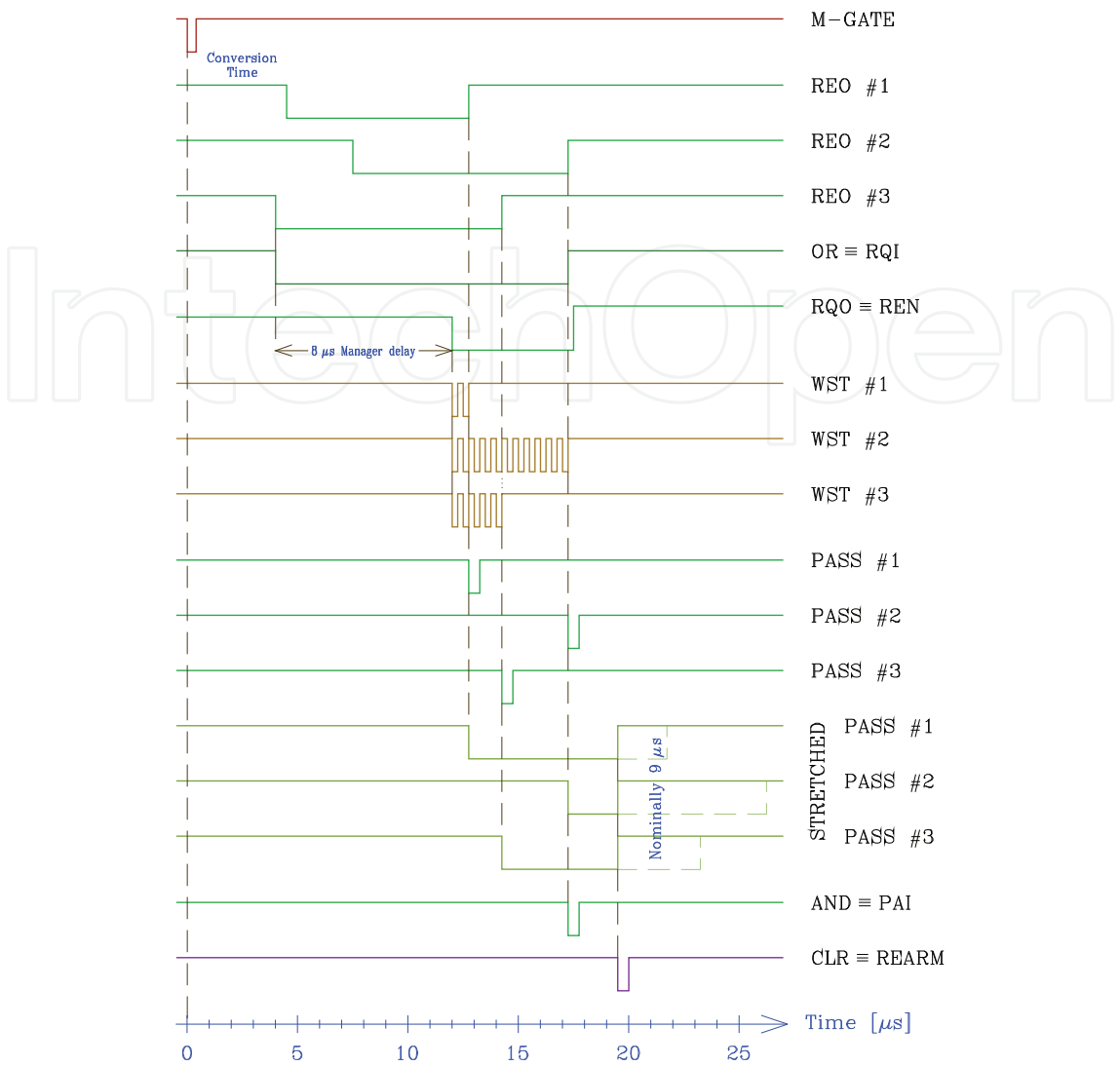


Fig. 5. FERA Readout timing – the most relevant signals for the Full FERA system shown in Fig. 4. To make the short pulses visible they are shown not to scale – the width of the M-GATE is about 50-100 ns, the write strobes (WST) are 50 ns wide with a 100 ns spacing, the PASS and CLR pulses are about 60-80 ns wide.

In addition the GATE signals passing through the Manager have to be adjusted (width and/or delay) before entering the Drivers of the individual sections. This action is again performed by the auxiliary logic. The above list of the Manager tasks contains implicitly the types of the logic system components. The required modules include Fan-Out units, logic OR and AND modules with both, overlap and shaped outputs, shaper-and-delay units and retriggeable gate generators. Although it is possible to assemble the auxiliary logic system from commercially available modules, such a solution would necessitate the use of ECL-NIM-ECL level converters at several stages. While designing the implementation of the Full FERA system it has been decided to construct a series of CAMAC-based logic modules⁴, with the

⁴ Electrical design and mechanical construction of the logic modules used in the Full FERA system is by P. Eberhardt.

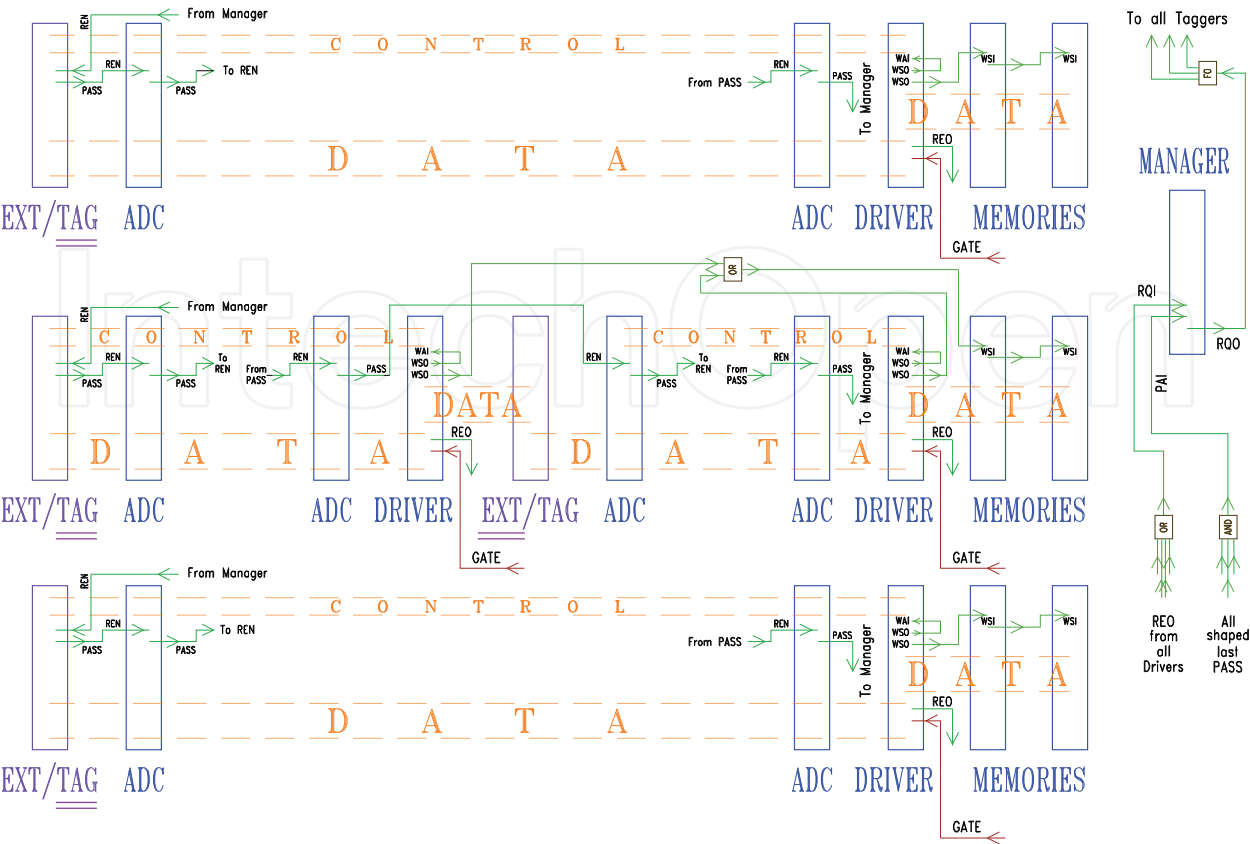


Fig. 6. Full FERA system with separate gate sections in one sub-system. Only the ECL busses and the REN/PASS chains are shown to point out the differences with respect to the configuration presented in Fig. 4.

input/output logic levels tailored to the specific demands of the FERA configuration. Using these special logic units allows to minimize the length of the cabling and make it more transparent for non-specialized users. The sequence of the most relevant FERA event cycle signals is presented schematically in Fig. 5. Again an example with three sub-systems is considered. The delay readout-request – readout-enable (RQO–REN) and the readout time span are assumed to be few μ s each (cf. next Section). Please note, that the readout request signals (REO's) of each sub-system can be set at slightly different times. When using the correctly set Taggers, this spread should be largely eliminated. One can observe the action of re-arming the PASS stretchers by the global clear signal.

Of course, within the Full FERA system it is possible to apply separate gates within each subsystem - see Fig. 6. One can break the data bus in two (or more) sections, applying the Driver/Extender pairs in an analogous way as described above. It should be noted that in such a configuration the readout request signal must contain also the “middle” Driver REO output in the OR of all requests and that in the separate-gate sub-system the Memories must be strobed by an OR of all sections WSO's. The Extender/Tagger module which acts as an Extender is connected to neither the control bus nor the readout chain.

5. Full FERA system performance

To investigate the rate capability of the Full FERA system let us assume that the experiment contains some 1000 channels, of which about 5-10% have valid conversions for a good

(triggered) event. Assume that about 60 parameters ('hits') are digitized in 20 modules for each event. Therefore at every trigger some 20 modules will prepare 4 data words to be transferred, i.e. the readout will consist of transmitting 80 Words (of 16 bit) to the buffering Memory.

The M-GATE signal defines time zero. Conversion times for various modules in the system are:

- Tagger – emulates $4\ \mu\text{s}$ conversion time.
- ADC – $4 \div 9\ \mu\text{s}$. Assume 10 bit resolution, thus conversion time of about $4.5\ \mu\text{s}$.
- TDC – $4 \div (10-12)\ \mu\text{s}$, depending on the number of hits.

Therefore the REQ signal will appear about $4\ \mu\text{s}$ after M-GATE and one has to program $\sim 8\ \mu\text{s}$ RQI-RQO delay in the Manager. Hence, the readout starts at about $12\ \mu\text{s}$ after the beginning of the event cycle.

The readout duration can be as short as few hundreds ns (with no hits and only the Tagger word present) or - for all 80 words - as long as $\geq 8\ \mu\text{s}$. Therefore the stretchers have to be set to $\sim 9\ \mu\text{s}$ and the transition time from REN to the PAI signal is about $9\ \mu\text{s}$.

After receiving PAI the Manager will generate CLR and after $\sim 3\ \mu\text{s}$ it will be ready for the next event cycle.

A conservative estimation for the event cycle duration is thus around $25\ \mu\text{s}$. It follows that an event rate of the order of 10^4 per second can be processed by the system with dead-time losses of about 2%. On the scale of the experiment sizes under discussion here such performance is very attractive.

Further limitation on the rate capability comes from the Memory emptying time, a slow procedure on the CAMAC DATAWAY. It should be noted, that this could be easily improved by replacing the CAMAC Memories by their VME version, allowing for much faster data transmission - see Fig. 7 for an example of connections within such implementation.

Let us consider the restraint caused by the CAMAC readout, assuming again three FERA subsystems with the Memories set to the 14 kWords capacity. At an overflow (Manager's LAM) there is thus approximately 40 kWords to be sent over the DATAWAY. The available time for that action is determined by the speed of the Memory filling.

Assume that the DAQ processor needs as much as about $2\ \mu\text{s}$ to extract one Word from the Memory and put it into the outgoing event stream. In such conditions the emptying of the whole set of 3 Memories (40 kWords) will take 80 ms, thus the maximum interrupt rate will be $12\ \text{s}^{-1}$.

Another cautious assumption concerns the memory filling - let us say that in the fastest-overflowing sub-system there are 30 Words at each event. Thus the Memory capacity corresponds to about 500 events.

By comparing the two numbers we obtain the *realistic event rate* for the Full FERA system operated in the pure CAMAC mode of about $6 \cdot 10^3\ \text{s}^{-1}$. One should keep in mind that since the CAMAC transfer takes place every 500 events, the interrupts (LAM's) are rather derandomized and therefore this rate is processed virtually *without* any dead-time losses.

An analogous estimation for the case when the Full FERA system is equipped with VME buffer Memories of 32 kWords capacity leads, with the assumptions of 80 kWords per event and as much as $0.25\ \mu\text{s}/\text{word}$ memory emptying speed, to the conclusion that the acceptable event rate (with the size as above) is around $5 \cdot 10^4\ \text{s}^{-1}$. It is impressive, however at such load the FERA itself (readout to memories) would generate a substantial dead-time.

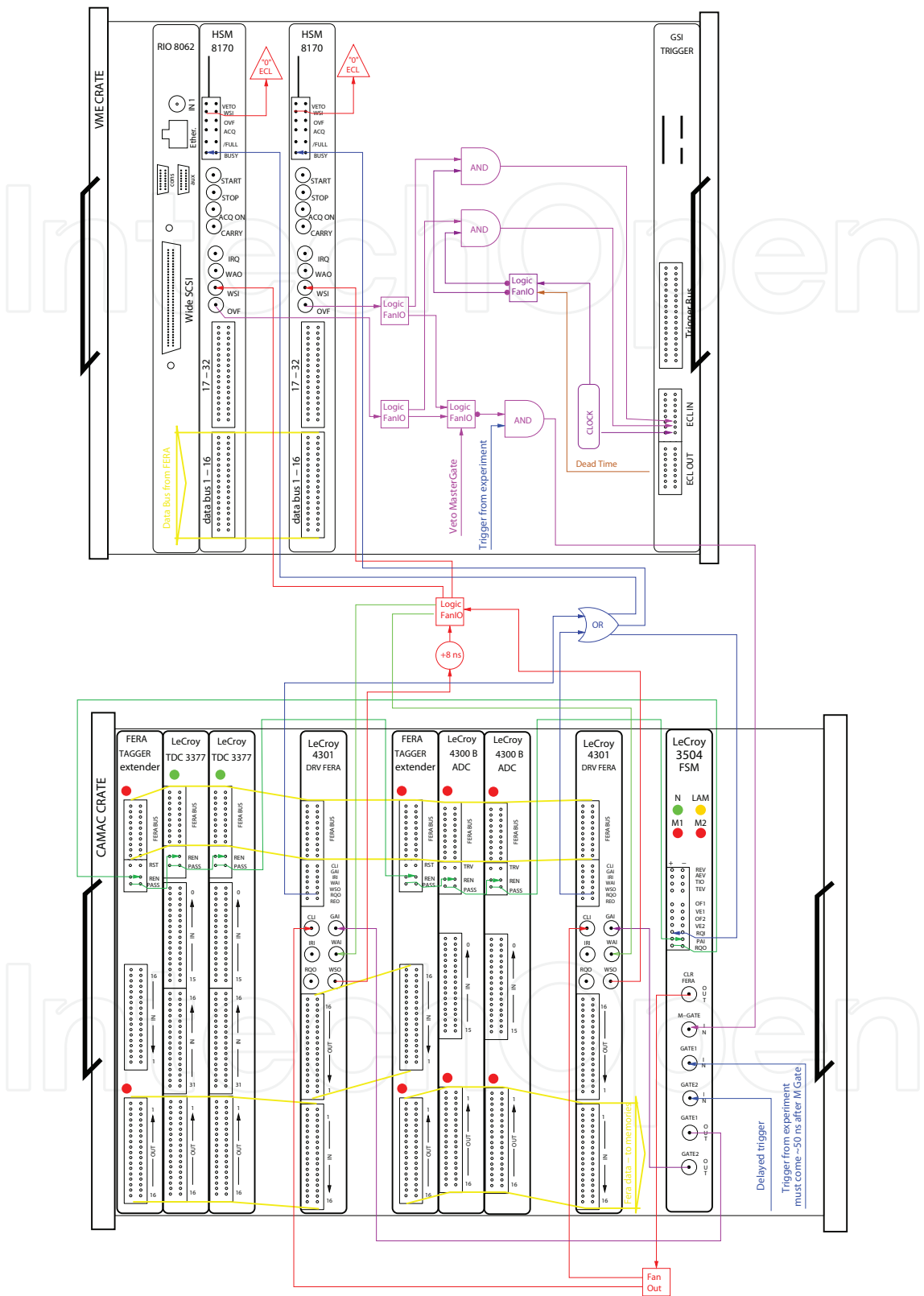


Fig. 7. Full FERA system equipped with the VME buffer Memories (here HSM 8170 serviced by a RIO2 front-end processor). The connections are slightly different than in the case of the CAMAC memories due to particularities in the requirements of the VME modules.

It is worth stressing that all the assumptions used in the above estimations are rather conservative and therefore a factor of about 2 reserve in the rate capability is most certainly incorporated. The exact number clearly depends very much on the particular experimental application. In any case, the estimated resulting Full FERA system performance is unparalleled in comparable DAQ systems.

6. Conclusions

This Chapter presents an important development in the area of FERA-based readout systems. A custom FERA Extender/Tagger CAMAC module is described, which offers the possibility to split FERA digitizing front-end electronics into several virtually independent sections, driven by separate, trigger-associated gates. These sections can be distributed over many CAMAC crates. The Tagger allows to fully exploit the buffering ability of the FERA system by enabling the parallel readout of several sub-systems, in which the event fragments are consistently, sequentially numbered. These fragments are then used to reconstruct full events in the back-end computer, removing the necessity to perform an on-line event building, therefore reducing the overall event readout time.

A configuration of the FERA system is presented in which a single Manager exerts control over the whole system, synchronizing the Memory readout to provide the best CAMAC data structure for the on-line monitoring software. The resultant Full FERA system can attain readout rates of about 1 MByte/s (i.e. some 6000 moderate-length events per second), which is very competitive with other comparable systems. With its extension to VME the data throughput can be as large as about 8 MByte/s (i.e. around 50000 events per second). This solution is reasonably simple but very reliable method for medium-sized experiments to upgrade and expand their readout electronics without major hardware investments. The Full FERA system has been successfully implemented in a number of recent precision experiments, in some of which the configuration has been extended to include also the generic PCOS III readout system of multi-wire proportional chambers (Barnet et al. 2000; Ban et al. 2006; Stephan et al. 2007; Stephan et al. 2009). The FERA system gains on capabilities due to now available modules, like Ortec Histogramming Memory HM413, CMCamac Driver, Memory and Histogrammer CMC203 or Wiener CAMAC-to-FERA Bridge. Logic modules based on FPGA allow to customize various functions to the FERA-compatible protocols. Examples of new implementations can be found e.g. in (Karpukhin et al. 2003; Ugorowski et al. 2006; von Reden et al. 2008). All that shows that the system is still vivid and worth considering when choosing readout/DAQ options for not-to-large experiments.

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