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# Active-Matrix Liquid Crystal Displays - Operation, Electronics and Analog Circuits Design

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## 1. Introduction

For more than four decades, Cathode Ray Tube (CRT) Displays have been the dominant display technology providing very attractive performance. Brightness, contrast ratio, high image quality, speed and resolution were the main high standard specifications that CRTs were satisfied.

The last two decades, there was a tremendous growth in small portable applications which required the necessary adjustment of the display technology to them. The large depth of the CRTs was the main disadvantage for preventing them to be used in these kinds of applications. Flat Panel Displays seem to be the most attractive solution to this problem. Displays engineers searched for many years in order to find the suitable flat panel display technologies that could replace CRT displays. The first successfully established flat panel technology was the plasma displays, which demonstrated to be of larger size and higher image quality compared to the CRT technology. However, the problem with the integration of plasma displays in small portable applications still exists. Finally, the inroad of the thin-film transistors liquid crystal displays (TFT-LCD), in late 1990's, was a milestone in the displays industry and technology.

The successful development of the TFT-LCDs was achieved not accidentally. It was the sequence of the liquid crystal cell technology development, in combination with the development of semiconductors technologies for large-area microelectronics on glass, like thin-film transistors. Although, both technologies were very-well known before the 90's, an extended research for establishing compatible fabrication processes for the materials and the manufacturing equipment has led to the TFT-LCDs realization.

TFT-LCDs were rapidly grown and dominated the displays industry, especially in small portable applications. The implementation of the TFT-LCD panel peripheral driving components with low-power CMOS blocks and, therefore, the compatibility with battery operation was the main reason for the ascendance of the TFT-LCD technology in small portable applications. Today, the TFT-LCD market has been expanded. They can be used in an extremely wide range of our everyday life products, like mobile phone applications, ATMs, PDAs, navigation systems, notebook PCs and home applications, such as wide screen TVs.

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At the beginning, when LCDs were used in calculators, watches and small sized displays, direct and passive matrix addressing were the applicable addressing methods. As the size, resolution and information content of the displays were increased, the number of the pixels array was, also, increased leading the existing addressing methods to become non-applicable. A solution to this problem was proposed by Lencher (Lechner et al., 1971) and by Marlowe (Marlowe & Nester, 1972). A switch TFT was added at each pixel of the display matrix and in this way the pixels were controlled independently with the use of the external driving voltages. The first external voltage controls whether the switch TFT will be turned "ON" or "OFF" and the second voltage is the necessary, to the liquid crystal, bias voltage which is stored to a capacitor. The storage capacitor is placed in parallel to the liquid crystal and ensures that the necessary liquid crystal voltage remains constant during the frame time. This addressing method is called Active Matrix and the displays that used this method are called Active Matrix Liquid Crystal Displays (AMLCDs).

In this chapter, the fundamentals of an AMLCD will be presented. The fundamentals include the operation description, the driving methods and circuitry and finally the analog circuits design by using polycrystalline silicon TFTs. At the beginning of the chapter, a short presentation of the thin-film transistors technology, including structures and operations modes, will be given. More attention will be given to the analog circuit design due to the difficulties that arise by implementing TFTs in circuits. Moreover, design techniques for overcoming these difficulties will be described in more details.

## 2. Thin-Film Transistors

### 2.1 Historical overview

In the past twenty years, the development of Thin-Film Transistors (TFTs) has become the spearhead of the electronic flat panel displays industry. However, the generation of TFTs is originated many years before, back to the earliest days of semiconductors physics. The TFTs principals and their potential utilities were settled nearly seventy years ago, but the remarkable development of the bipolar transistors and their technological cousin, the metal oxide semiconductor field-effective transistors (MOSFETs), has overshadowed the TFTs concept.

The first attempt for implementing a TFT device is traced back to the 40's and it was a thin-film field effect device used a germanium film (Bardeen & Brattain, 1948). The history and the structure of the TFTs, as it is known today, began with the work of Weimer (P. K. Weimer, 1962) at RCA Labs. in 1962. Polycrystalline cadmium sulphide (CdS) was the material that used for the thin-film and silicon monoxide was the insulator. Source and drain contacts were placed on the opposite side of the gate. This structure is called "staggered" and it is shown in fig. 1. Glass was used as the insulating substrate, forming in this way a three-terminal device. On the theoretical part, the analysis of the device characteristics was realized by Borkan and Weimer (Borkan and Weimer, 1963), based on Shockley's JFET analysis.

In the 70's, two very important events changed dramatically the prospects for TFTs. The first was the implementation of a thin-film semiconductor instead of crystalline bulk silicon material, like Cadmium Selenide (CdSe) (Broody et al., 1973). The impact of this implementation was the reduction of the fabrication cost and the decrease of the transistor size. The second landmark was the Active Matrix addressing method proposed by (Lechner et al., 1971) and the fact that the switch device needed in each pixel of the matrix can be materialized with the use of a TFT device.

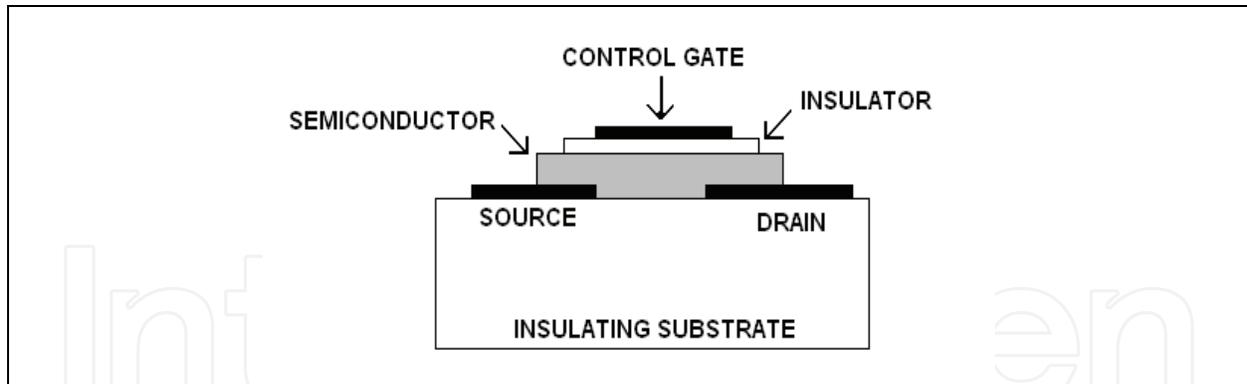


Fig. 1. Schematic diagram of Weimer's staggered CdS TFT structure.

The period from 1979 to 1981 was revolutionary for the TFT technology. In 1979, a new material was introduced for the implementation of the thin-film. (LeComber et. al., 1979) proposed a TFT using amorphous hydrogenated silicon (a-Si:H) as the active layer material. Amorphous hydrogenated silicon was preferred over the pure amorphous silicon due to the fact that it can be doped with both donors and acceptors forming n-type and p-type TFT devices. Thin-film, formed with a-Si:H, have no grain boundaries and it was the most cost-effective technology. However, the main disadvantage of this technology was the low mobility of the carriers and the instability of the device electrical characteristics.

In 1980, Lueder (Lueder, 1980) introduced a new approach in the TFT fabrication process. Photolithography was used instead of shadow masks that were being used since then. Their devices were optimized for liquid crystal displays applications, since the photolithography process made source-drain contacts that were self-aligned to the gate, causing the gate-source parasitic capacitance to be reduced. The compensation of the parasitic effects has improved the performance of the TFT-LCDs in the terms of the response time and the image quality.

In 1981, Depp (Depp et. al., 1981) from IBM proposed a polycrystalline silicon active layer. The use of chemical vapour-deposited polycrystalline silicon has improved the characteristics of the TFTs devices since the mobility has shown a significant increase. However, the chemical vapour-deposition was a high temperature process making the glass substrate in-appropriate. This was the reason for the replacement of the glass substrate with a high temperature substrate such as quartz.

In the forcoming years until now, the research of the TFT technology was focused on the improvement of the TFT devices characteristics and their fabrication process. Amorphous and polycrystalline silicon TFTs were the two main technologies that were used in the flat panel display industry. Recently, new TFTs technologies have been proposed, like nanocrystalline silicon (Pappas et. al, 2007.b), metamorphous silicon and organic TFTs (Lin et. al, 1997). These technologies have been emerged due to the constantly increasing performance of the flat panel displays which requires improved TFTs technologies. Furthermore, the introduction of new flat panel displays, like Organic Light Emitting Diode (OLED) displays, and the flexible substrate displays have created the need for new TFT technologies, compatible with the new types of flat panel displays.

## 2.2 Amorphous and polycrystalline silicon TFTs structures

Polycrystalline and amorphous silicon are the two most commonly used types of thin-film transistors in the display industry. Fig. 2 shows four basic structures of a-Si:H TFTs

according to the positions of the electrodes, insulator and the active layer. Staggered structures have already been described, whereas coplanar TFTs have all electrodes on the same side of the active layer. For better control of the active layer, the inverted structures of the above have been proposed. The inverted structures are also called bottom-gated structures. Amorphous silicon TFT technology can provide only n-channel devices because their electronic properties do not allow high-quality p-channel devices, since the ON-current is significant low. This is caused due to the low mobility (less than unity) of the holes along the active layer. The amorphous silicon TFTs market includes notebooks, desktop monitors and home LCDs televisions. The main advantage of the a-Si:H technology is the easy fabrication process with limited number of process steps making this technology cost efficient.

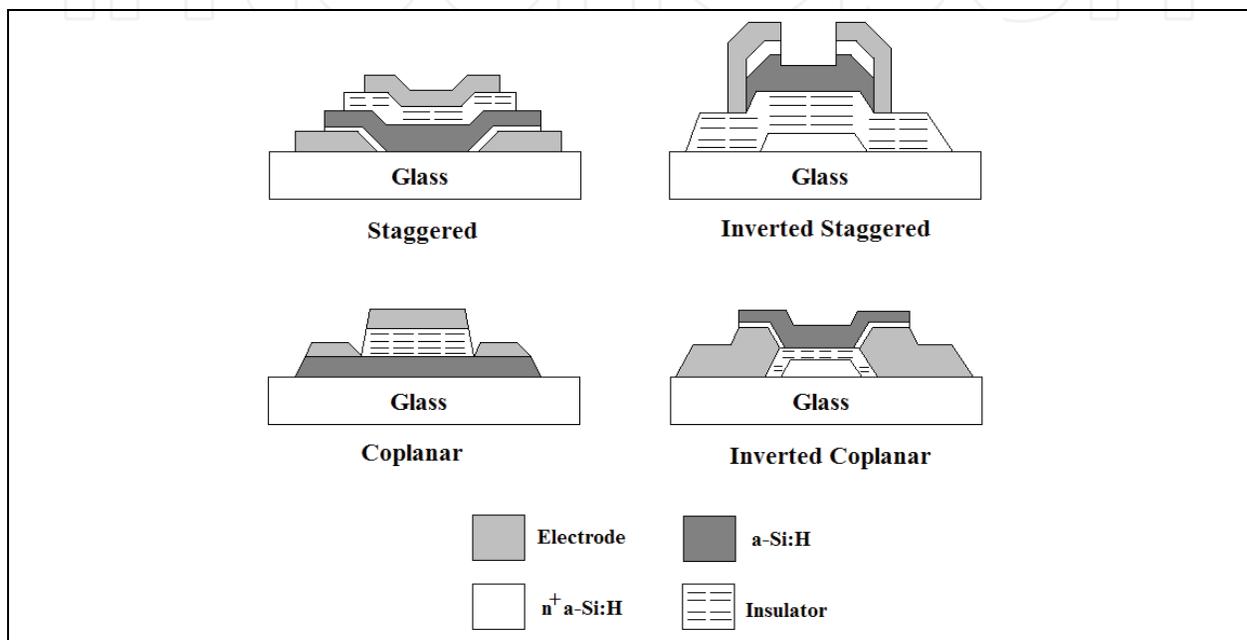


Fig. 2. Basic a-Si:H TFT structures.

On the other hand, polycrystalline silicon (poly-Si) technology can provide both n-type and p-type devices. Depending on the fabrication process, poly-Si TFT can be divided into high-temperature TFTs with fabrication processes similar to the ordinary silicon MOSFET devices and the low-temperature TFTs where the deposited amorphous silicon film is turned into polycrystalline silicon either with excimer laser annealing (ELA) or with solid state phase crystallization combined with ELA process. The basic top-gated poly-Si TFT structure is shown in fig. 3.

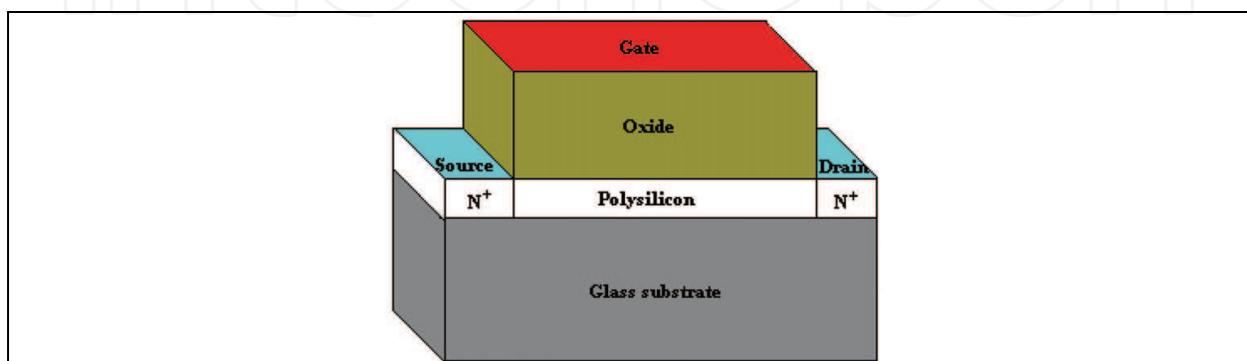


Fig. 3. Poly-Si top-gated TFT structure.

The main advantage of the poly-Si TFTs technology is the high carrier mobility (more than  $100 \text{ cm}^2 / \text{Vs}$ ), meaning that poly-Si TFTs can provide high driving current. The high driving current has led to the implementation of the peripheral driving circuits of an AMLCD with poly-Si TFTs, causing the reduction of the total fabrication cost and the realization of Systems on Glass (SoG).

### 2.3 Polycrystalline and amorphous silicon TFT operation

The operation of both poly-Si and a-Si TFTs is similar to the ordinary silicon MOSFETs operation. Typical transfer characteristics of n-type and p-type poly-Si and n-type a-Si TFTs, with gate dimensions  $W / L = 100 \mu\text{m} / 10 \mu\text{m}$ , are shown in fig. 4. As it can be seen from fig. 4, poly-Si TFTs have higher ON-current due to the higher carrier mobility. The TFTs operation can be divided into three working modes: cut-off, linear and saturation modes. The drain current of an n-type TFT can be presented with the following expressions for each mode of operation:

Cut-off mode:  $I_{DS} = 0$ , when  $V_{gs} < V_{thn}$

Linear mode:  $I_{DS} = \mu C_{ox} W [V_{eff} V_{ds} - V_{ds}^2 / 2] / L$ , when  $0 < V_{ds} < V_{eff}$

Saturation mode:  $I_{DS} = [\mu C_{ox} W V_{eff}^2] / 2L$ , when  $V_{eff} < V_{ds}$

where  $I_{DS}$  is the drain current,  $\mu$  is the effective surface mobility of the carriers,  $C_{ox}$  is the gate oxide capacitance per unit area,  $W$  is the effective gate mask width,  $L$  is the effective gate mask length,  $V_{ds}$  is the drain-to-source voltage and  $V_{eff}$  is the effective gate voltage, equal to the different between the gate to source voltage  $V_{gs}$  and the transistor threshold voltage  $V_{thn}$ ,  $V_{eff} = V_{gs} - V_{thn}$ .

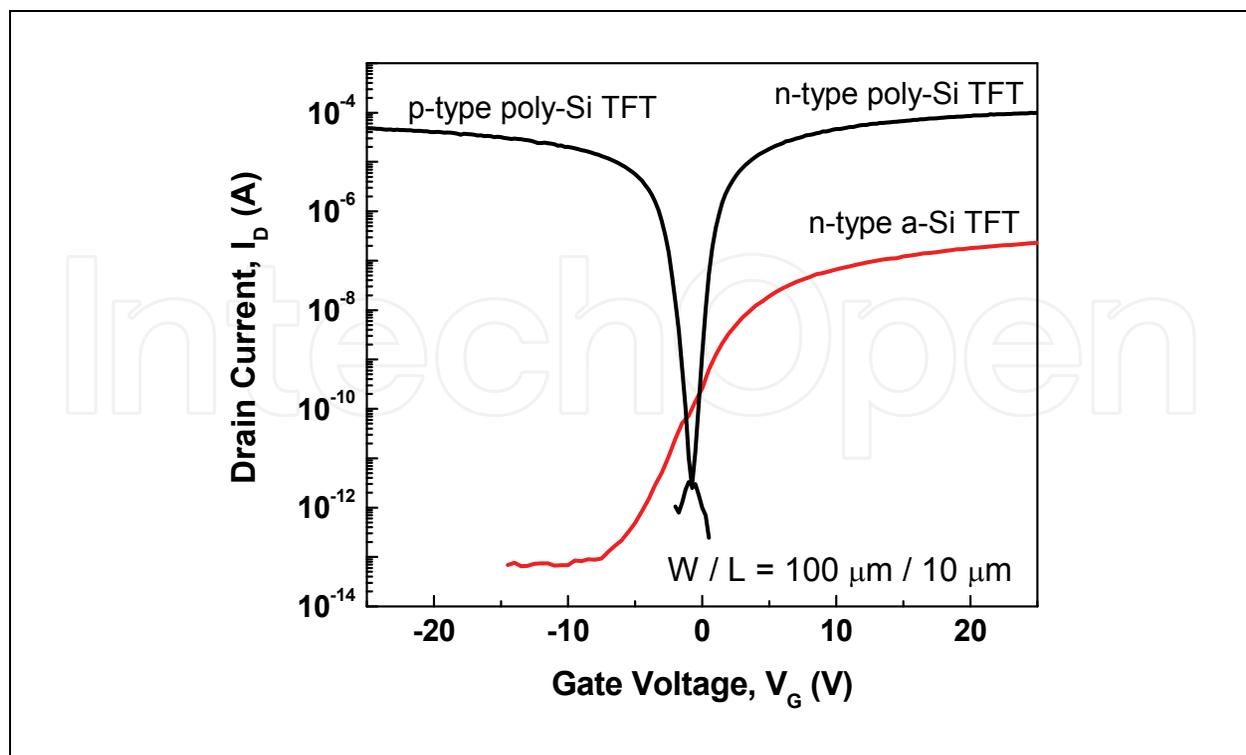


Fig. 4. Transfer characteristics of polysilicon and amorphous TFTs.

## 2.4 Instabilities of polycrystalline and amorphous TFTs

The expressions of the drain current for each working mode indicate the important role that the threshold voltage and mobility play in the TFTs operation. However, measurements in fabricated TFTs have shown that threshold voltage and mobility variations exist from device to device, even if the devices are implemented on the same wafer and with the same fabrication process.

For the poly-Si TFT technology, the threshold voltage and mobility variations are caused due the random distribution of the grain boundaries along the channel (Jagar et. al., 2003). The grain boundaries are produced when the amorphous silicon is turned into polycrystalline during the fabrication process and they can modeled as discontinues for the carriers along the active layer. For small sized display, the threshold voltage variation is about  $\pm 300$  mV (Zhang et. al., 2000), while for large substrate area it can be up to  $\pm 1$  V (Lee et. al., 1999).

Amorphous silicon TFT technology exhibits good uniformity in the electrical characteristics of the TFT devices over a large area even if some of the characteristics are rather poor, like the mobility. However, protracted bias stress will cause threshold voltage shift due to the inherent instability of the amorphous material (Powell et. al., 1989). The threshold voltage shift can be modeled by the equation (Den Boer, 2005)

$$\Delta V_{thn} = (V_{gs} - V_{thn}) \cdot \left( \frac{t}{\tau} \right)^{\beta} \quad (1)$$

where  $\Delta V_{thn}$  is the threshold voltage shift in the case of an n-type TFT and  $\beta$  and  $\tau$  are constants that depend on the temperature and the quality of the active layer-insulator interface. Threshold voltage shift can be more than 3 V (Arokia et.al., 2005) and even if it is temporal in nature, it can be considered to have the same impact on the circuits design as the threshold voltage variations of the poly-Si TFTs.

Another second order effect that produces instabilities in the TFTs operation is the impact ionization of the carriers which is known as “kink effect” (Valdinoci et. Al., 1997)). Kink effect appears when the device is operating in the saturation mode and for high values of the drain voltage. The result of the kink effect is an abrupt increase of the drain current caused by the impact ionization of the carriers near the drain electrode due to the high electric field. Kink effect can not be controlled, causing difficulties in the analog circuits design especially when high supply voltages are required. Among the variations that produce instabilities in the TFTs operation, the threshold voltage variations have the highest impact in the analog circuits design (Vaidya et. al., 2008) and compensation methods will be described in a next paragraph.

## 3. Addressing methods

There are three different addressing methods in the display technology, direct, passive matrix and active matrix. The addressing method that will be used in a LCD design is a very important choice, because the peripheral driving circuits of the pixel array depend on it. The addressing method can be selected by taking into account the specifications of the information content, the fabrication cost, the available TFT technology, the response time, the area and the power consumption, with the first three parameters being the most important.

### 3.1 Direct addressing method

The first used addressing method was the direct method. According to this method, its segment is directly connected and controlled individually by the peripheral electronics. The segments are arranged in such way so that they can produce the desired icon. The most common arrangement is the 7-segments, shown in fig. 5, used in simple alphanumerical displays, such as calculators and watches. In this method, no multiplexing is available and this is the reason for only being used in low information content applications. In the direct method, the smallest controllable component for the image production is called segment instead of pixel, which will be used in the two other addressing methods.

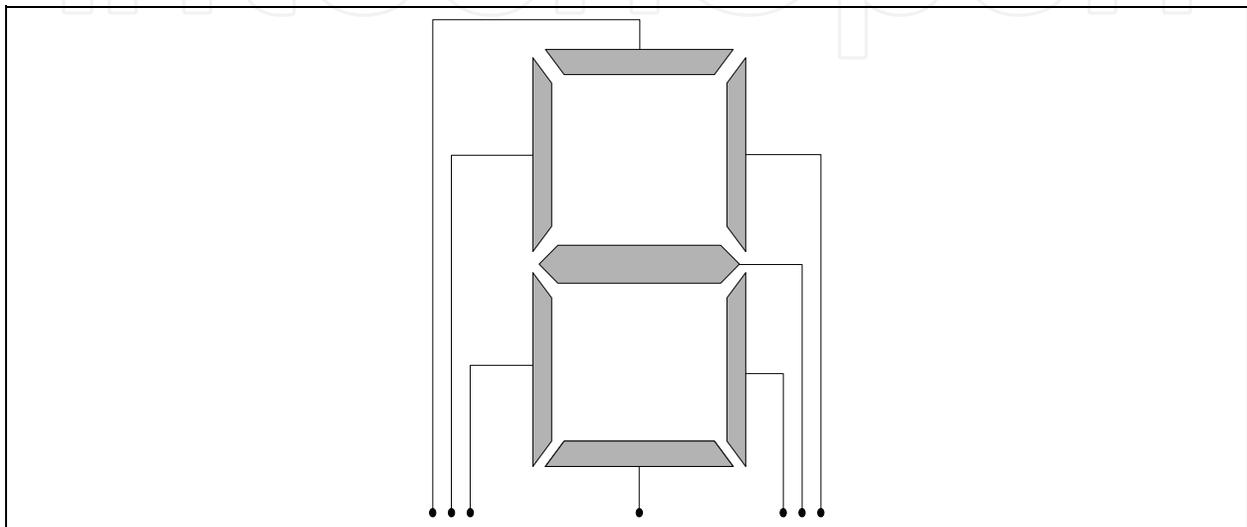


Fig. 5. 7-Segment arrangement with direct addressing method.

### 3.2 Passive matrix addressing method

As the displays and the information content were getting larger, the need for more picture elements was arisen. The solution to this problem was the modification of the segments arrangement into a pixels matrix with  $M$  rows and  $N$  columns. In this method, each pixel can not be controlled individually and a multiplexing addressing approach has to be realized. The new multiplexed addressing method was the passive matrix (PM). The configuration of the passive matrix addressing method is shown in fig. 6.

The passive matrix is a one-line-at-a-time driving method. During the programming time, a pulse from the row peripheral driver activates all the pixels of the programming line and at the same time the data voltage is delivered to the storage capacitor and the liquid crystal through the peripheral column driver. Passive matrix is the addressing method with the minimum number of interconnections. For example, for an  $M$  rows and  $N$  columns array, the direct method needs  $M \times N$  interconnections while the passive matrix method needs  $M + N$  interconnections. Furthermore, passive matrix is the simplest and the most cost-efficient method. However, the disadvantages of the passive matrix method are the low multiplexing capability and the crosstalk effect between the pixels. Crosstalk effect is caused because all the row-pixels are electrically related and a small dc voltage can be added to the pixel liquid crystal voltage from its neighbour pixels. The results of the crosstalk are the poor contrast ratio and the small active region of operation for the displays.

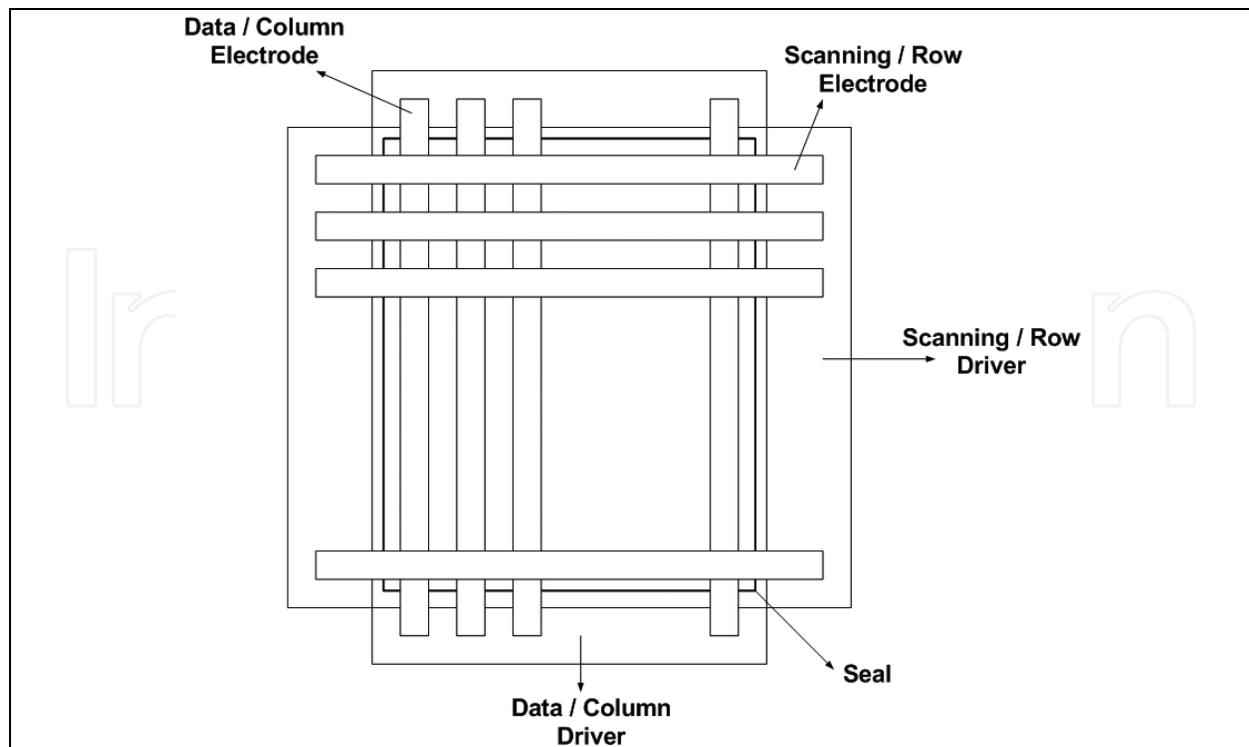


Fig. 6. Configuration of the passive matrix addressing method.

### 3.3 Active Matrix addressing method

The Active Matrix (AM) addressing method overcomes the multiplexing limitation of the PM method and the crosstalk effect. This can be achieved by incorporating a nonlinear control element, like a switch, in the cross point of the row and column lines (in series connection) of each pixel. The use of a switch will provide a 100 % duty ratio for the pixel by using the charge stored at the pixel during the row addressing time. Figure 7 illustrates the configuration of an AMLCD. The switch is controlled by two pulse signals which are produced by external driving circuits, the row and column drivers. As in most of the matrix addressed displays with line-at-a-time programming, the rows are scanned by a select gate pulse. The gate pulse of the selected row will turn "ON" the switch TFT of each pixel and simultaneously, the storage capacitor will be charged with the data voltage provided from the column driver. After the row time, the switch TFT will turn "OFF" as soon as the negative edge of the row pulse is delivered and the pixel will be isolated from all its neighbour pixels until the next frame time. In this way, the crosstalk effect and the multiplexing limitation are eliminated.

## 4. Active Matrix liquid crystal display electronics

The design of the displays electronics modules is an essential task due to the fact that the design defines the image quality of the display. The functionality of the electronics involves the acquisition of the incoming video signal, the signal processing and finally, the representation of the signal image on the pixels matrix. Therefore, the main objection of the electronics modules is the accurate supply of the data signal to each pixel with the right timing.

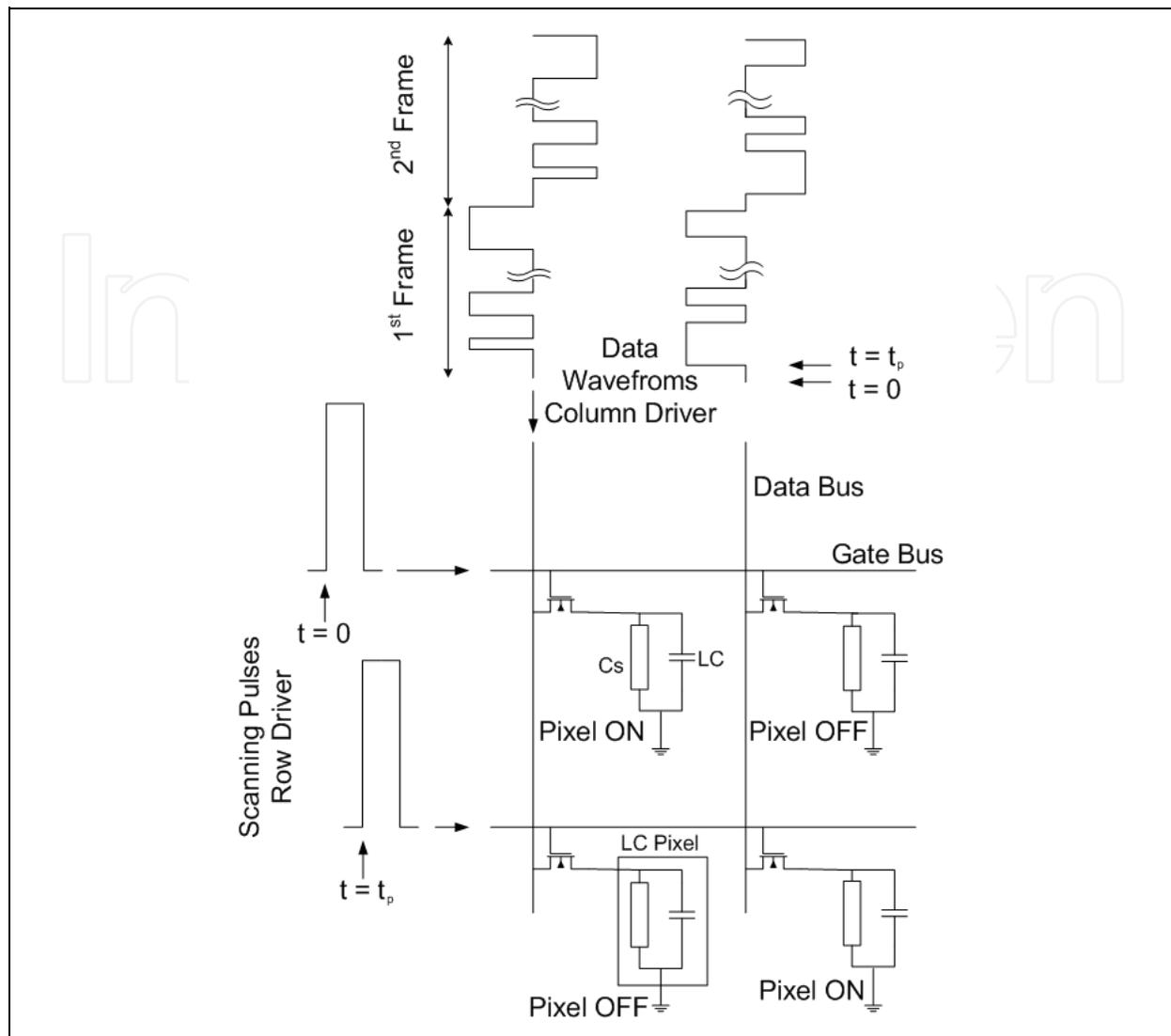


Fig. 7. Configuration of the active matrix addressing method.

#### 4.1 Electronics modules overview

Two of the most important parameters in the AMLCD design are the definition of the addressing method and the size of the pixels matrix. These two parameters will determine the peripheral driving electronics modules and the timing and programming issues. Furthermore, the types of displays format are separated based on the size of the pixels matrix, proving the significance of this parameter. The various displays format with their timing specifications are shown in Table 1.

The resolution of the display is referred to the number of the active pixels in each dimension, horizontal (rows) and vertical (columns). The first given number is the number of the columns and the second is the rows number. Higher resolution results in better image quality of the display. However, higher resolution for a standard matrix size requires additional hardware for its implementation; higher resolution is achieved by decreasing the size of the pixels. Furthermore, the ratio of the column number to the row number will determine the aspect ratio of the display.

Video Format	Resolution	H-Sync. @60Hz	System Clock	Panel Size
VGA	640x480	31 $\mu$ s	28 MHz	$\leq 10.4''$
SVGA	800x600	26 $\mu$ s	40 MHz	10.4'', 12.1''
XGA	1024x768	20 $\mu$ s	65 MHz	12.1'', 13.3'', 14''
QVGA	1280x960	16 $\mu$ s	104 MHz	13.3'', 14.1''
SXGA	1280x1024	15 $\mu$ s	108 MHz	14.1'', 15''
SXGA+	1400x1050	15 $\mu$ s	124 MHz	17'', 18.1''
HDTV	1920x1080	14 $\mu$ s	144 MHz	$\geq 24''$
UXGA	1600x1200	13 $\mu$ s	184 MHz	20.1'', 23''
QXGA	2048x1536	10 $\mu$ s	195 MHz	$\geq 30''$
QSXGA	2560x2048	8 $\mu$ s	256 MHz	$\geq 32''$
QUXGA	3200x2400	6 $\mu$ s	400 MHz	$\geq 36''$

Table 1. Displays format (VGA: Video Graphic Array, S : Super, X : Extended, Q : Quarter, U : Ultra, HDTV : High Definition Television)

$$\text{aspect ratio} = \frac{\text{columns number}}{\text{rows number}} \quad (2)$$

For example, in the case of a VGA display the aspect ratio is 4:3 while in HDTV is 16:9. Another important specification is the refresh rate of the display. Refresh rate is the number of times that an image is refreshed per second. A very usual mistake is the confusion between the refresh and frame rate. The refresh rate is the repeated illumination of identical frames, while the frame rate measures how often a display image can change into another. The refresh rate is calculated by dividing the horizontal scan rate by the number of horizontal pixels and multiplying the result by 0.95. The refresh rate is measured in hertz and a typical bandwidth is starting from 60 Hz for small displays and it can be up to 100 Hz for high motion displays. The refresh rate depends upon the monitor resolution and its maximum horizontal scan rate, as higher resolution necessitates more scan lines per second. Increased refresh rates reduce flickering and thereby reduce eye strain for a viewer. Because of this, it is advisable to purchase monitors that have a refresh rate between 75 and 85 Hz. For the timing (clock) issues, the horizontal synchronization (H-sync) period of each display format (i.e. the programming time of all the pixels of a row for a given refresh rate of 60 Hz) are shown in Table 1. The H-sync period is given by the following expression.

$$H - \text{Sync.} = \frac{1}{\text{refresh rate}} \div \text{rows number} \quad (3)$$

The system clock frequency is, also, depending strongly on the matrix size since it is given by the expression.

$$\text{System clock} = \frac{1}{H - \text{Sync.} \div \text{columns number}} \quad (4)$$

Figure 8 shows a block diagram of AMLCD electronics modules. An AMLCD consists of the pixels matrix, the peripheral column and row driving modules, the backlight, a timing - control unit and a booster module for producing DC voltages higher than the power supply voltage.

The pixels array and the row / column drivers are implemented using TFT technology meaning that they are fabricated on the glass substrate. The control and power supply generation blocks are separated, mounted on a PC board and connected to the row and column drivers on the one side and the host controller on the other. The control block may include level shifter, timing and analog functions generators. The objective of the control unit is to generate timing and data signals for biasing the row and column drivers, by taking as input digital signals which contain all the video, synchronization and timing information from the host system, which is a graphics controller chip.

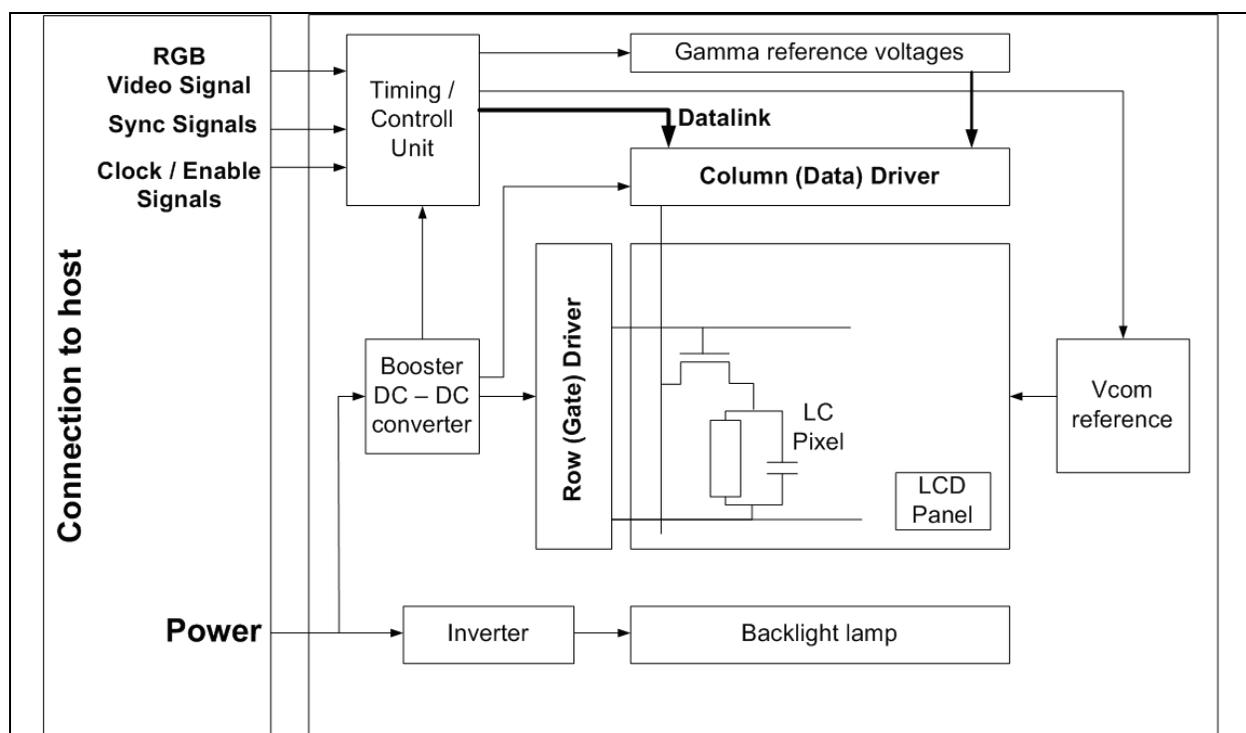


Fig. 8. Block diagram of an AMLCD architecture.

The architecture and design of the module electronics have a significant impact not only on the image quality of the display but also on the display system fabrication cost and power consumption. Figure 9 shows the contribution to the power consumption and the fabrication cost of each electronic module of a typical 10.4-in. backlit TFT-LCD. The typical power consumption of this display is 3 W at 150 cd/m<sup>2</sup> brightness.

Summarizing, an AMLCD designated for portable applications is expected to satisfy the specifications that are presented below:

- High Pixels Matrix (above QVGA)
- High Resolution (160 dots/inch)
- High Contrast Ratio ( $\geq 100 : 1$ )
- Full Color (8 bit/color)
- Full Motion Video (80 frames per second)
- Adequate Brightness (15-100 fl.)

- Wide Viewing Angle ( $\geq \pm 45^\circ$  in horizontal and vertical directions)
- Light Weight
- Small Volume (small depth)
- Low Power Consumption / High Luminous Efficiency
- Low Cost

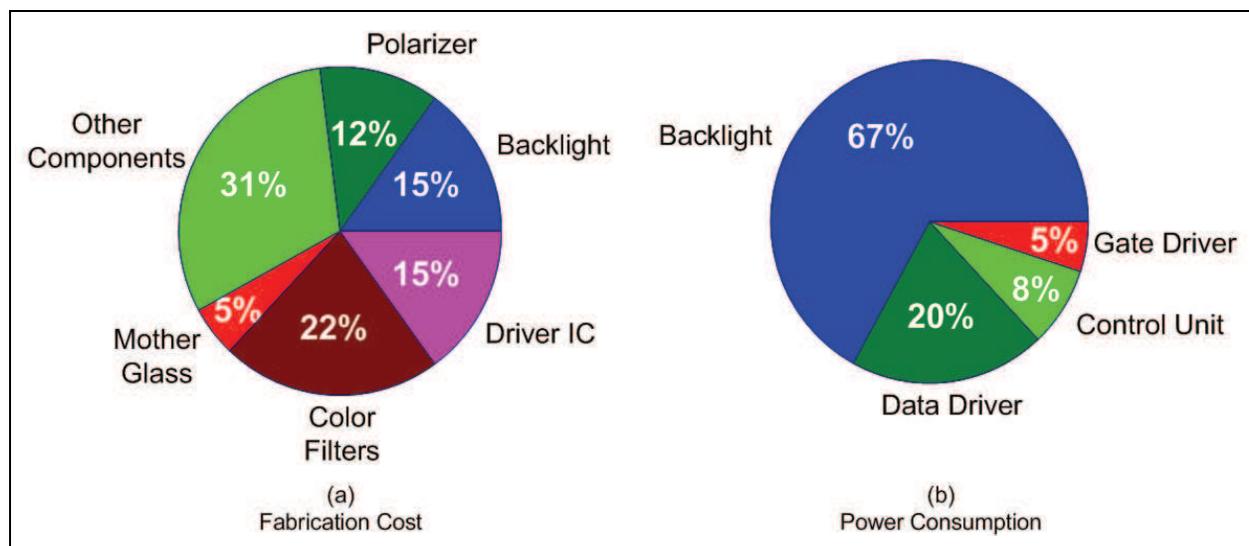


Fig. 9. (a) Fabrication cost contribution of each component. (b) Power consumption contribution of each electronic module.

#### 4.2 Pixel structure and design

Liquid Crystal Pixels are transmission type pixels with a backlight, meaning that they are not emitting their own light. While there are many types of liquid crystal materials such as smectics, nematics and cholesterics, twisted nematic (TN) display mode is the most advanced and popular. A TN pixel cell consists of two glass substrates coated on their inner surfaces with transparent electrodes and separated by several millimeters from each other. A nematic liquid crystal material fills the space between the two substrates and two polarizers are attached on both sides of the pixel with their polarization axis crossed. The polarizer is a three-layer composite film with a stretched iodine doped polyvinyl alcohol (PVA) polarizing film in the center and two outer films for protecting the PVA film from the ambient. Since the two substrates, each having alignment layer, are oriented with their alignments perpendicular to each other, liquid molecule is twisted initially. In the voltage-off state, the polarizers are oriented perpendicular and the incoming light from a back light source, whose polarity is twisted by the liquid crystal, is transmitted through the output polarizer. When a voltage is applied to the electrodes, the director of the molecules tends to orient themselves parallel to the applied field, since liquid crystal materials have positive dielectric anisotropy. In this situation, the polarization of the light transmitted through liquid crystal is crossed to the output polarizer resulting in the cut off of the light and thus creating a black state for the display pixel. This operation is called normally white mode, while normally black mode can be achieved by changing the polarizers to a parallel orientation. Figure 10 shows the configuration a TN pixel cell in a normally white mode.

The transmission (luminance) versus the applied voltage characteristic is shown in Fig. 11. The shown characteristic is for normal viewing angle and indicates that grayscale levels can

be achieved by varying the voltage across the LCD. Unfortunately, the transmission - voltage curve is viewing angle dependent, leading to grayscale errors and color shift in a display when it is viewed from significant angles to the display normal.

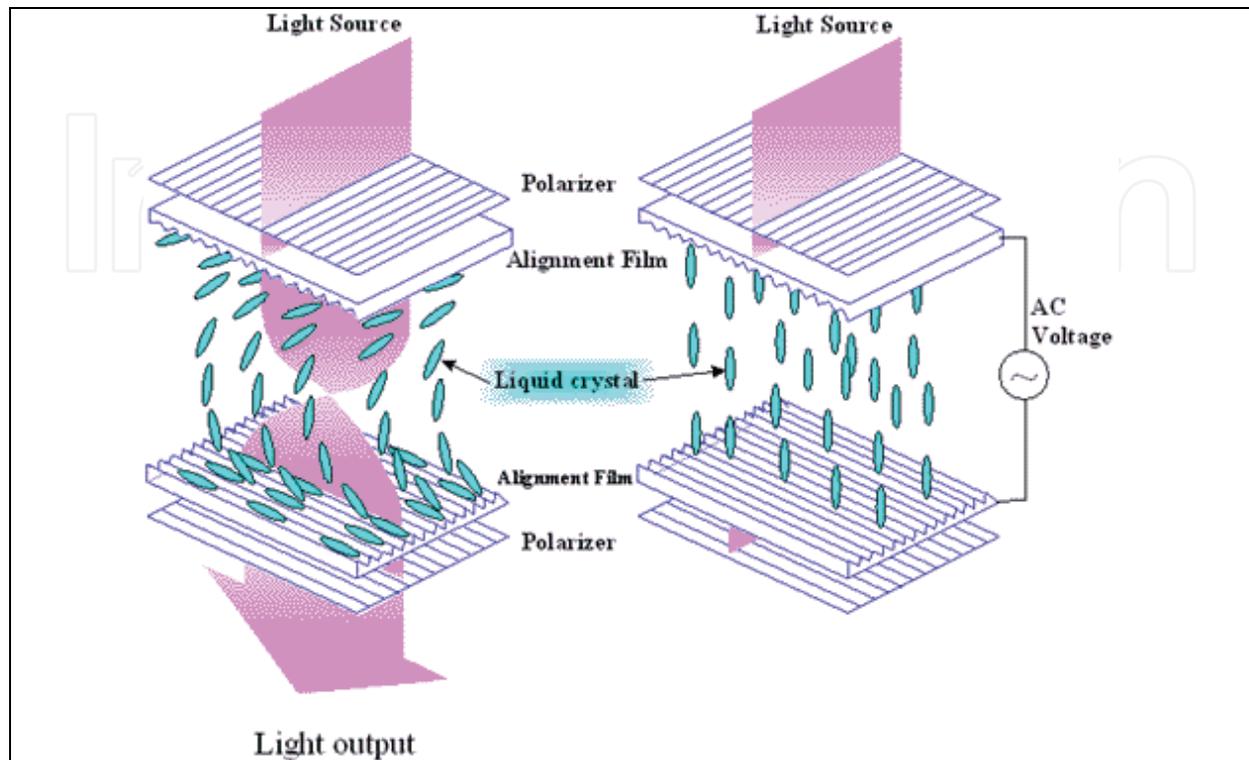


Fig. 10. Principle of operation of a TN pixels cell in a normally white mode.

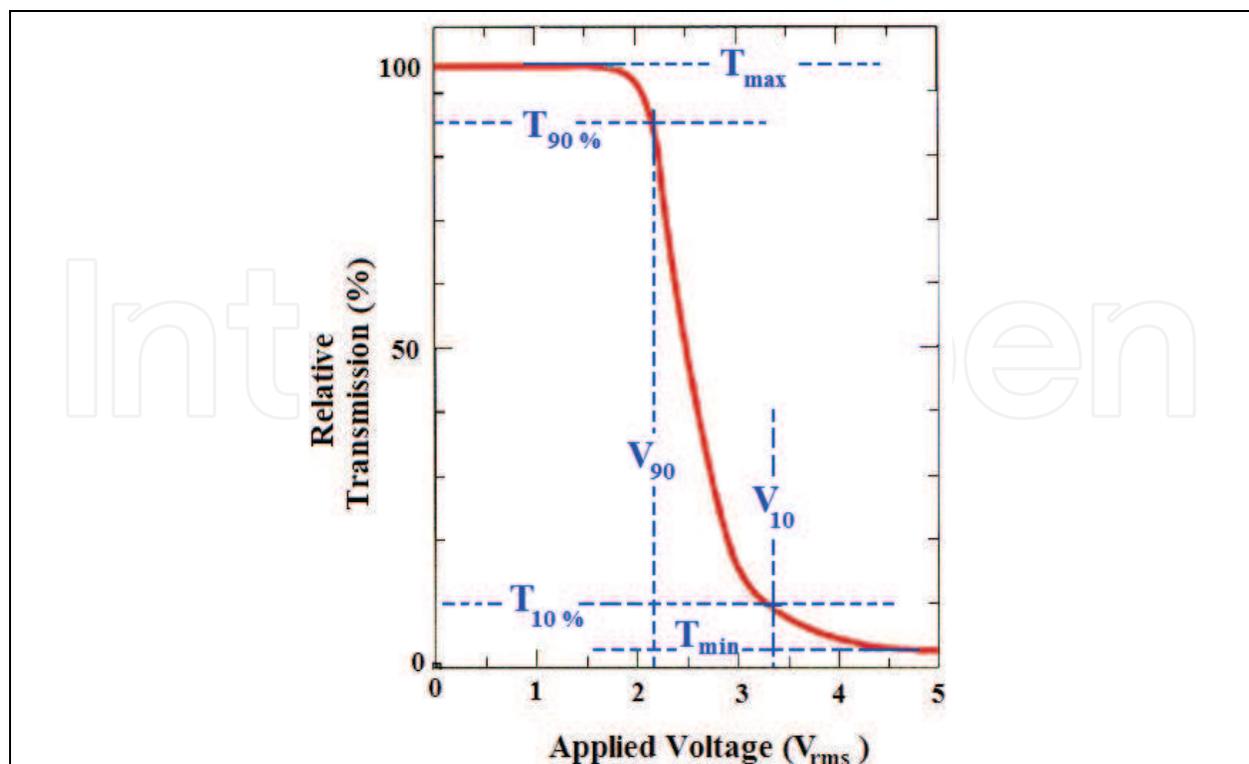


Fig. 11. Transmission versus applied voltage characteristic for normal viewing angle.

The equivalent circuit with the parasitic elements of a pixel cell and a typical TFT-LCD pixel layout are shown in fig. 12. The pixel consists of a switch TFT device, with the gate electrode connected to the row driver lines and the source electrode connected to the column driver lines. Furthermore, a storage capacitor is connected in parallel to the LC pixel capacitance.

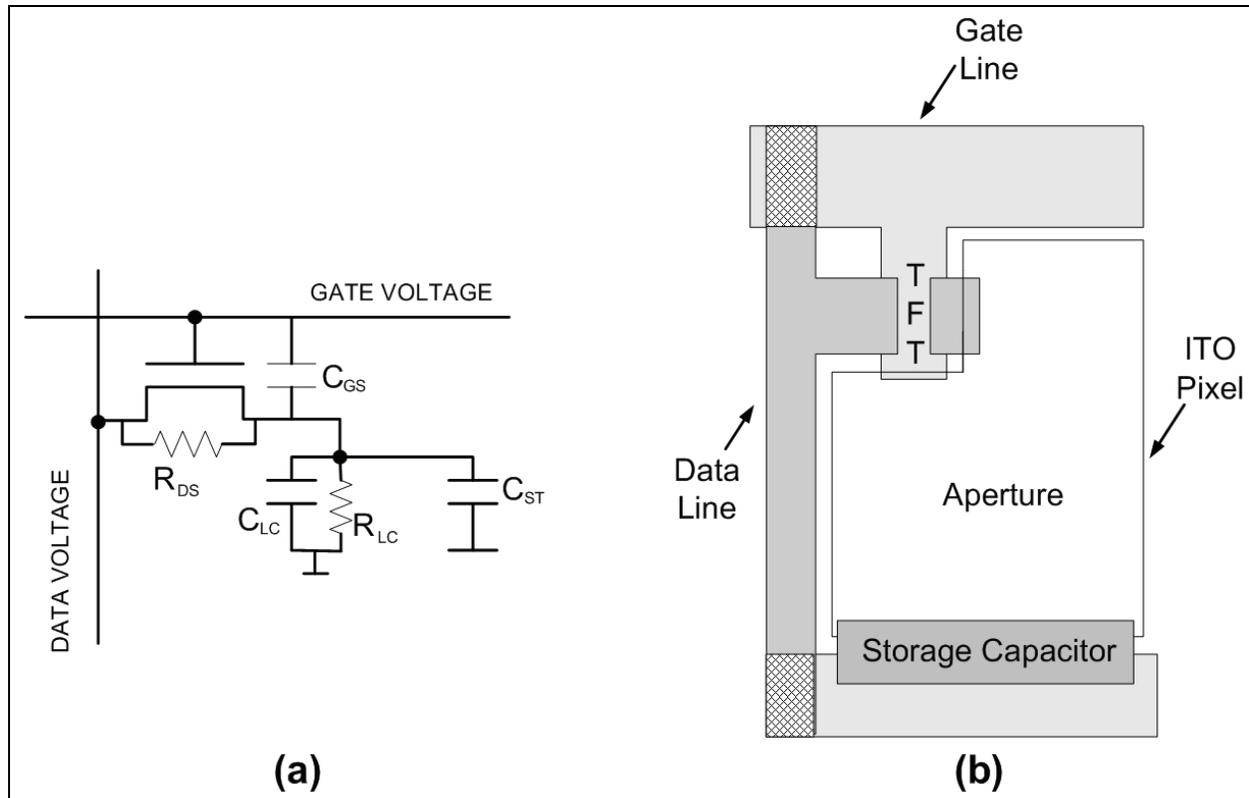


Fig. 12. (a) Equivalent circuit with the parasitic elements of a pixel and (b) typical pixel layout design.

The aperture part is the light transparent part and it is designated for the placement of the liquid crystal while the TFT, voltage lines and storage capacitor areas are non-light transparent. The ratio between the transparent portion of a pixel and its surrounding electronics is called aperture ratio or fill factor. Furthermore, in the shown layout design, the storage capacitor is connected to an adjacent row line resulting in the maximization of the aperture ration but the load capacitance of the row lines is, also, increased. The counter electrode of the LC pixel capacitor is the common ITO electrode on the opposite substrate (Den Boer, 2005). For large displays, this configuration is difficult to be used due to the large RC delay time of the row lines. In order to overcome this problem, a common storage bus can be placed in the aperture area which reduces the load capacitance of the row lines, but also reduces the aperture ration of the pixel.

The crosstalk effect is caused due to the column-line video-signal coupling during one frame and a DC component is being added to the AC data voltage. The DC component can not be entirely eliminated for all gray across the entire pixels matrix, resulting to slight difference in the pixel transmittance between the odd and even frames. A solution to this problem is the polarity inversion method. Apart from elimination of the DC component, the influence of the flicker on the display image quality is also eliminated with the use of a polarity inversion method. Four different polarity inversion methods have been widely used. Figure

13 shows the configuration of the four polarity inversion methods. The type of the polarity inversion method has an impact on the power consumption of the display. In the frame inversion method, all the pixels are driven to  $+V_p$  polarity in one frame period and then all of them are driven to  $-V_p$  polarity during the next frame period. This method is the most power-efficient method. However, this method is sensitive to the flicker and to vertical and horizontal crosstalk, meaning that this method can not be used in high image quality displays.

In the line and column inversion methods, the polarity of the pixels is alternated in the adjacent rows and columns, respectively. The line inversion method is compatible to the  $V_{com}$  modulation (Den Boer, 2005) while column inversion method is not compatible. Furthermore, the line inversion method consumes more power than the column inversion method because the capacitance of all row busses is charged and discharged every row time. Finally, the column inversion method has better results to the compensation of the flicker.

In the pixel inversion method, the polarity of each pixel is inverted from the polarity of its neighbouring pixels, by a combination of simultaneous row and column inversions. This produces the highest quality images by total elimination of the flicker and crosstalk effect. This method is not compatible with the  $V_{com}$  modulation and thus it requires high voltage column drivers leading to high power consumption.

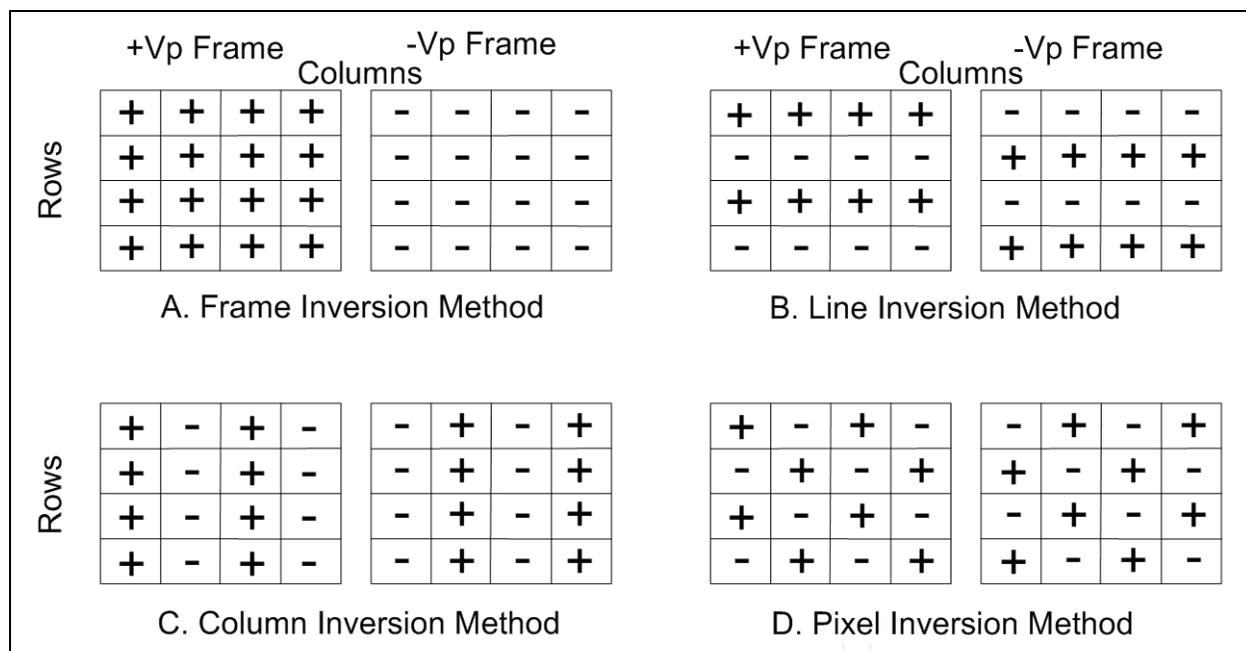


Fig. 13. Typical AMLCD polarity inversion methods.

A full color LCD display can be generated by incorporating red, green and blue color filters at the pixels. In order to produce the desirable color tone, the pixel is divided into three sub-pixels each one having red, green and blue color filter, respectively. The three sub-pixels have the same dimensions and the proper combination of each color tone; by applying the right voltages to the liquid crystals, the desired pixel emissive colour will be produced. The width of each sub-pixel is three times smaller than the sub-pixel length and when the three sub-pixels are very closely placed in parallel, a square full color pixel is produced. Figure 14 shows a full colour square pixel.

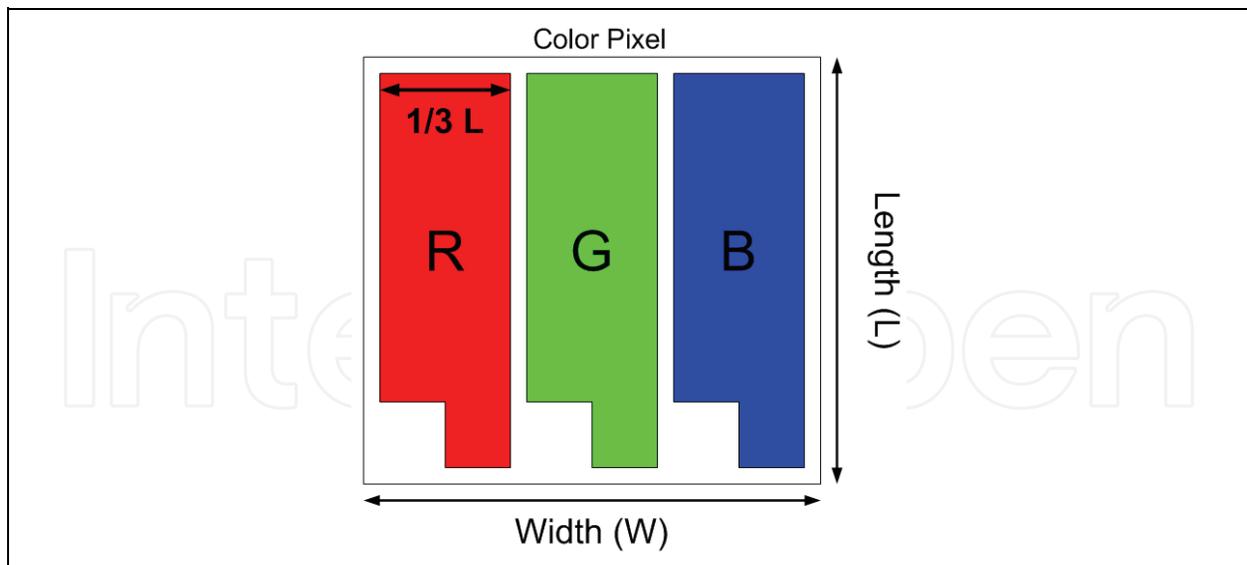


Fig. 14. Typical full color square pixel.

#### 4.3 Row (gate) and column (data) drivers

The pixels matrix on glass substrates is directly connected to the row and column drivers, implemented for integrated circuits. Figure 15 shows the basic architecture of a row driver. The operation of the row driver is based on the generation of the gate pulse, controlling the line of pixels to be programmed by turning "ON" or "OFF" the switch TFT device of each pixel. This is the reason for often being referred as gate driver. The generated, from the row driver, pulse has to satisfy the following specification: the selected gate pulse must be higher than the most positive column voltage by at least one TFT threshold voltage. The non-selected gate pulse must be lower than the lowest column voltage by at least one TFT threshold voltage. The above specifications ensure that the selected pixel stays "turned-on" during the programming period and "turned-off" during the emission period to hold the pixel charge. The duration of the gate pulses is about 10 – 50  $\mu$ s, depending on the display resolution as described in the systems clock frequency.

A row driver consists of a bi-directional shift register, level shifter, an enable system and an output buffer block. At the beginning, the input start (IS) bit selects a row at a time. If multiple cascaded chips architecture is available, the IS bit can be transferred to the second row driver and play the role of the start bit. This is the reason why IS's bit pin acts as both input and output pin. The DIR input controls the direction of the shift register, enabling the row driver to be mounted either at the left or at the right side of the display area. The enable system allows the output pulse to be turned to the non-selected edge before the end of the line time. The operation of this system is very important especially for large displays with high RC delay time of the lines, in order to avoid cross-talk effects by turning "OFF" the switch TFT devices for a few microseconds just before the data voltage is delivered to the pixels. Level shifters raise the voltages to the desirable output logical levels and the output buffers reduce the output impedance of the row driver so that the row lines can be driven by the output signals.

Column driver is more complex than the row driver. The operation of the column driver is to convert the input video signal into an output analog data signals for one row. The levels of the data signals represent the gray (or color) tone and all data signals are applied to the

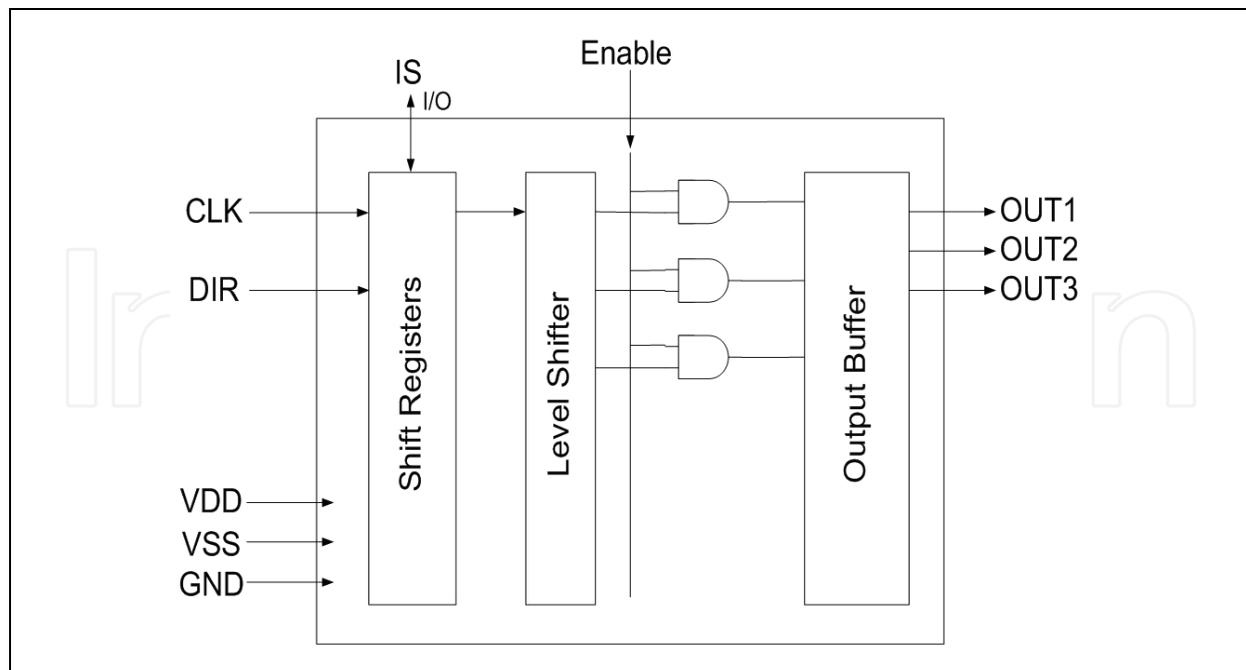


Fig. 15. Basic architecture of a row driver.

source of the switch TFT of all row's pixels simultaneously. The transmission - applied voltage curve (fig. 11) of the liquid crystal indicates that the liquid crystal requires about 5 V for its proper illumination. Considering the need of an AC drive signal, the required voltage swing across the LC material is about 10 V. In order to achieve a 10 V swing, the columns driver uses a 12 V power supply. The basic architecture of a column driver is shown in fig. 16.

A column driver consists of a bi-directional shift register which can be implemented with multiple chip architecture, like the row driver, in order to ensure either top or bottom mounting of the viewing area. The digital data signals for the red, green and blue channels are the input signals of the latch and the following, level shifter raises the signals to the proper voltage levels. The D/A converter is used for transforming the digital signal into analog gray scale levels. The reference input voltage  $V_{g\text{-cor}}$  is used for the gamma correction, while the POL signal controls the polarity inversion method that will be used. Finally, the output buffer has the same functionality as the output buffers of the row driver.

## 5. Analog circuits design

The main disadvantage of the TFTs technologies is the instability of the device electrical characteristics, like threshold voltage and carriers mobility, which have been described in a previous paragraph. These instabilities provoke the repeated implementation of the circuit blocks with constant specifications and identical performance, even if the blocks are placed on the same wafer. In digital blocks, the impact of the parameters variations is negligible due to the fact that TFTs are switching elements. On the other hand, in analog blocks, the effects of the parameters variations are a major problem that the designers have to overcome since the existing, in the literature, analog blocks can not be used. Furthermore, measurements have shown that the threshold voltage variation has stronger impact on the

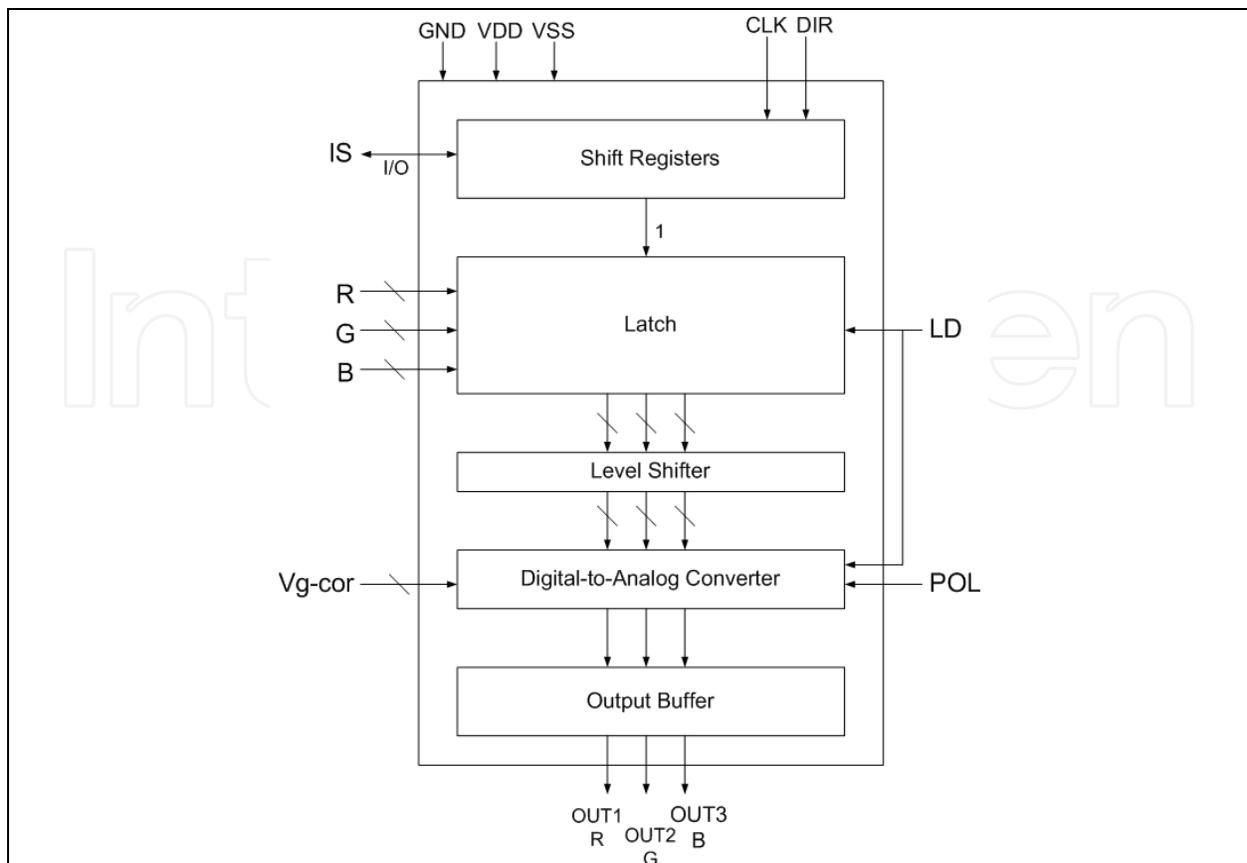


Fig. 16. Basic architecture of a column driver.

analog circuit performance than the mobility variation (Vaidya et. al., 2008), indicating that the new analog topologies have to be designed in such way so that threshold voltage compensation is achieved. In this paragraph, following the example of two compensation methods applied on an analog buffer design, complete description of the analog circuits design procedure with threshold voltage compensation is presented.

### 5.1 Analog buffer design

As it has already been mentioned, the analog buffer is the output stage of both row and column drivers and provides the necessary voltage to the row and column lines. The most commonly used topology for the analog buffer implementation is the common drain or source follower amplifier. The simple source follower type analog buffer is shown in fig. 17 (a). Although theoretically, the dc level of the output voltage is not the same as the dc level of the input signal, ideally the small-signal voltage gain is close to unity. In practical applications, the source follower exhibits an offset voltage from the input value, in which the offset voltage is mainly determined from the transistor threshold voltage since the final output voltage is equal to  $V_{GS} - V_{th}$ . For two source followers implemented with poly-Si TFTs, the output voltages will be different for the same applied input voltage due to the poly-Si TFTs threshold voltage variation. Furthermore, if these two source followers are used in the column driver architecture, a non-well controllable data voltage will be applied to the pixels resulting in the non-uniformity of the pixels brightness and gray scale. Therefore, source follower topologies with immunity in the threshold voltage variations have to be designed, in order to produce high quality image displays.

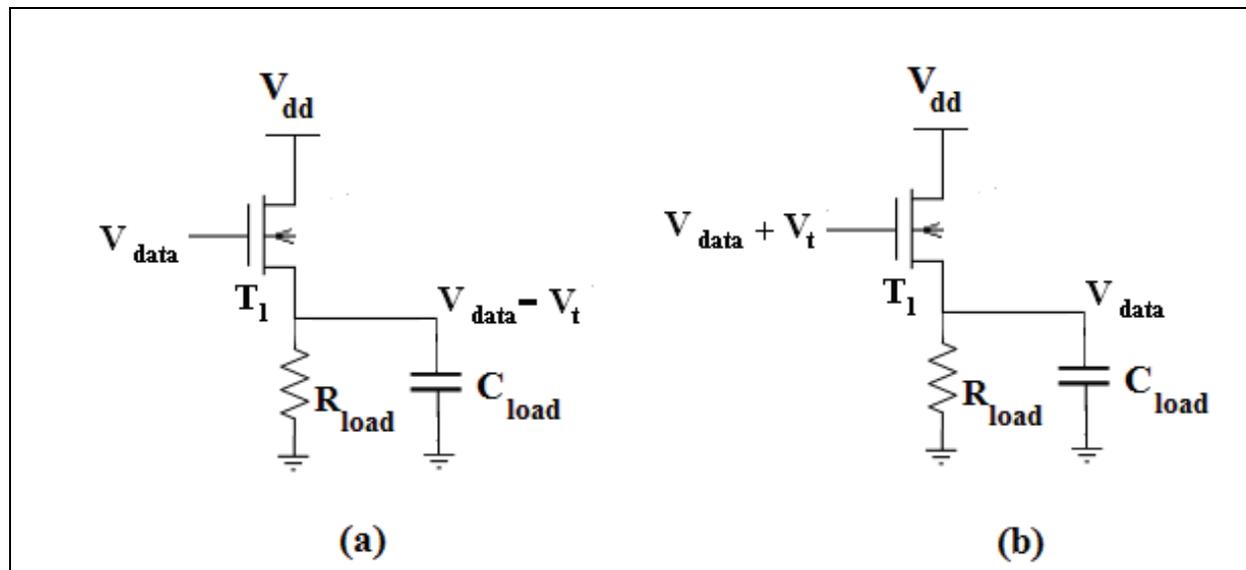


Fig. 17. (a) Typical source follower topology, (b) Source Follower topology with threshold voltage compensation.

Many compensation methods have been proposed including voltage mode or current mode threshold voltage compensation. All of them are based on increasing the input voltage by one threshold voltage by using an additional bias circuit topology, connected at the gate of the driving transistor. Figure 17 (b) shows the source follower topology with threshold voltage variations cancellation technique used in the column / row driver block.

For generation of an output voltage independent of the threshold voltage, a number of circuits have been proposed (Chun & Mok, 2004), (Tai et. al., 2005), (Chung et. al., 2001). The main similarity of the proposed circuits is the use of switches and additional control signals for sensing the threshold voltage of the driving transistor and the storage in a capacitor connected to the gate of the driving transistor. Therefore, the buffer operation has to be divided into compensation phase and data input phase. The disadvantage of these methods is that additional control signals are required in the configuration of the switches, which have to be generated from the row and column driver. Thus, changes in the architecture have to be made and circuit blocks have to be introduced, avoiding the storage capacitor which results in reduction of the buffer maximum frequency of operation. Recently, novel topologies of bias circuits have been proposed without requiring the use of either switches or storage capacitor, since the gate voltage is generated by either a static or a dynamic circuit. Each case is examined in the following paragraphs.

## 5.2 Static source follower

Figure 18 shows the topology of a static source follower with their timing diagram (Pappas et. al., 2007.a). The static source follower consists of five n-type poly-Si TFTs and only one bias voltage, which is proportional to the input data voltage, is required. For the theoretical analysis of the circuit, all TFTs have to operate in saturation mode. Furthermore, for poly-Si TFT devices which are very closely located on the same wafer and fabricated under the same conditions, their threshold voltage variation can be considered to be negligible compared to the threshold voltage variation over the whole panel. This assumption is generally accepted and it has been verified through measurements on fabricated circuits

(Lin and Tsai, 2007), (Jung et. al., 2007). The gate voltage is produced from the combination of M1 and M2 and M4 is the driving TFT. The operation of the static buffer can be divided into two phases.

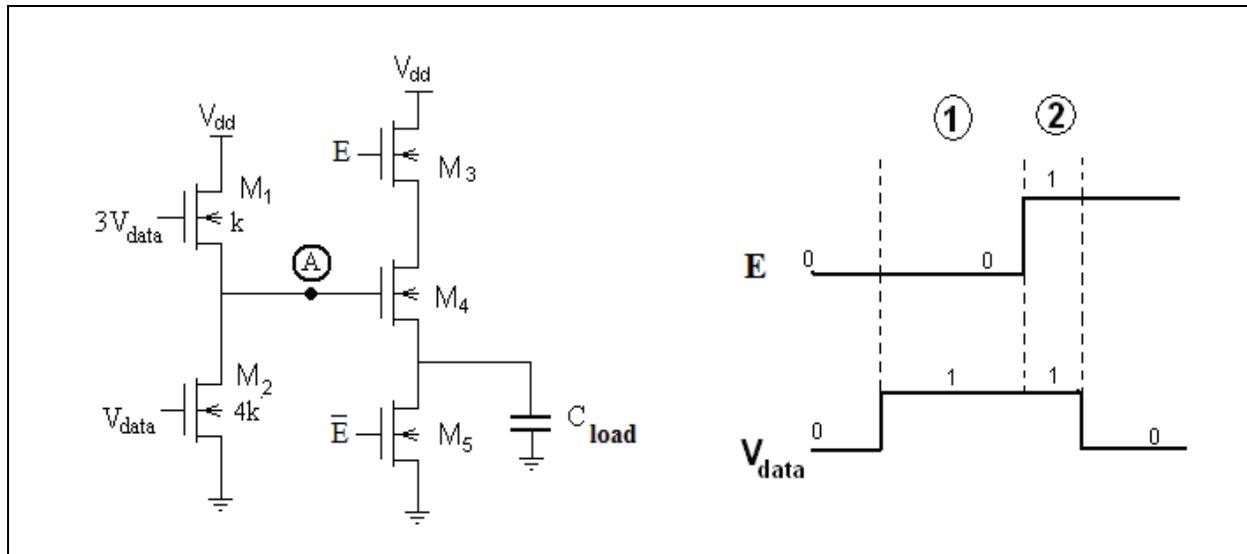


Fig. 18. Static source follower topology with its timing diagram.

During the first phase, the enable signal is at low voltage level causing the load capacitance to be discharged. At the same time, the data and bias voltages are applied to the buffer and node A is charged. The same current flows through transistors M1 and M2, while M2 has four times larger gate width than M1 ( $W_2 = 4W_1 \rightarrow k_1 = 4k_2$ ). Under these conditions, the node A voltage is calculated by the expression

$$I_{DS1} = I_{DS2} \rightarrow \frac{1}{2}k_1(V_{GS1} - V_{TH1})^2 = \frac{1}{2}k_2(V_{GS2} - V_{TH2})^2$$

$$\rightarrow V_{GS1} - V_{TH} = 2(V_{GS2} - V_{TH}) \quad (5)$$

The bias voltage is selected to be equal to  $3V_{data}$ . Therefore,  $V_{GS1} = V_{bias} - V_A = 3V_{data} - V_A$  and  $V_{GS2} = V_{data}$ . Applying these to eq. 5, we obtain

$$V_A = V_{data} + V_{TH} \quad (6)$$

Therefore, node A is charged to the proper voltage.

During the second phase of operation, the enable signal (E) is turned to high voltage level. In this situation, the driving transistor is connected as a source follower amplifier causing the load capacitor to be charged up to  $V_{data}$ . The theoretical analysis demonstrates that the static source follower exhibits high immunity to threshold voltage variations, since the output voltage is independent on the threshold voltage. The only change that has to be made in the column or row driver architecture is the addition of a circuit block, which will produce the bias voltage and the additional control signal (Enable). This circuit block can be a simple multiplier, because the bias voltage is proportional to the data voltage. The necessary change in the row/column driver architecture is shown in fig. 19.

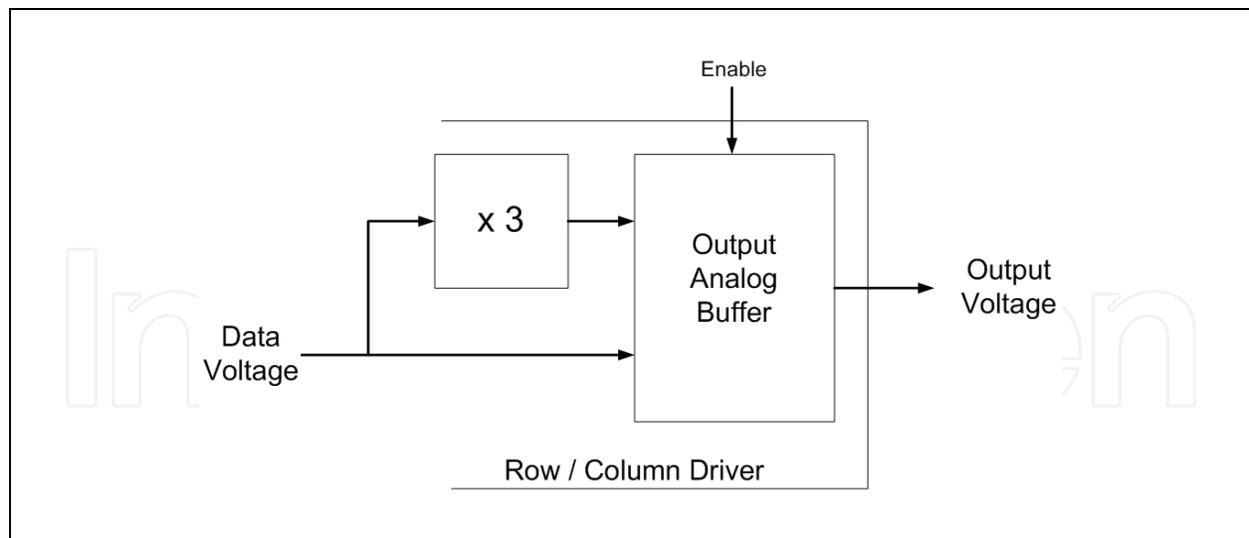


Fig. 19. Row/Column driver architecture with the use of the static source follower.

The advantage of the static source follower is the absence of switches and storage capacitor, leading to less real silicon area and higher maximum frequency of operation. However, the static source follower requires higher supply voltage, since all poly-Si TFTs have to operate in saturation mode and a high bias voltage is used. High power supply results in higher power consumption.

### 5.3 Dynamic source follower

Figure 20 shows the dynamic source follower topology and its timing diagram (Pappas et al., 2008). The dynamic source follower consists of five n-type poly-Si TFTs, a 2-to-1 multiplexer and two additional control signals. For the theoretical analysis of the buffer, the same assumption for the threshold voltage variation of closely placed devices is considered and all transistors have to operate in saturation mode. The control signal “Reset” can be used as the multiplexer select signal and as a reset signal for the buffer at the same time.

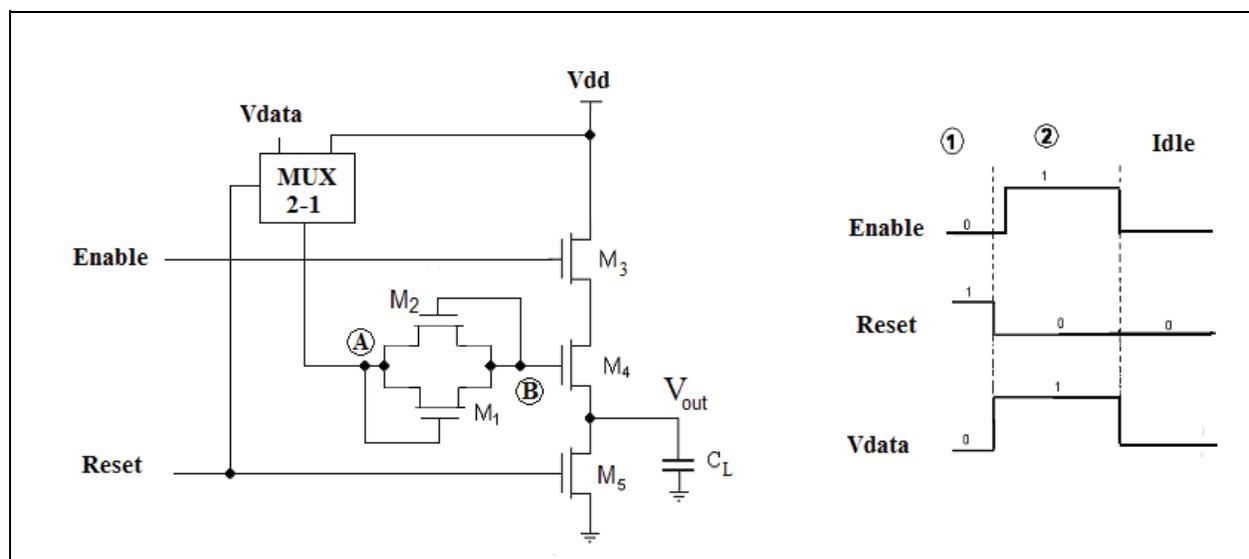


Fig. 20. Dynamic source follower topology with its timing diagram.

The operation of the dynamic source can be divided into three phases. During the first phase, the reset signal is at high voltage level causing the load capacitor to be discharged. At the same time, with the reset signal at high voltage level, the high voltage  $V_{dd}$  is selected from the multiplexer causing node B to be charged up to  $V_{dd} - V_{TH}$  due to the diode-connected transistor M1. During the second phase, the reset signal is turned to low voltage level and the data voltage is selected from the multiplexer causing node A to be charged up to the data voltage. Transistor M1 will turn "OFF" and node B will be discharged through M2 until the voltage at node B is equal to:  $V_B = V_{data} + V_{TH}$ , due to the diode-connected transistor M2 and the value of the node A voltage. When the voltage at node B obtain its proper value, the enable signal is turned to high voltage level and the driving transistor M4 is connected as a source follower amplifier causing the load capacitor to be charged up to  $V_{data}$ . When the load capacitor is completely charged, all signal will turn into their low voltage levels and the buffer will operate in idle mode.

The theoretical analysis demonstrates that the dynamic threshold voltage variation has no impact on the dynamic source follower functionality, without using switches and storage capacitor for sensing the threshold voltage. Furthermore, the dynamic source follower requires lower power supply compared to the static one, leading to lower power consumption. However, the dynamic source follower requires two additional control signals and a 2-to-1 multiplexer, indicating that changes have to be made in the row/column architecture. The row/column architecture with the use of the dynamic source follower is shown in fig. 21.

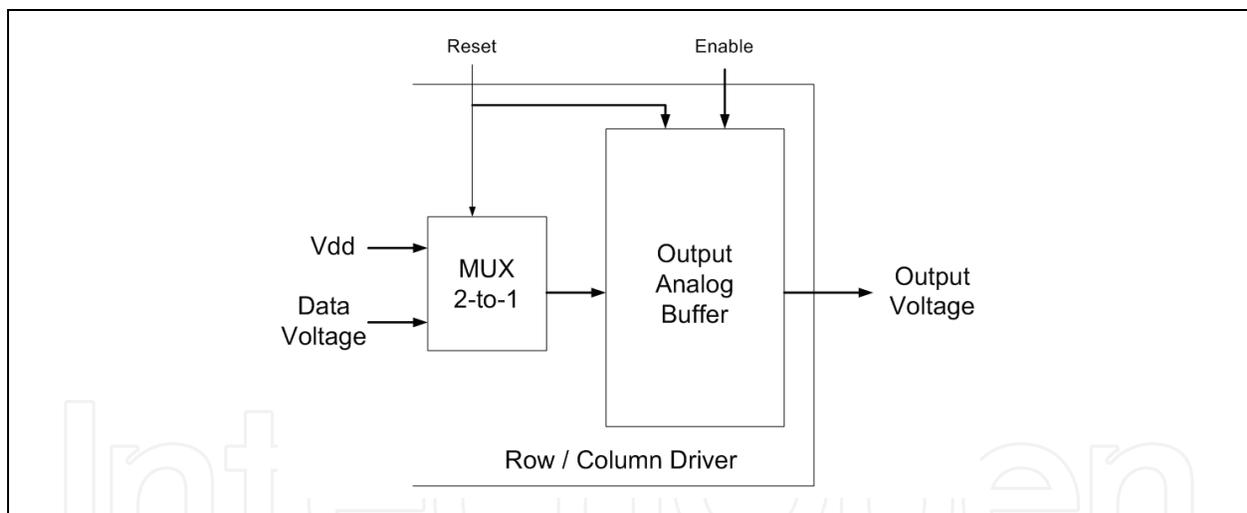


Fig. 21. Row / Column driver architecture with the use of the dynamic source follower.

#### 5.4 Verification of the analog circuits

The verification of the analog circuit functionality can be made through circuit simulations by using simulation programs, like Spice or CADENCE. A poly-Si TFT model is needed for the simulations and the most commonly used is the RPI poly-Si model developed by Rensselaer Polytechnic Institute (Shur et. al., 1997). In order to obtain realistic simulations, the TFT parameters must be extracted from fabricated devices (Pappas et. al., 2007). The parameters extraction can be realized by using, special designed for TFT technologies, CAD tools, like Silvaco ATLAS. For the design of circuits, one of the most significant parameter is the supply voltage. The supply voltage has to be high enough so all transistors will operate

in saturation mode and low enough in order to decrease the power consumption. Another trade-off is the dimensions of the transistors. The transistor dimensions have to be large enough to produce drain current able to charge the load capacitors and small enough to reduce the real silicon area of the circuits. Finally, statistical analysis for the threshold voltage variation in fabricated devices has to be made, enabling the modelling of the threshold voltage variations in Monte Carlo analysis (Pappas et. al., 2006). The results of the Monte Carlo analysis can demonstrate the impact of the threshold voltage variation on the functionality and performance of the circuits.

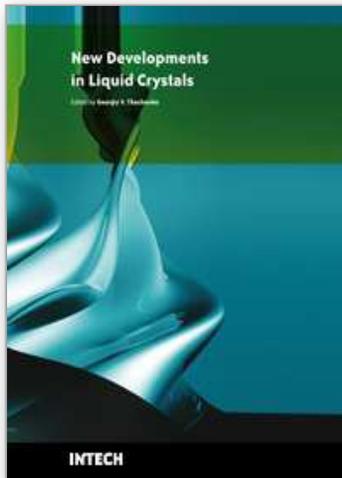
## 6. Conclusion

Active Matrix Liquid Crystal Displays, implemented with amorphous or polycrystalline silicon thin-film transistors, is the most attractive solution for the display industry. However, as the specifications become more and more demanding, the AMLCDs design and the TFTs device characteristics have to be improved. The AMLCDs electronics modules define the image quality of the display and the power consumption and, therefore, their architecture and design have a great impact on the AMLCD performance. The definition of these aspects and the detailed description of their functionality presented in this chapter can provide a helpful handbook for every designer.

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## **New Developments in Liquid Crystals**

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Liquid crystal technology is a subject of many advanced areas of science and engineering. It is commonly associated with liquid crystal displays applied in calculators, watches, mobile phones, digital cameras, monitors etc. But nowadays liquid crystals find more and more use in photonics, telecommunications, medicine and other fields. The goal of this book is to show the increasing importance of liquid crystals in industrial and scientific applications and inspire future research and engineering ideas in students, young researchers and practitioners.

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