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Applications of On-Chip Coplanar Waveguides to Design Local Oscillators for Wireless Communications System

Ramesh K. Pokharel, Haruichi Kanaya
and Keiji Yoshida
*Kyushu University
Japan*

1. Introduction

On-chip distributed transmission line resonators in CMOS technology have become the interest of research subjects recently (Ono et al. 2001; Umeda et al., 1994; Kanaya et al., 2006; Wolf, 2006) because of their size which becomes more compact, as the frequency of application increases. Among the various transmission lines, coplanar waveguide (CPW) has more engineering applications (Toyoda, 1996; Civello, 2005) because it is easy to fabricate by LSI technology since the signal line and ground plane exist on the same plane so that no via holes are required for integrating active components such as transistors on Si-substrate (Toyoda, 1996).

The applications of the CPW were reported for many on-chip LSI components. The CPW was exploited as an inductor and used to design a conventional-type matching circuit for LNA (Ono et al., 2001) in microwave-band frequency, and they are most popular in monolithic microwave integrated circuit (MMIC) (Umeda et al., 1994). However, the application of CPW lines as an inductor takes larger space than the conventional spiral inductors (Umeda et al., 1994). Some of the present authors have also implemented the on-chip CPW impedance-matching circuit for a 2.4 GHz RF front-end (Kanaya et al., 2006) and for 5GHz band power amplifier (Pokharel et al., 2008) using impedance inverters. In designing the matching circuits using impedance inverters and quarter wavelength resonators realized by on-chip CPW (Kanaya et al, 2006; Pokharel et al., 2008) the size of the matching circuits becomes compact thus reducing the chip area by about 30% than using spiral inductors for 2.4GHz-band applications and 40% for 5 GHz-band applications.

However, the applications of on-chip CPW resonators in designing other components such as a voltage-controlled oscillator (VCO) have not been reported yet. A conventional VCO consists of a LC-resonator to produce an oscillation at the frequency band of interest, and this LC-resonator may be replaced by a CPW resonator. Such possibilities are investigated in this paper. In a conventional VCO, the performance such as phase noise of the VCO depends on the quality (Q) factor of the LC resonator. Usually, a spiral inductor is used in

the resonator and these have quite low Q 's of around 3-5 at GHz frequency range and on the other hand, it takes large on-chip area in the expensive silicon substrate. The inductor can be either resonated with the device drain capacitance or by adding a shunt capacitor (on chip or off). Using bond wires instead of on-chip spiral inductors allows the design of low phase noise oscillators but makes the fabrication more difficult as it is difficult to precisely set the length of the bond wire. Also for use in Phase Locked Loop (PLL) applications it is necessary to have variable frequency or so called higher frequency tuning range (FTR). Therefore, it is not a wise practice to use bond wires in designing a VCO due to design difficulties in estimating the bond wires inductances.

In this paper, first, we propose a design method of a VCO using on-chip CPW resonator thus replacing an LC-resonator. First, transmission characteristics of the on-chip meander CPW resonator fabricated using TSMC 0.18 μm CMOS technology are investigated experimentally and an equivalent circuit is developed. Later, the application of on-chip resonator is also demonstrated to design 10 bits digitally-controlled oscillator (DCO). The derived equivalent circuit is used to carry out the post-layout simulation of the chip. One of the advantages of the proposed method to design VCO and DCO using on-chip CPW resonator than using a LC-resonator is smaller chip area.

2. Design of On-Chip CPW Resonator and Its Equivalent Circuits

In this paper, we use Advanced Design System (ADS2008A, Agilent Technologies) for designing active elements and Momentum (Agilent Technologies) for passive elements for schematic design. Co-simulation option was used for electromagnetic characterization of hybrid structures consisting of active and passive elements together. We first develop the equivalent circuit for on-chip meander CPW resonator using experimental results and latter, the circuit is used to carry out the post-layout simulation of the chip.

The on-chip meander CPW resonator is designed, fabricated, and measured using TSMC 0.18 μm CMOS technology. This process has 1-poly and 6-metal layers and the thickness of the top metal is 3.1 μm . The conductance of the metal and dielectric permittivity (ϵ_r) of the SiO_2 are $4.1 \times 10^7 \text{ S/m}$ and 4.1, respectively. The upper layer is covered by lamination whose relative permittivity is 7.9.

Fig. 1 shows the layout and chip photos of on-chip CPW resonator designed and characterized by EM simulator. In Fig. 1(a), the enlarged portion of the layout is illustrated to show its structure in detail where the signal line and slot size is 5 μm each, respectively. Bottom metal (Metal-1) is used as ground plane covering all portion of CPW to reduce the losses. Therefore, we prefer to call this CPW as conductor-backed CPW. Total length of the resonator is 3300 μm which is supposed to be shorter than a quarter-wavelength resonator at 5.2 GHz. The chip photo of the on-chip CPW resonator is shown in Fig. 1(b) and Fig. 1(c). Please note that a small stub at the center CPW pad (dummy pad of right side) in Fig. 1(b) is to de-embed the interconnect between metal 6 terminal of the CPW resonator and the pad. The microwave characteristics are measured by using air coplanar probes (Cascade Microtech, GSG150) and vector network analyzer (HP, HP8722C) in Air coplanar probe station (Cascade Microtech Inc.). The CPW pads are 100 μm square and have coplanar configurations so that characteristic impedance is 50 Ω .

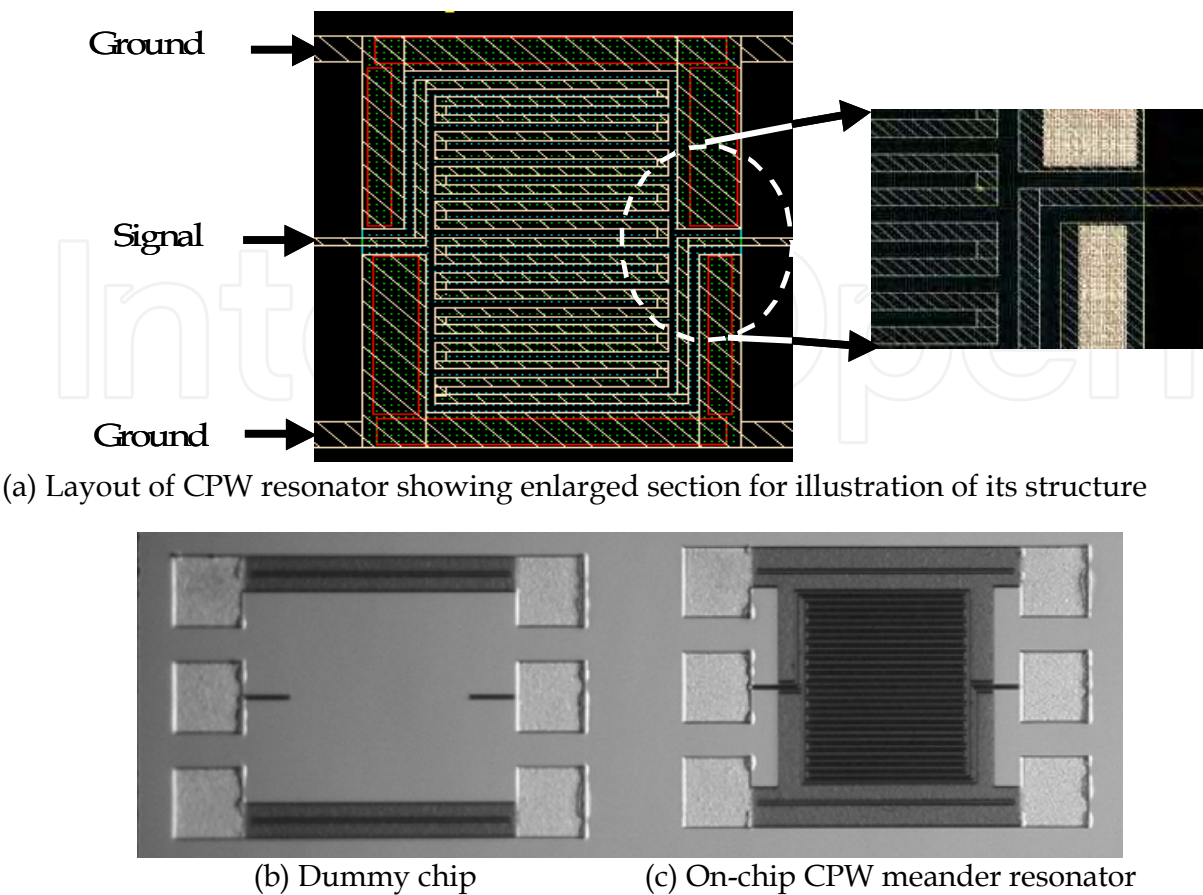


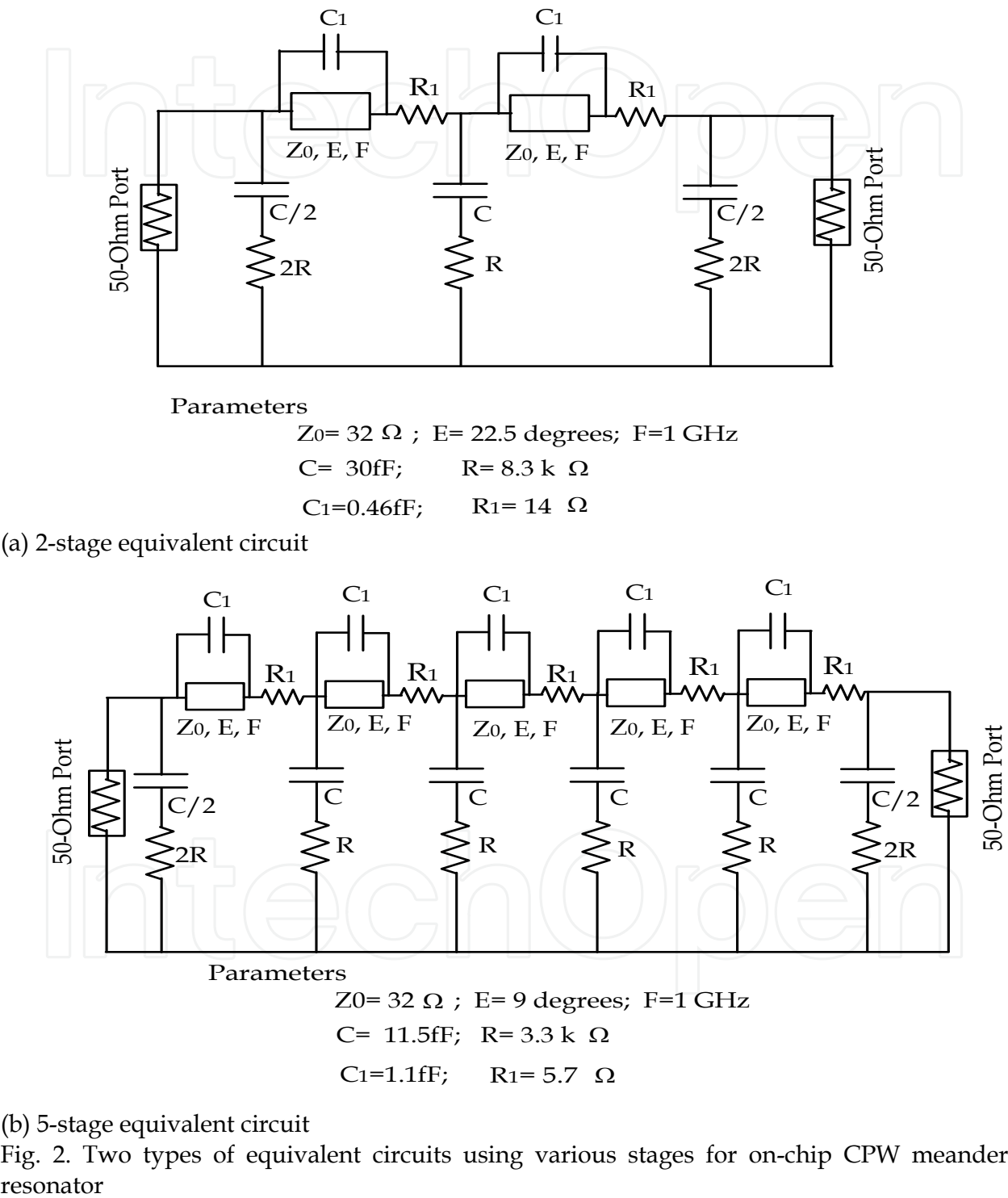
Fig. 1. Layouts and chip photographs of CPW resonator.

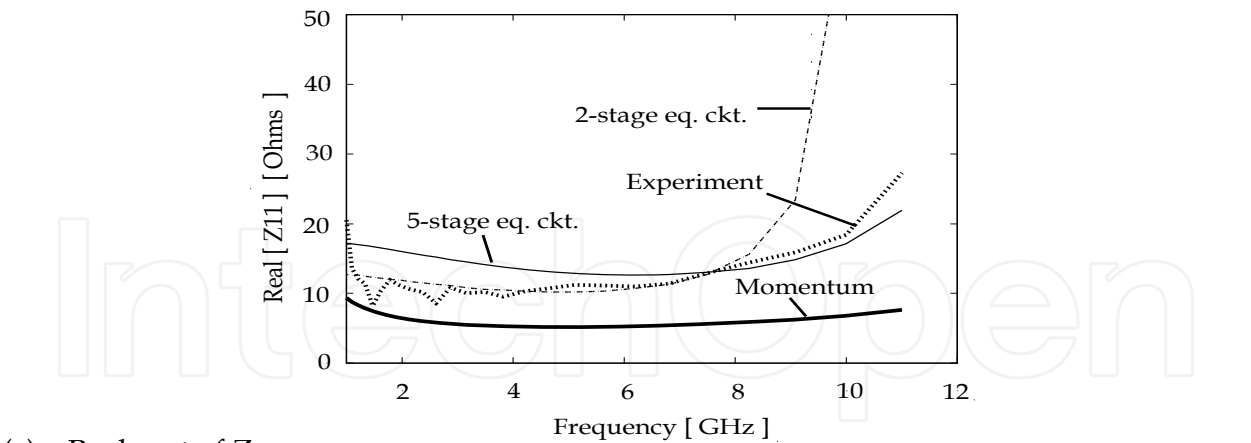
The measured data must be de-embedded in order to remove the parasitic effects of interconnects, pads and contacts surrounding the device (Civello, 2005). Therefore, in Fig. 1(b), chip photo of a dummy pad and in Fig. 1(c), chip photo of the CPW resonator are shown. In order to de-embed the measured raw data, at first, we measure S-parameters of total (Fig. 1(c)) and open dummy chip (Fig. 1(b)), respectively. Next, S-parameters are transformed into Y-parameters according to Equation (1) to get the Y-parameters (Y_{TML}) of the transmission-line resonator only.

$$[Y]_{TML} = [Y]_{total} - [Y]_{dummy} \tag{1}$$

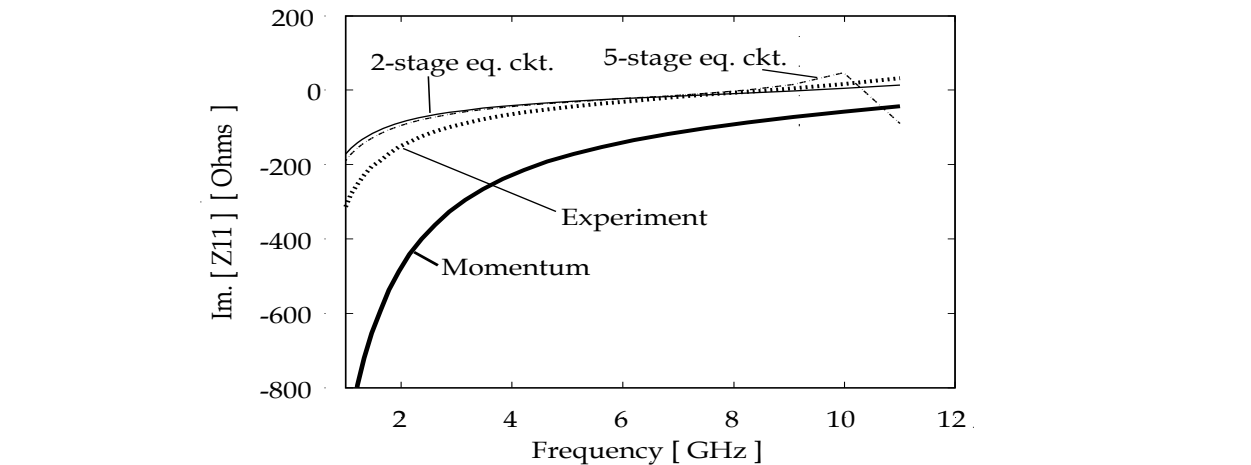
Y-parameters are then converted to Z-parameters in order to compare the results between simulation using the Equivalent circuits of Fig. 2. In Fig. 2, two equivalent circuits are developed using 2-stages and 5-stages for CPW resonator in meander structure, where ideal transmission lines are represented by the parameters such as characteristic impedance (Z_0), electrical length of each part (E), and frequency (F). Furthermore, C_1 represents the mutual capacitance between the meander lines, R_1 is the resistive loss of the line in each segment, and the parameters R (resistance), C (Capacitance) represent the silicon substrate of the corresponding segment. In Fig. 2(b), where 5-stage model of equivalent circuit is shown, the meander line is divided into shorter segments, therefore parameters of each segment of the model such as R_1 , C_1 , E will differ from 2-stage model of Fig. 2(a). Each parameters in both models are noted below each figure. Here, model parameters for Si-substrate (R, C) are

estimated by the dielectric characteristics, and the rest of the parameters of the meander line are estimated by fitting to the measured results, because our main goal is to develop a simple model which can be incorporated in ADE simulation to carry out the post-layout simulation of the chip that consists of on-chip CPW resonators.



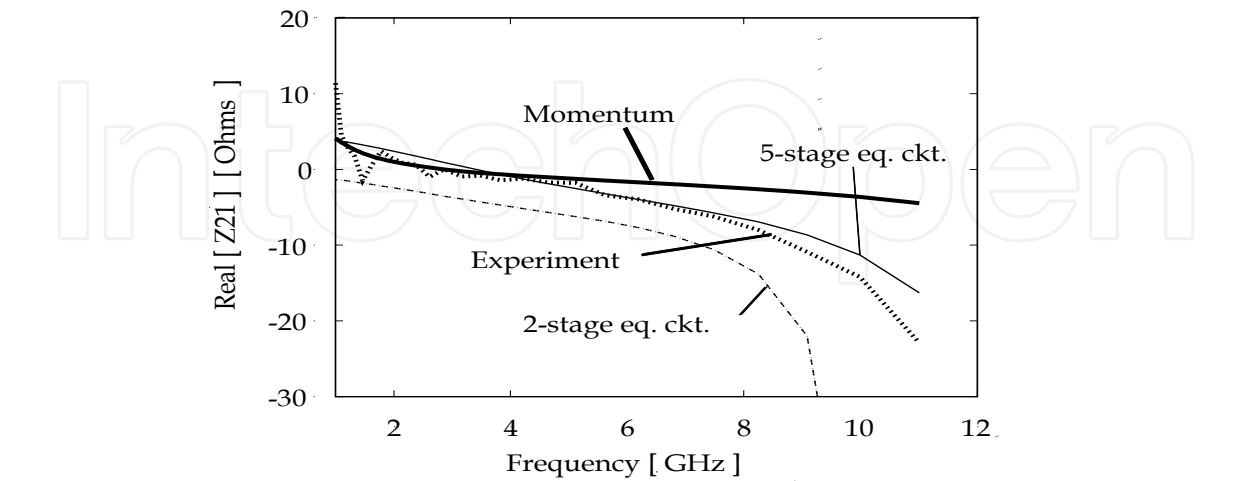


(a) Real part of Z_{11}

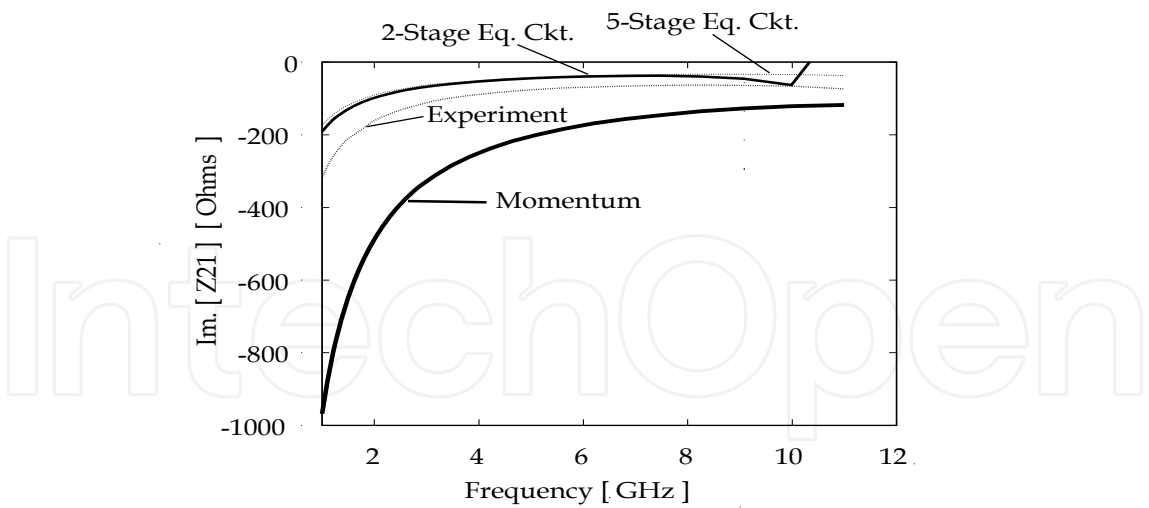


(b) Imaginary part of Z_{11}

Fig. 3. Comparison of simulated Z_{11} -parameters using two-types of equivalent circuit models with Momentum-simulation and measured results



(a) Real part of Z_{21}



(b) Imaginary part of Z_{21}
Fig. 4. Comparison of simulated Z_{21} -parameters using two-types of equivalent circuit models with Momentum-simulation and measured results

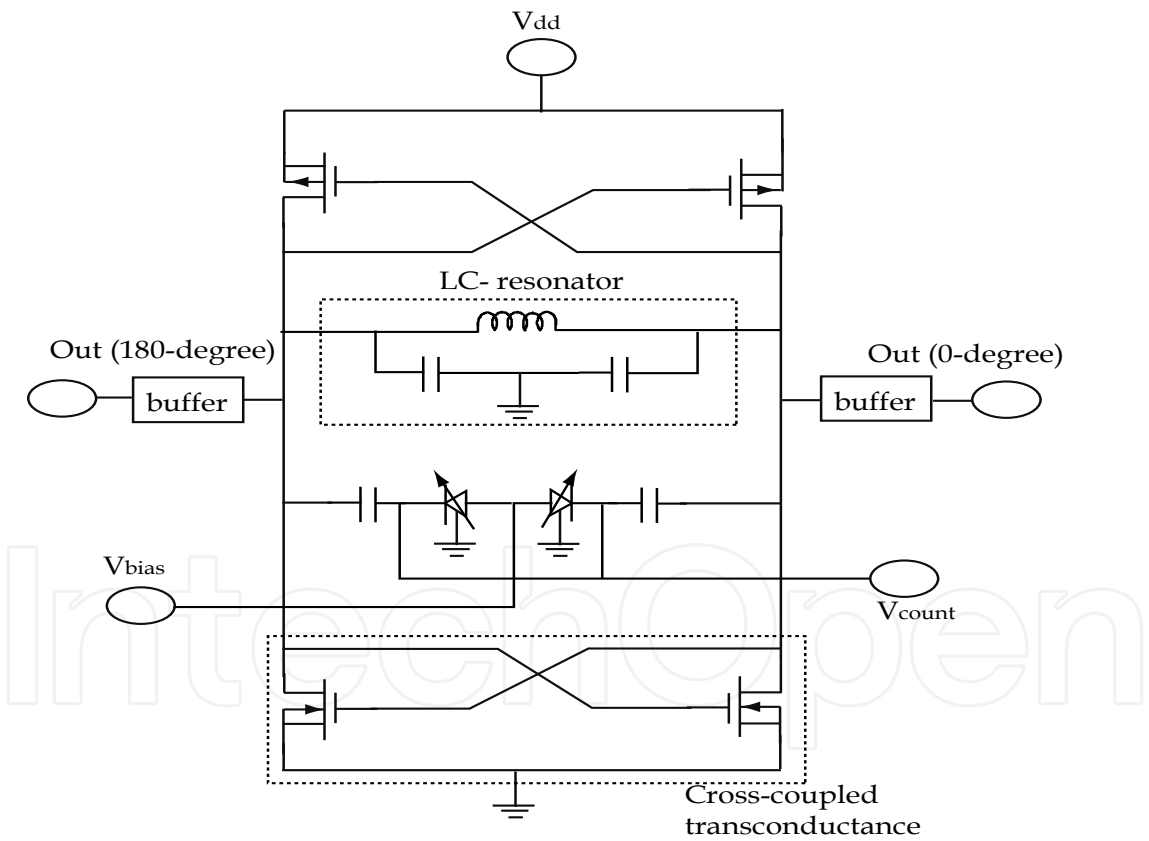


Fig. 5. Schematic of conventional VCO employing LC-resonator

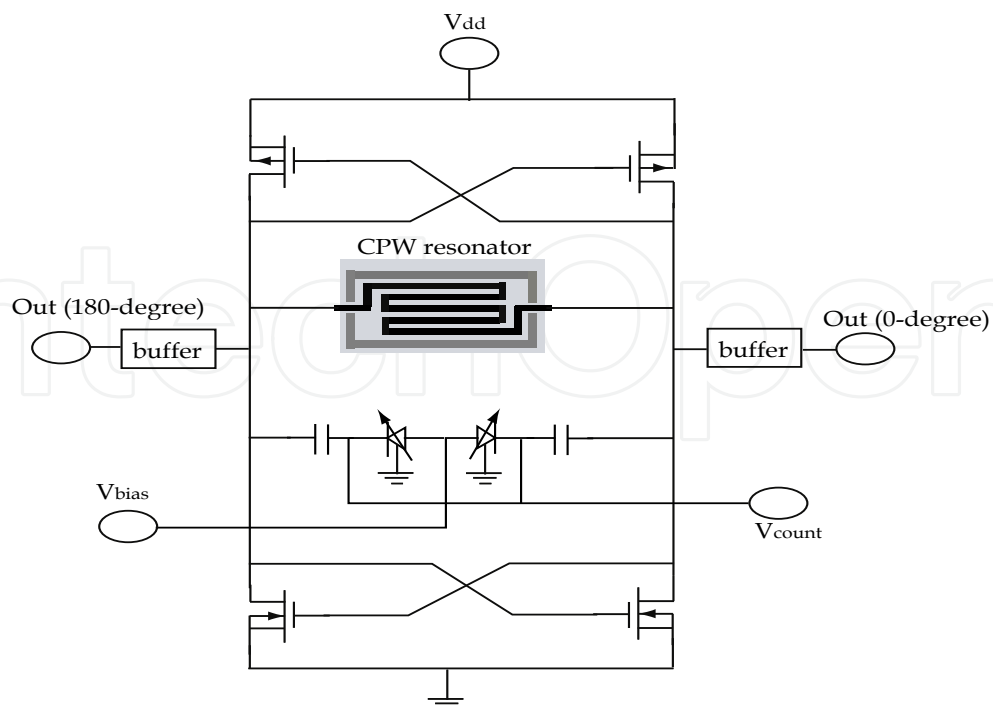
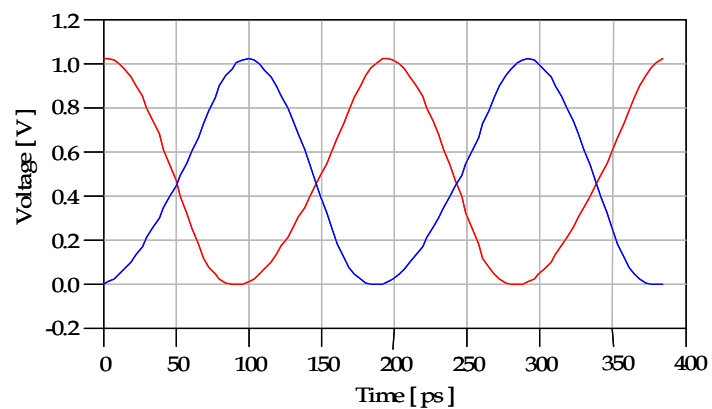
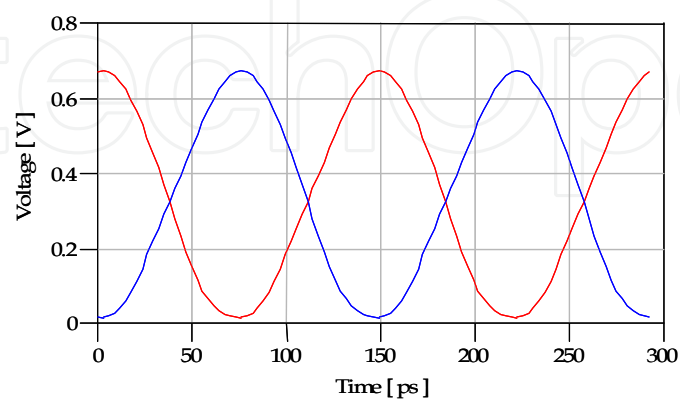


Fig. 6. Schematic of Proposed VCO employing on-chip CPW resonator



(a) Simulation results of VCO using LC-resonator having differential output waveforms



(b) Simulation results of VCO using on-chip CPW-resonator having differential output waveforms

Fig. 7. Output voltage waveforms of designed VCOs

Finally, the Z-parameters which are transformed from S-parameters are compared with measured results and simulation by Momentum in Fig. 3 and Fig. 4, respectively. Here we choose Z-parameters because of the simplicity to illustrate the comparison in closer range in linear scale. In Fig. 3, real and imaginary parts of Z_{11} -parameters are compared where circuit simulation results using the proposed equivalent circuits will reproduce more closely with measured results than the simulation by Momentum. This tendency is also similar in Fig. 4 where real and imaginary parts of Z_{21} -parameters are compared. Up to 7 GHz, both equivalent circuits produce good agreement with the experiment results, therefore in this paper, 2-stage equivalent circuit of Fig. 2(a) is used onwards in ADE simulation to carry out the post-layout simulation of the whole chip of VCO employing on-chip CPW resonator.

3. Design of VCO Using On-Chip CPW Resonator

A conventional VCO (Dai & Harjani, 2003; Hajimiri & Lee, 2004) mainly consists of three parts such as (i) LC-resonator (ii) Varactor (iii) Cross-coupled transconductance circuit as shown in Fig. 5 where the LC tank circuit determines the frequency of oscillation and form the drain loads. Frequency dependant signals at the drains are then 'cross-coupled' to the other devices' gate, which creates a negative impedance of value $-1/g_m$ at the drain terminals. As VCO is usually used in a phase-locked loop (PLL) in a wireless transceiver, it is necessary to have variable frequency, which is measured in terms of frequency tuning range (FTR) corresponding to center frequency. To make the fixed frequency oscillator into a variable frequency oscillator, it is necessary to tune the capacitive load and for this purpose, a voltage-tuned capacitor known as varactor is added into the resonator.

Fig. 5 and Fig. 6 show the schematics of the designed VCOs. In Fig. 5, schematic of LC-VCO is shown and that of using the proposed CPW resonator is shown in Fig. 6. In Fig. 5, the parasitic capacitances of the $1/g_m$ devices will increase the minimum capacitance of the varactor reducing the tuning range of the VCO whereas in Fig. 6, the equivalent capacitance of the varactor and CPW resonator will decrease which results in the higher FTR of the proposed VCO using on-chip CPW resonator which is to be illustrated in Fig. 11.

Fig. 7 shows the post-layout simulation of waveforms of the maximum voltage swing of the designed VCO where the maximum peak voltage of LC-VCO is greater than that of the VCO using on-chip CPW resonator and this is clearly reflected in the performance of the phase noise of the VCO in Table 1 to be discussed later.

4. Fabricated Chips and Measurement Results

We designed, fabricated and measured two VCOs as shown in the schematics of Fig. 5 and Fig. 6, respectively for comparison purpose. However, from onward, we will present the graphs of measured results of the proposed VCO using on-chip CPW resonator only and will summarize the final results of both VCOs in Table 1.

Fig. 8 shows the chip photo of the proposed VCO that employs on-chip CPW resonator. The output of both VCOs is designed with buffer circuits so that it provides good matching with the measurement equipments such a spectrum analyzer. Phase noise of the VCO is measured using a Signal Source Analyzer (E5052B SSA, Agilent Technologies) and keeping the chip inside a shield box. While measuring the phase noise of the VCO, the chip was placed inside a small shield room to protect the phase noise from the effect of the low-

frequencies inference, therefore we designed both VCOs with SMA connector rather than CPW probes because, if we design the VCO with the pads for the CPW coplanar probes, we can not measure inside a shield box.

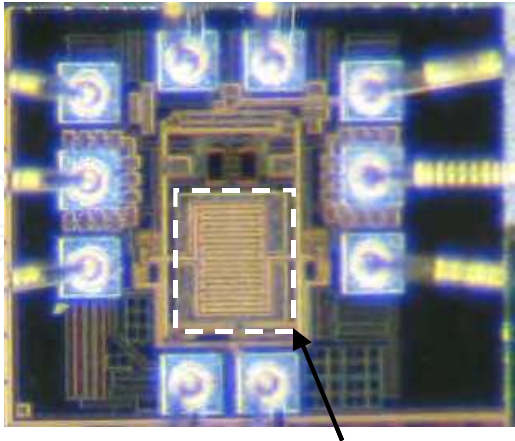


Fig. 8. Chip photograph of designed VCO using on-chip CPW resonator in TSMC 0.18μm CMOS

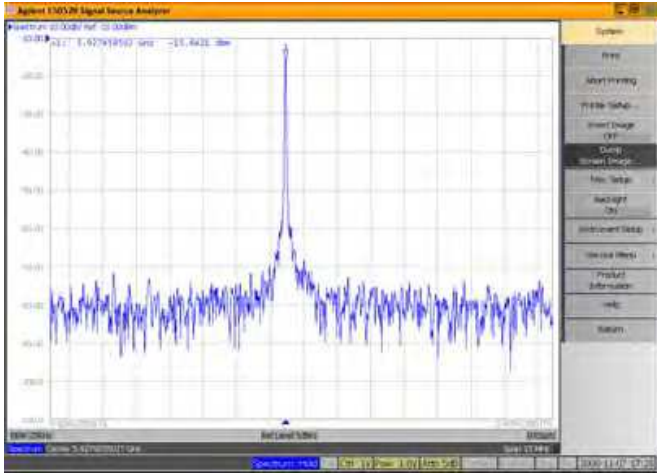


Fig. 9. Spectrum of output power of the VCO employing on-chip CPW resonator measured by SSA

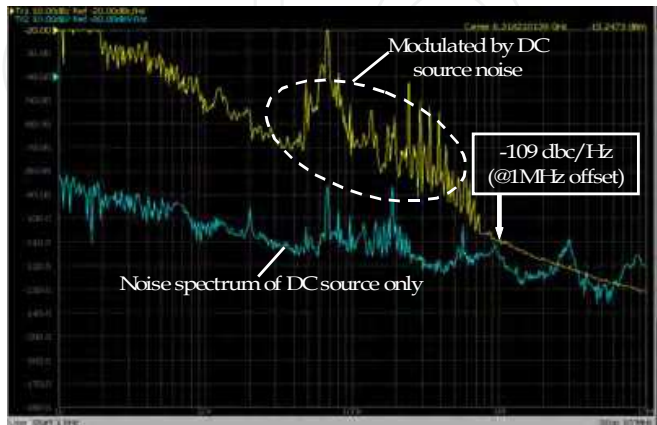


Fig. 10. Phase noise of the proposed VCO using on-chip CPW resonator with noise of DC source only measured by SSA

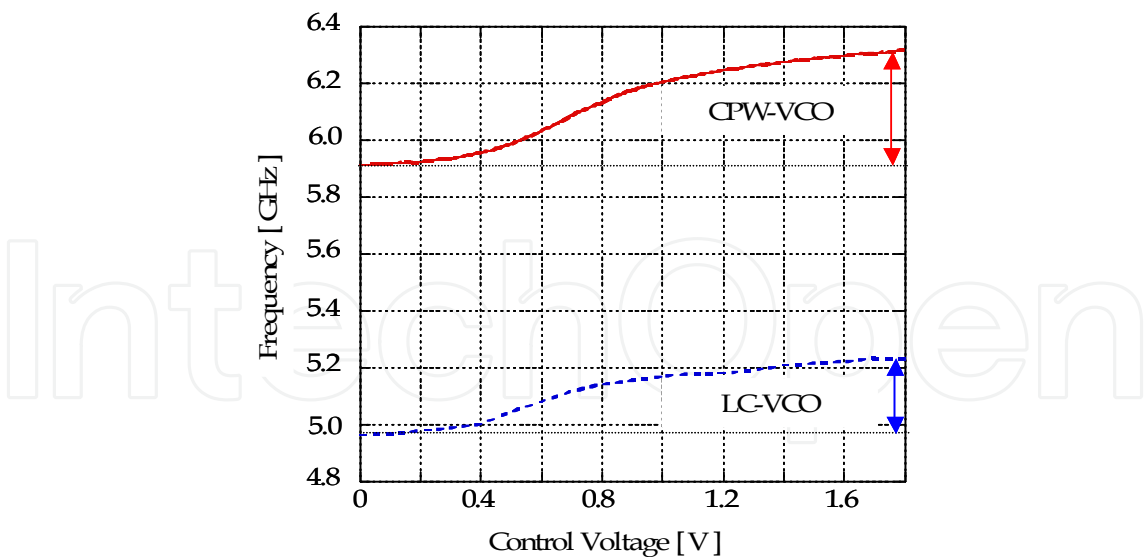


Fig. 11. Measured frequency-tuning range (FTR) showing comparison between FTR of the proposed VCO with that of LC-VCO

	LC resonator	CPW resonator
Center Frequency [GHz]	5.2	5.9
FTR [%]	5.4	10.9
Phase noise [dBc/Hz@1MHz]	-114	-109
Area [m^2]	1.4×10^{-7}	1.1×10^{-7}

Table 1. Comparison of measured parameters between two vcos using lc resonator and on-chip cpw resonator, respectively. [ftr=frequency-tuning range]

The output power spectrum is measured by SSA which is shown in Fig. 9. Fig. 10 shows the measured phase noise of the proposed VCO. The phase noise measurement demands a dc sources free from any low-frequencies noise. Among them, the relatively pure two DC sources can be obtained from SSA but our VCO layout needs three DC sources for biasing. Therefore, we use two DC sources from SSA and a commercial DC source for remaining one. Due to this impure DC source, the spectrum of phase noise below 900KHz-offset frequency in Fig. 10 is affected by noise of the DC source. The long wires that connects the DC source and the chip that placed inside a shield box when completes a ground path with SSA, acts as a inductance and in turn becomes a loop antenna, which is the main reason of the modulated phase noise below 900MHz-offset frequency in Fig. 10. To clarify this issue, we also plotted the noise spectrum of DC source only in Fig. 10 with phase noise of the VCO and it validates the explanation above. Therefore, it is inferred that a pure DC source is inherent to measure the phase noise of a VCO and the wires that connect the DC source and the chip should be as short as possible.

The comparison of measured FTR of the proposed VCO employing on-chip CPW resonator with that of LC-VCO is shown in Fig. 11 where FTR of the proposed VCO has larger FTR than that of LC-VCO. To make the fixed frequency oscillator into a variable frequency

oscillator, varactor is connected as a capacitive load to a resonator. But the parasitic capacitances of the 1/gm devices will increase the minimum capacitance of the varactor reducing the tuning range of the conventional LC-VCO whereas in the proposed VCO, the equivalent capacitance of the varactor and CPW resonator will decrease which results in the higher FTR of the proposed VCO in Fig. 11.

Table 1 shows the comparison of the parameters of the proposed VCO using on-chip CPW resonator with VCO employing LC-resonator. From the table, it is noted that the VCO using CPW resonator has advantages in terms of chip size and frequency-tuning range (FTR). On the other hand, it has slightly poor performance in terms of phase noise but this design technique can be implemented for higher frequency applications whereas in designing a LC-VCO, the self-resonance of inductor prevents its applications beyond that frequency.

5. Application of On-Chip CPW Resonator to Design a Digitally Controlled Oscillator

5.1 Introduction of Digitally Controlled Oscillator (DCO)

Scaling down of CMOS technology and reduction in supply voltage complicates the implementation of RF integrated circuits in deep submicron CMOS process and demands the use of digital-assisted approaches in their circuit implementation (Matsuzawa, 2008). An oscillator, being a critical component of all digital phase locked loop (ADPLL) for future generation wireless transceiver, is necessary to be implemented using digital signals to control its frequency tuning characteristics.

Recently, various types of DCO architectures were proposed and implemented in deep submicron CMOS technology (Staszewski et al., 2005, Fahs et al., 2009). The DCO implemented in ring structure (Fahs et al., 2009) gives poor phase noise performance with high power consumption, and they are, therefore, hardly suitable for multi-GHz wireless applications. In a DCO implemented using a LC-resonator (Staszewski et al., 2005), on-chip inductor (L) is inherent which increases the chip size and in turn, results in high price. In this Section, we will propose a 10bit DCO using on-chip CPW resonator and MIM capacitors instead of the LC-resonator.

5.2 Design, Fabrication, and Experimental Results of 10 bit DCO

The proposed schematic of the designed 10 bit DCO is shown in Fig. 12 where the core of the DCO is similar to the VCO explained in chapter 3 which employed the on-chip CPW resonator instead of LC resonator. Furthermore, varactors are replaced by a capacitor bank made of MIM capacitors which are controlled by 10 bit digital signals so that wide tuning range is realized. Figure 13 shows the chip photograph of the proposed DCO to test the proposed concept of designing a DCO using on-chip CPW resonator. The control pins were wire bonded to a package and the package was placed on a PCB and externally controlled similarly as in the VCO. The output of DCO is designed with buffer circuits to provide a good matching to the measurement equipments. The measured DC power consumed by the DUT was about 75.8 mW at 1.8 V supply, and simulation shows that about 61% of total power was consumed by the buffer circuits only. The exact power consumption of the proposed DCO can be predicted when two separate DC supply source were designed for DCO core and buffer circuits, respectively. Figure 14 shows the one of the signal spectrums measured which verifies the DCO is operating at 5.2 GHz producing the power of -16 dBm.

Phase noise of the DCO was measured similarly as VCO previously. The chip was wire bonded to PCB as shown in Figure 13 and then to SMA connectors to facilitate to measure the phase noise inside the shield box. The digital controls bits are inputted through the digital pads. Figure 15 shows the phase noise of the DCO where the phase noise was to be -114 dBc/Hz (@1 MHz offset frequency).

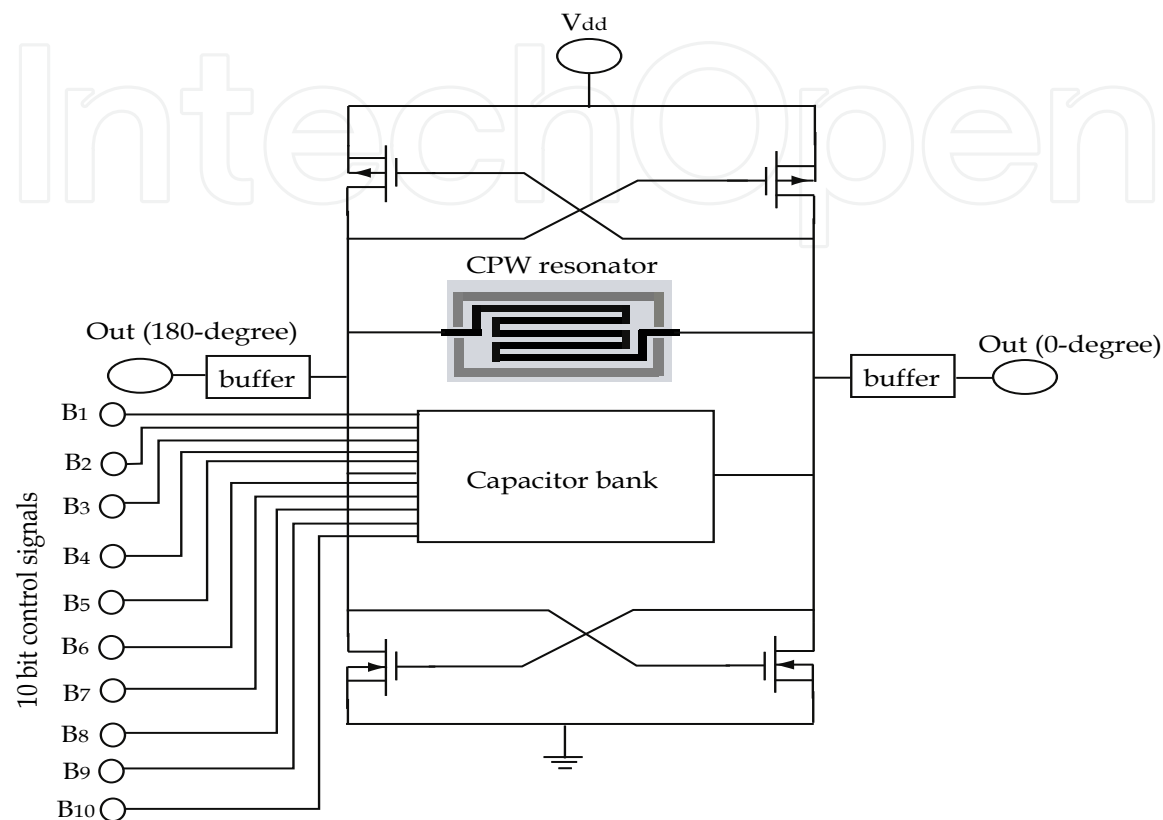


Fig. 12. Schematic diagram of 10 bit DCO using on-chip CPW resonator

We observed some modulated waves from the offset of 100 kHz to 800 kHz, and this is mainly due to the noise introduced along with the digital signals and through the interconnecting cables to the control pins.

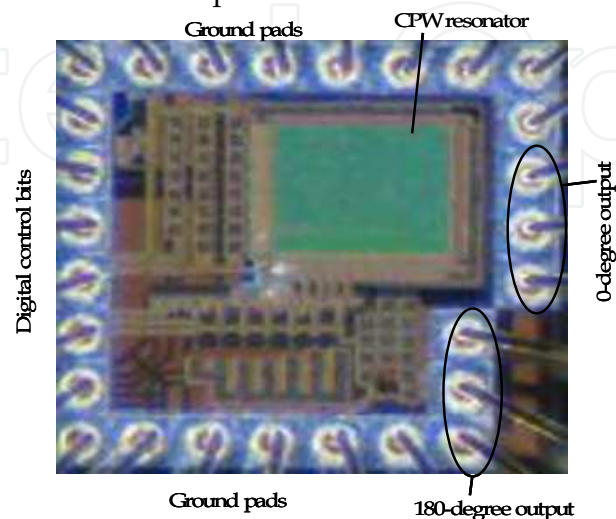


Fig. 13. Schematic diagram of 10 bit DCO using on-chip CPW resonator

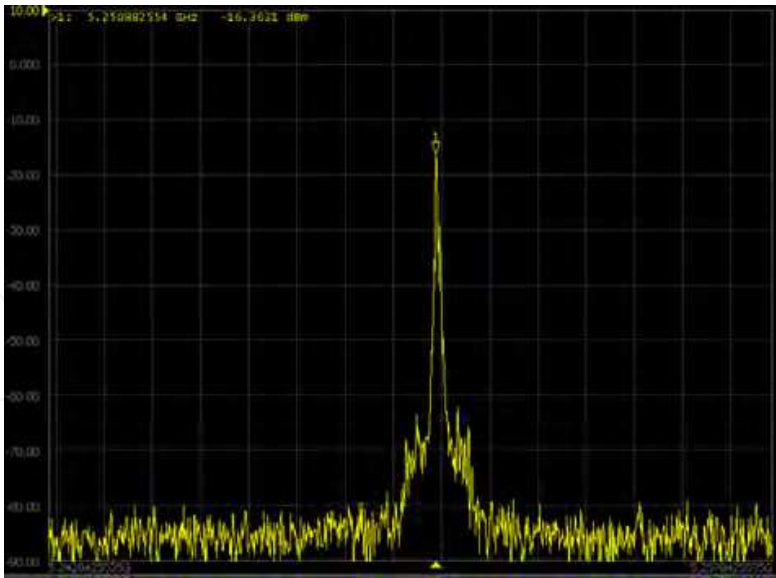


Fig. 14. Measured signal spectrum of 10 bit DCO using on-chip CPW resonator

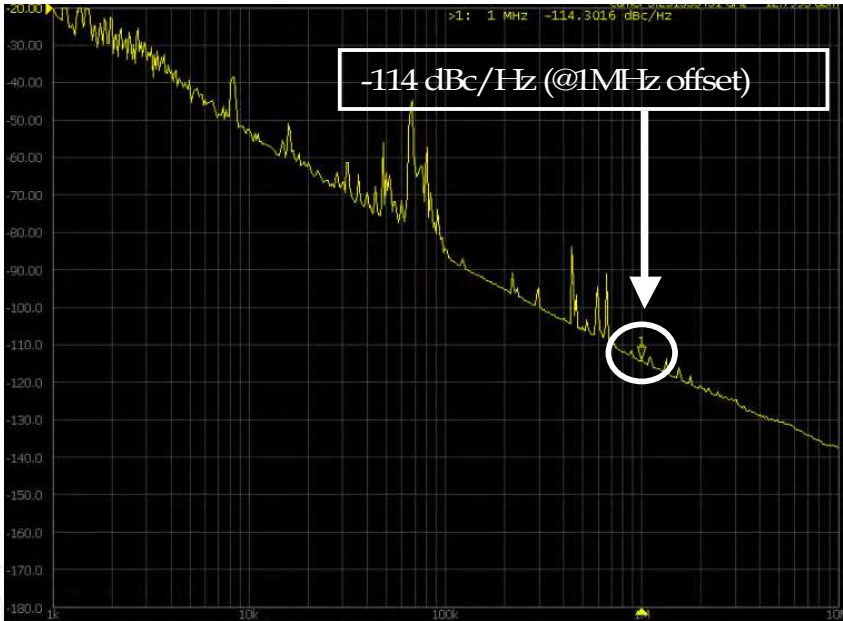


Fig. 15. Measured phase noise of 10 bit DCO using on-chip CPW resonator

	Central freq. [GHz]	Tuning step [kHz]	Power dissipation [mW]	Phase noise [dBc/Hz]	Chip size [mm ²]
Proposed TML DCO	5.0	400	75.8	-114	0.18
LC-DCO	5.0	400	75.6	-115	0.23

Table 2. Comparison of performance of the proposed TML DCO and that of a conventional LC-DCO

Table 1 shows the comparison of the performances of the proposed 10 bit DCO and another one is conventional 10 bit DCO that employed LC resonator which was also designed and tested by the authors to compare the performance with the proposed DCO. In the table, it shows that the proposed DCO has about 30% less chip area than the conventional DCO using LC resonator under similar other parameters.

6. Conclusion

The applications of on-chip CPW resonator was demonstrated to design a VCO and DCO at 5 GHz band. First, we examined the characteristics of the on-chip resonator in meander structure theoretically and experimentally in 0.18 μm CMOS technology. Then, a VCO employing on-chip CPW resonator instead of LC-tank resonator is proposed, designed and fabricated using the same technology and latter a 10 bit DCO. The advantages of employing CPW resonator is the wide frequency-tuning range, and it also saves about 30% of chip size whereas the measured other performance of the proposed oscillators are comparable to that of an oscillator using LC resonator. The design technique is applicable for higher frequencies. Furthermore, the CPW resonator in meander structure can be designed to exploit the vacant space of the layout so the chip size can be further reduced.

An equivalent circuit is developed to reproduce the experimental results of the on-chip CPW resonator whose model parameters are useful to extract RCX (Resistance-Capacitance extraction) of the chip.

7. Acknowledgement

This work was partly supported by a grant of Knowledge Cluster Initiative implemented by Ministry of Education, Culture, Sports, Science and Technology (MEXT), JSPS.KAKENHI (Wakate-B and Kiban-B), and JST-Seeds Excavation (B). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Technologies.

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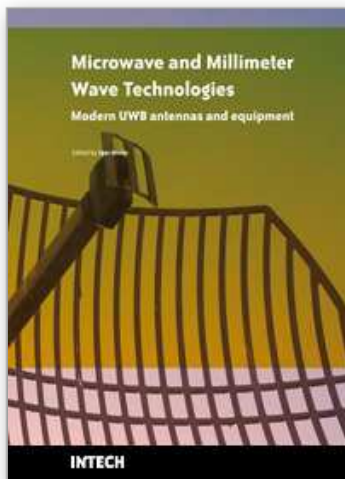
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Microwave and Millimeter Wave Technologies Modern UWB antennas and equipment

Edited by Igor Mini

ISBN 978-953-7619-67-1

Hard cover, 488 pages

Publisher InTech

Published online 01, March, 2010

Published in print edition March, 2010

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

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