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Single-Phase Distributed Generation System Based on Asymmetrical Cascaded Multilevel Inverter

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1. Introduction

The attention and researches on distributed generation systems have been increasing lately and this situation tends to increase more and more. The main reasons for it are the growth of the discussions about environmental issues, the development of renewable energy sources technologies and the imminent possibility of an energy crisis. Power electronics devices are an useful alternative in this process. Power electronics can improve the dynamic response of the distributed generation systems, increase its global efficiency and permit the operation of a large number of systems based on photovoltaic cells, fuel cells or wind turbines. Besides these systems can be also an alternative UPS system if they were not connected to the grid utility.
Generally low power distributed generation systems are connected to the grid utility at low voltage levels ($\leq$13.8kV), which are considerably affected by the presence of nonlinear loads. It means that these systems must be controlled considering harmonics, resonances and other power quality issues. In case of single-phase systems (residential power generation) the attention on those disturbances must be bigger. According to (Jung, Bae, Choi & Kim, 2006), a lot of researches about three-phase systems have been presented but a few number of single-phase systems that operates connected to grid utility or not have been studied. There are five possible obstacles for it:

- The main control concepts of three-phase systems are based on $dq0$ transformation and they can not be applied directly in single-phase systems.
- If they could be applied after some modifications, the $dq0$ components would not be equal to constant values for situations involving harmonics, resonances or unbalance.
- The classical control of exchange power by changes on angle phase and on amplitude voltage is based on sinusoidal steady-state equations.
- The use of reactive power control systems assumes that the reactive power concept has already been defined.

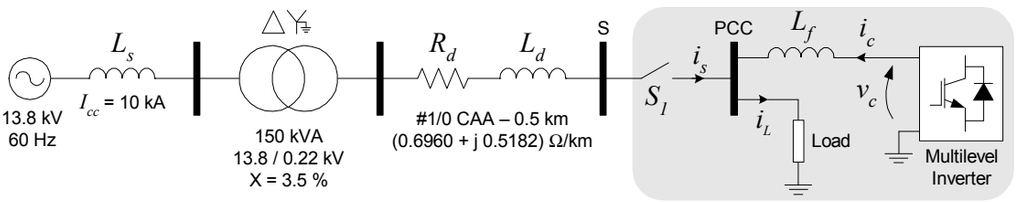


Fig. 1. Grid connection diagram of the DGS.

- High costs of inverters and renewable energy technologies disable a expansion of small distributed generation systems, mainly on single-phase applications.

The proposed distributed generation system (DGS) is connected to a single-phase grid utility and it is supplied by DC voltage sources. Details about it and its operation modes are presented. Simulation and experimental results are also presented. Finally the conclusions about the effectiveness of the proposed DGS are drawn.

2. Distributed Generation System (DGS)

The structure of the proposed DGS consists of an inverter connected to the PCC (Point of Common Coupling) by an inductance (see Figure 1). The inductance L_f could represent a power transformer element or just a first order low pass filter element. Besides, this inductance is responsible for injecting current into PCC throw it and also for attenuating the impact of high frequency components from the inverter output voltage (v_c) on the inverter current (i_c).
The main purpose of the DGS is to supply load continuously even if an abnormal condition (a grid failure or an islanding situation) has occurred. At this point, the DGS has similarities with on-line UPS systems. When there is not an abnormal condition occurring, the DGS operates at the grid-connected mode. The voltage at PCC is held by the grid utility and variations on it could change the operation mode of the DGS. During the grid-connected mode the DGS could supply all the load power (active and nonactive), only a part of it (in addiction to the grid utility supply) or supply all the nonactive power of load (like an active power filter would do). However, this last possibility does not represent exactly a distributed generation scheme. Considering that all the load power is supplied by the DGS, the inverter current (i_c) should be equal to the load current (i_L) and the source current (i_s) should be null. Except when a high di_L/dt occurs and it demands energy rapidly from the grid utility. It happens mainly for nonlinear loads due to the inductance L_f and to the dynamic response limitations of the inverter. If the inverter maximum power is higher than the load power, the DGS could use this spare power for delivering active power to the grid utility. This situation represent a distributed generation scheme and that is why it is not an UPS system.
The DC-links of the inverter could be supplied by an amount of fuel cells, photovoltaic (or solar) cells or both. There is also the possibility of wind turbines supplying them by energy storage in batteries. The energy from those elements should be conditioned by an isolated DC/DC converter before being stored in batteries, capacitors or another storage element. As the primary energy of the DGS comes from DC voltage sources or DC switching power supplies, the proposed DGS could be characterized as an asynchronous (or nonrotational) system.

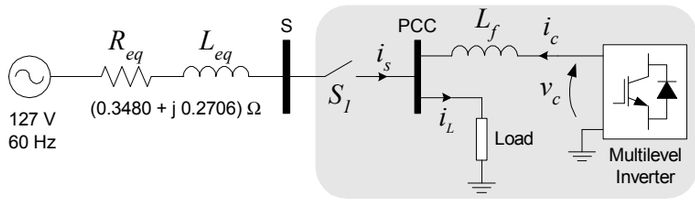


Fig. 2. Grid connection diagram of the DGS with an equivalent circuit of the Area EPS.

2.1 Grid Connection

Figure 1 shows the connection of the multilevel inverter to the PCC by an inductance. The load (or an amount of loads) is also connected to the PCC. According to (*IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, 2003), the complex formed by the load, the inverter and the PCC is called Local EPS (from Electric Power System). The Local EPS stood out in Figure 1 and the switch S_1 (closed or open) determines if the Local EPS is connected, respectively, to the utility grid or not. The utility grid away from switch S_1 is called Area EPS, as in (*IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, 2003). During the grid-connected mode (switch S_1 closed), the DGS operates as a controlled current source connected in parallel to the load. And during the stand-alone mode (switch S_1 open), as a controlled voltage source. Additional information about these modes is available in subsections 3.1 and 3.3.

The considered Area EPS is a common radial power system and consists of a low voltage bus (127/220V) connected to the high voltage bus (13.8kV) by a power transformer in series and a typical distribution line. The grid frequency is 60Hz. The DGS is single-phase and it is connected at the low voltage for representing a possible power exchange among utility grid and residential consumers. At the low voltage bus, the effect of harmonics from nonlinear loads increases and the DG system should attempt this and others disadvantages. The Area EPS presented in Figure 1 could be replaced by its equivalent circuit per phase. Considering a short circuit current equals to 10kA at the high voltage bus (13.8kV) and data available in Figure 1, the calculated equivalent circuit of Area EPS is presented in Figure 2.

2.2 Multilevel Inverter

The utility-interactive inverter of the DGS consists of a multilevel structure with 19 levels produced by an asymmetrical cascaded topology (Daher et al., 2005; Pimentel, 2006; Rodriguez et al., 2002; Silva et al., 2005b). Figure 3 shows the structure of the used inverter. Instead of the symmetrical, the asymmetrical topology produces a high number of levels using a few numbers of switching devices and H-bridge cells. The asymmetrical and symmetrical topologies should be formed by 3 and 9 H-bridge cells, respectively, to allow the same 19 possible levels in the output voltage. For single-phase or low voltage applications, this feature of the asymmetrical topology could be useful due the number and the type of available primary energy sources. There may be different types of sources naturally isolated from each other. For example, the distinct sources could be a group of solar cells, another of fuel cells and other of wind turbines interfaced by converters. That was one of the reasons for choosing the asymmetrical topology. Others are related to power quality and conducted EMI.

The main disadvantages of the used multilevel inverter are: many switching devices; the DC voltages should be isolated from each other; the DC voltage value of the highest voltage H-bridge cell rises rapidly if the numbers of levels increases fairly; and its control system and

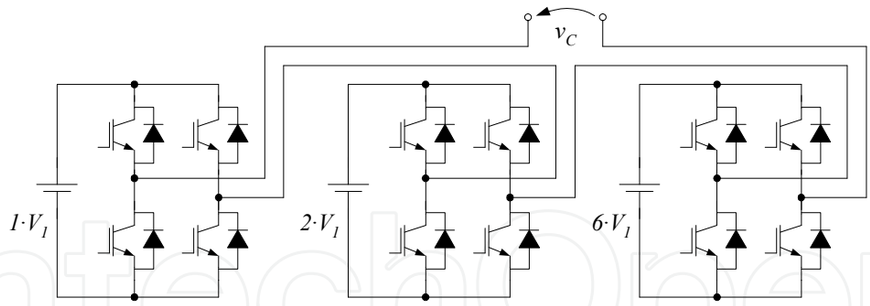


Fig. 3. Asymmetrical cascaded multilevel inverter with 19 levels.

modulation strategy are not simple (Rech & Pinheiro, 2005; Silva et al., 2005a). However the asymmetrical topology produces an output voltage v_c waveform with lower THD than the standard PWM 3-level inverter. Besides, it can operates at low switching frequency. Both advantages can eliminate the second order (or higher) low pass filters (LC filters) that are responsible for reducing the harmonics from the inverter output voltage before connecting it to the PCC. The low Total Harmonic Distortion (THD) of v_c decreases the impact of the switching components on the power quality at PCC and on the current i_c supplied by the multilevel inverter. Reducing the impact on i_c, the magnitude of conducted EMI is also attenuated. Even if a PWM modulation were used by only the lowest voltage H-bridge cell, the conducted EMI would be attenuated due to the lower voltage involved.
The multilevel inverter can achieve high voltage levels using a lot of H-bridge cells that operates at low voltage levels. This characteristic could permit a directly connection of the inverter to high voltage buses without using power transformers (Rodriguez et al., 2002). The configuration of the cascaded topology should be "1:2:6" to produce 19 levels on the inverter output voltage. According to this configuration, the DC voltages of the lowest voltage, of the middle voltage and of the highest voltage cells should be equal to V_1, $2V_1$ and $6V_1$, respectively. The lowest voltage cell (DC voltage equals to V_1) operates with a 3-level PWM modulation strategy to cover all the possible voltage range among levels and to reduce the voltage error. The others cells operate at low switching frequency with a special modulation strategy presented in (Lipo & Manjrekar, 1999; Pimentel, 2006; Rech et al., 2002; Silva et al., 2005a).

3. Operation Modes and Transitions

The state of switch S_1 determines which mode of operation is responsible for controlling the proposed DGS: grid-connected mode or stand-alone mode. However it is necessary two auxiliary control systems for determining the state of this switch and its transitions. These auxiliary systems should determine that the switch must be open if it were closed, and vice versa. The auxiliary control systems of the proposed DGS: an islanding detection scheme; and a procedure for grid synchronization before reconnection. These operation modes and their transitions are represented as a state machine in Figure 4.

3.1 Grid-Connected Mode

During the grid-connected mode, the DGS is able to deliver active power from the Local EPS to the Area EPS and supply all the active and the nonactive power of the load. A suitable inverter current control is very important because the DGS operates as a controlled current

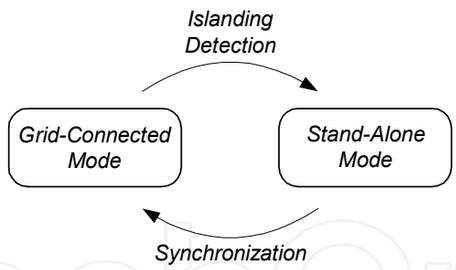


Fig. 4. Operation modes and transitions of the DGS.

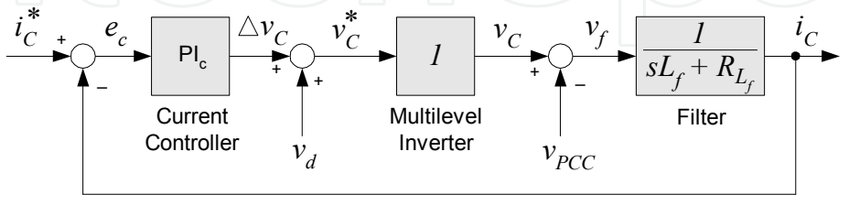


Fig. 5. Inverter current control diagram during grid-connected mode.

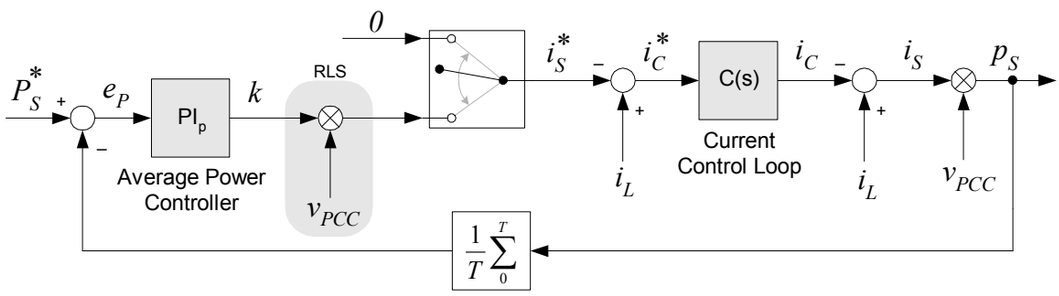


Fig. 6. Source average power control diagram during grid-connected mode.

source. Besides the exchange of active power between Local EPS and Area EPS should result in a source power factor closed to unity. This is achieved by the source average power control.

3.1.1 Current Control

The inverter current control diagram is shown in Figure 5. It is very similar with those used in active power filters. A PI controller with a high time constant is used to guarantee that current error e_c be null at the grid frequency (60Hz). The output of the PI controller (Δv_c) is added to the voltage v_d (a feed-forward action) to elaborate the reference signal of the inverter output voltage $v_c{}^*$. This signal is used by the modulation strategy to create the real inverter output voltage v_c. From variations on v_c it is possible to control the inverter current i_c by the inductance L_f. The voltage v_d could be equal to the PCC voltage or to a sinusoidal signal waveform which frequency is determined by the islanding detection scheme. The reference signal waveform to the inverter current $i_c{}^*$ comes from the source average power control.

3.1.2 Average Power Control

The source average power control diagram is shown in Figure 6. The average value of the source instantaneous power p_s is equal to source active power (i.e., $\overline{p_s} = P_s$). That is why the control is based on $\overline{p_s}$. The source average power control is responsible for regulating P_s and for defining the reference signal waveform to the inverter current ${i_c}^*$. If none active power is delivered to the Area EPS (i.e., ${i_s}^* = 0$), the signal ${i_c}^*$ is equal to the load current i_L and the DGS supplies all the active and nonactive load power. If an amount of extra active power is available for delivering to the Area EPS, the signal ${i_c}^*$ is equal to the sum of the load current i_L with the reference signal waveform of the source current ${i_s}^*$. The reference signal ${i_s}^*$ is obtained from the multiplication of the PCC voltage v_{PCC} with the output average power PI controller k. This multiplication represents a technique called "Resistive Load Synthesis" (RLS) (Nunez-Zuniga et al., 2000; Silva et al., 2005b). The delivering of only active power to the Area EPS is possible because current and voltage have the same waveform in the RLS technique, just like in a resistor. A PI controller with a very low time constant and a low proportional gain is used to guarantee that average power error e_p be null at 0Hz. It is important to notice that the reference source average power P_s^* must assume negative values to permit a correct delivering of active power to the Area EPS (e.g., $P_s^* = -500$W). A procedure to calculate the parameters of the source average power PI controller is also given in (Pimentel, 2006).

3.2 Islanding Detection

An abnormal condition of grid utility should determine that the Local EPS operates disconnected ("islanded") from the Area EPS. That is called islanding and the main islanding situations are grid failure, under/over voltage and under/over frequency. During the grid-connected mode the voltage at PCC is held by the grid utility. If an islanding situation happens the PCC voltage would be uncontrolled, the load current would follow these unintentional changes, the Local EPS could supply wrongly some loads from Area EPS and the inverter current control may be unstable. Besides the DGS should not be controlled at the grid-connected mode anymore, it should be controlled at the stand-alone mode thereafter. An islanding detection scheme is necessary to select the right operation mode and to change the state of switch S_1 for avoiding those related problems with the DGS. The proposed DGS uses an active islanding detection based on an active technique called "Active Frequency Drift with Positive Feedback" (AFDPF) (Jung, Choi, Yu & Yu, 2006). The positive feedback action is responsible for forcing an unstable condition of the PCC voltage.

The basic concept of active islanding detection techniques is to modulate a power system parameter and to measure its corresponding system response (Jung, Choi, Yu & Yu, 2006). Passive islanding detection techniques could failure if there is no power exchange between Local EPS and Area EPS or could generate unintentional islanding situations, which must be avoided. Originally the AFDPF technique presented in (Jung, Choi, Yu & Yu, 2006) introduces a small perturbation at the inverter output current modulating its frequency. The proposed islanding detection scheme modulates also the frequency but introduces these perturbation at the inverter output voltage by the voltage signal v_d. The signal v_d is produced from some data collected by a PLL and a FWD (Fundamental Wave Detector) that are pursuing the PCC voltage (see Figure 7). The PLL and the FWD are presented in (Marafao et al., 2005). The logical signal ISD is high when an islanding situation has been detected.

The frequency of the PCC voltage (f_{PCC}) is used to calculate the chopping factor (cf) as in (1). The initial chopping factor cf_0 is equal to 0.0083264 and it represents the chopping factor

when there is no frequency error. The initial frequency f_{PCC_0} is equal to 60Hz and the gain k_f is equal to 1.0.

$$cf = cf_0 + k_f \cdot \left(f_{PCC} - f_{PCC_0}\right) \tag{1}$$

The chopping factor (cf) is used to determine the distortion factor (d) as in (2). The factor d describes how many higher the frequency distortion (f_d) is than f_{PCC} and it is very important to the positive feedback. If there is a frequency error, the factor d would tend to increase that frequency error and to destabilize the frequency at PCC. It happens continuously and the islanding situation could be detected if the values of under/over voltage and under/over frequency were reached. When there is no frequency error, f_d is equal to 60.05Hz.

$$d = \frac{f_d}{f_{PCC_0}} = \frac{1}{(1 - cf)} \tag{2}$$

The factor d is used to produce the distortion angle (θ_d) from the phase angle of the voltage at PCC (θ_{PCC}) as in (3). The angle θ_{PCC} is manipulated by scaling its range during each half period of f_{PCC}. It results in a change of the rise time of the angle θ_{PCC} as is shown in Figure 8(a). If f_d is higher than f_{PCC}, θ_d would rise faster (a frequency drift up situation) than θ_{PCC} during each half period. Otherwise, it rises slower (a frequency drift down situation).

$$\theta_d = \begin{cases} d \cdot \theta_{PCC}, & \text{if } (0 < \theta_{PCC} \leq \pi) \\ \pi + \left[d \cdot (\theta_{PCC} - \pi)\right], & \text{if } (\pi < \theta_{PCC} \leq 2\pi) \end{cases} \tag{3}$$

The distortion angle (θ_d) and the peak value of the fundamental voltage at PCC (V_{PCC_1}) are used to compose the distortion voltage (v_d) as in (4). Therefore, v_d receives all the modifications produced by the d at θ_{PCC}. It changes the frequency of the distortion voltage waveform on each half-cycle as is shown in Figure 8(b). The distortion voltage (v_d) is added to the output current controller (Δv_c) to produce the reference signal of the inverter output voltage. This action qualifies the DGS for detecting islanding situations even when there is a minimal power exchange between Local EPS and Area EPS.

$$v_d = V_{PCC_1} \cdot \sin\left(\theta_d\right) \tag{4}$$

3.3 Stand-Alone Mode

During the stand-alone mode the Local EPS is disconnected from the Area EPS and the DGS becomes a controlled voltage source that supplies the load. Therefore the main purpose of this operation mode is to keep voltage at the PCC closed to a sinusoidal waveform with a peak voltage equals to $127\sqrt{2}$V ($\equiv$179.605V), a frequency equals to 60Hz and an initial phase angle equals to value of the grid phase angle just before islanding. The inverter must provide an output voltage that is composed by the desired voltage to PCC and by a compensation for the voltage drop across the inductance L_f caused due the load current.

3.3.1 Voltage Control

It is possible to achieve the purpose of the stand-alone operation mode using a control system that regulates the inverter output voltage based on a feedback of the PCC voltage. The voltage control system diagram is shown in Figure 9. It uses a proportional plus resonant controller (P+Ress) instead of the traditional PI compensator for annulling the voltage error e_v at 60Hz. At this frequency, both controllers have different frequency responses. The reason for it is the

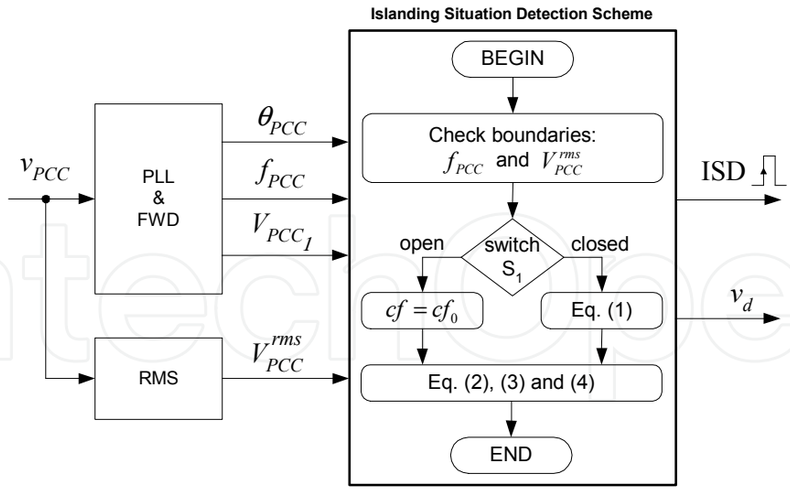
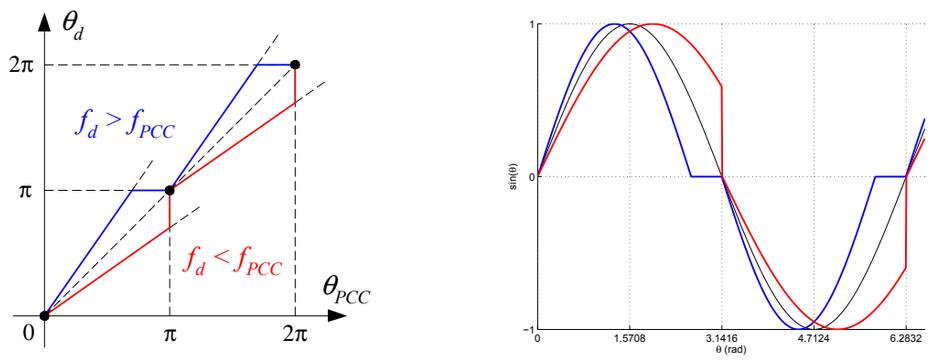


Fig. 7. Data flux of the islanding detection scheme.



(a) (b)

Fig. 8. AFDPF angle (a) and waveform (b) modifications with frequency drift up (blue) and frequency drift down (red).

frequency response of both controllers at 60Hz. The P+Ress controller has a high gain at 0Hz and at 60Hz, while the PI controller has only at 0Hz (Zmood & Holmes, 2003). It means that voltage error e_v at 60Hz could be null if a P+Ress controller were used. This is an attractive characteristic because the reference signal of PCC voltage v_{PCC}^* is a sinusoidal waveform with frequency equals to 60Hz. Others control schemes have been tested to regulate the peak value or the RMS value of the PCC voltage using PI controllers, but they were not so suitable as the control scheme shown in Figure 9 was.

The proportional part of the P+Ress is represented by the gain α_1 and it is responsible for the transient response of the controller. The resonant part is represented by the resonant frequency ω_1 ($2\pi 60$rad/s) and by the gain β_1. At steady-state the output of the resonant part is a sinusoidal waveform at 60Hz with a stable amplitude, that could be faster achieved if the gain β_1 were increased. The P+Ress controller is also known as synchronous controller or

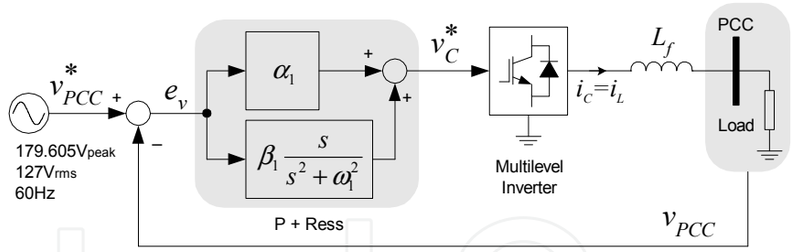


Fig. 9. PCC voltage control diagram during stand-alone mode.

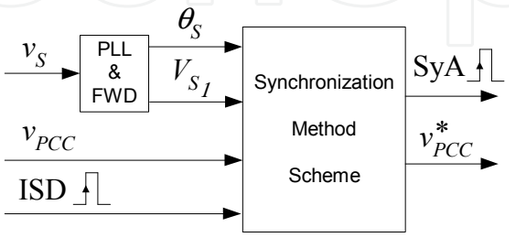


Fig. 10. Data flux of the SM scheme.

stationary frame controller because its resonant frequency is at fundamental (or synchronous) frequency.

3.4 Synchronization

During the stand-alone mode, the voltage at the PCC bar is controlled by the DGS and the voltage at the "S" bar is unknown and independent just because the switch S_1 is open (see Figure 2). The S voltage (v_S) is controlled by the Area EPS operator and it could not be exactly equal to the PCC voltage. If they were not equal in amplitude, in phase angle or in frequency, the switch S_1 should not be closed. That is why a synchronization method (SM) is necessary to adjust the PCC voltage with the purpose of decreasing these differences and reconnecting the Local EPS to Area EPS.

The scheme of the used synchronization method is shown in Figure 10. It is noticed that the SM receives data from the voltage v_S by a PLL (θ_S and V_{S_1}), from the PCC voltage (v_{PCC}) and from the islanding detection method (ISD). The SM process all of these collected data and provides two output signals: the logical signal (SyA) that means "Synchronism Achieved"; and the reference signal of the PCC voltage (v^*_{PCC}). The signal SyA is high if the error voltage were below an acceptable level for some cycles of the PCC voltage and if the signal ISD were high. An association of both logical signals, ISD and Sya, could be used to determine the state of switch S_1.

The elaboration of the reference signal v^*_{PCC} is based on a PLL, which is similar to that used by the islanding detection scheme. When the logical signal ISD is low, the phase angle of v^*_{PCC} (θ^*_{PCC}) is equal to θ_S and the peak voltage of v^*_{PCC} ($V^*_{PCC_1}$) is equal to V_{S_1}. After ISD has became high, θ^*_{PCC} varies cyclically (60Hz) from 0 to 2π with an initial value based on θ_S just before ISD had become high, and $V^*_{PCC_1}$ is equal to $127\sqrt{2}$V. If a stable and nominal voltage has been checked at the "S" bar during the stand-alone mode, the SM starts up. The SM adjusts slowly

(for a few cycles of 60Hz) the peak voltage $V^*_{PCC_1}$ and the phase angle θ^*_{PCC} for equalling them to V_{S_1} and θ_S, respectively.

4. Simulation Results

A model of the proposed DGS has been simulated using the software PSIM. An uncontrolled bridge rectifier with an DC output capacitor supplying a resistor was considered as the load connected to PCC. By it, the performance of the DG system has been tested considering non-linear loads. Table 1 presents the main parameters used by the simulation model.

Parameter	Value	Units
Maximum Output Inverter Voltage $v_{c_{max}}$	$1.15 \times 127\sqrt{2}$	V
Filter Inductance L_f	3.85	mH
Filter Resistance R_f	0.01	Ω
Grid Equivalent Inductance L_{eq}	0.70	mH
Grid Equivalent Resistance R_{eq}	0.35	Ω
AC Input Rectifier Inductance L_{ac}	4	mH
AC Input Rectifier Resistance R_{ac}	0.01	Ω
DC Output Rectifier Capacitance C_{dc}	470	μF
DC Output Rectifier Resistance R_{dc}	$100 - 200$	Ω

Table 1. Parameters of the simulation model

The normal operation (normal condition, without islanding situations) of the DGS during the grid-connected is presented in Figure 11. The DGS is connected to PCC at t=0.3s and it starts to supply immediately all the load current i_L. At t=0.4s the DGS starts to deliver active power to the Area EPS in addition with the load current supply. The reference source active power P^*_s is equals to -500W and it is achieved after t=0.45s. The phase angle of the source current i_s (lagging by 180ř) proves the injecting of that active power into the Area EPS.
The islanding detection scheme was also tested by the simulation model. Figure 12 shows its test results. Considering that there was no power exchange between Local EPS and Area EPS (i.e., $\overline{p_s} \rightarrow 0$), an islanding situation (an abnormal condition) has occurred at t=0.5s. From this point, the PCC voltage waveform v_{PCC} contains all the output inverter voltage harmonics attenuated by the filter inductance. The islanding is detected at t=0.5316s by an under frequency protection. The under frequency level was reached by the variation of f_d on v_d and on v_{PCC} as a result. It validates the islanding detection scheme. After detecting the islanding, the switch S_1 is open at t=0.5316s and the DGS starts to operate at the stand-alone mode. Therefore v_{PCC} is controlled and held closed to its reference signal, a sinusoidal waveform. This procedure guarantees a uninterrupted load supply even during abnormal conditions.
The grid utility supply could be available a few cycles after the failure or it could take a long time. While it not occurs, the DGS operates at the stand-alone mode continuously. During the simulation, the availability of grid utility at the "S" bar was reestablished at t=0.8s but with another phase angle, i.e., its value is different from the phase angle of the voltage at PCC. At t=1.0s the SM starts to run and adjusts the frequency of the PCC voltage for equalling both phase angles θ_{PCC} and θ_S, as is shown in Figure 13. It is noticed that the f_{PCC} and V_{PCC_1} varies slowly along the time due the synchronization adjustments. The signal Δv represents the difference between v_S and v^*_{PCC}.

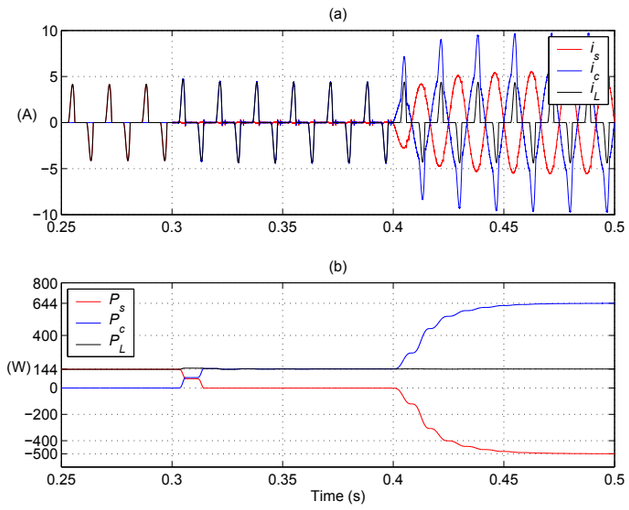


Fig. 11. Current waveforms (a) and active power waveforms (b) during a normal operation of the grid-connected mode.

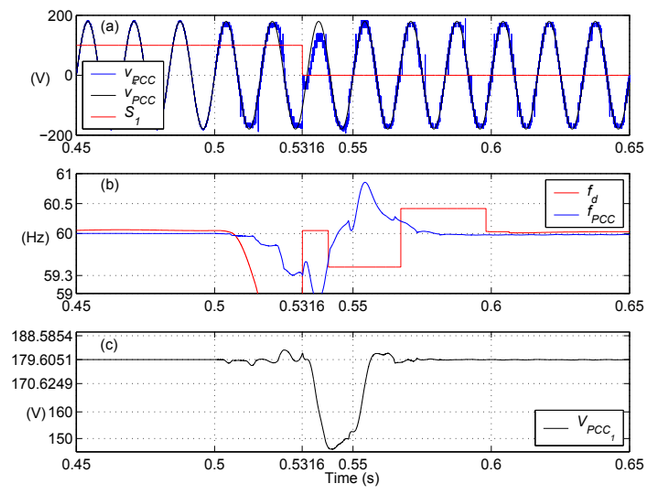


Fig. 12. Islanding detection and stand-alone mode: (a) v_{PCC} (blue), v^*_{pcc} (black) and S_1 gate signal scaled by 100 (red); (b) f_d (red) and f_{PCC} (blue); (c) V_{PCC_1}.

Figure 14 shows the behavior of the Δv and frequency f_{PCC} during the SM adjustments. If they were lower than predetermined levels (e.g., $\pm 1\%$) for five consecutive cycles of 60Hz, the SM allows the reconnection of Local EPS and Area EPS by setting the SyA signal. It happens at t=1.559s and the switch S_1 is closed at this time, as it is shown in Figure 15. After the reconnection, the operation of the DGS returns to the grid-connected mode and the islanding detection scheme is reactivated.

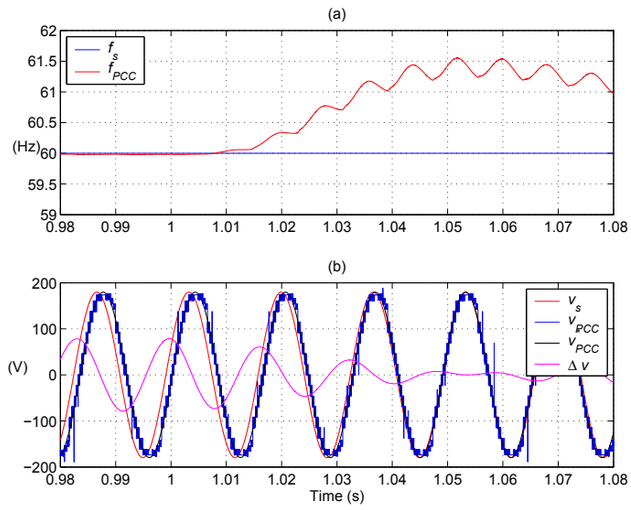


Fig. 13. After $t = 1.0$s, the SM adjusts f_{PCC} (a) for equalling θ_{PCC} and θ_S (b).

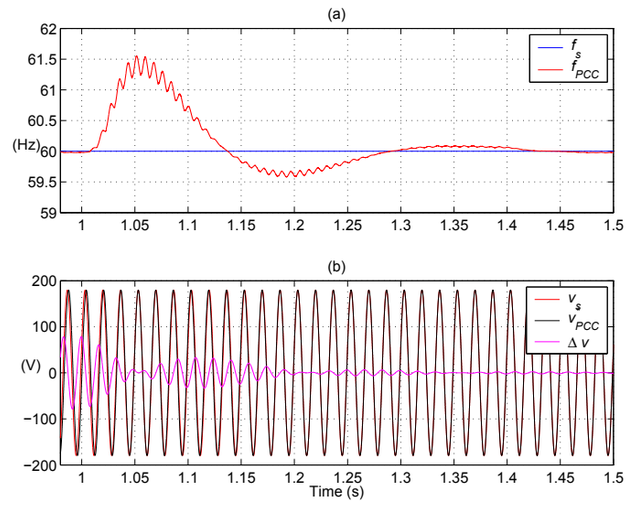


Fig. 14. Behavior of f_{PCC} (a) and Δv (b) during the synchronization adjustments after $t = 1.0$s

5. Experimental Results

A multilevel inverter supplied by isolated DC voltage sources was used to compose a prototype of 1kW for validating the proposed DGS. As the configuration of the asymmetrical cascaded multilevel inverter should be "1:2:6", these DC voltage sources were equal to 22.95V, 45.90V and 137.70V. The lowest voltage cell (22.95V) operates with a 3-level PWM modulation strategy to cover all the possible voltage range among levels and to reduce the voltage error. The highest and middle voltage cells operate at low switching frequency with a special modulation strategy presented in (Lipo & Manjrekar, 1999; Pimentel, 2006; Rech & Pinheiro, 2005; Silva et al., 2005a).

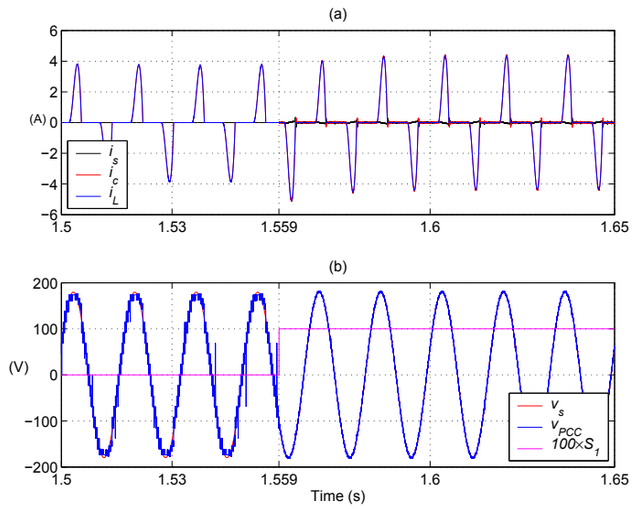


Fig. 15. Reconnection at $t = 1.559$s: (a) current waveforms; (b) voltage waveforms and S_1 gate signal scaled by 100 (magenta).

The DGS prototype is implemented with integrated power modules IRAMX16UP60A as the semiconductor devices and is controlled by a fixed-point DSP TMS320F2812. The prototype parameters are similar to those simulation model parameters presented in Table 1. Additional parameters are: sampling frequency equals to 36kHz; and switching frequency equals to 18kHz. The considered load is also similar to that from the simulation model, i.e., a nonlinear load.

Figure 16 shows the connection of the DGS to PCC and its performance for supplying all the load current during the grid-connected mode. Differently from the simulation model, the DGS prototype does not supply immediately all the load power. It happens gradually for one cycle of 60Hz and facilitates the stability of the prototype operation. However it happens just at the initialization of the prototype. Future load changes must be supplied immediately by the DGS.

After the stabilization of the DGS operation and the current controller, the prototype is able to provide an extra active power to the Area EPS. Figure 17 shows the behavior of the current and voltage waveforms after the active power injection has been started. After that the DGS supplies the load power and the source active power. The source average power controller achieves a stable operation point after two cycles of 60Hz and the source active power is similar with its predetermined reference. Besides the load power supply has not been interrupted and the load current has not been changed. It could be noticed from Figure 17 that the source current has the same waveform of the PCC voltage. This similarity validates the RLS technique and the exchange of only active power between Local EPS and Area EPS.

Figure 18 shows the operation of the DGS during the stand-alone mode. The nonlinear load are still powered by the DGS and the load current i_L waveform is similar to that load current during the grid-connected mode shown in Figures 16 and 17. It is noticed from Figure 18 that the load voltage (at PCC bar, v_{PCC}) is similar to its reference signal v^*_{PCC}, which is a sinusoidal waveform with a frequency of 60Hz and a peak voltage of $127\sqrt{2}$V. This is possible because the voltage control compensates the voltage drop at inductance L_f caused by the load current

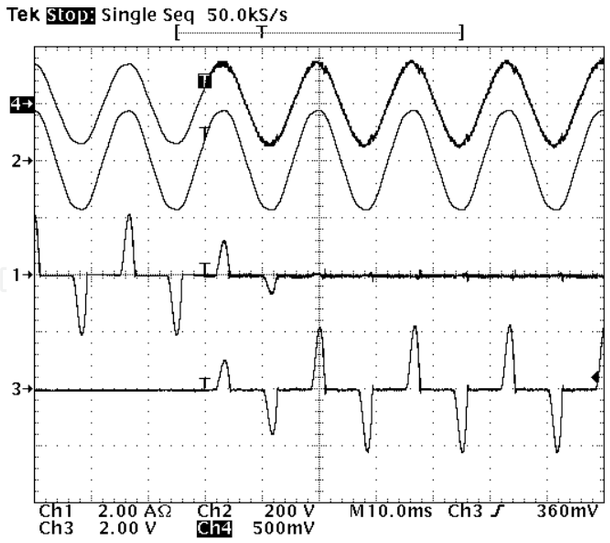


Fig. 16. From top to bottom: v_c (Ch4, 250V/div), v_{PCC} (Ch2, 200V/div), i_s (Ch1, 2A/div) and i_c (Ch3, 2A/div).

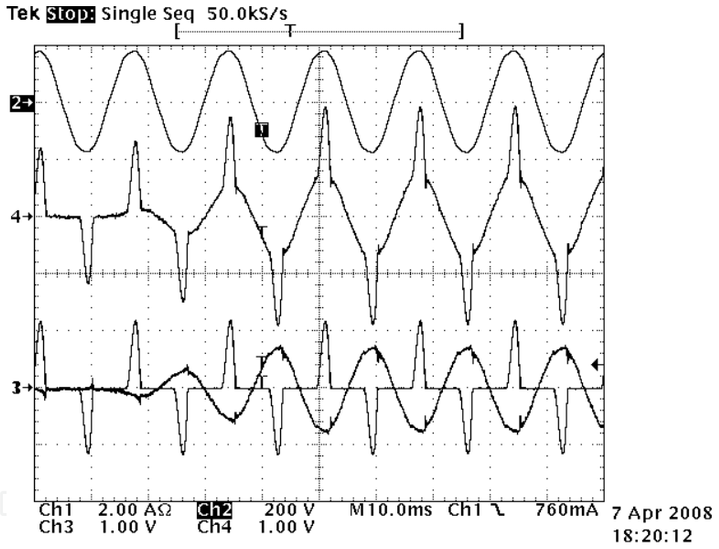


Fig. 17. From top to bottom: v_{PCC} (Ch2, 200V/div), i_c (Ch4, 2A/div), i_L (Ch4, 2A/div) and i_s (Ch1, 2A/div).

i_L. The drop voltage is added to the reference signal v^*_{PCC} by the gain α_1 from the P+Ress controller (see Figure 9). Voltage distortions are also added by α_1 and it allows the DGS to handle with linear and nonlinear loads. All those adjustments are made in the reference signal of the inverter output voltage v^*_c. In Figure 18 the signal v^*_c was adjusted mainly at the peak voltage due to the nonlinear load characteristics. The inverter output voltage v_c follows those adjustments.

High frequency components of the load voltage v_{PCC} in Figure 18 are due to the switching frequency (18kHz) from the lowest voltage cell (V_1) of the multilevel inverter that operates ac-

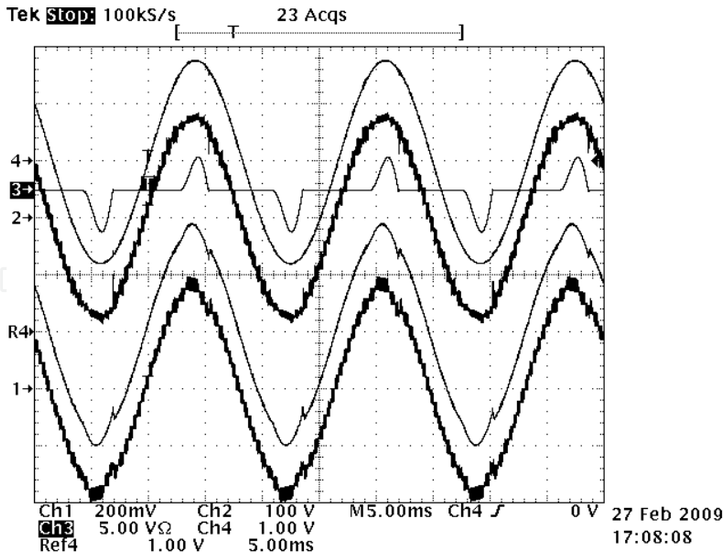


Fig. 18. From top to bottom: v^*_{PCC} (Ch4, 100V/div), i_L (Ch3, 5A/div), v_{PCC} (Ch2, 100V/div); v^*_c (Ref4, 100V/div) and v_c (Ch1, 100V/div).

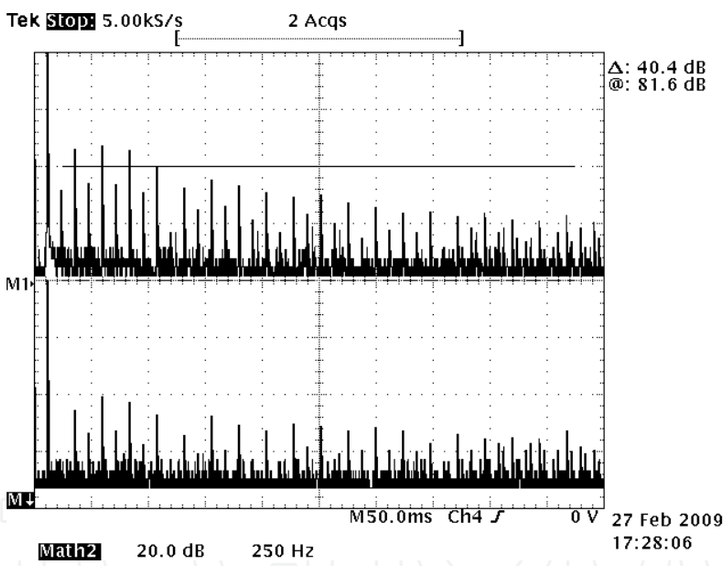


Fig. 19. From top to bottom: FFT of v_c (M1, 20dB/div) and FFT of v_{PCC} (M2, 20dB/div), both voltages from Figure 18.

cording to PWM. Those high frequency components can be also noticed in the output voltage v_c of multilevel inverter. Although both voltages (v_{PCC} and v_c) suggest a poor power quality in a time domain analysis, they are well from the frequency domain point of view. Figure 19 shows the harmonic spectrum of both voltages during the situation presented in Figure 18. The switching frequency carrier (18kHz) and its multiple frequencies are not shown because Figure 19 shows frequency response until 2.5kHz. It is noticed that harmonic amplitudes of voltages v_c and v_{PCC} are, respectively, 35dB lower ($\leq$1.78%) and 40dB lower ($\leq$1%) than fundamental amplitude. The measured THD values were 118% to i_L, 4.1% to v_c and 1.7% to

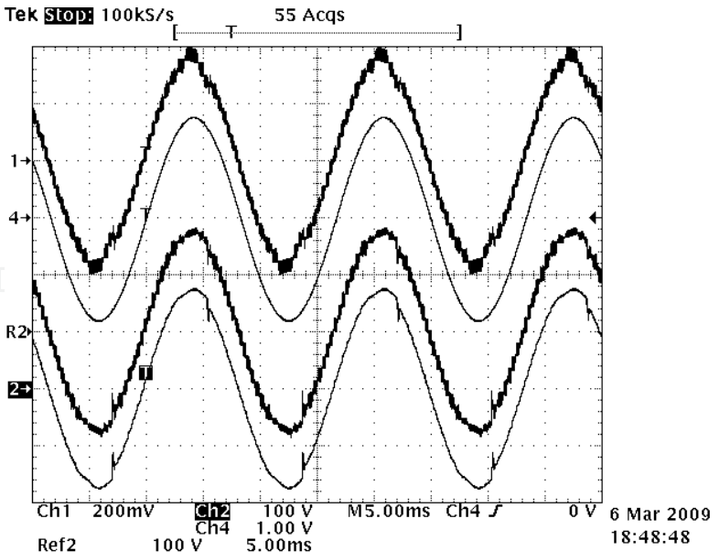


Fig. 20. From top to bottom: v_c (Ch1, 100V/div), v^*_{PCC} (Ch4, 100V/div), v_{PCC} without (Ref2, 100V/div) and with LC filter (Ch2, 100V/div).

v_{PCC}. The low THD of voltage v_{PCC} confirms that the load voltage is similar to a sinusoidal waveform. Besides, it is lower than the maximum THD requirement (5%) presented in (*IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, 2003). In addition, each individual harmonics should be also evaluated for attending (*IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, 2003) in all harmonic requirements.
Considering that a filtered sinusoidal voltage were required at the PCC bar, a LC filter could be used. The design procedure of the elements to that LC filter are relaxed due the low THD of voltage produced by the multilevel inverter. The inductance of the LC filter will be lower in size than that designed for 3-level PWM inverters considering the same capacitance on both cases. Besides a specific modulation strategy that decreases the amplitude of some harmonics (e.g., Selective Harmonic Elimination) may be also used. As the switching frequency is 18kHz, a cut-off frequency closed to 5kHz could be chosen. Considering an inductance L_f equals to 3.85mH (same value of Table 1) and a capacitance C_f equals to 330nF, the natural resonance frequency of LC filter (without load) is equal to 4.46kHz. Figure 20 shows the filtered load voltage for these design values. It is noticed that the high frequency components have been attenuated and the load voltage is more similar to its reference signal.
Figure 21 shows the frequency response of voltage v_{PCC} using and not the designed LC filter. With only the L filter, the switching frequency carrier can be noticed at 18kHz and its multiple at 36kHz. Using the LC filter, they have been attenuated by 20dB at least. By the way, frequency components closed to resonance frequency of LC filter have been fairly increased. It has indicated that the damped resonance frequency was approximately 3.75kHz. The THD of load voltage was equivalent on both cases (≈2%) because low frequency harmonics are more significant to THD evaluation than high frequency harmonics.

6. Conclusion

A proposal of a single-phase distributed generation system with the ability to handle linear and nonlinear loads is presented. Details about the utility-interactive multilevel inverter, grid

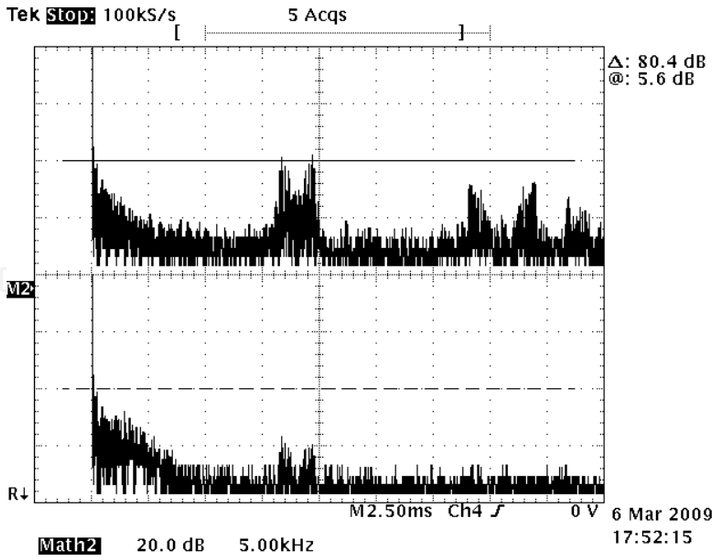


Fig. 21. From top to bottom: FFT of v_{PCC} without (M2, 20dB/div) and with LC filter (Ref2, 20dB/div), both voltages from Figure 20.

connection, voltage levels and operation modes have been described. Concepts of the control schemes used by the DGS have been discussed. Simulation results have been presented for illustrating those concepts and facilitating a prototype model design.

A prototype of the proposed DGS has been implemented and it operates based on a fixed-point DSP TMS320F2812. The validity of the proposed DGS during the grid-connected mode and the stand-alone mode has been proved by the experimental results. The current controller of the grid-connected mode is based on a PI compensator. During the experimental tests, it was noticed that this type of controller has not a wide range of possible operation points and it could not be efficient even if it were stable. The initialization issue could be solved using another type of current controller, probably a nonlinear type. The authors are still working on this issue and on the attempt to get additional experimental results from the prototype.

The similarity between voltage v_{PCC} and its reference signal v^*_{PCC} turns easier to validate the effectiveness of the proposed synchronization method. All the adjustments for decreasing the difference between voltages v_{PCC} and v_S are made by the reference signal v^*_{PCC}. This procedure seems to be less difficult to test than that used by the proposed islanding detection scheme.

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Distributed Generation

Edited by D N Gaonkar

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In the recent years the electrical power utilities have undergone rapid restructuring process worldwide. Indeed, with deregulation, advancement in technologies and concern about the environmental impacts, competition is particularly fostered in the generation side, thus allowing increased interconnection of generating units to the utility networks. These generating sources are called distributed generators (DG) and defined as the plant which is directly connected to distribution network and is not centrally planned and dispatched. These are also called embedded or dispersed generation units. The rating of the DG systems can vary between few kW to as high as 100 MW. Various new types of distributed generator systems, such as microturbines and fuel cells in addition to the more traditional solar and wind power are creating significant new opportunities for the integration of diverse DG systems to the utility. Interconnection of these generators will offer a number of benefits such as improved reliability, power quality, efficiency, alleviation of system constraints along with the environmental benefits. Unlike centralized power plants, the DG units are directly connected to the distribution system; most often at the customer end. The existing distribution networks are designed and operated in radial configuration with unidirectional power flow from centralized generating station to customers. The increase in interconnection of DG to utility networks can lead to reverse power flow violating fundamental assumption in their design. This creates complexity in operation and control of existing distribution networks and offers many technical challenges for successful introduction of DG systems. Some of the technical issues are islanding of DG, voltage regulation, protection and stability of the network. Some of the solutions to these problems include designing standard interface control for individual DG systems by taking care of their diverse characteristics, finding new ways to/or install and control these DG systems and finding new design for distribution system. DG has much potential to improve distribution system performance. The use of DG strongly contributes to a clean, reliable and cost effective energy for future. This book deals with several aspects of the DG systems such as benefits, issues, technology interconnected operation, performance studies, planning and design. Several authors have contributed to this book aiming to benefit students, researchers, academics, policy makers and professionals. We are indebted to all the people who either directly or indirectly contributed towards the publication of this book.

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