We are IntechOpen, the world's leading publisher of Open Access books
Built by scientists, for scientists

6,900
Open access books available

185,000
International authors and editors

200M
Downloads

154
Countries delivered to

Our authors are among the

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS
BOOK CITATION INDEX
INDEXED

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

Templated Si-based nanowires via solid-liquid-solid (SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode, synthesis, morphology control, characteristics, and electrical transport

Jae Ho Lee and Robert E. Geer
College of Nanoscale Science and Engineering
University at Albany, SUNY
USA

1. Introduction

The 'scaling down' of device and interconnect features in CMOS technology to the deep sub-100 nm regime has motivated substantial research focusing on the development of nanoscale building blocks formed via self-assembled or 'bottom-up' synthesis to complement prevailing lithographic or 'top-down' CMOS processing. Examples of such nanoscale building blocks include metallic and semiconducting nanowires or nanobelts, carbon nanotubes and, most recently, n-layer graphenes. In particular, one-dimensional (1-D) nanostructures have attracted much attention because of their unique electrical, optical, mechanical and thermal properties and their potential utility in a wide variety of nanoelectronic and optoelectronic applications. Non-carbon 1-D nanomaterials fabricated from bottom-up synthesis can be used as fundamental building blocks for nanoscale devices and circuits and may have the potential to replace certain, conventional top-down processes. In particular, silicon nanowires (SiNWs) may be an attractive alternative to conventionally processed Si transistors if their intrinsic self-assembly can be harnessed to obviate the need for complex lithographic techniques for device fabrication. In addition, SiNWs can potentially function as both the switch (i.e. transistor) and local interconnect (e.g. metal silicide nanowire) to form an inherently integrated nanoelectronic system – potentially on the same self-assembled nanostructure (Morales *et al.* 1998; Lu *et al.* 2007; Colli *et al.* 2007; Wu *et al.* 2004). Recent research has demonstrated that Si-based silicide nanowires may yield performance superior to conventional Cu interconnects at sub 10-nm wire widths which highlights the excellent potential for SiNW-based systems (Wu *et al.* 2004; Zhang *et al.* 2000; Kim *et al.* 2005; Kim *et al.* 2003). And since NiSi has been shown to be a good electrical contact material for gate, source and drain in Si CMOS (Lavoie *et al.* 2003; Kittl *et al.* 2003; Morimoto *et al.* 1995), NiSi nanowires, in particular, comprise an attractive nanoscale building block material (Wu *et al.* 2004).

Currently, several methods are available to synthesize silicon nanowires including laser ablation (Morales *et al.* 1998; Zhang *et al.* 1998), physical vapor deposition (Zakharov *et al.*

2006), thermal evaporation (Yu *et al.* 1998), and chemical vapor deposition (Westwater *et al.* 1997; Cui *et al.* 2001; Hochbaum *et al.* 2005). In the literature these methods have been roughly categorized according to the underlying growth modes described, respectively, as solid-liquid-solid (SLS) growth (Paulose *et al.* 2003; Yan *et al.* 2000), vapor-liquid-solid (VLS) growth (Wagner *et al.* 1964; Givargizov *et al.* 1975), and oxide assisted growth (OAG) (Zhang *et al.* 2001a; 2001b; Zhang *et al.* 2003).

For eventual technological impact it is essential to understand the fundamental processes by which SiNWs are synthesized as well as develop approaches to tailor the functionality of SiNWs through post-growth processing. *This chapter reviews recent novel research results in both areas regarding SiNW-based materials.* Section 2 presents a brief overview of the fundamental growth mechanisms of SiNWs. Sections 3 and 4 describe the experimental methodology for SiNW growth and the details of SLS and VLS SiNW synthesis, respectively, used for the research presented here. Section 5 details the utilization of post-growth processing SiNWs in the formation of conductive core-shell nanostructures. This includes detailed electrical transport testing and modeling. Section 6 reviews the recent observation of a novel SLS-based SiNW growth mode in which nanowire growth is preferentially initiated at oxide-meditated etch pits in the crystalline Si wafer substrate. Lastly, Section 7 presents a brief summary of the work described in this chapter and highlights opportunities for future research and development.

2. Growth Mechanisms

The solid-liquid-solid (SLS) growth approach is a relatively straightforward technique to synthesize silicon nanowires because it does not require a gas phase precursor such as SiH_4 or $SiCl_4$. Via the SLS process, as shown in Fig. 1, silicon nanowires can be directly grown on a silicon substrate which acts as the silicon source (Paulose *et al.* 2003). In the SLS process a catalyst is deposited on a single-crystal silicon substrate. The annealing of the catalyst-deposited Si substrate results in metal-silicon alloy nano-droplet formation. Continuous diffusion of silicon atoms from the substrate to the droplet at elevated temperatures causes saturation of silicon atoms inside the alloy droplet which leads to precipitation of silicon at the surface of the droplet. The surface Si precipitate forms a Si growth front resulting in nanowire formation from the catalyst because of a negative temperature gradient at the droplet surface (e.g. due to a gas flow) (Paulose *et al.* 2003).
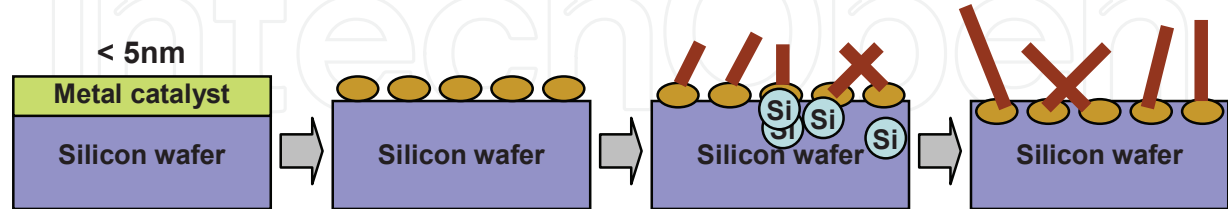

Fig. 1. Schematic representation of solid-liquid-solid (SLS) nanowire growth.

The vapor-liquid-solid (VLS) growth mechanism is widely cited method for nanowire synthesis. It utilizes silane (SiH_4) or $SiCl_4$ instead of a bare silicon wafer for the silicon source, or a laser ablated Si-metal catalyst target (Morales *et al.* 1998; Chen *et al.* 2002). The VLS growth mode was first described in detail decades ago (Wagner *et al.* 1964). A metal catalyst (Au in our experiments) is used in VLS growth as favored sites for absorption of the gas phase precursor. As temperature increases, the thin Au catalyst films break into nano-

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   169

scale droplets above the eutectic temperature and Au-Si alloy nanodroplets are formed that supersaturate upon continued exposure to the precursor gas, resulting in the precipitation of the solid nanowire, shown in Fig 2. In contrast to SLS growth, the alloy clusters can generally be observed at the tips of the wires.
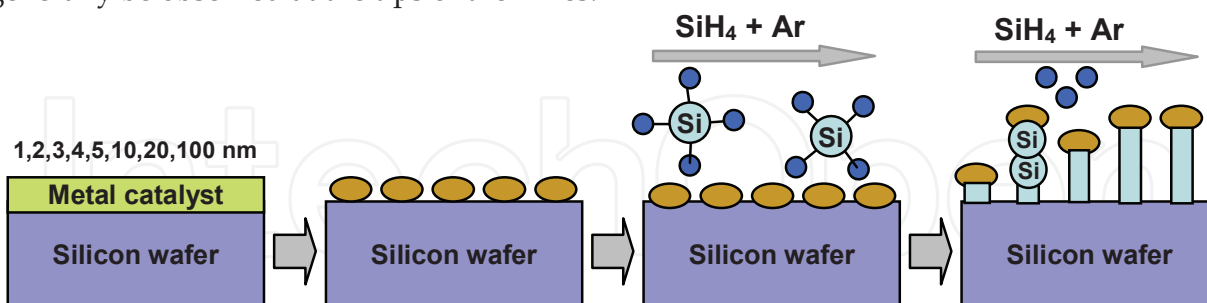

Fig. 2. Schematic representation of vapor-liquid-solid (VLS) nanowire growth.

In contrast to the SLS and VLS SiNW growth modes, SiNW synthesis via oxide assisted growth (OAG) is induced by the presence of silicon oxide instead of a metal catalyst. During the process Si-rich oxide clusters prefer to form Si-Si bonds among one another while oxygen-rich silicon oxide cluster prefers to form Si-O bonds with other oxygen rich SiO_x clusters (Zhang *et al.* 2001a; 2001b; Zhang *et al.* 2003). Highly reactive silicon atoms in the deposited silicon-rich oxide clusters are strongly bonded to the silicon substrate. In the same cluster, exposed non-bonded, reactive silicon atoms exposed to the vapor phase act as nuclei for adsorption of additional reactive silicon oxide clusters (Zhang *et al.* 2003). The result is the formation of a self-assembled Si-rich oxide growth front exhibiting a wire-like morphology.

3. Experimental Methods

For the SiNW synthesis described in this chapter p-type (100) and (111) silicon wafers with electrical resistivity in the 1-20 Ω•cm range were used. Wafers were cleaned with diluted hydrofluoric acid (5%) to remove the native oxide layer and ultrasonicated in acetone to remove organic contamination. The cleaned samples were immediately loaded into a physical vapor deposition (PVD) chamber (evacuated to 5×10^{-7} torr) for sputtering of a Au catalyst film with a thickness of 4 nm for SLS growth. For VLS nanowire growth, a Au catalyst film was deposited on the Si substrate with a thickness that varied from 1-100 nm. Following Au deposition the silicon samples were placed inside an annealing chamber. The annealing chamber was evacuated to a base pressure of approximately 5 Torr and backfilled with high purity (99.999%) Ar gas. The total pressure of the system was then raised to atmospheric pressure through an Ar gas flow. For SLS nanowire growth, the Au-deposited Si samples were annealed at 1000 °C (30 minute ramping time) under Ar (also 99.999 % purity) gas flow at 2,000 sccm. The annealing duration, as shown in Fig. 3, was varied from 10 minutes to 120 minutes after the temperature ramp to investigate the effect of annealing time on the Si nanowire diameter, length, and overall morphology.
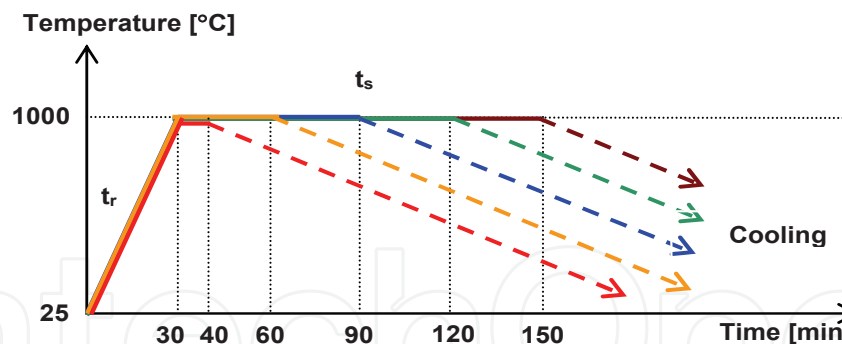
Fig. 3. Annealing duration conditions for SLS growth.

To investigate the SLS SiNW synthesis process, various experimental parameters including Ar gas flow rate and sample position within the chamber were varied. Au-deposited samples were positioned at various points from a lower temperature region within the chamber near the inlet of Ar gas (as compared to the center of the annealing chamber). Early stages of SLS SiNW growth were observed with a shorter annealing duration (typically, below 15 minutes – see Section 6). The temperature inside the oven could be reduced by utilizing an Ar flow with 2,000 sccm when the oven heater is turned off; however, there was a latent annealing duration of approximately 8 min while temperature cooled to ~ 800 °C. To eliminate this unnecessary duration and to enable investigation of the early stages of nanowire growth, 20,000 sccm of Ar was flown inside the chamber, which quenched the growth relatively quickly. Vapor-liquid-solid (VLS) SiNW growth was also investigated to optimize growth rate and diameter distribution. The Au catalyst film thickness was varied from 1 to 100 nm in thickness. Likewise, an optimized VLS SiNW growth rate in the reactor was achieved at a temperature of 500 °C.

For core-shell metal and metal-silicide wire structures surface metallization of SiNWs utilized nickel and the tungsten. Metal deposition and subsequent thermal processing was carried out for as-deposited SiNWs to investigate surface silicide formation. Nickel was deposited on the nanowires via e-beam evaporation (calibrated for an effective blanket film thickness of 150 nm) on SLS and VLS SiNWs. Tungsten was deposited on VLS SiNWs with 2 nm and 4 nm thickness likewise using an atomic layer deposition (ALD) process. Nickel deposited SiNW samples were annealed using a rapid thermal annealing system at 550 °C for 5 min (for SLS, VLS nanowire samples) and at 600 °C for 5 min (for SLS nanowire samples) with a 10 min ramping time to compare resultant SiNW morphologies (subsequently investigated by scanning electron microscopy (SEM)).

Metal-coated SiNWs and as-grown SiNWs were dispensed on metal-patterned Si wafers to carry out two-point and four-point electrical conductivity measurements. Electrical contacts were formed using direct-write Pt electrode deposition within a dual-beam focused ion beam SEM (FIB-SEM). Structural and compositional properties of these wires were analyzed using scanning electron microscopy (SEM), energy dispersive x-ray spectroscopy (EDS), and transmission electron microscopy (TEM).

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport 171

4. Synthesis of Silicon Nanowires

4.1 Solid-liquid-solid (SLS) growth

Scanning electron microscopy (SEM) micrographs of typical SLS SiNWs synthesized for various-length anneals at 1000 °C are shown in Fig. 4. The furnace temperature was ramped to 1,000 °C for 30 min under 2,000 sccm Ar flow. After the ramp the furnace temperature was held constant for durations ranging from 10 minutes to 120 minutes. The effects of SLS-growth annealing duration have been reported (Lee *et al.* 2008). An approximately bimodal diameter distribution was observed. In the previous work (Lee *et al.* 2008), variation of the anneal duration and Ar gas flow rate served to quench the SiNW growth and also served to coarsely regulate nanowire diameter. This preliminary conclusion follows from the basic SLS growth mechanism if high Ar flow rates (~ 20,000 sccm) are sufficient to reduce the temperature at the alloy droplet below that necessary for SiNW growth.
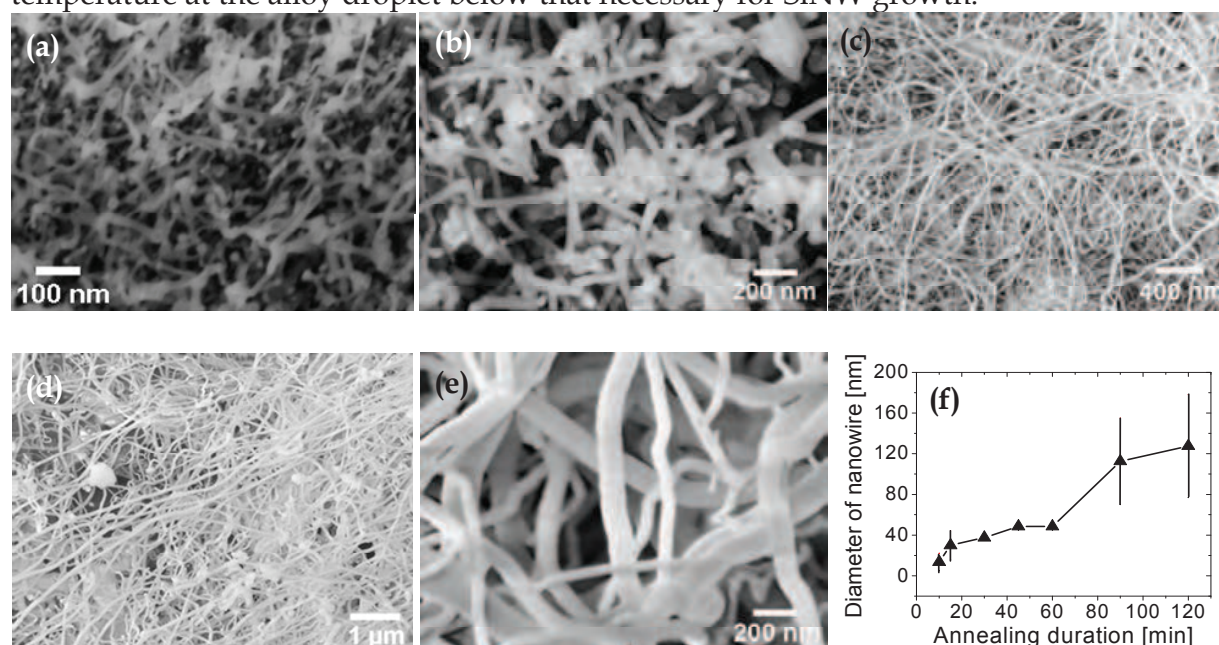

Fig. 4. SEM micrographs of SiNWs synthesized at 1000 °C for anneal durations of (a) 10 min, (b) 15 min, (c) 45 min, (d) 90 min, (e) 120 min. Diameters ranged from 5 nm to 178 nm. (f) Dependence of annealing duration on SLS nanowire growth (Lee *et al.* 2008).

Transmission electron microscopy (TEM) was used to carry out compositional and structural analyses of SLS nanowires (Fig. 5(a)). Nanowires were detached from the initial silicon wafer using ultrasonication in a methanol solution as described above. A selected-area electron diffraction (SAED) pattern (Fig. 5(b)) was acquired from an individual SiNW and indicated a locally amorphous structure. The EDS spectra of as-deposited SiNWs on highly oriented pyrolytic graphite (HOPG) substrates indicated the presence of oxygen (Fig. 5(c)) and implied that the nanowires are likely SiO_x in nature, consistent with the observation of an amorphous microstructure. It should be noted that nanowires grown via the SLS method are generally in an amorphous state, while crystalline nanowires have been typically observed via VLS growth. This may result from the high temperature of the SLS growth process and the relatively high growth rates of those nanowires, which lead to amorphous rather than crystalline microstructure.
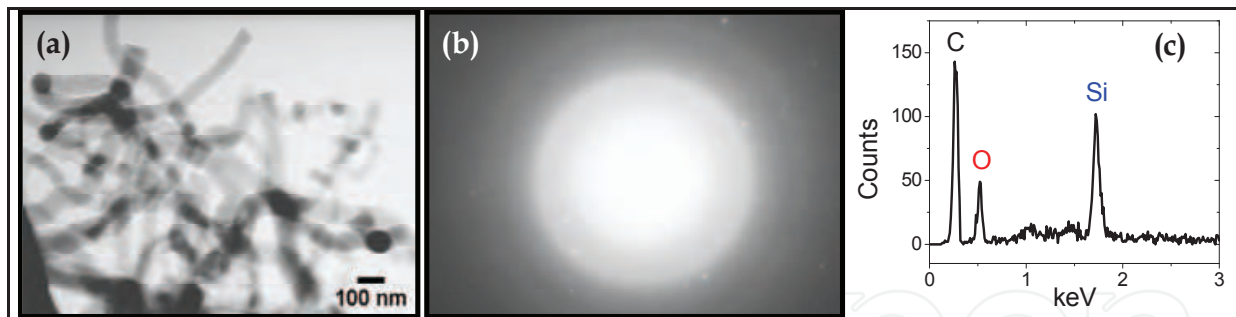
Fig. 5. (a) TEM micrograph of SLS-grown SiNW, (b) SAED pattern. (c) EDS spectra of SiNW. Si and O are the primary elements detected. The SEM-EDS was performed on an HOPG substrate. The carbon peak is due to the substrate.

4.2 Vapour-liquid-solid (VLS) growth

SEM micrographs of VLS SiNWs synthesized for various catalyst Au thicknesses at 500 °C are shown in Fig. 6. It is clearly apparent that the VLS-grown nanowires show a linear morphology instead of the entangled structure exhibited by SLS grown nanowires. The tilted SEM micrograph (Fig. 6(e)) confirms the vertical growth of nanowires from the Si wafer. In Fig. 6(f) a silicon pillar structure was observed.
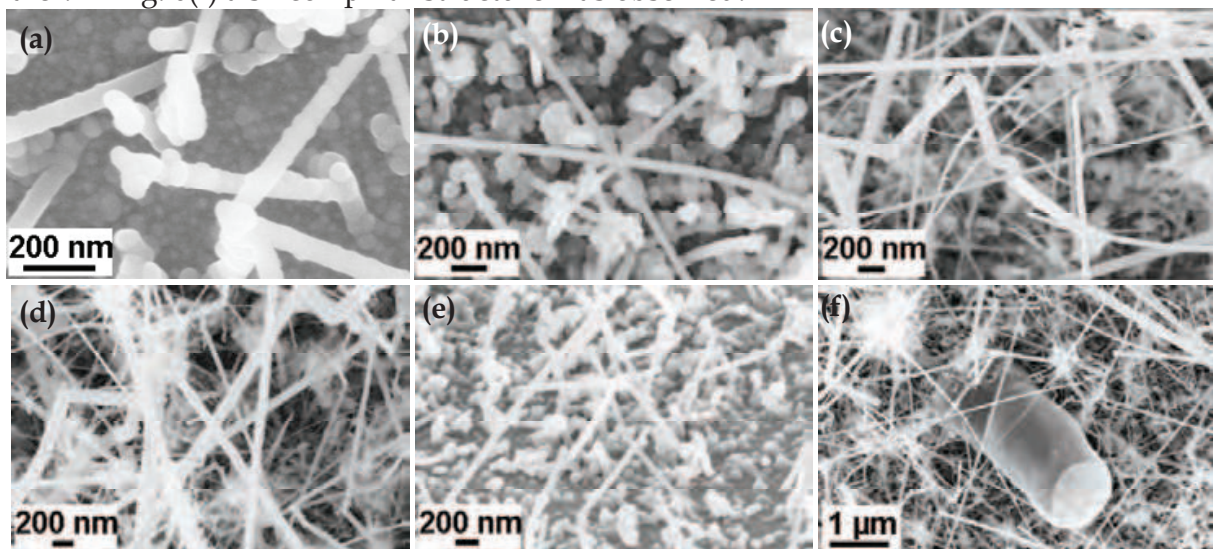

Fig. 6. VLS SiNW growth density and SiNW morphology as a function of Au film catalyst thickness. SEM images of VLS SiNWs for Au catalyst thickness of (a) 1 nm, (b) 5 nm, (c) 20 nm and (d) 100nm. VLS SiNW diameters ranged from 5 nm to 120 nm, (mean ~ 60 nm). (e) Tilted SEM image to show vertical SiNW growth, (f) SEM imaging showing a Si pillar structure formed during SiNW growth.

If sufficient processing control could be established, such large self-assembled Si structures may have potential for use in 3D IC interconnections upon metallization or metal silicidation. Ni was also used as a catalyst for VLS growth (Fig 7.). Experimental results show that the SiNW morphology from a Ni catalyst is similar to that of Au-catalyzed VLS SiNWs. Bi-directional growth was observed at the edge of one Ni-catalyzed VLS SiNW sample (Fig 7(b)).

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
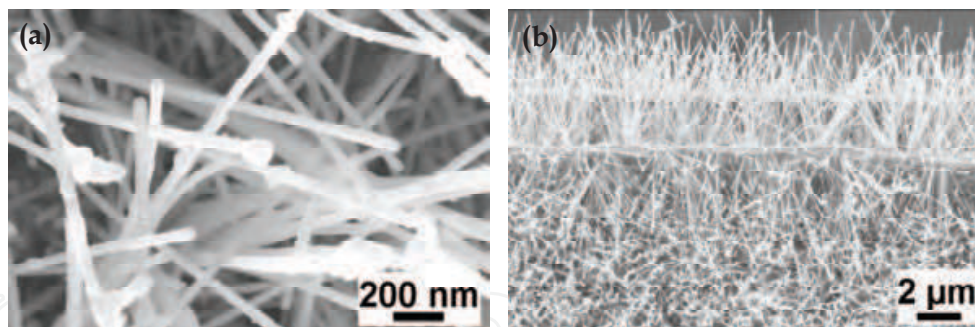synthesis, morphology control, characteristics, and electrical transport   173

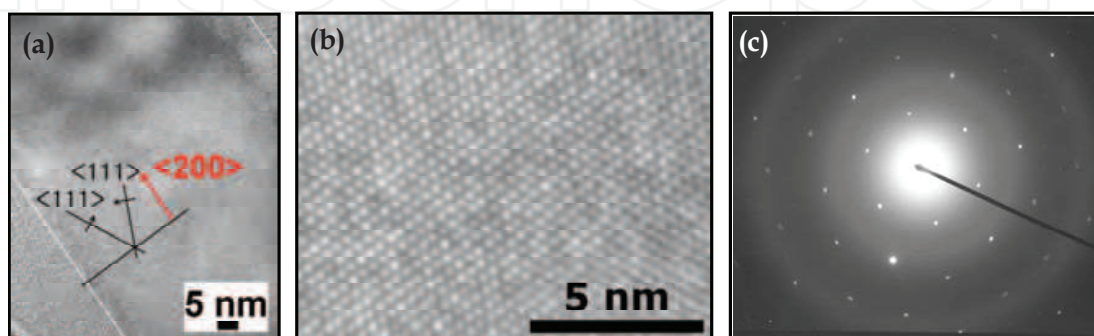Fig. 7. SEM micrographs, (a) VLS SiNW growth using Ni catalyst, (b) bi-directional growth.

Fig. 8. (a) TEM micrograph of VLS SiNW to extract growth direction (<200>), (b) lattice structure of VLS SiNW, (c) selected-area electron diffraction (SAED) patterns from a SiNW. The SEAD pattern shows the perfect crystalline structure of an as-grown VLS SiNW.

Transmission electron microscopy (TEM) of VLS SiNWs was also undertaken for compositional and structural analyses (Fig. 8) and for comparison with SLS-grown nanowires. VLS Si nanowires were detached from the initial silicon wafer using ultrasonication in a methanol solution as described above. Selected-area electron diffraction (SAED) patterns (Fig. 8(c)) indicated a crystalline structure for all VLS nanowires investigated. It should be noted that nanowires grown via VLS are typically crystalline, while amorphous nanowires have been typically observed via SLS growth. Both trends agreed with the work presented here.

The physical properties of both VLS and SLS SiNWs were further investigated with Raman scattering. Figure 9(a)-(c) shows Raman spectra of an as-grown SLS and VLS SiNW compared to that of the Si wafer substrate. The SLS SiNW Raman peak is located at 509 cm^{-1}, and the VLS SiNW Raman peak is located at 517 cm^{-1} while the Si substrate Raman peak is located at 520 cm^{-1}. All peaks correspond to the first-order transverse optical phonon mode (TO) in locally ordered Si. The substantial SiNW TO peak shift and broadening evident in the SLS SiNW results from the substantial local Si-Si disorder. This observation is consistent with prior Raman measurements of SiO$_x$ systems (Yu *et al.* 1998; Li *et al.* 1999; Li *et al.* 2005). Figure 9(d)-(f) compares the Raman spectra for the same phonon mode from an as-grown VLS SiNW, a similar VLS SiNW following 56 days of ambient exposure, and an as-grown SLS SiNW. Following substantial ambient exposure the Si Raman peak is broadened and shifted to 498 cm^{-1} indicative of significant oxidation and possible amorphization.
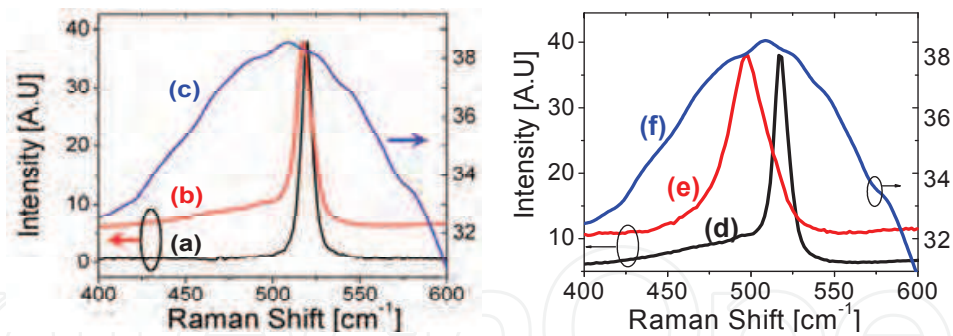
Fig. 9. (Left) Si-Si Raman band from (a) silicon wafer, (b) as-grown VLS SiNW, and (c) as-grown SLS SiNW. (Right) Si-Si Raman band from (d) as-grown VLS SiNW, (e) VLS SiNW after 56 days ambient exposure, and (f) as-grown SLS SiNW.

5. Core-shell Approaches for Metallic Channel Formation

5.1. Synthesis, metallization, structural and compositional characterization of SLS SiNWs

To investigate the formation of conductive shells on SiNWs, nickel was deposited on as-grown SLS SiNWs via e-beam evaporation calibrated for an effective blanket film thickness of 150 nm. Post-deposition thermal processing was carried out for nickel silicide formation (550 °C for 5 minutes via rapid thermal annealing (RTA) and 600 °C for 5 minutes with a 10 minute ramp). The post-anneal nanowire surface morphology was sensitive to the anneal temperature and ramp rate. Rapid ramps resulted in an atomically-smooth Ni-SiNW surface morphology. Slow annealing resulted in a rough Ni-SiNW surface morphology indicative of non-uniform silicide domain formation, as shown in Fig. 10(a), (b), and (c).
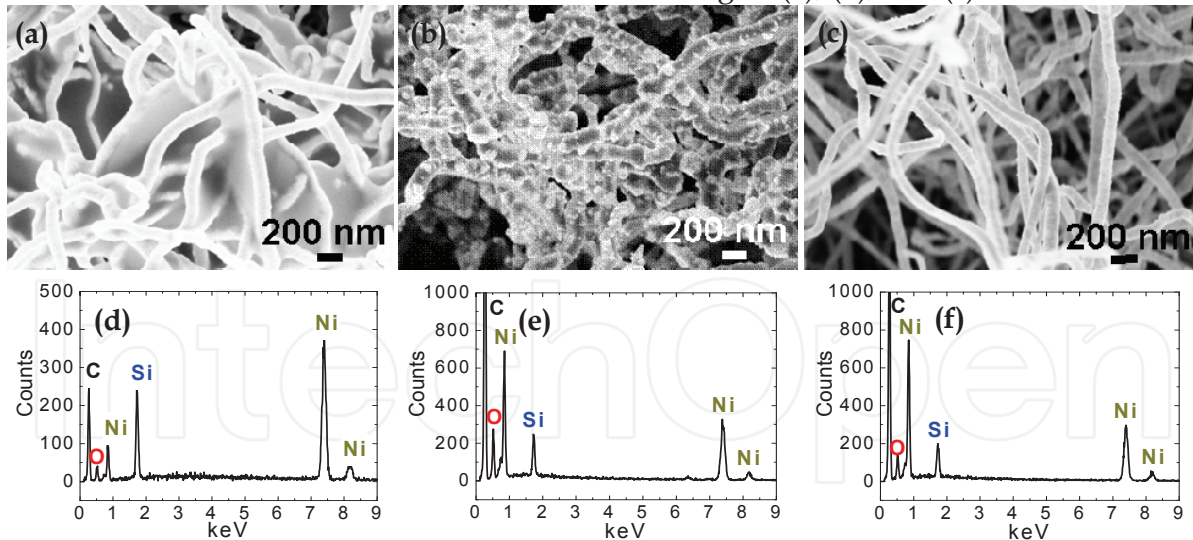

Fig. 10. (a), (d) SEM image and EDS spectrum of as-grown SiNWs after Ni deposition. (b), (e) SEM image and EDS spectrum of Ni-deposited SiNWs after slow annealing at 600 °C for 5 min in Ar ambient with oxygen filter. Note the rough NW surface morphology. (c), (f) SEM image and EDS spectrum of Ni-deposited SiNWs after rapid thermal annealing (RTA) at 550 °C for 5 min in N_2 ambient, Note the smooth NW surface morphology.

Energy dispersive x-ray spectroscopy (EDS) was performed for post-annealed Ni-deposited SiNWs on a HOPG substrate for compositional analysis. Figure 10(d), (e), and (f) shows EDS

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   175

spectra of SiNWs after Ni deposition, after slow annealing, and after RTA, respectively. These results confirm the presence of nickel on individual SiNWs after thermal processing. Note the substantial increase of the Lα peak (0.85 keV) relative to the Kα peak (7.47 keV) for the annealed Ni-SiNWs. This implies nickel silicide formation (Kim *et al.* 2005; Song *et al.* 2007 ; Lee *et al.* 2004). The EDS data in Fig. 10 also confirm the presence of oxygen in the SiNWs. The Ni decoration on the surface of a nanowire after RTA is also shown in the SEM and TEM images of Fig. 11(a) and (b).
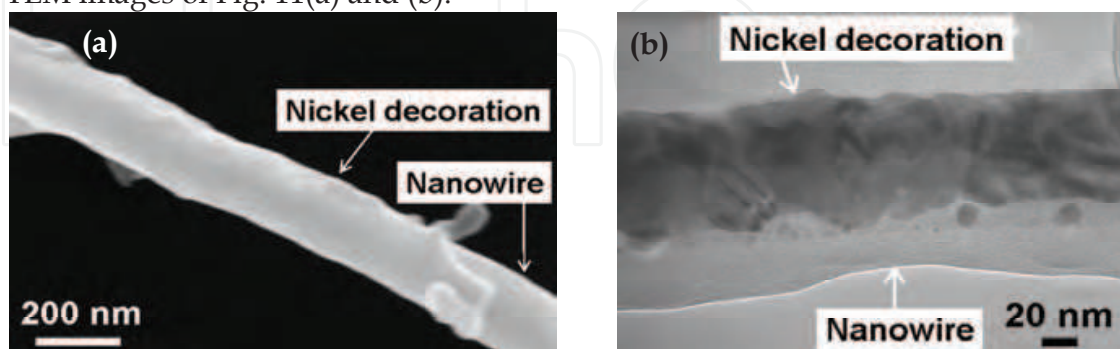

Fig. 11. (a) SEM image of Ni decorated SLS SiNW after RTA on HOPG substrate, (b) TEM image of Ni decorated SLS SiNW after RTA.

5.2. Synthesis, metallization, structural and compositional characterization of VLS SiNWs

Similar to the SLS SiNWs, nickel was deposited on as-grown VLS SiNWs by e-beam evaporation calibrated for an effective blanket film thickness of 150 nm. Post-deposition thermal processing was carried out for nickel silicide formation at 550 °C for 5 minutes via RTA. SEM micrographs in Figs. 12(c) and (d) show that deposited Ni does not coat VLS SiNWs conformally. The asymmetric coating induces mechanical deformation during RTA processing due to thermal expansion differences (Fig. 12(g)). To investigate nickel silicide formation during RTA processing, energy dispersive x-ray spectroscopy (EDS) was performed for as-grown SiNWs (Fig. 12(b)), post-annealed Ni-deposited SiNWs (Fig. 12(f)), Ni-etched nanowires after RTA (Fig. 12(i)), and Ni-etched nanowires without RTA (Fig. 12(k)). Samples for EDS analysis were transferred to a HOPG substrate for compositional analysis. EDS data confirmed that Ni was completely removed during the etching process in the absence of RTA. In contrast Ni was present for samples that underwent RTA. This implies Ni silicide formation at the Ni/SiNW interface since the Ni etchant used does not attack stoichiometric nickel silicide phases. Fast Fourier transform (FFT) diffraction patterns and TEM micrographs of Ni silicided nanowires suggest that they are crystalline (Fig. 13).

VLS SiNWs were also coated with tungsten (2-4 nm thick layer) via an atomic layer deposition (ALD) process. This process was chosen for its ability to provide a conformal coating of W on the high surface area SiNWs. Following W ALD, the samples were annealed in the RTA furnace at 800 °C under a N_2 flow to form W silicide. TEM-EDS was performed on the resulting structures to confirm the presence of W (Fig. 14) although it is not, in principle, possible to distinguish WO_x from WSi_x from this data.
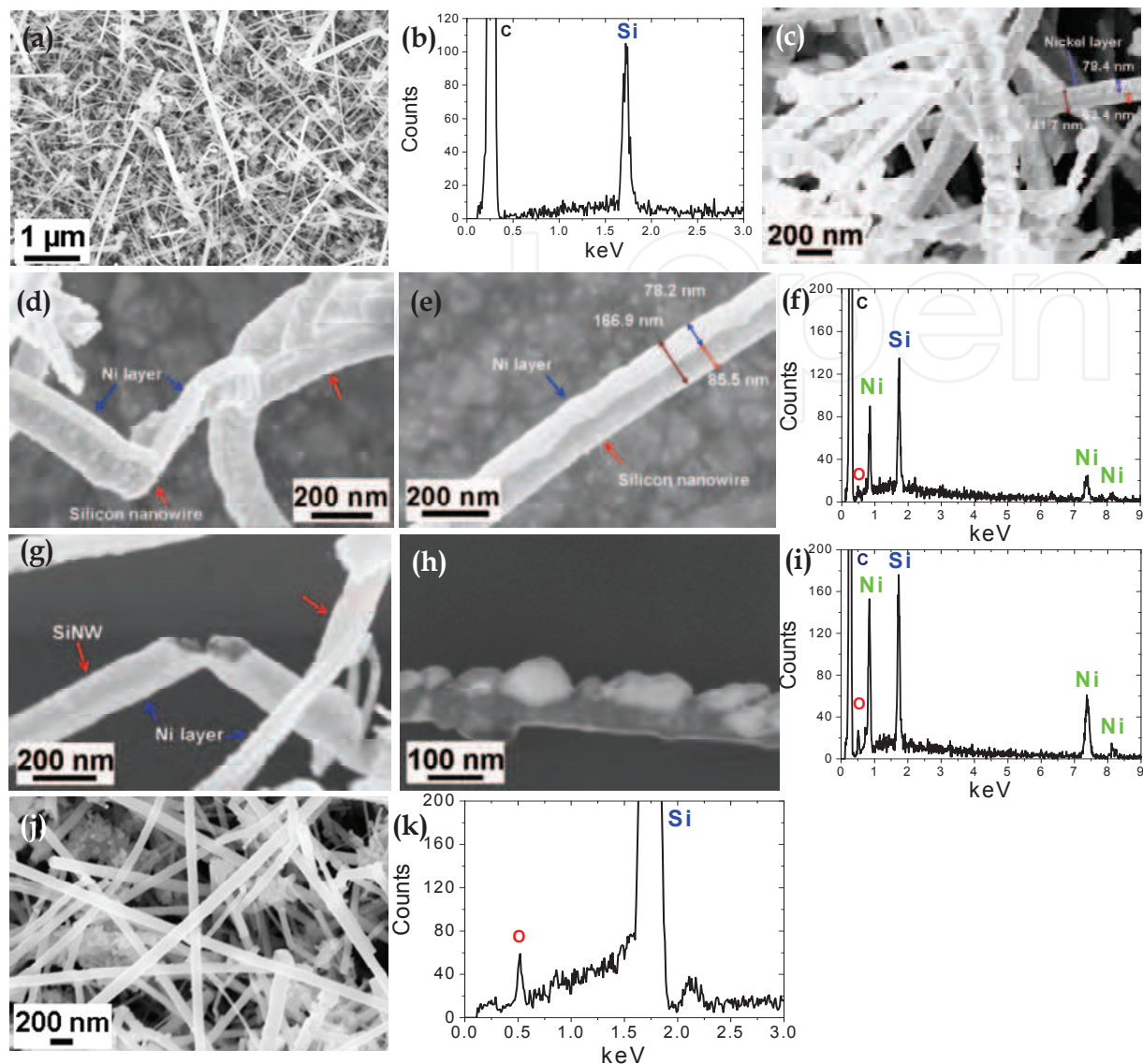
Fig. 12. (a) SEM micrograph of as-grown VLS SiNWs; (b) EDS of as-grown VLS SiNWs; (c) SEM micrograph after Ni coating; (d) (e) and (f) SEM images and corresponding EDS data for VLS Ni-SiNWs after RTA; (g) (h) and (i) SEM images and corresponding EDS data for post-RTA Ni-SiNWs followed by Ni etching; (j) and (k) SEM and corresponding EDS data for Ni-SiNWs after Ni etch (no RTA); (i) and (k) imply the presence of $NiSi_x$.
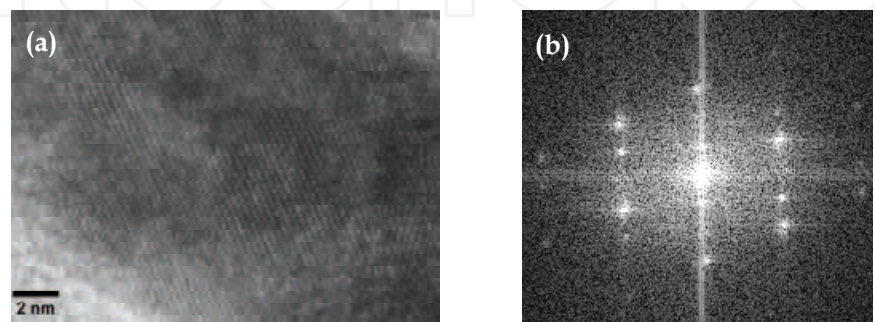

Fig. 13. (a) TEM of a $NiSi_x$-coated nanowire, (b) fast fourier transform of the same nanowire

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   177
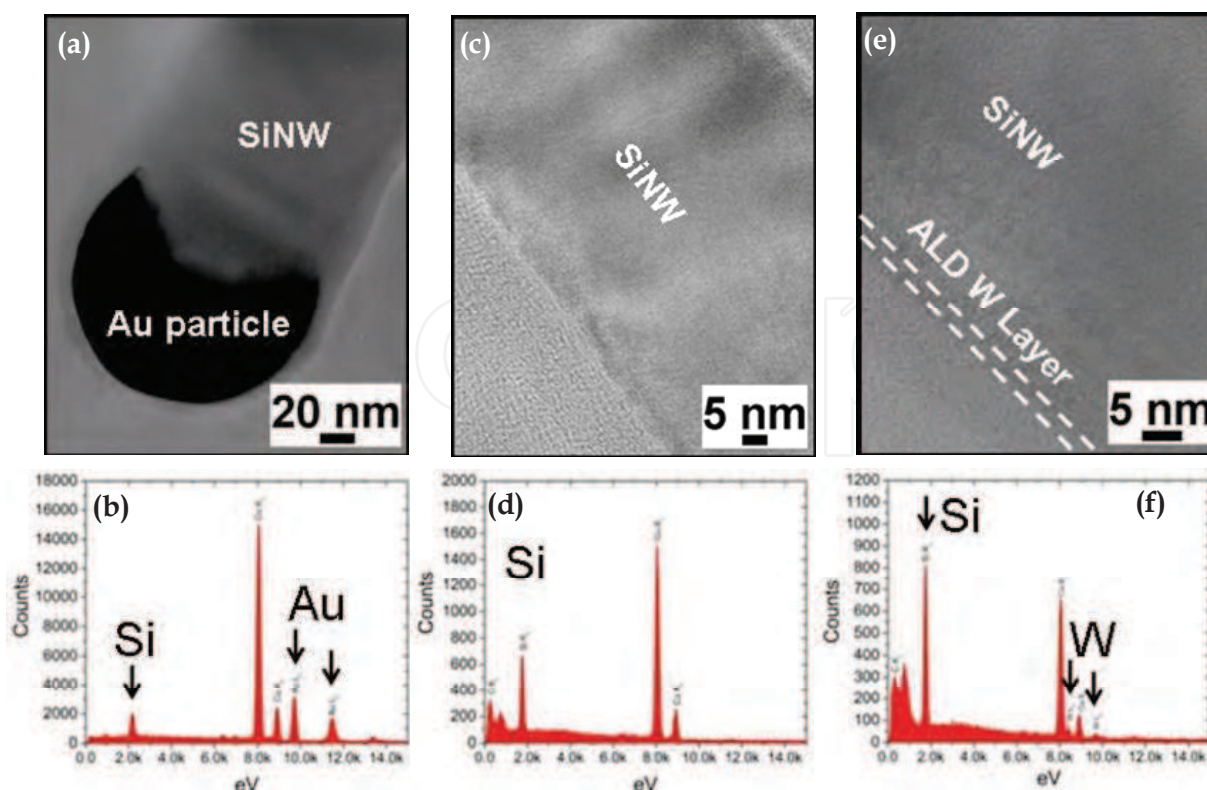
Fig. 14. (a) SEM image of Au catalyst particle at the head of a VLS SiNW, (b) corresponding EDS spectrum (c) SEM image at the center of the nanowire, (d) corresponding EDS spectrum, (e) SEM image of the edge of an ALD-W coated VLS SiNW (nominal W thickness ~ 2-4 nm), (f) corresponding EDS spectrum confirming presence of W.

5.3. Electrical transport of as-grown and metal-coated SiNWs

As-grown silicon nanowires via SLS and VLS and metal/metal-silicide coated SiNWs (both SLS and VLS) were dispensed on SiO_2-coated Si wafers patterned with a metal (Au) electrode pattern to carry out electrical conductivity measurements. Electrical contacts between the dispensed SiNWs and the Au electrodes were formed via direct-write FIB-based Pt deposition. Figures 15(a) and 15(c) display a SEM micrograph and associated current-voltage characteristic, respectively, of an as-grown SLS SiNW. The I-V response of the SLS SiNW is linear and the two-point resistivity of similar SiNWs ranged from 20 Ωcm to 2×10^5 Ωcm. The observed electrical resistivity range for as-deposited SiNWs rules out a dominant SiO_2 stoichiometry, although it is not inconsistent with local SiO_x compositions within the nanowire. (No current measurement was possible for open Pt electrodes confirming the insulative properties of the SiO_2 dielectric in the electrical test structure).

The resistivity of thermally processed Ni-SLS SiNWs (Section 5.1) was measured by two- and four-point electrical resistivity measurements (Fig. 15 (b), (d), (e)). Two- and four-point measurements yield resistances of 2 MΩ and 55 kΩ respectively, for the 9.2 μm long Ni-SLS SiNW with a diameter of 165 nm. Assuming, for the sake of simplicity, that the entire SiNW has been converted to a metal silicide phase the latter value implies an equivalent resistivity of 0.013 Ωcm. This data point is represented by a black circle in Fig. 15 (f). Figure 15 (f) also shows the electrical resistivity distribution of other as-grown SiNWs (blue squares) and Ni-SiNWs (red circles). The lowest measured effective electrical resistivity was 0.02 Ωcm

assuming complete silicidation. (This assumption is discussed in more detail in the following section). After thermal processing of evaporated Ni, the SLS SiNW conductivity is increased up to 7 orders of magnitude.
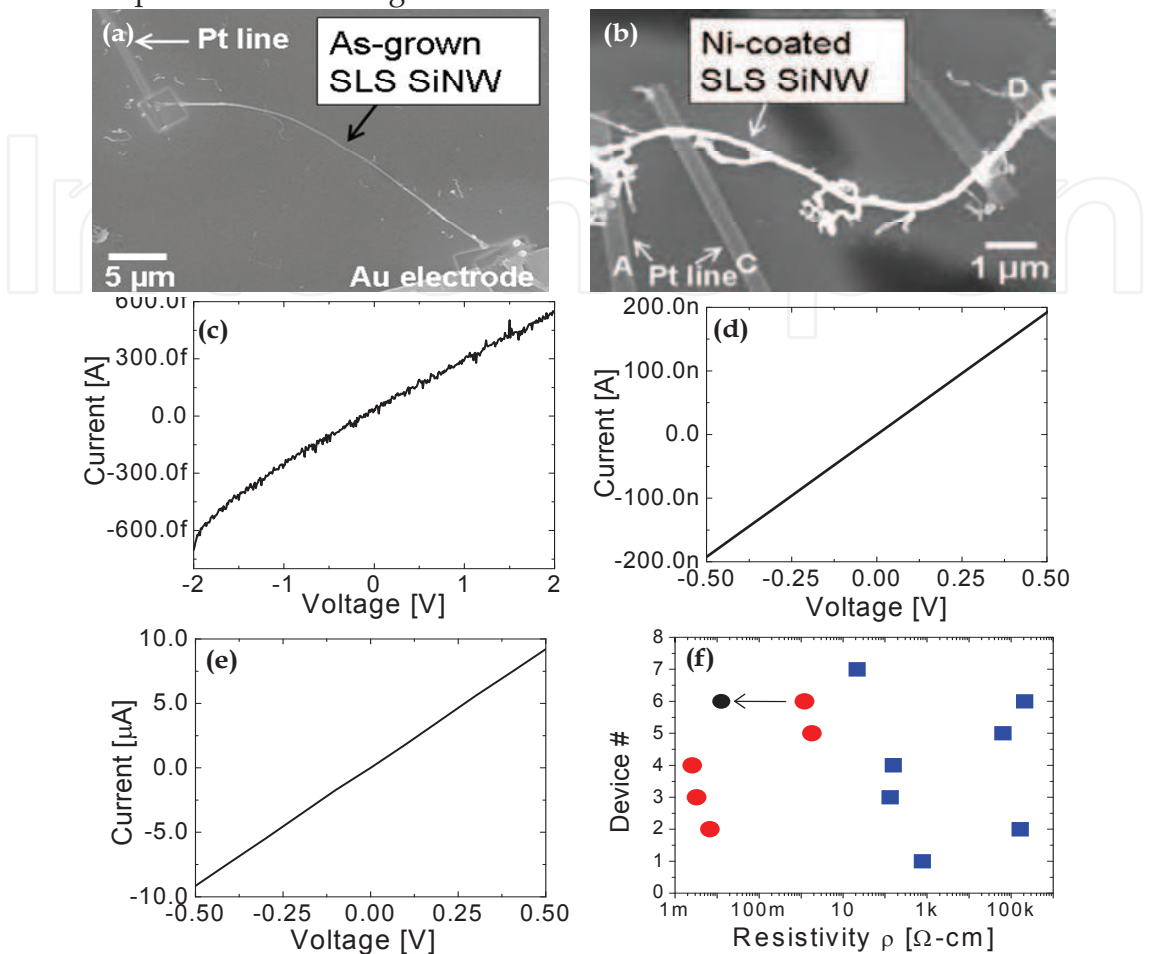

Fig. 15. SEM micrographs of (a) as-grown SLS SiNW in 2-point test structure and (b) annealed Ni-SLS SiNW in 4-point test structure. (c) 2-point I-V data of as-grown SLS SiNW (29.2 μm length, 168 nm diam.), (d) 2-point I-V data of annealed Ni-SLS SiNW (9.2 μm length, 165 nm diam.), (e) 4-point I-V data of annealed Ni-SLS SiNW (9.2 μm length, 165 nm diam.), (f) electrical resistivity from as-grown SiNWs (blue squares) and annealed Ni-SiNWs (red circles). Arrow indicates resistivity drop using 4-point in place of 2-point I-Vs.

Figure 16 shows representative SEM micrographs and associated current-voltage characteristic of an as-grown VLS SiNW, a W-coated VLS SiNW, and a NiSi$_x$ VLS SiNW, respectively. The as-grown VLS SiNW exhibits the expected I-V response for undoped Si. W-coated and NiSi$_x$ nanowires exhibit ohmic conductance (surface). Four-point electrical resistivity measurements were performed on 6 groups of nanowire devices: as-grown VLS SiNWs, NiSi$_x$ VLS nanowires (Ni by e-beam evaporation), ALD W-coated nanowires (2nm W, non-annealed), ALD W-deposited nanowires (2nm W, annealed), ALD W-deposited nanowires (4nm W, annealed), and Ni catalyst SiNWs. Figure 17 shows the electrical resistivity distribution of all 6 groups of these nanowires including as-grown SLS SiNWs and as-deposited Ni-SiNWs as well as as-grown VLS SiNWs. For this plot it was assumed that all Ni-metallized SiNWs were completely converted to metal silicide (i.e. the entirety of

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport 179

the SiNW cross-section is metallic) and that electrical conduction was confined to the W-region of the W-coated SiNWs. As expected, metallization increased nanowire electrical conductivity by as much as 8 orders of magnitude.
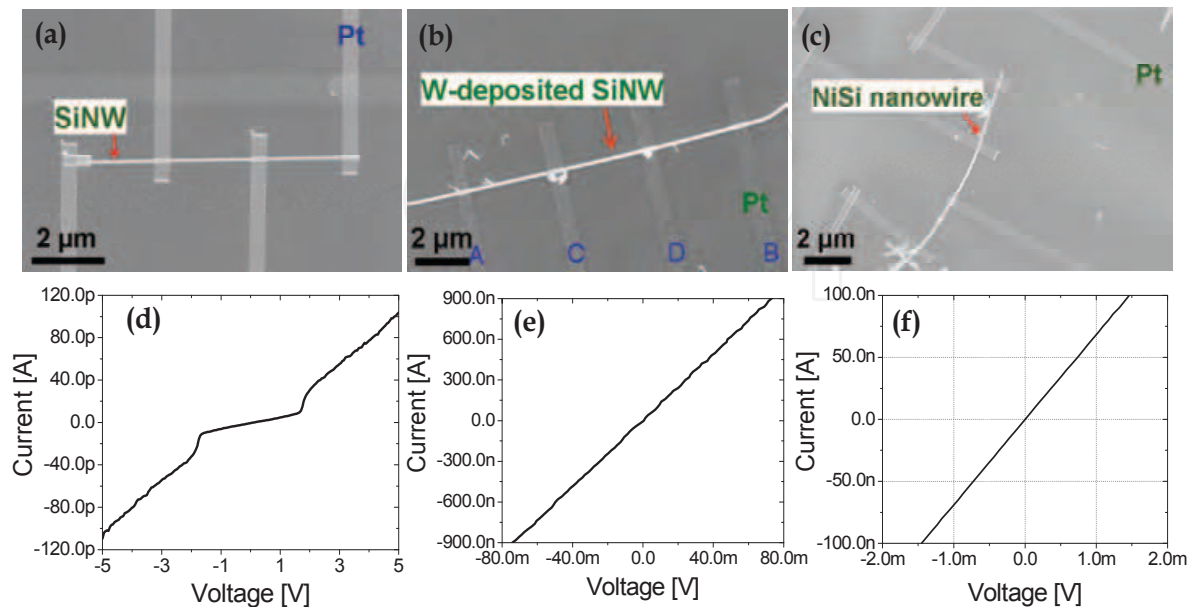

Fig. 16. (a) As-grown VLS SiNW, (b) ALD-W coated SiNW, and (c) NiSi$_x$ SiNW on 4 point electrical test structures. (d) I-V plot of the SiNW shown in (a), (e) I-V plot of the ALD-W coated SiNW shown in (b), (f) I-V plot of NiSi$_x$ nanowire shown in (c)
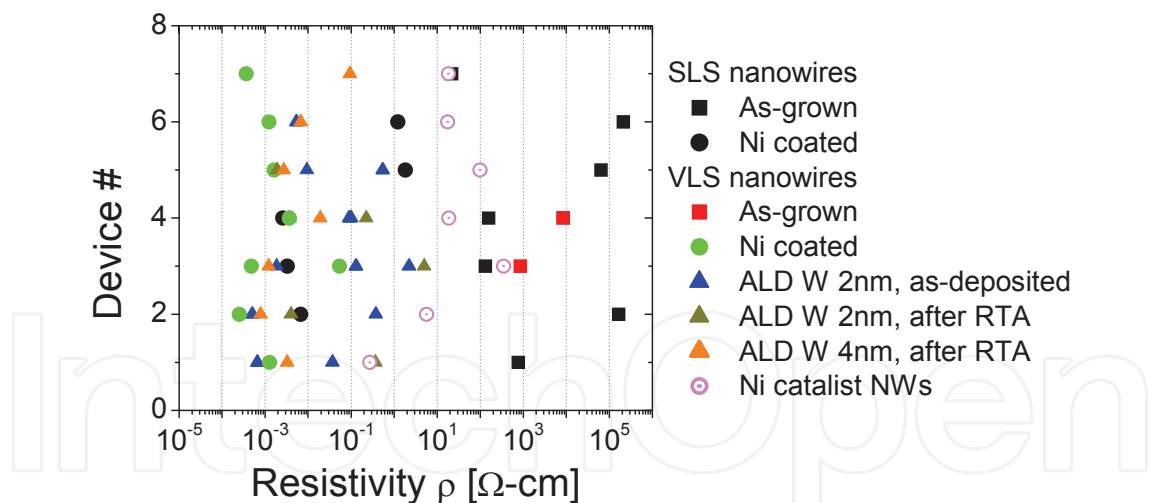

Fig. 17. Comparison of measured electrical resistivity from SiNWs. Device groups include as-grown SLS and VLS SiNWs, Ni-coated SiNWs, NiSi$_x$ nanowires, ALD W-coated VLS SiNWs (2nm W-non-annealed, 2nm W-annealed, and 4nm W-annealed), and Ni catalyst SiNWs.

5.4. Modeling and simulation of electrical transport

To further elucidate the silicidation and metallic conduction of metallized SiNWs analytical and finite-element modeling was carried out. The modeling was restricted to ALD W-coated SiNWs due to the relative uniformity of the W film. Firstly, it was necessary to estimate the

thickness of the post-RTA WSi_2 layer relative to the thickness of a remnant W layer – in the event not all W was consumed during silicidation. Figure 18 schematically illustrates this situation wherein the post-RTA, W-coated SiNW is divided into three distinct radial regions: 1) a single crystalline Si core; 2) a WSi_2 annular region; and 3) an outer W region. Based on simple stoichiometric arguments the annular width of the WSi_2 region depends on the amount of Si and W consumed during the silicidation reaction. Based on bulk Si, W, and WSi_2 unit cell sizes, the thickness of the WSi_2 layer as depicted in Fig. 18 can be calculated as a function of consumed W fraction. These calculations are shown in Fig. 19(a). The overall electron transport across a WSi_2-coated SiNW was simulated using COMSOL Multiphysics finite element analysis software. Figure 19(b) shows current flow through a modeled W/WSi_2-coated SiNW. The current is confined primarily to the WSi_2 region.
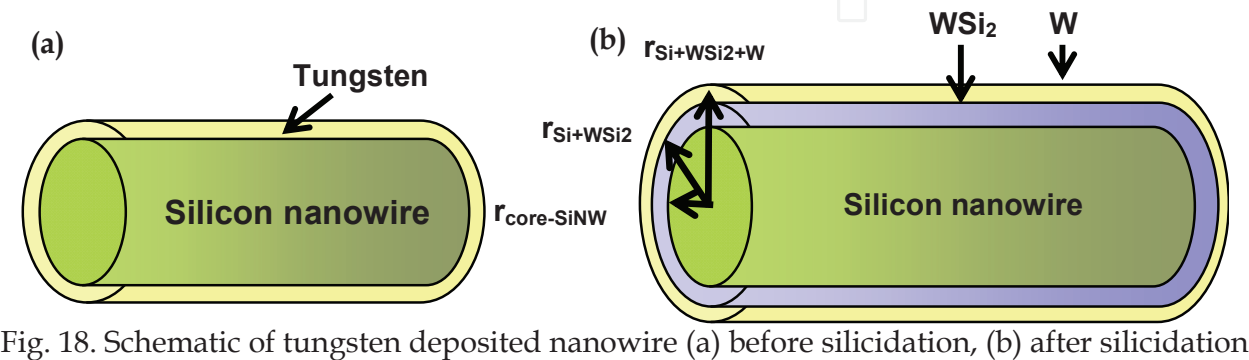

Fig. 18. Schematic of tungsten deposited nanowire (a) before silicidation, (b) after silicidation

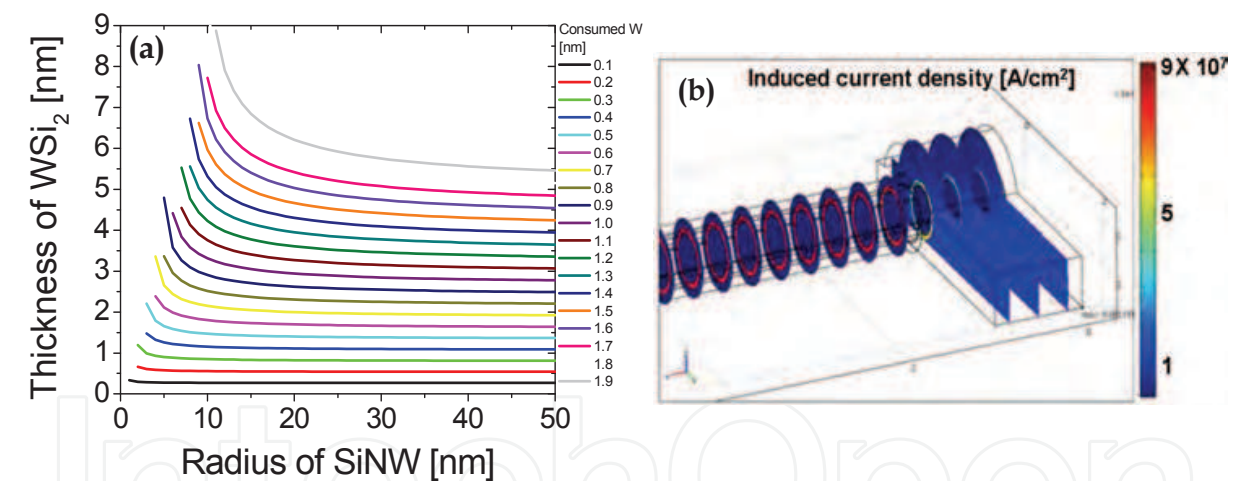
Fig. 19. (a) Thickness (radius) change of the metallic WSi_2 annular region during silicidation for a 2 nm tungsten film as a function of W fraction, (b) representative result of COMSOL Multiphysics simulation. The Si-WSi_2-W structure was used under voltage bias with a metal electrode. Current density was calculated along the nanowire axis. The red circular region denotes the current-carrying annulus.

The resistivity modeling utilized a simple expression to incorporate finite size effects in the W and WSi_2 annular films. Shown in Equation 1, this expression for thin film electrical resistivity is expressly for the case where surface scattering is dominant (Hauder *et al.* 2001; Wissmann *et al.* 2007; Lee *et al.* 2004):

$$\rho = \rho_o + \rho_{GB} + \rho_{SS} + \rho_{SR} \approx \rho_o + \rho_{SS} \approx \rho_o \{1 + (3/16) \cdot l_o/d\} \tag{1}$$

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   181

Here, ρ_o is the bulk resistivity, ρ_{GB} is the grain boundary scattering contribution, ρ_{SS} is the surface scattering contribution, ρ_{SR} is the roughness contribution, l_o is the electron mean free path, and d is thickness of the film.

For W, ρ_o and l_o are approximately equal to 8.7 μΩ-cm and 33 nm, respectively (Steinhogl *et al.* 2005). For WSi$_2$ these values are 46 μΩ-cm and 10nm, respectively (Santucci *et al.* 1998). Therefore, an ideal annular resistivity for the 2 nm W-coated VLS SiNW would be 34. 8 μΩ-cm. The best experimental resistivity of the 2 nm ALD W coating on the VLS SiNW in this measured for this work was 506 μΩ-cm. The order of magnitude difference implies that surface roughness, thickness variation, and, possibly, local compositional variations (e.g. oxidation) have a large effect on the effective W-coating electrical resistivity. For the case of the WSi$_2$ coatings the best measured experimental resistivity was 910 μΩ-cm for an RTA-process 4 nm ALD W coating on a VLS SiNW. Assuming full silicidation the thickness of WSi$_2$ was 11 nm which translated to an ideal resistivity (using Eq. 1 via the COMSOL package) of 58 μΩ-cm. As for the case of the W film the order of magnitude difference between idealized model and experiment is attributed to disorder and compositional variation in the WSi$_2$ coating. Modeling results show most current flows through the WSi$_2$ shell layer as expected (Fig. 19(b)).

6. Novel Growth Mode of Solid-liquid-solid (SLS) Silicon Nanowires

The growth processes for the SLS Si nanowires described in Sections 4 and 5 were optimized with respect to SLS SiNW diameter control and overall nanowire length for evaluation of Ni-based and W-based metallization, electrical transport, and comparison with VLS SiNWs. Those optimization studies also focused on the very early and intermediate stages of SLS SiNW growth and yielded critical insights regarding the initial nucleation of SLS nanowires. Specifically, a novel and previously unreported, high temperature solid-liquid-solid (SLS) silicon nanowire growth mode has been observed and investigated. In this novel mode SLS nanowire nucleation and subsequent growth was uniquely promoted by – and coupled to – the formation of thermally-etched pyramidal pits in the Si substrate which formed during the high-temperature anneal phase BEFORE the onset of SLS SiNW formation. The silicon-oxide-mediated thermal pit formation process enhanced Si transport to Au-Si alloy droplets directly adjacent to the pyramidal pits. Consequently, SLS nanowire nucleation and growth was preferentially promoted at the pit edges. The catalytic nature of the pyramidal pits resulted in the observation of SLS nanowire 'blooms' at the pit locations. Subsequent nanowire growth – occurring both at the pit sites and from Au-Si alloy droplets distributed across the planar surfaces of the Si wafer – eventually occluded the pits complicating experimental observation of this mode. A rapid ramp of the Ar gas flow introduced to the SLS growth chamber at selected points in the annealing cycle was sufficient to quench nanowire growth and permit experimental observation of this novel mode. This newly observed process is termed 'thermal pit-assisted growth.' Section 6.1 describes the experimental configuration for growth mode analysis of SLS Si nanowires. Section 6.2 documents the experimental observations of the stages of thermal pit-assisted SLS SiNW growth and presents compositional analysis for determination of Au-Si alloy droplet disposition with respect to the pyramidal pits. Section 6.3 presents and discusses a schematic outline of the thermal pit-assisted growth mode.

6.1. Experimental configuration for growth mode analysis of SLS Si nanowires

Central to the observation of thermal pit-assisted SLS SiNW growth was the ability to differentially quench SiNW growth across the sample for comparative SEM analysis. As noted in Section 3 quenching was achieved by positioning Au-deposited samples near the chamber's Ar gas inlet (as compared to the center of the annealing chamber) to exploit the large spatial and temporal temperature gradients. For short annealing durations (typically, below 15 minutes) the temperature near the Ar inlet was rapidly modulated via gas flow. Low Ar flows (~2,000 sccm) introduced upon deactivating the heater yielded a slow cool down (approximately 8 min to reduce chamber temperature below 800 ^{o}C and cease SLS SiNW growth – i.e. latent annealing). High Ar flows (~20,000 sccm) resulted in a rapid quench over tens of seconds and was effective at preserving early stage growth configurations and substantially reducing the duration of latent annealing.

Figure 20 shows a SEM micrograph of a sample adjacent to the Ar inlet within the annealing chamber (low temperature/fast quench region). This single sample exhibited various regions reflecting different stages of SLS Si nanowire growth.
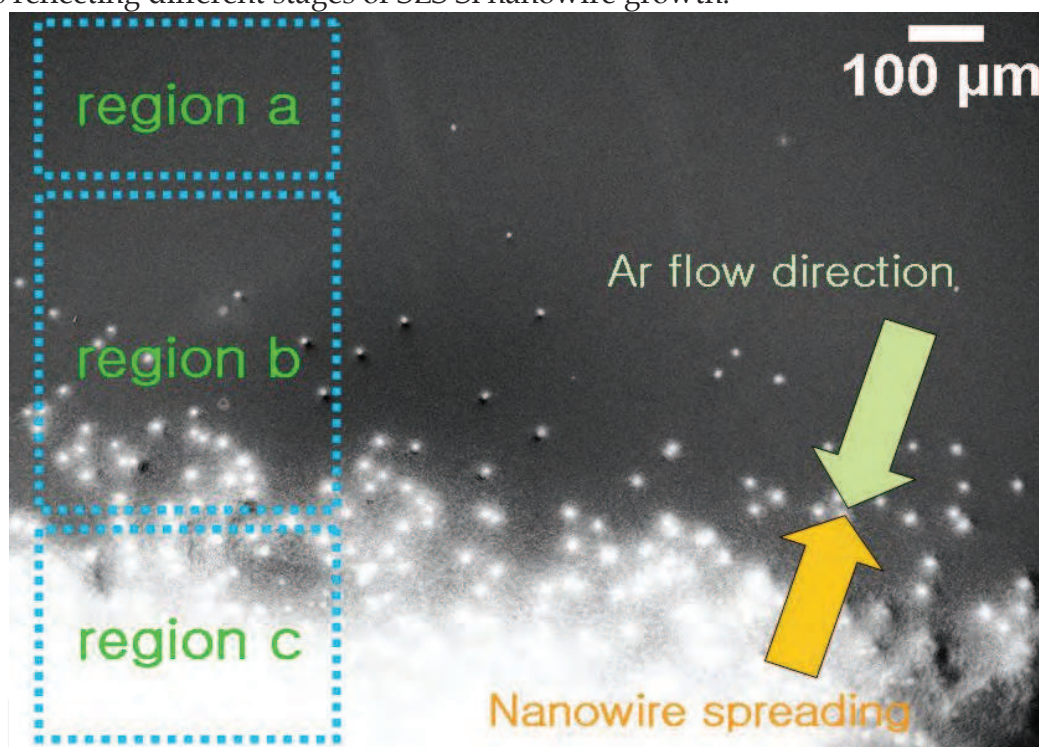

Fig. 20. SEM image of a sample placed close to the Ar inlet inside the oven (low temperature/fast quench region). This sample has three distinct regions in terms of differentiable SLS Si nanowire growth stages.

Three regions were identified. In region (a) Au-Si alloy nanoparticles reside on the surface although SiNW nucleation had not yet occurred (the Au-Si particles are not visible in the magnification shown in Fig. 20). In region (b) so-called 'germinated' Si nanowires could be observed. In region (c) fully-formed Si nanowires were clearly present. Figure 21(a) shows Au-Si alloy particles from the region 'a' depicted in Fig. 20. Little if any SiNW nucleation is evident. The SEM micrographs shown in Figs. 21(b) and (c) were acquired in the 'b' region and clearly capture the initial formation of Si nanowires from droplets wherein the amorphous Si nanowire can be seen emerging or 'germinating' from the droplets. Flower-

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   183

like structures were observed (Figs. 21(d), (e)) from the 'c' region in which dense SLS SiNW nucleation was localized. SEM micrographs from deeper within the 'c' region also show dense mats of nanowires from the flower-like structures that had spread out and locally covered the substrate (Fig. 21(f)). The morphology of this latter feature is more consistent with SLS SiNW morphologies observed from regions of the substrate located at the center of the chamber. SLS nanowires originating from the flower-like structures were substantially greater in length and density than more isolated SLS Si nanowires nucleating nearby. *On closer inspection, the flower-like nanowire clusters were seen to originate from pyramidal pits in the Si substrate. This growth mode has not been heretofore observed for SLS Si nanowires.*
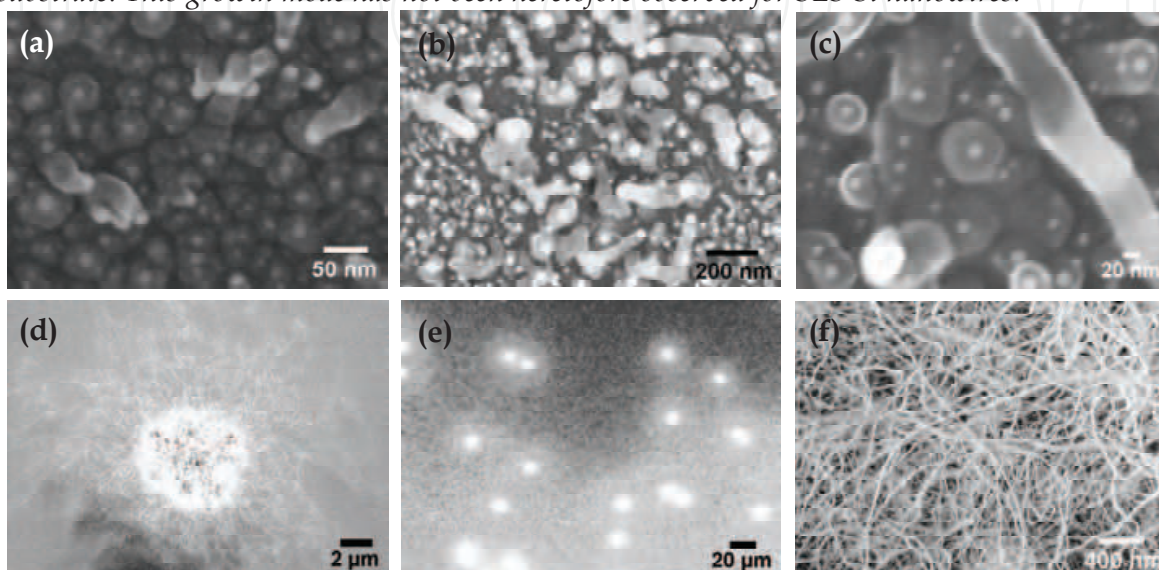

Fig. 21. SEM images of SiNWs at various regions on a single sample in growth. (a) Au-Si alloy particles, (b) and (c) germination of SiNWs, (d) and (e) flower-like nanowire nucleation regions, (f) normal morphology of nanowires.

6.2. Experimental observation of a novel SLS Si nanowire growth sequence

Before elaborating on the observation of the 'thermal pit assisted growth mode' it is important to differentiate it from previously reported SLS growth processes. In SLS SiNW growth the Au-Si alloy droplet is generally observed at the bottom of the nanowire on the surface of the substrate. It has been previously observed that SiNWs can nucleate from alloy droplets inside pits on the silicon surface – pits that had been created by the inflow of the silicon to the alloy droplet (Paulose *et al.* 2003; Sekharet *et al.* 2008; Kim *et al.* 2008). This type of growth was also observed for the work reported here. An example is shown in Fig 22(a). SLS Si nanowire growth can also proceed without necessitating pit formation (Wang *et al.* 2006; Elechiguerra *et al.* 2004). Such a process was also observed for the work reported here (Figs. 22(b), and (c)). These conventional processes (growth modes) are typically used to explain the growth mechanism of SLS nanowires.
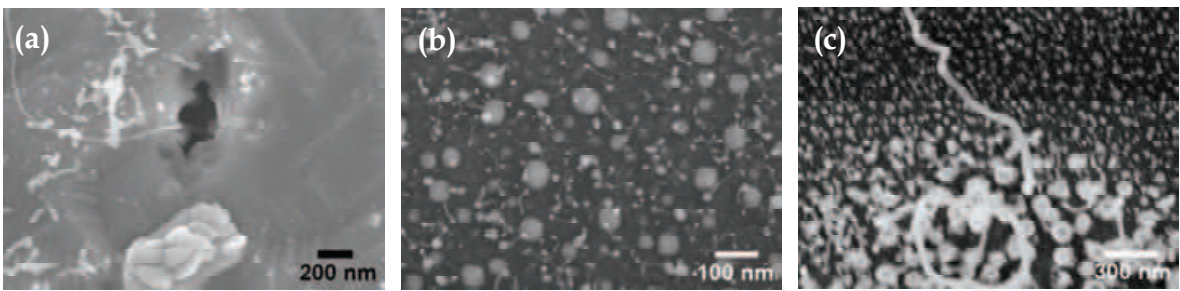
Fig. 22. SEM images of: (a) nanowire and pit created by the inflow of the silicon to the alloy droplet, (b) nanowires directly grown from the substrate and nanoparticles, (c) nanowire germination and growth.

However, these growth modes are distinct from the sequence depicted in Fig. 21. Due to the spatial and temporal thermal gradients afforded by sample placement in the chamber and the rapid Ar gas flow, a spatially-resolved 'timeline' for this novel growth process was documented via SEM imaging at appropriate positions on the substrate. A clear and more detailed series of micrographs documenting this thermally-quenched sequence of SLS Si nanowire growth steps is shown in Fig. 23.
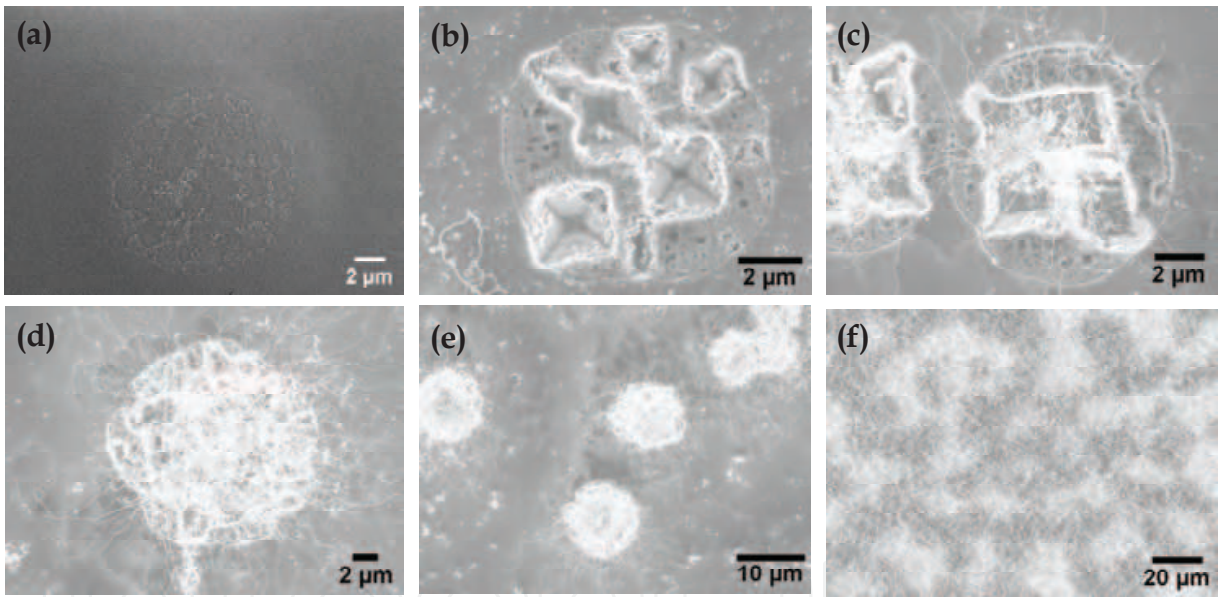

Fig. 23. SEM images of nanowire synthesis steps via thermal pit assisted growth, (a) formation of 'embryos' on Si substrate, (b) thermal pit formation - the pyramidal pits are created by a thermal etching process, (c) initial nanowire growth between the pits, (d) coverage of pyramidal pit by SLS SiNWs (e) nanowires covering multiple pits, (f) nanowires coalescing from neighboring pyramidal pits to cover the substrate.

Figure 23(a) shows the first step in thermal pit assisted SLS SiNW growth – a circular region approximately 10 μm in diameter of local volume discontinuity (swelling) developed in the Si wafer substrate. Regions of the substrate which saw lower temperatures did not exhibit these features. The volume discontinuity is attributed to local oxidation of the Si substrate. Similar localized volume increases have long been observed during thermal oxidation processing of Si (section 6.3). Figure 23(b) shows the next step in this novel SLS Si growth

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   185

mode – thermally-induced formation of pits in circular oxidation regions. These pits were pyramidal in shape with sidewalls comprised of intersecting {111} planes in the (100) silicon wafer. It was observed for multiple samples and experimental runs that the pyramidal pits in the Si substrate were formed *prior* to SLS Si nanowire growth. Figures 23(c) and 23(d) show SiNW nucleation and growth which occurred preferentially at the pyramidal pits. Figures 23(e) and 23(f) shows coalescence of SLS SiNWs from the pyramidal pit regions.

Figure 24 affords closer inspection of the pyramidal pit area at the onset of SLS SiNW nucleation. Firstly, Au-Si alloy droplet concentration is localized at the edge of the pyramidal pits (Fig. 24(a)). Secondly, the silicon oxide growth front defining the circular region encompassing the pyramidal pit is clearly visible (black arrows in Fig. 24(b)). The silicon oxide exhibits a granular or porous structure consistent with the local oxidation-induced volume change.
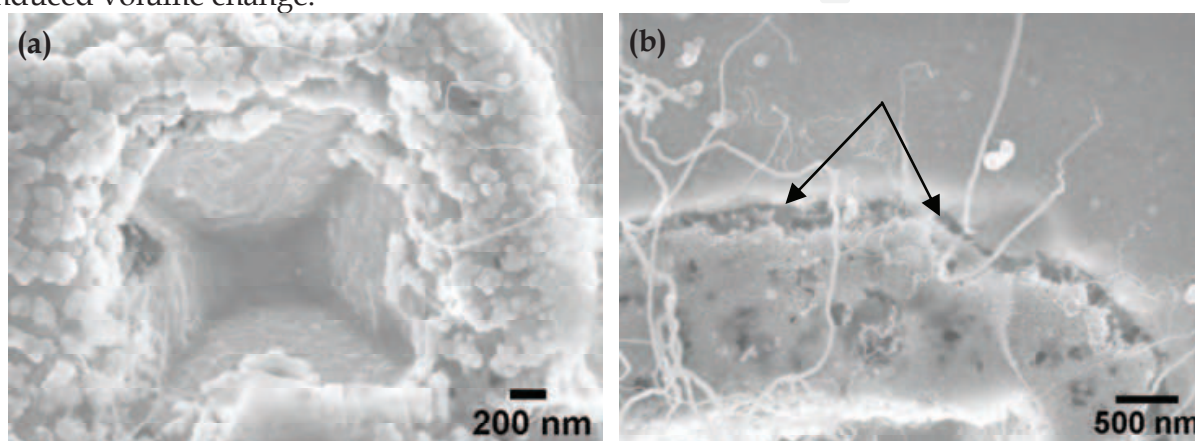

Fig. 24. SEM images: (a) the center of a pit showing Au-Si alloy particles on the edge of the pit; (b) the border of the pit area. In (b) The growth front separating the crack oxidized region from the Si surface is clearly visible (black arrows).

The material disposition associated with the regions in and around the pyramidal pits shown in Figs. 23 and 24 was investigated via SEM-based energy dispersion spectroscopy (SEM-EDS). Representative SEM-EDS spectra acquired in and near a cluster of pyramidal pits are shown in Fig. 25. Figure 25(a) shows a SEM-micrograph of the pit cluster and positions where EDS spectra were acquired. An EDS spectrum acquired from the bright region at the edge of the pits is shown in Fig. 25(b) and confirms the presence of Au, Si, and O, as expected for the presence of Au-Si alloy droplets (see Fig. 24(a)) and SiO_x. The lower contrast region between the pits (but within the circular oxidized region) reveals no Au (Fig. 25(c)) and implies that Au-Si alloy droplets congregate preferentially at the pit edges (although the spectrum confirms the presence of oxidized Si). Away from the circular region confining the pits, EDS of the bare Si substrate does show smaller amounts of oxygen (Fig. 25(d)) which is attributed to the native oxide. Interestingly, EDS data from the very center of a pit (Fig. 25(e)) shows no appreciable Au or O. Trace amounts of O are observed further up the pit walls, closer to the pit edge (Fig. 25(f)). Combined with the SEM image data of Figs. 21, 23 and 24, the EDS data of Fig. 25 enabled the formulation of a SLS SiNW growth mechanism promoted by the pyramidal pits. An elaboration of this mechanism is provided in the following section.
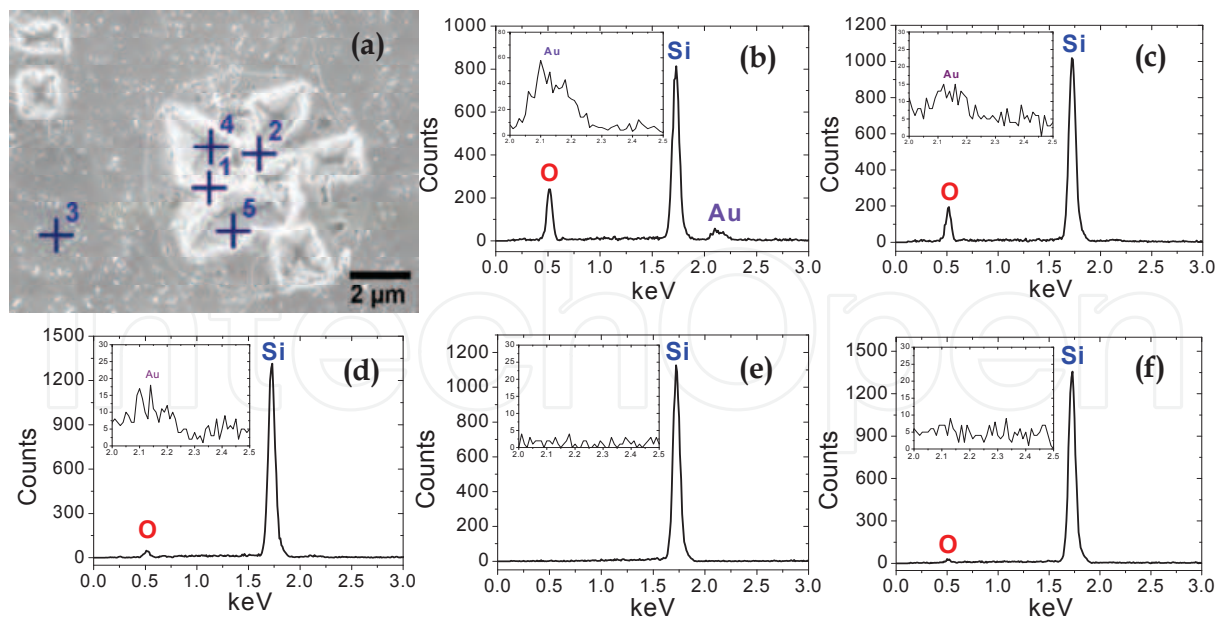
Fig. 25. SEM-EDS spectra at a thermal pit cluster. (a) SEM image of the pit cluster; (b) EDS spectrum at a high-contrast region near a pit-edge (position 1); (c) EDS spectrum at a low-contrast region between pits (position 2); (d) EDS spectrum at the silicon substrate away from the pit cluster (position 3); (e) EDS spectrum at the center of a pyramidal pit (position 4); (f) EDS position at the sidewall of a pyramidal pit near the edge (position 5).

6.3. Mechanistic description of thermal-pit-assisted SLS Si nanowire growth

Based on extensive SEM micrograph and SEM-EDS analysis (consistent with data shown in Figs. 21, 23, 24, and 25) of thermal pit assisted SLS SiNW growth it is concluded that a four-step sequence typifies this growth mode: (1) Nucleation/growth of circular silicon oxide regions; (2) thermal-driven pyramidal pit formation; (3) enhanced Au-Si alloy droplet formation at pyramidal pit edges; and (4) onset of SLS SiNW growth from enhanced Au-Si alloy droplets.

The first step in the aforementioned sequence is consistent with previous observations of the decomposition and removal of SiO at high temperatures (1100 °C) from Si wafers, leaving nearly circular regions several microns in diameter (Rubloff *et al.* 1986; Tromp *et al.* 1985). In this process, solid state SiO_2 reacts with solid Si atoms to form volatile SiO groups. This reaction and the subsequent release of SiO are consistent with the circular regions shown in Figs. 23 and 25 and the porous microstructure within these regions seen in Fig. 24(b).

The oxidation kinetics in the circular regions are also consistent with pyramidal pit growth at high temperatures (> 1000 ºC). As noted in Section 6.2, Fig. 23(b) indicates that the thermally-etched pyramidal pits are formed along (111) planes from the (100) silicon wafer in agreement with observations of other research groups (Ueda *et al.* 2004; Reisman *et al.* 1990; Suzuki 2000a; 2000b). Trace amounts of oxygen enhanced this thermal etching process at high temperatures (Reisman *et al.* 1988, Reisman *et al.* 1990) with pits originating at Si substrate dislocation sites (Yazdi *et al.* 2007). This supports our observation of pyramidal pit growth in the circular oxidized regions of the Si substrate (Figs. 23(a) and 23(b)). The source of the oxygen is attributed to solid state SiO_2 (Reisman *et al.* 1988), not gas-phase oxygen from the chamber. Indeed, research has shown that pyramidal pit formation occurred preferentially under low oxygen partial pressure (below 3×10^{-5} atm) during annealing in Ar

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   187

(Suzuki 2000a; 2000b; Suzuki 2001). Those researchers observed no pit formation at higher partial oxygen pressures. This is consistent with our experimental configuration. High purity industrial grade Ar (99.999%) was utilized in our experiment with an oxygen filter loop. The estimated partial pressure of oxygen in our system is at least 10^{-6} atm from the Ar gas and does not approach levels close to 3×10^{-5} atm even considering other oxygen sources (e.g. quartz tube furnace, sample holder, vacuum excursions, etc…).

The formation of volatile SiO groups as a driving force for the pyramidal etch front is confirmed by the EDS spectrum in Fig. 25(e). No oxygen or Au is evident at the very center of the pit while small trace amounts of oxygen (but no Au) are revealed on the pyramidal pit sidewall nearer the pit edge. The relatively high SiO partial pressure at the pit results in adsorption on Au nanoparticles near the pit edges. This has two primary results. Firstly, Si saturation occurs in the Au-Si alloy droplets at the pit edges comparatively faster than for Au-Si alloy droplets formed on the planar Si wafer surface away from the pyramidal pits. Secondly, oxygen from the SiO species adsorbed on the Au nanoparticles is available to react with the Si substrate thus driving the circular SiO_x growth front and promoting additional pyramidal pits. As the pits cluster, their etch fronts converge, enhancing local concentration of Au-Si alloy droplets leading to a density of SLS SiNW nucleation sites. This speculation is wholly consistent with the observation of a relatively high density of Au-Si alloy nanoparticles adjacent to the thermally generated pits (Figs. 23(c) and 24(a)). Also, Au-Si alloy droplets at the pit edges exhibited, on average, larger diameters as compared to alloy nanoparticles formed at the planar Si wafer surface away from the pits. As a natural consequence, SLS Si nanowires nucleate and grow more rapidly from the Au-Si alloy droplets at the thermally-generated pit edges as compared with Au-Si alloy droplets at the planar Si wafer surface. This speculation is strongly supported by SEM micrographs shown in Figs. 23(e), (f).

It is essential to differentiate the mechanism described above with so-called oxide-assisted growth (OAG). In OAG thermal evaporation or laser ablation is used to evaporate SiO or SiO_2-Si. The resulting SiO vapor decomposes into Si and SiO_2 resulting in a nanowire-like growth front as described in the literature (Zhang *et al.* 2001a; 2001b; Zhang *et al.* 2003). In our experiment, the volatile SiO results specifically from pit formation. Nanowire growth is specifically catalyzed by Au nanoparticles at the pit edges which serve as SiO adsorption sites. The Au nanoparticles simultaneously promote Si nanowire formation through the SLS process *and* maintain local SiO_x growth further promoting pit formation.

This process is described, schematically in Fig. 26. An Au-coated Si wafer is loaded into the chamber. As the sample is heated the Au film dewets to form Au nanoparticles, resulting in Au-Si alloy droplets on the substrate. At selected regions, larger Au-Si alloy droplets are formed via ripening effects. Dangling bonds associated with substrate silicon atoms promote local oxidation (from both low partial pressure gas phase oxygen and solid oxide sources) as shown in Fig. 26(a). Continued oxidation and SiO volatilization lead to the formation of circular SiO_x regions (Fig. 26(b)) and eventually to pyramidal pit etching (Fig. 26(c)). Continued pit etching results in an increase in volatile SiO concentration which promotes relatively faster Si saturation of Au-Si alloy droplets (Fig. 26(d)). This promotes more rapid SLS SiNW growth compared with nucleation on the planar Si substrate. If pyramidal pit density is sufficient a mat-like morphology of thermal pit assisted SiNWs coalesces and forms a dense network or SiNWs.
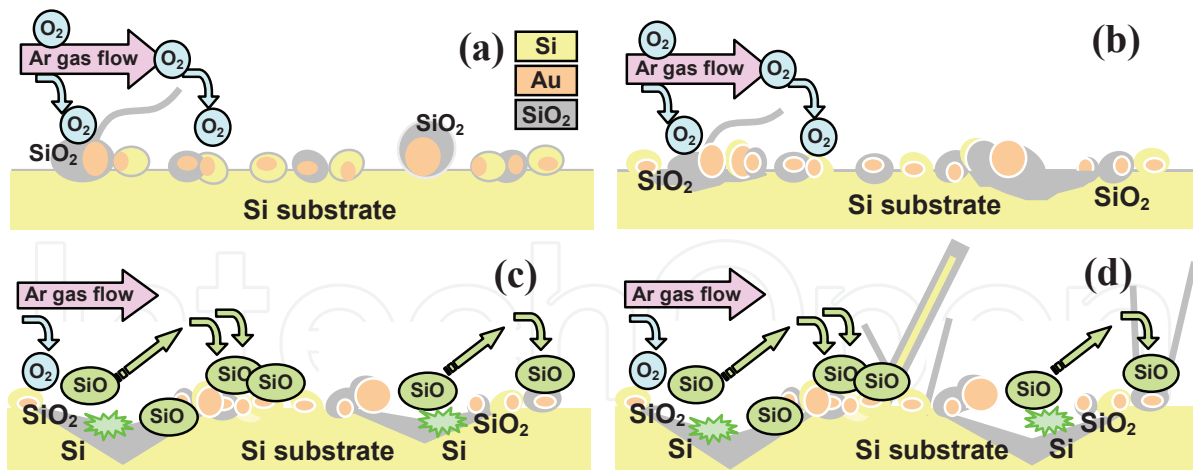
Fig. 26. Schematic illustration of mechanism of thermal pit assisted growth mode, (a) oxidation of germinated silicon, (b) oxidation of silicon substrate, (c) reaction between solid state SiO$_2$ and Si, resulting in volatile SiO and etched pit. Volatile SiO groups can adsorb to Au-Si alloy droplets at the pit edge. (d) nanowire growth from accumulated Au-Si alloy droplets.

7. Conclusion

Self-assembled Si nanowires were synthesized via SLS and VLS growth processes and characterized as a template for surface metal silicide formation for electron transport. Also, the fundamental kinetics and growth mechanisms of SLS Si nanowires were investigated. The diameter of all nanowires investigated ranged from 5 nm to 180 nm. The diameter of as-grown SLS SiNWs was controlled, to an extent, through the annealing time.

Post-growth Ni deposition and thermal processing was carried out for nickel silicide formation at the SLS SiNW surface. The surface morphology of post-annealed SLS Ni-SiNWs was sensitive to anneal temperature and ramp rate. Rapid ramps resulted in an atomically smooth Ni-SiNW surface morphology. Slow annealing resulted in a rough Ni-SiNW morphology indicative of nonuniform domain formation. The presence of Ni on the surface of SLS SiNWs after RTA processing was confirmed via SEM and TEM imaging. EDS measurements also confirmed that the nickel remains on the SLS SiNW surface after thermal processing. Moreover, the substantial increase of the Lα peak (0.85keV) relative to the Kα peak (7.47 keV) in the EDS spectra for the annealed Ni-SiNWs strongly implies nickel silicide formation. Electrical conductivity measurements were performed on as-grown SLS Si nanowires and metal-silicide coated SLS Si nanowires by two-point and four-point methods. NiSi-coated SLS SiNWs exhibited an improvement in electrical conductivity of several orders of magnitude compared with that of as-grown SLS silicon nanowires.

VLS Si nanowire synthesis was carried out to study formation of surface metal silicide layers. That process utilized a SiH$_4$/Ar mixture at 500 °C. The diameters of VLS SiNWs were modulated by catalyst thickness and annealing duration. TEM analysis confirmed grown VLS SiNWs were crystalline with a <200> growth direction. TEM-EDS results showed ALD W was successfully deposited on the surface of SiNWs (~ 2 nm, 4 nm thickness). E-beam evaporated Ni was deposited on VLS SiNWs. SEM-EDS confirmed Ni remained on the VLS nanowire surface after etching the excess Ni. This observation strongly implied NiSi formation. Fourier transform analysis of TEM selected-area-diffraction-patterns likewise

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport   189

implied NiSi formation. Simulation and modeling were performed to investigate electrical transport on W silicide layer. I-V characteristics of W-coated VLS SiNWs and Ni-decorated SiNWs showed an improvement in electrical conductivity (~ 8 orders of magnitude) compared with that of as-grown VLS silicon nanowires. Electrical resistivity measurements confirm ohmic behaviour for electron transport. ALD Ni will be a prospective candidate for silicide formation on SiNW surfaces in the future due to the conformal nature of its deposition and growth.

A previously unreported SLS growth process was observed. For that growth process it is concluded that the high temperature formation of pyramidal etch pits in the Si wafer substrate resulted in local enhancement of Au-Si alloy droplet formation through production of volatile SiO groups from a solid state SiO_2-Si reaction. Saturation of the Au-Si alloy droplets at the pyramidal pit edges due to adsorption of SiO groups occurred more rapidly than Si saturation of Au-Si alloy droplets at the planar Si wafer surface. This resulted in relatively faster SLS SiNW nucleation and growth. This growth mode is termed 'thermal pit assisted growth.'

8. References

Chang, C. & Shen, P. (2000) Thermal-etching development of a-Zn_2SiO_4 polycrystals: effects of lattice imperfections, Mn-dopant and capillary force. *Materials Science and Engineering*, A288, 42–46, 0921-5093

Chen, Y. Q.; Zhang, K.; Miao, B.; Wang, B. & Hou, J. G. (2002). Temperature dependence of morphology and diameter of silicon nanowires synthesized by laser ablation. *Chemical Physics Letters*, Vol. 358, 396-400, 0009-2614

Colli, A.; Fasoli, A.; Beecher, P.; Servati, P.; Pisana, S.; Fu, Y.; Flewitt, A. J.; Milne, W. I.; Robertson, J.; Ducati, C.; De Franceschi, S. ; Hofmann, S. & Ferrari, A. C. (2007). Thermal and chemical vapor deposition of Si nanowires: Shape control, dispersion, and electrical properties. *Journal of Applied Physics*, Vol. 102, 034302, 1089-7550

Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J. & Lieber, C. M. (2001). Diameter-controlled synthesis of single-crystal silicon nanowires. *Applied Physics Letters*, Vol. 78, No. 15, 2214-2216, 1077-3118

Elechiguerra, J. L.; Manriquez, J. A. & Yacaman, M. J. (2004) Growth of amorphous SiO2 nanowires on Si using a Pd/Au thin film as a catalyst. *Applied Physics A*, Vol. 79, 461–467, 1432-0630

Filonov, A. B.; Tralle, I. E.; Dorozhkin, N. N.; Migas, D. B.; Shaposhnikov, V. L.; Petrov, G. V.; Anishchik, V. M. & Borisenko, V. E. (1994). Semiconducting properties of hexagonal chromium, molybdenum, and tungsten disilicides. *Physica Status Solidi (b)*, Vol. 186, No. 1, 209-215, 1521-3951

Futagami, M. & Hamazaki, M. (1982). Thermal etching of 100 silicon surface. *Japanese Journal of Applied Physics*, Vol. 21, No. 12, 1782, 1347-4065

Givargizov, E. I. (1975). Fundamental aspects of VLS growth. *Journal of Crystal Growth*, Vol. 31, 20-30, 0022-0248

Hauder, M.; Gstöttner, J.; Hansch, W. & Schmitt-Landsiedel, D. (2001). Scaling properties and electromigration resistance of sputtered Ag metallization lines. *Applied Physics Letters*, Vol. 78, No. 6, 838-840, 1077-3118

Hochbaum, A. I.; Fan, R.; He, R. & Yang, P. (2005). Controlled growth of Si nanowire arrays for device integration. *Nano Letters*, Vol. 5, No. 3, 457-460, 1530-6992

Kim, G. B.; Yoo, D. J.; Baik, H. K.; Myoung, J. M.; Lee, S. M.; Oh , S. H. & Park, C. G. (2003). Improved thermal stability of Ni silicide on Si 100 through reactive deposition of Ni. *The Journal of Vacuum Science and Technology B*, Vol. 21, 319-322, 1520-8567

Kim, J. & Anderson, W. A. (2005). Spontaneous nickel monosilicide nanowire formation by metal induced growth. *Thin Solid Films*, Vol. 483, 60-65, 0040-6090

Kim, J. H.; An, H. H.; Woo, H. J. & Yoon, C. S. (2008). The growth mechanism for silicon oxide nanowires synthesized from an Au nanoparticle/ polyimide/ Si thin film stack. *Nanotechnology*, Vol. 19, 125604, 1361-6528

Kittl, J. A.; Lauwers, A.; Chamirian, O.; Van Dal, M.; Akheyar, A.; De Potter, M.; Lindsay, R. & Maex, K. (2003). Ni- and Co-based silicides for advanced CMOS applications. *Microelectronic Engineering*. Vol. 70, 158-165, 0167-9317

Lavoie, C.; d'Heurle, F. M.; Detavernier, C. & Cabral, C. (2003). Towards implementation of a nickel silicide process for CMOS technologies. *Microelectronic Engineering*, Vol. 70, 144-157, 0167-9317

Lee, J. H.; Rogers, P.; Carpenter, M. A.; Eisenbraun, E. T.; Xue, Y. & Geer, R. E. (2008). Synthesis and properties of templated Si-based nanowires for electrical transport. *Proceedings of 8th IEEE Conference on Nanotechnology*, 584-587, Dallas, TX, USA, Aug. 2008

Lee, J. W.; Kim, J. K.; Kim, S. H.; Sun, H. J.; Yang, H. S.; Shon, H. C. & Kim, J. W. (2004). Physical and electrical characteristics of physical vapor-deposited tungsten for bit line process. *Japanese Journal of Applied Physics*, Vol. 43, No. 12, 8007-8012, 1347-4065

Lee, K. S.; Mo, Y. H.; Nahm, K. S.; Shim, H. W.; Suh, E. K.; Kim, J. R. & Kim, J. J. (2004). Anomalous growth and characterization of carbon-coated nickel silicide nanowires. *Chemical Physics Letters*, Vol. 384, 215-218, 0009-2614

Li, B. Z & Aitken, R. G. (1985). Electrical transport properties of tungsten silicide thin films. *Applied Physics Letters*, Vol. 46, No. 4, 401-403, 1077-3118

Li, B.; Yu, D. & Zhang, S. L. (1999). Raman spectral study of silicon nanowires. *Physical Review B*, Vol. 59, No. 3, 1645-1648, 1538-4489

Li, C.; Fang, G.; Sheng, S.; Chen, Z.; Wang, J.; Ma, S. & Zhao, X. (2005). Raman spectroscopy and field electron emission properties of aligned silicon nanowire arrays. *Physica E*, Vol. 30, 169-173, 1386-9477

Lu, W & Lieber, C. M. (2007). Nanoelectronics from the bottom up. *Nature Materials*, Vol. 6, 841-850, 1476-4660

Morales, A. M. & Lieber, C. M. (1998). A laser ablation method for the synthesis of crystalline semiconductor nanowires. *Science*, Vol. 279, No 9, 208-211, 1095-9203

Morimoto, T.; Ohguro, T.; Momose, S.; Iinuma, T.; Kunishima, I.; Suguro, K.; Katakabe, I.; Nakajima, H.; Tsuchiaki, M.; Ono, M.; Katsumata, Y. & Iwai, H. (1995). Self-aligned nickel-mono-silicide technology for high-speed deepsubmicrometer logic CMOS ULSI. *IEEE Transactions on Electron Devices*, Vol. 42, No. 5, 915-922, 0018-9383

Templated Si-based nanowires via solid-liquid-solid
(SLS) and vapor-liquid-solid (VLS) growth: Novel growth mode,
synthesis, morphology control, characteristics, and electrical transport 191

Murarka, S. P. (1983). *Silicide for VLSI Applications*, Academic Press Inc., New York, 0125112203

Pan, Z. W.; Dai, Z. R.; Ma, C. & Wang, Z. L. (2002). Molten gallium as a catalyst for the large-scale growth of highly aligned silica nanowires. *Journal of the American Chemical Society*, Vol. 124, No. 8, 1817-1822, 1520-5126

Paulose, M.; Varghese, O. K. & Grimes, C. A. (2003). Synthesis of gold-silica composite nanowires through solid-liquid-solid phase growth. *Journal of Nanoscience and Nanotechnology*, Vol. 3, 341-346, 1361-6528

Reisman, A.; Edwards, S. T. & Smith, P. L. (1988). On the thermal etching of silicon. *Journal of The Electrochemical Society*, Vol. 135, No. 11, 2848-2858, 1945-7111

Reisman, A.; Temple, D. & Smith, P. L. (1990). Further comments on the thermal etching of silicon: The surface morphology of (100), (111) and (110) wafers in the temperature range 900°C-1150°C. *Journal of The Electrochemical Society*, Vol. 137, No. 1, 284-290, 1945-7111

Rubloff, G. W.; Tromp, R.M.; Van Loenen, E. J.; Balk, P. & LeGoues, F.K. (1986). Summary abstract: high temperature decomposition of SiO2 at the Si/SiO2 interface. *The Journal of Vacuum Science and Technology A*, Vol. 4, No, 3, 1024-1025, 1520-8559

Santucci, S.; Lozzi, L.; Passacantando, M.; Picozzi, P.; Petricola, P.; Moccia, G.; Alfonsetti, G.; & Diamanti, R. (1998). Studies on structural, electrical, compositional, and mechanical properties of WSi_x thin films produced by low-pressure chemical vapor deposition. *Journal of Vacuum Science and Technology A*, Vol. 16, 1208-1212, 0734-2101

Sekhar, P. K.; Ramgir, N. S.; Joshi R. K. & Bhansali, S. (2008). Selective growth of silica nanowires using an Au catalyst for optical recognition of interleukin-10. *Nanotechnology*, Vol. 19, 245502, 1361-6528

Song, Y. & Jin, S. (2007). Synthesis and properties of single-crystal β3-Ni3Si nanowires. *Applied Physics Letters*, Vol. 90, No. 17, 173122, 1077-3118

Steinhogl, W.; Steinlesberger, G.; Perrin, M.; Sheinbacher, G.; Schindler, G.; Traving, M.; & Engelhardt, M. (2005) Tungsten interconnecs in the nano-scale regime. *Microelectronic Engineering*, Vol. 82, 266-272 0167-9317

Suzuki, T. (2000a). Effect of annealing a silicon wafer in argon with a very low oxygen partial pressure. *Journal of Applied Physics*, Vol. 88, No. 11, 6881-6886, 1089-7550

Suzuki, T. (2000b). Relation between the suppression of the generation of stacking faults and the mechanism of silicon oxidation during annealing under argon containing oxygen. *Journal of Applied Physics*. Vol. 88, No. 2, 1141-1148, 1089-7550

Suzuki, T. (2001). Oxygen partial pressure dependence of suppressing oxidation-induced stacking fault generation in argon ambient annealing including oxygen and HCl. *Applied Surface Science*, 180, 168-172, 0169-4332

Tromp, R.; Rubloff, G. W.; Balk, P. & LeGoues, F. K. (1985). High-temperature SiO2 decomposition at the SiO2/Si interface. *Physical Review Letters*, Vol. 55, No. 21, 2332-2335, 1092-0145

Ueda, K. & Yoshimura, M. (2004). Formation of micromeshes by nickel silicide. *Thin Solid Films*, Vol. 464-465, 208-210, 0040-6090

Wagner, R. S. & Ellis, W. C. (1964). Vapor-liquid-solid mechanism of single crystal growth. *Applied Physics Letters*, Vol. 4, No. 5, 89-90, 1077-3118

192   Cutting Edge Nanotechnology

Wang, C. Y.; Chan, L. H.; Xiao, D. Q.; Lin, T. C. & Shiha, H. C. (2006). Mechanism of solid-liquid-solid on the silicon oxide nanowire growth. *The Journal of Vacuum Science and Technology B*, Vol. 24, No. 2, 613-617, 1520-8567

Westwater, J.; Gosain, D. P.; Tomiya, S.; Usui, S. & Ruda, H. (1997). Growth of silicon nanowires via gold/ silane vapor–liquid–solid reaction. *The Journal of Vacuum Science and Technology B*, Vol. 15, No. 3, 554-557, 1520-8567

Wissmann, P. & Finzel, H. (2007). *Electrical resistivity of thin metal films*, Springer, Berlin, New York, 3540484884

Wu, Y.; Xiang, J.; Yang, C.; Lu, W. & Lieber, C. M. (2004). Single-crystal metallic nanowires and metal/ semiconductor nanowire heterostructures. *Nature*, Vol. 430, 61-65, 1476-4687

Yan, H. F.; Xing, Y. J.; Hang, Q. L.; Yu, D. P.; Wang, Y. P.; Xu, J.; Xi, Z. H. & Feng, S. Q. (2000). Growth of amorphous silicon nanowires via a solid–liquid–solid mechanism. *Chemical Physics Letters*, Vol. 323, 224-228, 0009-2614

Yazdi, G. R.; Syvajarvi, M. & Yakimova, R. (2007). Formation of needle-like and columnar structures of AlN. *Journal of Crystal Growth*, Vol. 300, 130-135, 0022-0248

Yu, D. P.; Bai, Z. G.; Ding, Y.; Hang, Q. L.; Zhang, H. Z.; Wang, J. J.; Zou, Y. H.; Qian, W.; Xiong, G. C.; Zhou, H. T. & Feng, S. Q. (1998). Nanoscale silicon wires synthesized using simple physical evaporation. *Applied Physics Letters*, Vol. 72, No. 26, 3458-3460, 1077-3118

Zakharov, N.D.; Werner, P.; Gerth, G.; Schubert, L.; Sokolov, L. & Gösele, U. (2006). Growth phenomena of Si and Si/Ge nanowires on Si (111) by molecular beam epitaxy. *Journal of Crystal Growth*, Vol. 290, No. 1, 6-10, 0022-0248

Zhang, R. Q.; Chu, T. S.; Cheung, H. F.; Wang, N. & Lee, S. T. (2001a). High reactivity of silicon suboxide clusters. *Physical Review B*, Vol. 64, No. 11, 113304, 1538-4489

Zhang, R. Q.; Chu, T. S.; Cheung, H. F.; Wang, N. & Lee, S. T. (2001b). Mechanism of oxide-assisted nucleation and growth of silicon nanostructures. *Materials Science and Engineering*, C16, 31–35, 0928-4931

Zhang, R. Q.; Lifshitz, Y. & Lee, S. T. (2003). Oxide-assisted growth of semiconducting nanowires. *Advanced Materials*, Vol. 15, 635-640, 1521-4095

Zhang, X. W.; Wong, S. P.; Cheung, W. Y. & Zhang, F. (2000). Formation and electrical transport properties of nickel silicide synthesized by metal vapor vacuum arc ion implantation. *Material Research Society Symposium*, Vol. 611, C6.5.1

Zhang, Y. F.; Tang, Y. H.; Wang, N.; Yu, D. P.; Lee, C. S.; Bello, I. & Lee, S. T. (1998). Silicon nanowires prepared by laser ablation at high temperature. *Applied Physics Letters*, Vol. 72. No. 15,1835-1

Cutting Edge Nanotechnology

Edited by Dragica Vasileska

The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Jae Ho Lee and Robert E. Geer (2010). Templated Si-based Nanowires via Solid-Liquidsolid (SLS) and Vapor-Liquid-Solid (VLS) Growth: Novel Growth Mode, Synthesis, Morphology Control, Characteristics, and Electrical Transport, Cutting Edge Nanotechnology, Dragica Vasileska (Ed.), ISBN: 978-953-7619-93-0, InTech, Available from: http://www.intechopen.com/books/cutting-edge-nanotechnology/templated-si-based-nanowires-via-solid-liquidsolid-sls-and-vapor-liquid-solid-vls-growth-novel-growt

INTECH

open science | open minds