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Compact Modeling of Carbon Nanotube Transistor and Interconnects

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Silicon based devices have dominated mainstream computing for the last four decades. Achieving sustainable scaling of physical dimensions and device performance (Moore, 1965) has been key to their success. However, due to limitations in fundamental physics, materials, and manufacturing limits, this scaling trend has slowed down. Examples of major bottlenecks for continual scaling include short channel effects, high leakage currents(Wann et al., October 1996), excessive process variations(Bowman et al., 2002) and reliability issues(Chen et al., February 1985). These pitfalls are posing dramatic challenges to fabrication of circuits with scaled silicon devices. As we approach these fundamental limits in planar CMOS process, it becomes imperative to search for alternative materials, structures, devices as well as design paradigm to replace silicon transistor as the building block of future nanoelectronics.
Novel structures like FinFETs(Hisamoto et al., 2000) and Trigate devices(Doyle et al., 2003), strained channel to enhance carrier mobility(Welser et al., 1994) and high-K/metal gate to reduce gate leakage current(Chau et al., 2004) have been proposed. These innovations have limited potential and will extend the scaling by a generation or two. Amongst more radical search for new devices and materials, carbon nanotube electronics has attracted significant attention owing to their high intrinsic carrier mobility.
For the sake of simplicity, carbon nanotubes can be defined as hollow cylinders made up of one (single-walled) or more (multi-walled) concentric layer of carbon atoms arranged in a hexagonal lattice structure, which is similar to a rolled-up sheet of graphene. With diameters of 1-4 nm and the length extending to several micrometers, carbon nanotube is essentially a one dimensional object possessing unique properties attributed to low dimensional structures, such as 1-D density of state for carriers (McEuen et al., 2002). This enables reduced phase space for scattering and near ballistic transport of carriers when the device dimension is less than the mean-free path for scattering. Depending on the direction in which the graphene sheet is rolled up, single-walled carbon nanotubes is either metallic or semiconducting. Hence CNT transistor and interconnect can be made out of semiconducting and metallic nanotubes, respectively. Functional field effect transistors with semiconducting carbon nanotube channel(Lin et al., 2005; Zhang et al., 2006) and metallic nanotubes as interconnects(Close & Wong, 2007) have been demonstrated. Theoretically, it is possible to get current densities much higher than that of silicon devices with a similar dimension(Raychowdhury et al., 2006) using multiple CNTs in parallel.
To speed up the evolution of this novel alternative technology, parallel efforts in circuit design are essential. For this purpose, the development of compact model is a vitally important

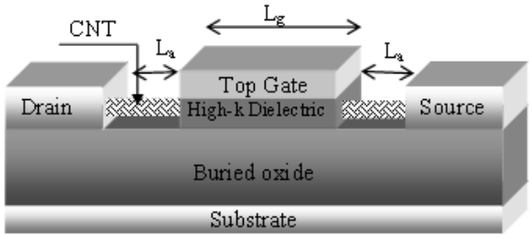


Fig. 1. Cross-section of a generic SW-CNT structure with top gated region as the intrinsic transistor of length L_g and highly doped undated access region of length L_a as the extrinsic part

step that enables circuit simulation and exploration. Early work on carbon nanotube transistor modeling assumed doped source-drain junctions resulting in optimistic performance projections (Guo et al., 2002). The CNT-FET model developed in (Castro et al., 2002) accurately calculated the degradation of current due to presence of Schottky barriers at the contacts. However, it requires self-consistent numerical iterations to calculate the final current and tunneling probability. Currently most of the models developed for carbon nanotube transistors and interconnects employ some kind of numerical approach (Guo et al., 2004; Wong et al., Nov. 2006) to obtain the I-V and C-V characteristics. Though highly physical and accurate, such numerical approaches reduce the computation efficiency and are not suitable for large-scale circuit simulations. Some other modeling approaches include threshold voltage based models(Raychowdhury et al., 2004) and models that resort to SPICE simulator to solve iterative differential equations and compute the surface potential (Deng & Wong, 2007a).
In this chapter, we discuss the development of an integrated compact model for carbon nanotube transistors and interconnects that is non-iterative and SPICE compatible. Initial models concentrated on modeling only the ballistic transport model of the transistor channel. However, the effect of the Schottky barrier at the metal source-drain contacts cannot be decoupled from the channel region. The developed model accounts for the presence of these barriers accurately. The implemented model has been systematically verified with TCAD simulations and measured data. Using this model, we benchmark digital and analog performance metrics and compare them with 22nm CMOS process to explore design potentials with CNTs.

1. Model Development

The cross-sectional view of a typical carbon nanotube transistor is shown in Fig. 1. The basic structure is similar to a conventional FET with the channel replaced by a semiconducting carbon nanotube. The similarity to the structure of CMOS device improves the compatibility with today's process and design infrastructure.
In the ideal case for ballistic transport, the source and drain electrodes would behave as reservoirs that supply and sink mobile carriers without any reflection at the source and drain. This is true only when there are ideal source and drain contacts, i.e., no significant energy barrier between the channel and the contact. There has been extensive work on finding the appropriate contact material for the CNT-FET (Chen et al., 2005) but they all have a finite energy gap when contacting the carbon nanotube forming a Schottky barrier. The device performance is primarily limited by the Schottky contact, depending on the properties of the contact material

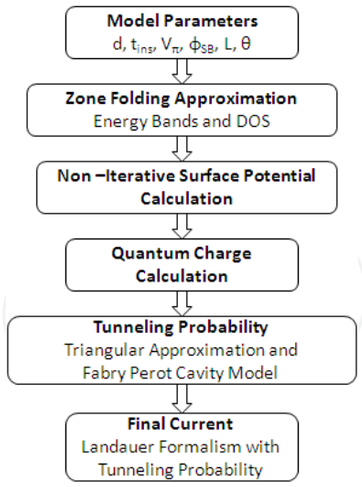


Fig. 2. Flowchart describing the model development

and the nanotube. The energy gap is sensitive to the work function of the contact, the diameter of the nanotube, as well as the chirality.
In this section, we will first discuss the intrinsic channel and relate the physical parameters to the electrical equivalents by the Zone-folding approximation. Using linear approximations, we derive an expression for surface potential. Then the impact of the Schottky barrier on the drain current is studied and integrated into the model. Based on similar modeling principles of the channel and the contact, a compact model of CNT interconnect and CNT-FET are developed. Fig. 2 shows a flowchart describing the CNT-FET compact model. Details of the physical mechanisms and model derivations of the CNT interconnect model are discussed in the next section.

1.1 Zone-folding approximation

We begin with characterizing the structure of single-walled carbon nanotubes (SWCNT) and defining its basic electronic properties such as band-gap, density of states etc. A SWCNT device is essentially a one-dimensional nanowire formed by rolling a two-dimensional graphene sheet. The $2s$, $2p_x$ and $2p_y$ orbitals form σ bonds in graphene. Since the σ bonds are weakly coupled to the $2p_z$ orbitals, they form π bonds, which give rise to the electronics properties of graphene. The E-k values for graphene can be obtained from the tight-binding model given by (1),

$$E_{g2D}(k_x,k_y) = \underset{-}{+}t\left\{1+4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) +4\cos^2\left(\frac{k_y a}{2}\right)\right\}^{1/2} \quad (1)$$

To get the bandstructure of carbon nanotubes, we begin with the bandstructure of graphene given in (1), apply periodic boundary conditions along the circumference of the nanotube. The rolling-up of the honeycomb lattice of the graphene sheet along a specific direction, known as

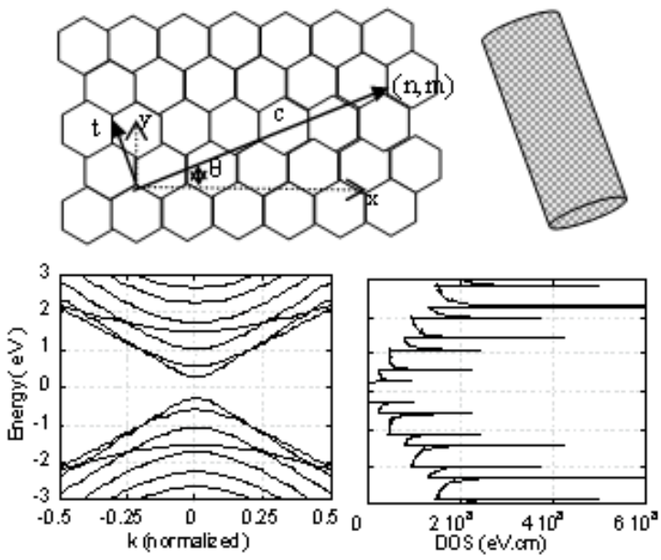


Fig. 3. Honeycomb lattice graphene sheet showing the chiral vectors (n,m) and the corresponding E-k diagram calculated using (1) and DOS using (2)

the chiral vector (shown in Fig. 3), causes the quantization of the wave-vector space along its direction.

A chiral vector can be denoted by the coordinates (n,m). If (n-m) is a multiple of 3, the carbon nanotube is metallic, else it is semi-conducting. To calculate the current, the electron density of states (DOS) near the Fermi level is required. Classical tight-binding models are used to accurately compute the DOS. At low bias, the DOS D(E) at energy E can be approximated as expressed in (2) (Guo & Lundstrom, 2006),

$$D(E) = \frac{D_0|E|}{\sqrt{E^2 - {E_n}^2}} \text{ where } D_0 = \frac{8}{3\pi V_\pi a} \tag{2}$$

All variables used in the above equations are defined in Table 1. For a more detailed discussion on the band-structure of carbon nanotubes, zone-folding approximation and complete derivation the interested reader is referred to (Guo & Lundstrom, 2006).

1.2 Surface-potential based modeling

On applying a gate voltage V_G is applied, the surface potential (ϕ_s) is modulated. The expressions for surface potential and the total charge are as follows :

$$\phi_s = V_{GS} - \frac{|Q_{CNT}|}{C_{ins}} \tag{3}$$

$$\begin{aligned} Q_{CNT} =& N_0 \sum_n \int_{E_n} F\left(\sqrt{E^2 - E_n^2}, \mu_s\right) \\ &+ F\left(\sqrt{E^2 - {E_n}^2}, \mu_s - V_{DS}\right) dE \end{aligned} \tag{4}$$

where

$$F(E,\mu) = \frac{1}{1+e^{(E-\mu)}}(\text{Fermi-Dirac Integral}) \tag{5}$$

and n is the number of sub-bands under conduction.
The conventional method to compute the ϕ_s (using the conduction-band minima and DOS calculated from Table 1 and (2), respectively) involves numerically solving the 1-D poisson equation and the total charge equation self-consistently. In spite of being accurate, this method is computationally intensive and inappropriate for compact modeling and circuit simulations. Additionally, SPICE solvers may encounter convergence errors when loaded with a task of solving complicated numerical functions. Hence, a linearized equation for ϕ_s has been derived. By eliminating numerical iterations, the simulation speed is considerably improved making the model suitable for large scaling circuit simulation.
We derive a closed form linear approximation for surface potential from the fundamental equations of channel charge and bias conditions. From (3) and (4)

$$\begin{aligned}\phi_s =& V_{gs} - \frac{N_0}{C_{ins}}\sum_n \int_{E_n} \frac{1}{1+exp\left(\frac{E-V_s-E_n-\phi_s}{KT}\right)} \\ &+ \frac{1}{1+exp\left(\frac{E-V_d-E_n-\phi_s}{KT}\right)} dE \\ =& V_{gs} - \gamma \sum_n \Bigg[ln\left(1+e^{\left(\frac{E_f-V_s-E_n-\phi_s}{KT}\right)}\right) \\ &+ ln\left(1+e^{\frac{(E_f-V_d-E_n-\phi_s)}{KT}}\right)\Bigg]\end{aligned} \tag{6}$$

For low bias voltages, the first order approximation (6) is linear. Hence, we may write the equation as

$$\begin{aligned}\phi_s =& V_{gs} - \sum_n \gamma \Big[\frac{(E_f - V_s - E_n - \phi_s)}{KT} \\ &+ \frac{(E_f - V_d - E_n - \phi_s)}{KT}\Big]\end{aligned} \tag{7}$$

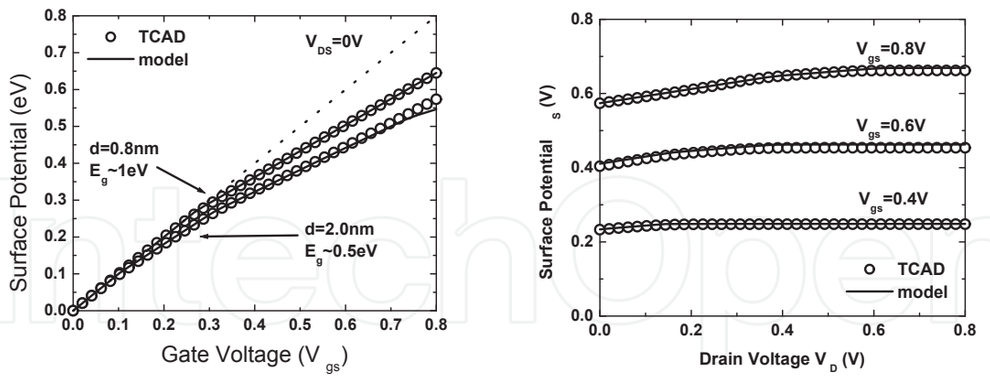
Moving ϕ_s from RHS on to the LHS and re-arranging the terms, we get the non-iterative closed form expression for surface potential as follows

$$\phi_s = \sum_n \left(\frac{V_t \gamma (\xi_s |\xi_s| + \xi_d |\xi_d|)}{2(1+2\gamma)} \right) - V_{gs} \tag{8}$$

where $\gamma = N_0/C_{ins}$, and

$$\xi_{s,d} = \frac{(E_f - V_{s,d} - E_{o,p} + V_{gs})}{V_t}; |\xi_{s,d}| = \begin{cases} 1, & \text{if } \xi_{s,d} > 0, \\ 0, & \text{if } \xi_{s,d} < 0. \end{cases}$$

This expression forms the basis of the compact model. All existing models (Castro et al., 2002; Deng & Wong, 2007a; Guo et al., 2004; 2002; Raychowdhury et al., 2004; Wong et al., Nov.



(a) (b)

Fig. 4. ϕ_s as a function of V_{gs} and V_{ds} for d=0.8nm and 2nm The voltage range chosen is the region where there is good gate control and FET-like behavior

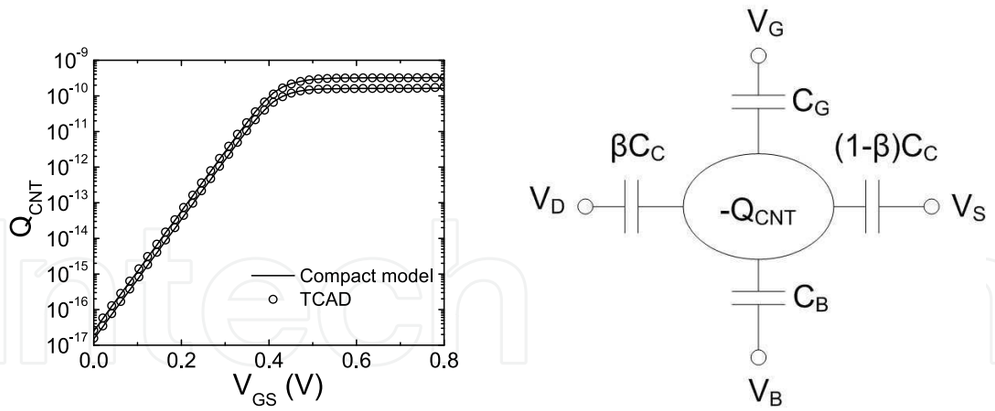
2006) use some kind of self-consistent numerical methods to solve for ϕ_s. Fig. 5(b) shows the variation of surface potential as a function of V_{GS} and V_{DS}, for different diameters. At low voltages, the model is in good agreement with the numerical simulations and no regional approximations are required in the expression. The surface potential is a function of the diameter, temperature and gate dielectrics to the first order. At higher voltages, higher sub-bands are filled and therefore the slope of the line in Fig. 5(b) changes and this behavior is modeled by (8).

1.3 Capacitance Model

Surface potential is calculated using (3), a function of Q_{CNT}. However, Q_{CNT} itself is a function of ϕ_s and most other models employ self-consistent iterations to solve for charge and surface potential. As explained in the previous subsection, we approximate the charge in each sub-band to be linear to get a closed form solution for surface potential. With ϕ_s known, the quantum charge Q_{CNT} can be calculated in closed form as well. Fig. 5 shows a plot of quantum charge calculated with respect to varying gate voltage for V_{DS}=0.2 and 0.8V.
Rate of change of quantum charge with respect to gate voltage is given by

$$\frac{\partial Q_{CNT}}{\partial V_G} = \frac{\partial Q_{CNT}}{\partial \phi_s} \frac{\partial \phi_s}{\partial V_G} \tag{9}$$

where the term $\partial Q_{CNT}/\partial \phi_s$ is known as quantum capacitance, C_Q. Since the model shows excellent agreement with TCAD simulations is demonstrated for Q_{CNT} vs. V_G (Fig. 5) and ϕ_s vs. V_G (Fig. 4), the effect of quantum capacitance is implicit and need not be calculated separately. A capacitance branch model similar to (Deng, 2007), shown in Fig. 5(b), is used to calculate the intrinsic voltages that are effective inside the channel.
Extrinsic capacitance such as parasitic fringe capacitance, inter-electrode capacitance and coupling capacitance between adjacent gates in multiple gate/multiple nanotube device geometries can dominate over the intrinsic capacitance and impact the performance of a CNT-FET. A provision for including non-ideal extrinsic capacitance has been incorporated in our compact model in the form of parasitic capacitance, C_p, which is a fitting parameter. The exact value



(a) (b)

Fig. 5. (a) Q_{CNT} as a function of V_{GS} for V_{DS}=0.2V and 0.8V and CNT diameter 1nm. (b) The capacitance divider network used in the model. C_C and β are fitting parameters.

of C_p is device-geometry dependent and can be estimated from the expressions in (Deng & Wong, 2007b; John & Pulfrey, 2006; Paul et al., 2006).

1.4 Schottky Barrier modeling

The Schottky barrier height ϕ_{SB} depends on the work function difference and the barrier width depends on the insulator thickness. The total current at the junction is the sum of thermoionic emission and the tunneling current through the barrier. Hence it is important to accurately model carrier conduction in a CNT FET through the Schottky barrier. Transmission coefficients for a single barrier are calculated using the WKB approximation (Nakanishi et al., 2002) as follows

$$T(E) = exp\left[-\int_{z_i}^{z_f} k(z)dz\right] \tag{10}$$

The WKB approximation does not take into account reflection between the source and drain junctions. The conductance of the actual device is lower than calculated (Heinze et al., 2002). The Fabry-Perot Cavity model is used to include the effect of reflection given as

$$T(E) = \frac{T_s(E)T_d(E)}{T_s(E) - T_s(E)T_d(E) + T_d(E)} \tag{11}$$

The WKB approximation (D.Jimenez, Jan 2007) has two exponential terms in the E-k space which does not have a closed form solution. Approximating the barrier profile as a triangle allows us to get a closed form solution and results in negligible loss in accuracy. Extending on the derivation in (D.Jimenez, Jan 2007), we have the following

$$E - E(z) = \pm\frac{3a}{2}V_\pi\sqrt{{k_n}^2 + {k_z}^2}$$

where
$E(z)$=energy profile of conduction/valence band
k_n=momentum component of nth sub-band

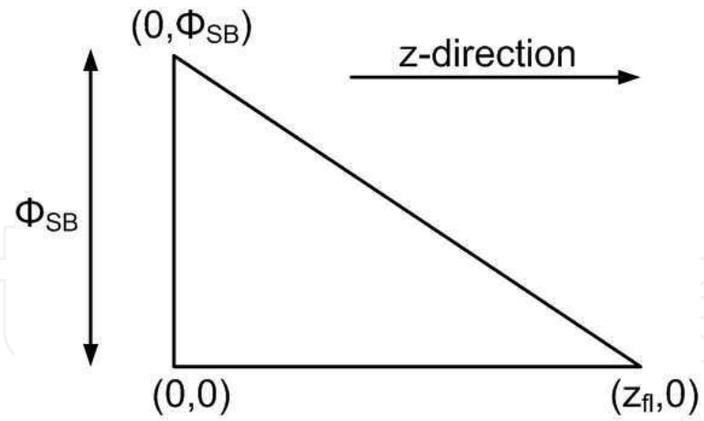


Fig. 6. Triangular Schottky Barrier Height model used in deriving the closed form expression for Tunneling Probability.

k_z=momentum component along direction of electron transport
$a = 0.142nm$, the carbon-carbon bond distance
Hence

$$k_z = \sqrt{\frac{4\left[E - E(z)\right]}{(3aV_\pi)^2} - {k_n}^2}$$

Using the value of k_z in (10),

$$T(E) = exp\left[-\int_{z_i}^{z_f} \sqrt{{k_n}^2 - \frac{16\left[E - E(z)\right]^2}{(3aV_\pi)^2}} \right] \tag{12}$$

In order to get an expression for $E - E(z)$, a triangular barrier profile as shown in Fig. 6 is used, which gives us

$$\begin{aligned} E(z) &= -\frac{\phi_{sb}}{z_{fl}}(z) + \phi_{sb} \\ E - E(z) &= E - \phi_{sb} + \frac{\phi_{sb}}{z_{fl}}(z) \end{aligned} \tag{13}$$

From (12) and (13), we get a closed form expression for tunneling probability in (14). The limits of the integration are $z_i = 0$ and $z_f = z_{fl}$, where $z_{fl} = [-t_{ins}/2]ln(E/\phi_{sb})$.

$$T(E) = exp\left[\frac{-t_{ins}k_n}{\phi_{sb'}} \left(E' \sqrt{1 - K'^2} + (E - \phi_{sb'})E_t \right) \right] \tag{14}$$

where

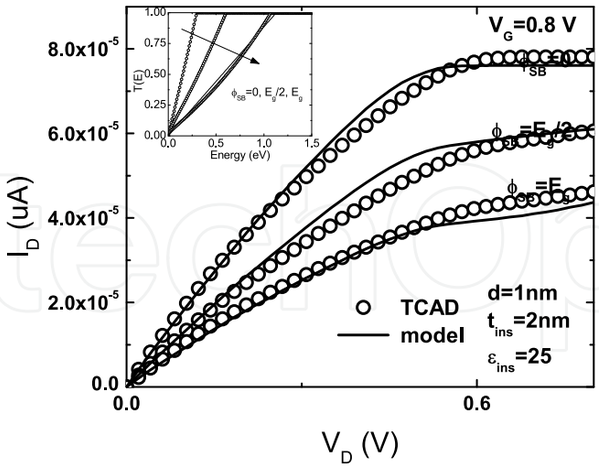


Fig. 7. I_{ds} vs. V_{ds} at V_{gs}=0.8V for three different barrier heights. The inset shows the variation in the tunneling probability (numerical vs. triangular approximation) for the different contacts.

$$
\begin{aligned}
E_t &= \sqrt{\left(1 - K(E - \phi_{sb'})\right)^2} - sin^{-1}(-E'\sqrt{1 - KE'^2}) \\
&\quad + sin^{-1}(\phi_{sb'} - E) \\
K &= \left(\frac{q\pi}{4k_n N_0}\right) \\
E' &= (E - \phi_{sb'}) + \phi_{sb'} ln\left(\frac{E}{\phi_{sb'}}\right) \\
\phi_{sb'} &= \mu_{s,d} + \phi_{sb}
\end{aligned} \tag{15}
$$

Fig. 7 demonstrates the excellent agreement between the triangular approximation model and the numerical model for the contact part. The tunneling probability equation given by (14) is solved at the source and drain junctions and (16) is used to compute the final current.

$$
\begin{aligned}
I = \frac{4q}{h} \sum_n \int_{E_n} & sgn(E)T(E)\Big[F(sgn(E)(E, \mu_s)) \\
& + F(sgn(E), (E, \mu_s - V_{ds}))\Big] dE
\end{aligned} \tag{16}
$$

where $sgn(E) = 1$ or -1 for conduction and valence band respectively and $F(\mu, E)$ is as defined in (5).

Using the equations and results discussed above, (summarized in Table. 1), a physics based compact model of CNT FET is completed and implemented in VerilogA. It is computationally efficient and supports transient simulations. The I-V characteristics are presented in Fig.

Physical constants

V_π	C-C Bonding Energy	2.97eV
a	C-C Bonding Length	0.142nm
q	Charge	$1.6e^{-19}$ C
V_t	Thermal Voltage	26mV

Model Parameters

d	Diameter(m)	θ	Chiral Angle (deg)
L	Nanotube length (m)	t_{ins}	Insulator thickness (m)
ϕ_{sb}	Barrier height (eV)	ϵ_{ins}	Insulator Dielectric Constant

Derived Parameters

Energy Gap (eV)	$E_g = 2V_{pi}a/d$
Sub-band Energy Levels (eV)	$E_n = (E_g/8)(6n - 3 - (-1)^n)$
Intrinsic Carrier Conc.	$N_0 = 4q/(3\pi V_\pi a)$
Insulator Capacitance	$C_{ins} = \frac{2\pi\epsilon_r\epsilon_0}{\log((t_{ins}+d/2)/(d/2))}$

Table 1. Constants and Parameters used in the Model

8(a). These results prove that the model is scalable to different diameters and bias conditions. Since we use the surface potential approach, scattering effects that may further affect the I-V characteristics can be easily incorporated in the future.

2. Transistor Model Validation and Extraction

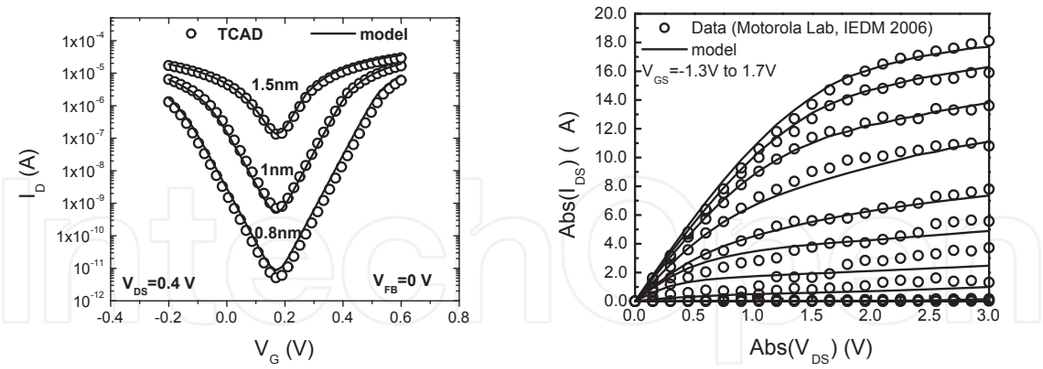
The parameters enlisted in Table 2 comprise the SPICE based circuit model for CNT FET. Running simulations by varying each parameter enables us to gain detailed insight on its impact on the design potential of the CNT FET.

2.1 Extraction procedure

Our compact model can be used to comprehend measurement data in order to gain process-related insight such as parasitics, variations etc. This is achieved by properly tuning the model parameters enlisted in Table 2. A capacitor divider network similar to (Deng, 2007) is assumed in this model, as shown in Fig. 5(b). C_C, the coupling capacitance and β are the two primary fitting paramters from this network.

Scattering effects are not directly incorporated in the model. The fitting parameter *mob* is used to capture the effect of scattering in the nanotube and is multiplied to the final current computed in (16) in the model. *mob* value is dependent on the length of the nanotube and lies between 0 and 1. Appropriate values for this parameter can be obtained from published results (Deng, 2007) .The main fitting steps are

1. Define instance parameters; calculate physical parasitics (C_C is set to a very small value, which is about 1/10 of the insulator capacitance).
2. Csubfit: tuned to fit I_{DS} vs. V_{GS} at low V_{DS} (0.1V) and V_{BS} fixed. This is to match the flat bland voltage.



(a) (b)

Fig. 8. (a) I_{ds} as a function of V_{gs} for d=0.8nm, 1nm and 1.5nm. $V_{FB} = 0V$ $t_{ins} = 2nm$ $\epsilon_r = 25$ and $L = 10nm$. (b) Model validation with experimental data. Both scales show absolute values of drain voltages and currents (Amlani et al., 2006).

3. β: tuned to fit I_{DS} vs. V_{DS} at a high V_{GS} to match the saturation region (basically the shape of the I_{DS} vs. V_{DS} curve).
4. C_p: tuned to match I_{DS} vs. V_{GS} in the subthreshold region, at high V_{DS}; ϕ_{SB} also needs to be tuned to match I_{DS} vs. V_{GS} in the saturation region.
5. $R_{D,S}$: tuned to primarily match I_{DS} vs. V_{DS} in the linear region. $R_{D,S}$ also affects the saturation region. Hence, iterations may be required to get the correct fit.
6. *mob*: used to match the saturated drain current.

2.2 Model Validation

Using the extraction procedure described in the previous section, the model has been validated with published measurement data (Amlani et al., 2006) as shown in Fig. 8(b). An interesting feature of the fitting is the exact replication of the gap in the I-V plot, which is due to the multiple band conduction in carbon nanotubes.
The I-V characteristics in general have the following trends:

- The off current varies exponentially with diameter and barrier height.
- The on current degrades with barrier height and increases linearly with diameter.

These conclusions have been confirmed in previous models. But the new model helps us run SPICE simulations fast enough to benchmark circuits performance. All the results in the next section are generated using the Verilog-A model that supports DC and transient analysis for a single inverter several times faster than numerical simulations in MATLAB.

3. Interconnect modeling

Metallic CNT possess properties of high mechanical and thermal stability, thermal conductivity and high current carrying capabilities (Naeemi et al., Feb. 2005)(Srivastava & Banerjee,

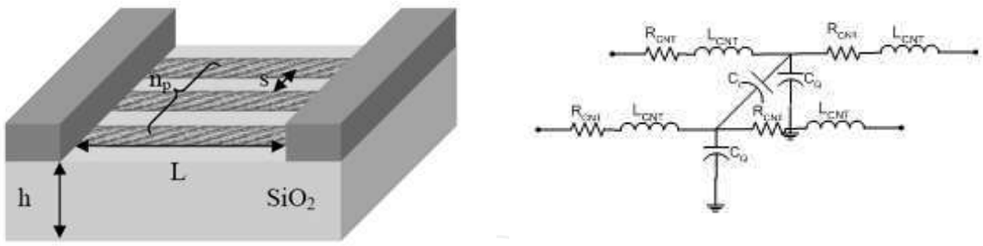
Parameter	Description	Default (units)
Instance Parameters		
d	Diameter	2nm
θ	Chiral angle $(0 \leq \theta < 30^o)$	0
$tins$	Insulator thickness	10nm
$eins$	Dielectric constant of insulator	9
$tback$	Backgate insulator thickness	130nm
$eback$	Dielectric constant of substrate	3.9 (SiO_2)
L	Gate length	100nm
$type$	n-type=1 p-type= -1	1
Model Parameters		
$phisb$	Schottky barrier height	0eV
mob	Mobility parameter	1
R_s	Parasitic Source access resistance	0 ohm
R_d	Parasitic Drain access resistance	0 ohm
β	Coupling Coefficient	1
C_C	Coupling Capacitance	7aF
C_p	Parasitic Capacitance	120aF

Table 2. Spice Model File Parameters

2005) making them candidates for interconnects. Ideally, metallic SWCNT's have a fermi velocity of about $8X10^5$ m/s (M.S. Dresselhaus & Eklund, 1996) but in reality the ballistic motion is degraded by several scattering mechanisms. The scattering mechanisms has been been discussed in several previous publications (Park et al., 2004; Raychowdhury & Roy, 2006). The resistance is normally modeled by a set of piece-wise linear equations. In this work we present a continuous expression for the resistance of the interconnect and the resistance of the contact making them suitable for SPICE simulators. For the sake of simplicity, the effect of temperature on resistance has not been included in this model. For a detailed discussion on the effect of temperature on resistance of metallic CNTs, the reader is referred to (Pop et al., 2007). The circuit model for the interconnect is shown in Fig. 9(b). At high frequencies, the inductance and the capacitance determine the total impedance of the interconnect. The following subsections present the DC and small-signal parameters of the CNT interconnect.
Due to the nature of the band structure, in an ideal ballistic motion regime, the resistance is constant as expressed in (17)

$$R_{ballistic} = \frac{h}{4e^2} = \frac{1}{G_0} \tag{17}$$

However, when the length of the interconnect is much longer that the mean free path (MFP), several scattering mechanisms dominate. At low bias, the predominant mechanism is the acoustic phonon scattering with a MFP of $1\mu m - 1.6\mu m$ Park et al. (2004). As the bias voltage increases, the electrons can scatter from band to band and also within the same band. This



(a) (b)

Fig. 9. (a) Cross-section of a generic interconnect using carbon nanotubes. (b) Circuit model for CNT interconnect

leads to optical phonon scattering and zone-boundary scattering. These scattering mechanisms are well-known and have been modeled in the past. In this compact model, we derived a single equation to continuously model all these scattering effects across multiple regions as shown in (18),

$$G(V,L) = G_{op\_zo} + \frac{V_{eff}[G_{acc} - G_{op\_zo}]}{V} \tag{18}$$

where

$$V_{eff} = V_{cr} - \frac{1}{2}\left[(V_{cr} - V - \delta) + \sqrt{(V_{cr} - V - \delta)^2 + 4V_{cr}\delta}\right]$$

3.1 Resistance

Here a piece-wise linear model for resistance (Raychowdhury & Roy, 2006) is modified by including V_{eff} which ensures that mobility is a continuous function of the bias voltage and length facilitating convergence in circuit simulators . The dependence of length and bias voltage on the resistance of a CNT interconnect is shown in Fig. 10(a).

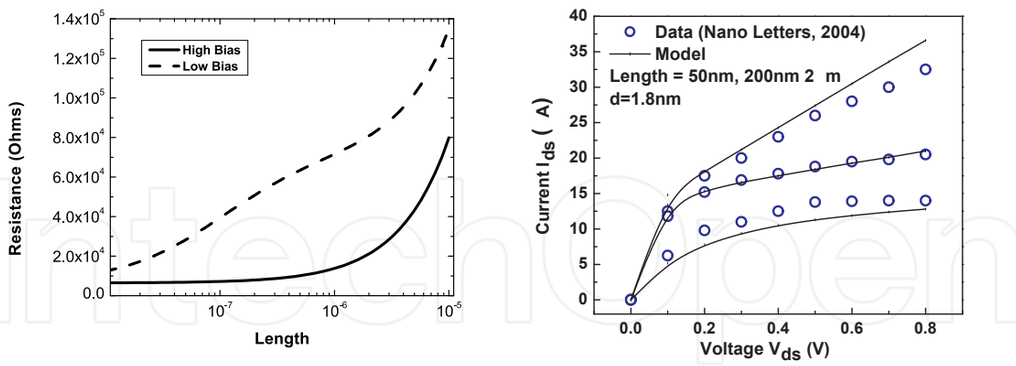
3.2 Capacitance and Inductance

As shown in Fig. 9(a) carbon nanotube interconnects are usually formed by arranging arrays of nanotubes aligned next to each other with the terminals at the ends of the two tubes. The coupling capacitance between two adjacent nanotubes C_C, and the quantum capacitance within the nanotube C_q have considerable effect on its conduction properties. The coupling capacitance has the form

$$C_c = \frac{\pi\epsilon L}{log\left(\frac{d}{S} + \sqrt{\left(\frac{d}{S}\right)^2 + 1}\right)} \tag{19}$$

And the quantum capacitance is given by

$$C_q = \frac{4e^2 L}{\pi h v_f} \tag{20}$$



(a) (b)

Fig. 10. (a) Resistance of a carbon nanotube interconnect with varying length for high and low bias across the terminals. (b) Interconnect model validation with measured data for varying length. Diameter of the metallic nanotubes are 1.8nm.

Carbon nanotubes posses two kinds of inductances, the magnetic or mutual inductance and the kinetic or self-inductance. As discussed in detail in (Raychowdhury & Roy, 2006), kinetic inductance dominates mutual inductance in a one-dimensional structure like carbon nanotubes and hence we only consider kinetic inductance in the model. This is given by

$$L_e = \frac{h}{2e^2 v_f} \tag{21}$$

Carbon nanotubes have two modes of propagation, with two electrons in each mode (spin up and spin down). This results in a total of four modes of propagation giving one-fourth of the total inductance calculated in (21) and four times the quantum capacitance given in (20).

3.3 Interconnect model extraction and verification

Three model parameters, V_{crit}, l_{acc} and l_{zb} are used to model the optical phonon scattering, acoustic phonon scattering and zone boundry phonon scattering respectively. The SPICE circuit parameters for the interconnect model are enlisted in Table 3.
The rest of the parameters are geometry dependent.

1. Coupling capacitance is either calculated by external 2D or 3D solvers such as Raphael (*Raphael Interconnect Analysis Program Reference Manual*, n.d.) and entered as an instance parameter, or can be calculated internally by (19).
2. If CNT length ranges between 10nm and 1μm, V_{crit} is tuned in the range of 0.08 to 0.16 to decrease the resistance. If CNT length is greater than 1μm, acoustic phonon scattering dominates and therefore l_{acc} changes the slope of the curve.
3. If the contacts are short and ohmic then R_n and R_p can be ignored.
4. At high current values the ϕ_{SB} value is extracted.

The model is validated against measured data in Fig. 10(b).

Parameter	Description	Default value
Instance		
d	Diameter	1nm
np	Number of CNTs in parallel	1
s	Spacing between CNTs	10nm
e_{ins}	Dielectric constant of insulator	25
Cc	Coupling Capacitance	0
h	Substrate insulator thickness	100nm
L	Gate length	100nm
Model		
$phisb$	Schottky Barrier height	0eV
V_{crit}	Optical-phonon scattering parameter	0.16eV
R_p, R_n	Parasitic Access Resistance	0 ohm
l_{acc}	Mfp for acoustic phonon scattering	1.0 um
l_{zb}	Mfp for zone boundary phonon scattering	20nm

Table 3. Interconnect Model File Parameters

4. Design Insights

The developed compact model for CNT transistors accurately predicts I-V and C-V characteristics. It is scalable to key process and design parameters such as diameter, chirality, gate dielectrics, and bias voltages. Using the model, we explore design possibilities with CNT in order to identify the optimum design space. CNT with L=100nm is compared with 22nm CMOS (PTM) for both analog and digital applications. For consistency we have used $V_{FB} = Vdd/2$(NCNT) and $-Vdd/2$(PCNT). The dielectric material used has ϵ_r = 25. Parasitic capacitances have been lumped into a single parameter based on published values (J. Deng, Sept.2006). Since all the characteristics are mainly dependent on the diameter of the nanotube, our analysis is for varying diameters. Above 1.8nm, the SB-FET has I_{ON}/I_{OFF} less than 50 and is not included in this study.

4.1 Digital Design

Numerous simulations of FO4 inverter comparing CNT FETs with 22nm CMOS have been undertaken to study the effect of Schottky barrier height (Source/Drain contact material), gate dielectric thickness, leakage power, supply voltage scaling and process variations on digital design (Balijepalli et al., 2007). It is found that for smaller diameters of the range of 1-1.5nm and optimum contact materials, up to 10X improvement in speed, power and energy consumption is observed as compared to 22nm CMOS. The speed contours have been plotted for adequate scaling in dielectric thickness to ensure the same performance. By varying the diameter, Fig. 11 shows that up to 10X increase in speed can be achieved when compared to 22nm CMOS.

The reason for diameters of 1-1.5nm being optimal is depicted by the shaded region in the Fig. 11. Larger diameters have higher leakage and are harder to switch off. Smaller diameters have

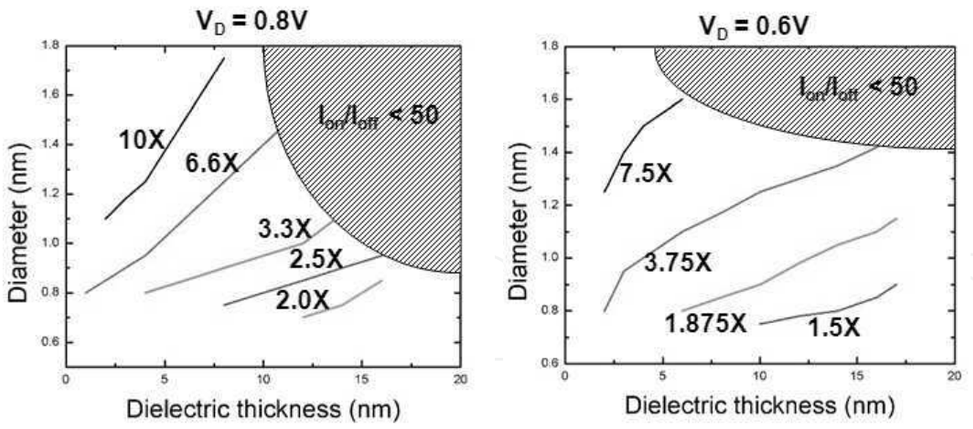


Fig. 11. Speed contours for varying diameters and t_{ins} for V_{DD} = 0.8V and 0.6V

a 5X decrease in speed compared to larger diameter CNTs. Thus, there is a trade-off between speed and power in using CNT FET for digital applications, similar as that of CMOS.

4.2 Analog Design

If parasitic capacitance is reduced, CNTs have another advantage in very low quantum capacitance. The device can have very high cut-off frequency given by (Akinwande et al., 2006).

$$f_T = \frac{g_m}{2\pi C_g} \tag{22}$$

Based on the above equation, cut-off frequency for a 2nm diameter CNT transistor is calculated to be around 120 GHz in our model. An in-depth critique of the high frequency performance of carbon nanotube field effect transistors is given in (Pulfrey & Chen, 2008) which discusses the effect of nanotube chirality (diameter), oxide permittivity and other process parameters on f_T. These effects can be incorporated in our model with minimal effort.

The two major hurdles preventing large scale manufacturing of CNT based devices are lack of measurement technique to characterize analog performance and reducing the parasitic capacitance during fabrication. The AC gain and frequency response are mainly controlled by the transconductance (g_m) and output impedance (R_{out}). Here we plot the variation of output impedance of CNT FET compared to 22nm CMOS (Fig. 12). For a fair comparison, R_{out} is calculated for the same saturation current of both devices. For CMOS, R_{out} vs. V_{DS} is mainly influenced by the triode region, channel length modulation, drain induced barrier lowering (DIBL) and finally substrate current induced body effect (SCBE) with increasing V_{DS} (Huang et al., 1992). In CNTs, R_{out} is affected by the linear, saturation and ambipolar characteristics of the device. As shown in Fig. 12, due to better saturation characteristics in CNTs, a CNT FET can have up to 25X higher R_{out} compared to 22nm CMOS for the same saturation current.

5. Conclusion

In this chapter, a detailed procedure for developing compact models for carbon nanotube transistors and interconnects has been presented. Since the developed model does not use any iteration-based calculations, is scalable with process and design parameters and is highly accurate, it increases the scope of predictive design research. These models have been used for

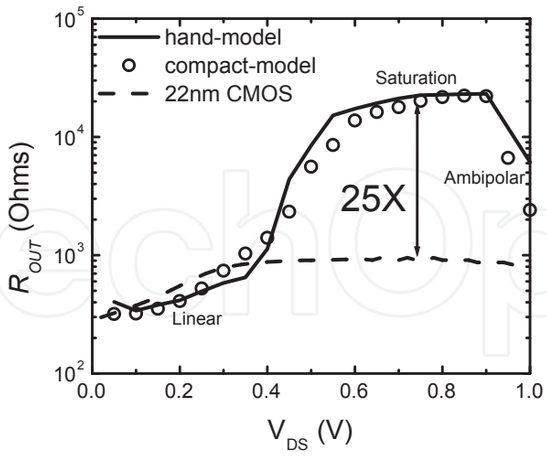


Fig. 12. R_{out} as a function of drain voltage, compared with 22nm CMOS with same saturation current. Regions affecting R_{out} are annotated.

circuit simulation to benchmark the performance of carbon nanotube transistors with 22nm bulk CMOS transistors providing important perspective on the design trade-offs and potential of CNT based devices. Thus, compact modeling serves as one of the most important bridges between CNT process and design giving key insights into the development of carbon nanotube based electronics.

6. References

Akinwande, D., Close, G. F. & Wong, H.-S. P. (2006). Analysis of the Frequency Response of Carbon Nanotube Transistors, *Nanotechnology, IEEE Transactions on* **5**(5): 599 – 605.

Amlani, I., Lewis, J., Lee, K., Zhang, R., Deng, J. & Wong, H.-S. P. (2006). First demonstration of ac gain from a single-walled carbon nanotube common-source amplifier, pp. 1–4.

Balijepalli, A., Sinha, S. & Cao, Y. (2007). Compact modeling of carbon nanotube transistor for early stage process-design exploration, *ISLPED '07: Proceedings of the 2007 international symposium on Low power electronics and design*, ACM, New York, NY, USA, pp. 2 – 7.

Bowman, K. A., Duvall, S. G. & Meindl, J. D. (2002). Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration, *Solid-State Circuits, IEEE Journal of* **37**(2): 183 – 190.

Castro, L., John, D. & Pulfrey, D. (2002). Towards a compact model for schottky-barrier nanotube fets, pp. 303–306.

Chau, R., Datta, S., Doczy, M., Doyle, B., Kavalieros, J. & Metz, M. (2004). High-κ/MetalñGate Stack and Its MOSFET Characteristics, *IEEE Electron Device Lett.* **25**(2004): 408 – 410.

Chen, I. C., Holland, S. & Hu, C. (February 1985). Electrical Breakdown in Thin Gate and Tunneling Oxides, *IEEE Trans. Electron Devices* **32**: 413 – 422.

Chen, Z., Appenzeller, J., Knoch, J., Lin, Y.-M. & Avouris, P. (2005). The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors, *Nano Lett.* **5**: 1497 – 1502.

Close, G. F. & Wong, H.-S. P. (2007). Fabrication and Characterization of Carbon Nanotube Interconnects, *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* pp. 203 – 206.

Deng, J. (2007). A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its applicationópart i: Model of the intrinsic channel region.

Deng, J. & Wong, H.-S. (2007a). A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its ApplicationóPart I: Model of the Intrinsic Channel Region, *Electron Devices, IEEE Transactions on* **54**(12): 3186 – 3194.

Deng, J. & Wong, H.-S. (2007b). Modeling and analysis of planar-gate electrostatic capacitance of 1-d fet with multiple cylindrical conducting channels, *Electron Devices, IEEE Transactions on* **54**(9): 2377–2385.

D.Jimenez, e. (Jan 2007). A simple drain current model for schottky-barrier carbon nanotube field effect transistors, *Nanotechnology* **18**(2): 025201. ID: 61221.

Doyle, B., Boyanov, B., Datta, S., Doczy, M., Hareland, S., Jin, B., Kavalieros, J., Linton, T., Rios, R. & Chau, R. (2003). Tri-Gate fully-depleted CMOS transistors: Fabrication, design and layout, *VLSI Symp. Tech. Dig.* pp. 133 – 134.

Guo, J., Datta, S, Lundstrom & M (2004). A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors, *Electron Devices, IEEE Transactions on* **51**(2): 172 – 177.

Guo, J. & Lundstrom, M. (2006). *Nanoscale Transistors: Device Physics, Modeling and Simulation*, Springer.

Guo, J., Lundstrom, M. & Datta, S. (2002). Performance projections for ballistic carbon nanotube field-effect transistors, *Applied Physics Letters* **80**(17): 3192–3194.
URL: *http://link.aip.org/link/?APL/80/3192/1*

Heinze, S., Tersoff, J., Martel, R., Derycke, V., Appenzeller, J. & Avouris, P. (2002). Carbon nanotubes as schottky barrier transistors, *Phys. Rev. Lett.* **89**(10): 106801.

Hisamoto, D., Lee, W.-C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T.-J., Bokor, J. & Hu, C. (2000). FinFET-a self-aligned double-gate MOSFET scalable to 20 nm, *IEEE Trans. Electron Devices* **47**(12): 2320 – 2325.

Huang, J. H., Liu, Z. H., Jeng, M. C., Ko, P. K. & Hu, C. (1992). A physical model for MOSFET output resistance, *Electron Devices Meeting, 1992. Technical Digest., International* pp. 569 – 572.

J. Deng, H.-S. W. (Sept.2006). *A circuit-compatible SPICE model for enhancement mode carbon nanotube field effect transistors*, Synopsys Inc.

John, D. L. & Pulfrey, D. L. (2006). Switching-speed calculations for schottky-barrier carbon nanotube field-effect transistors, **24**(3): 708–712.
URL: *http://link.aip.org/link/?JVA/24/708/1*

Lin, Y.-M., Appenzeller, J., Chen, Z., Chen, Z.-G., Cheng, H.-M. & Avouris, P. (2005). High performance dual-gate carbon nanotube FETs with 40-nm gate length, *IEEE Electron Device Lett.* **26**: 823 – 825.

McEuen, P. L., S, F. M. & Park, H. (2002). Single-walled carbon nanotube electronics, *Nanotechnology, IEEE Transactions on* **1**(1): 78 – 85.

Moore, G. E. (1965). Cramming more components onto integrated circuits, *Electronics* **38**(8).

M.S. Dresselhaus, G. D. & Eklund, P. (1996). *Science of Fullerenes and Carbon Nanotubes*, Elsevier Inc.

Naeemi, A., Sarvari, R. & Meindl, J. D. (Feb. 2005). Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI), *IEEE Electron Device Lett.* **26**(2): 84 – 86.

Nakanishi, T., Bachtold, A. & Dekker, C. (2002). Transport through the interface between a semiconducting carbon nanotube and a metal electrode, *Phys. Rev. B* **66**(7): 073307.

Park, J.-Y., Rosenblatt, S., Yaish, Y., Sazonova, V., Ustunel, H., Braig, S., Arias, T. A., Brouwer, P. W. & McEuen, P. L. (2004). Electron-Phonon Scattering in Metallic Single-Walled Carbon Nanotubes, *Nano Lett.* **4**(3): 517 – 520.

Paul, B., Fujita, S., Okajima, M. & Lee, T. (2006). Impact of geometry-dependent parasitic capacitances on the performance of cnfet circuits, *Electron Device Letters, IEEE* **27**(5): 380–382.

Pop, E., Mann, D. A., Goodson, K. E. & Dai, H. (2007). Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates, *Journal of Applied Physics* **101**(9): 093710.
URL: *http://link.aip.org/link/?JAP/101/093710/1*

Pulfrey, D. L. & Chen, L. (2008). Examination of the high-frequency capability of carbon nanotube fets, *Solid-State Electronics* **52**(9): 1324 – 1328. Papers Selected from the 37th European Solid-State Device Research Conference - ESSDERC'07.
URL: *http://www.sciencedirect.com/science/article/B6TY5-4ST45Y8-1/2/35986f4a38a6adca353dfae27fc40cf2*

Raphael Interconnect Analysis Program Reference Manual (n.d.). Synopsys Inc.

Raychowdhury, A., Keshavarzi, A., Kurtin, J., De, V. & Roy, K. (2006). Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits-DC Analysis and Modeling Toward Optimum Transistor Structure, *Electron Devices, IEEE Transactions on* **53**(11): 2711 – 2717.

Raychowdhury, A., Mukhopadhyay, S. & Roy, K. (2004). A circuit-compatible model of ballistic carbon nanotube field-effect transistors, *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* **23**(10): 1411 – 1420.

Raychowdhury, A. & Roy, K. (2006). Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies, *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* **25**(1): 58 – 65.

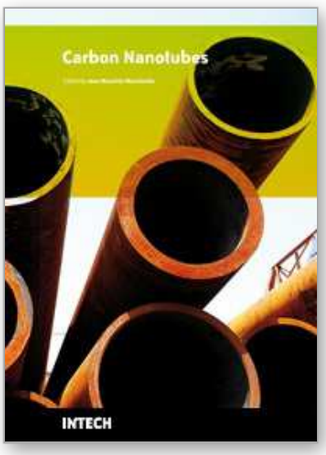
Srivastava, N. & Banerjee, K. (2005). Performance analysis of carbon nanotube interconnects for vlsi applications, *Computer-Aided Design, 2005. ICCAD-2005. IEEE/ACM International Conference on* pp. 383–390.

Wann, C. H., Noda, K., Tanaka, T., Yoshida, M. & Hu, C. (October 1996). A Comparative Study of Advanced MOSFET Concepts, *IEEE Transactions on Electron Devices* **Vol. 43**(No. 10): 1742 – 1753.

Welser, J., Hoyt, J. L. & Gibbons, J. F. (1994). Electron mobility enhancement in strained-Si n-type metal-oxideñsemiconductor field-effect transistors, *IEEE Electron Device Lett.* **15**(3): 100 – 102.

Wong, H.-S., Deng, J., Hazeghi, A., Krishnamohan, T. & Wan, G. (Nov. 2006). Carbon nanotube transistor circuits - models and tools for design and performance optimization, *ICCAD* pp. 651–654.

Zhang, G., Wang, X., Li, X., Lu, Y., Javey, A. & Dai, H. (2006). Carbon Nanotubes: From Growth, Placement and Assembly Control to 60mV/decade and Sub-60 mV/decade Tunnel Transistors, *Electron Devices Meeting, 2006. IEDM '06. International* pp. 1 – 4.



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This book has been outlined as follows: A review on the literature and increasing research interests in the field of carbon nanotubes. Fabrication techniques followed by an analysis on the physical properties of carbon nanotubes. The device physics of implemented carbon nanotubes applications along with proposed models in an effort to describe their behavior in circuits and interconnects. And ultimately, the book pursues a significant amount of work in applications of carbon nanotubes in sensors, nanoparticles and nanostructures, and biotechnology. Readers of this book should have a strong background on physical electronics and semiconductor device physics. Philanthropists and readers with strong background in quantum transport physics and semiconductors materials could definitely benefit from the results presented in the chapters of this book. Especially, those with research interests in the areas of nanoparticles and nanotechnology.

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