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Dimension Increase in Metal-Oxide-Semiconductor Memories and Transistors

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1. Introduction

This chapter describes a trend in dimension increase in structures of semiconductor memories and transistors focusing on metal-oxide-semiconductor, MOS devices. One, two, and three-dimensional (3-D) structures correspond to a legacy of grown-junction bipolar transistor, planar MOS transistor, and trench-capacitor dynamic-random-access memory, DRAM (Sunami et al., 1982-b & 1984), respectively. Flash memory has recently begun to employ 3-D stack of memory cells (Endoh et al., 2001).

To maintain the sufficient margin in DRAM operation, storage capacitance value should be kept as big as possible against scaling of memory cell area. In response to the requirement, 3-D capacitor has been introduced. The capacitor can be increased with the increase in the height of the capacitor without enlargement of planar area of the memory cell. First commercially available trench-capacitor DRAM appeared in mid 1980's at 1-M bit era together with stack-capacitor cell (Koyanagi et al., 1982). Recent stack-capacitor DRAM has begun to utilize a 3-D cylindrical capacitor same as trench capacitor cell.

While, MOS transistor has been shrunk continually from 12 μm to 45 nm with planar 2-D structure since early 1970's to date. An empirical fact that smaller MOS device leads to higher performance was theorized with the scaling theory (Dennard et al., 1968). However, hazardous short channel effects become obvious in sub-μm channel length regime. It is predicted that commercially usable minimum MOS device might be in the range of 5-10 nm. To cope with the short-channel effects vertical-channel transistors such as trench transistor (Richardson et al., 1981), surrounding gate transistor, SGT (Takato et al., 1988), and DELTA (Hisamoto et al., 1991) were proposed. Subsequently they have been extensively investigated these ten years. It is expected that the vertical transistor such as FINFET (Choi et al., 2001) will soon be applied to products to overcome the short-channel effects of 2-D transistor leading to a new era of 3-D LSI.

To summarize device trends in volume and size, increase in device count per chip and shrinkage of feature size are shown in Fig. 1. More than one-million fold increase in the device count has been achieved these 40 years leading to almost the same increase in processor performance. This has been driving enormous development of electronics and information technology.

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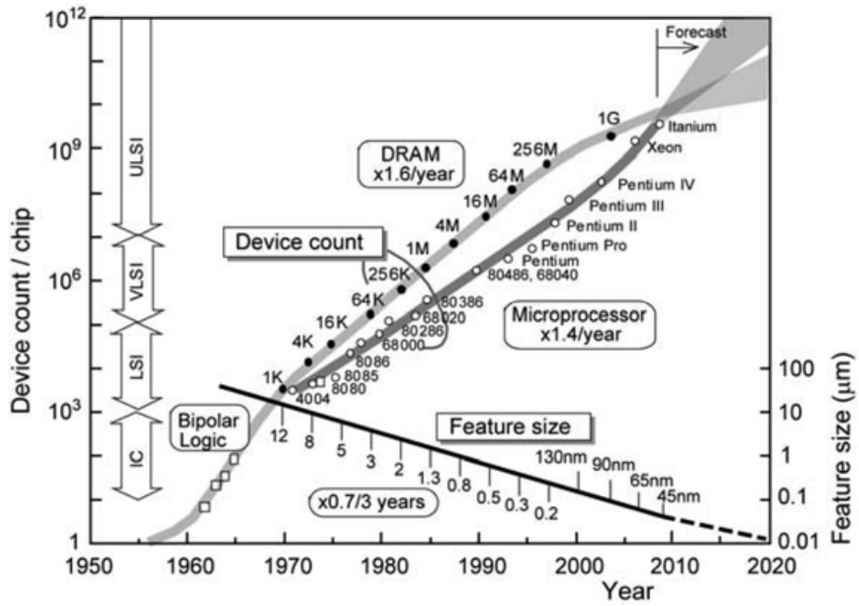


Fig. 1. Trends in device count/chip and feature size of MOS device. A DRAM cell consists of two devices of a cell transistor and a storage capacitor.

2. Grown-junction bipolar transistor as 1-D structure

It is well known that the first transistor invented in mid 1940's was a point-contact germanium bipolar transistor. Then, grown-junction type bipolar transistor became the first commercially successful semiconductor device (Teal et al., 1951). Although real devices are actually fabricated in 3-D structure, an operation mechanism of this bipolar transistor is based on 1-D current flow in principle.

Bipolar devices had been dominant in semiconductor market until early 1970's, and then MOS devices took over their position featuring less power consumption, denser packing, superior thermal stability, etc. Bipolar devices still survive in limited applications in fields of figh-frequency low-noise, inexpensive small scale IC, and high power. Besides, a kind of combination structure of bipolar and MOS transistors is insulated-gate bipolar transistor, IGBT. IGBT utilizes both an advantage of voltage-driven gate of MOS transistor and that of high current drivability of bipolar transistor. IGBT becomes a major device in power electronics such as electricity control in electric and hybrid cars.

No further description is made in this chapter since the major topic here is "scaling and higher integration of semiconductor device."

3. Invention of trench-capacitor DRAM cell as a quasi-3-D structure

3.1 Advent of DRAM

First DRAM was introduced to the market in 1970 by Intel with a 1-Kbit chip using three-transistor DRAM cells (Regitz & Karp, 1970). Subsequently, former 4-Kbit DRAM which was still employing 3-transistor cell began to be installed in IBM's mainframe computers. This was just the time when MOS devices were proven to deserve application as highly reliable main memory in mainframes. Until that time, MOS devices had been regarded as insufficiently stable.

A few years later 4-Kbit DRAM using the one-transistor cell (Dennard, 1968) was being widely manufactured. This memory cell trend is shown in Fig. 2 for equivalent circuit configuration. Since one-transistor cell was much smaller than two of others, very low-cost manufacturing was possible. Its low cost has been contributing to the development of personal computer. Then, the DRAM capacity has been increasing by a factor of four every three years until today. As modern computers are based on von Neumann's architecture, main memory is a key device together with processor. Along with the prosperity of computing, the demand for memory has increased to produce a world-wide 30-B$ market in 2009 for DRAM. Even if the main customer is still personal computer, various applications are extending DRAM's usage, e. g. cell phone, game machine, personal audio, and video machine, etc.

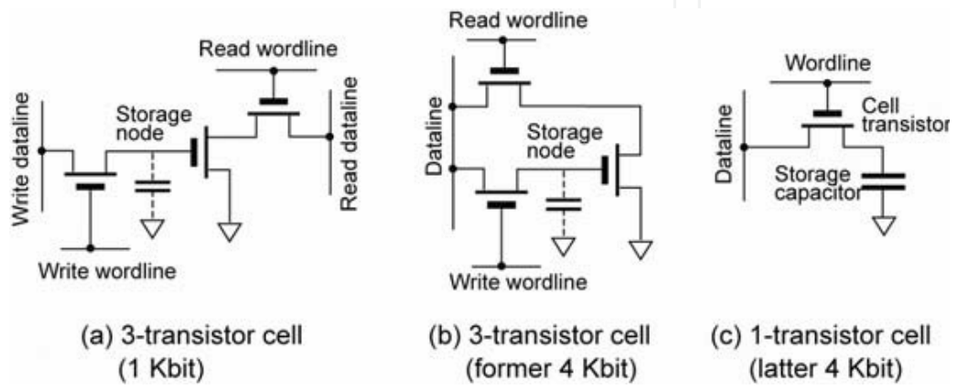


Fig. 2. Trend in DRAM cell configuration.

3.2 Key factor of cost

The strongest driving force for growing of DRAM market is undoubtedly "price". Therefore, various development efforts have been focusing on reduction of manufacturing cost. One of major effort is primarily devoted to finer patterning. The bit cost has decreased by a factor of 10^{-6} during 30 years since 1970, and 1-Gbit product has already been sold at the less price of 1-Kbit. Since chip cost is closely related to number of chips on a wafer, the wafer size has been continually increased to be such as 50, 75, 100, 125, 150, 200, and now 300 mm in diameter. Together with the diameter increase, memory cell size has been reduced to be 1/3 in each DRAM generation in volume production to absorb chip size increase. Consequently, the chip size has been enlarged at most up to 10 times despite the bit increase by a factor of 10^6 from 1 Kbit to 1 Gbit. Then, memory cell size decreases down to a factor of 10^{-5} as shown in Fig. 3.

3.3 Invention of trench-capacitor DRAM cell

In response to chip size reduction to cope with 4-times increase in memory capacity, the memory cell size has been reduced to almost one-third in each generation, previously shown in Fig. 3. The DRAM cell, so-called 1-transistor cell, consists of one cell transistor and one storage capacitor. Key specifications in DRAM operation, such as noise margin, soft-error durability, operational speed, power consumption, strongly depend on the capacitance of storage capacitor (Dennard, 1984). The capacitance value, C_S is expressed as

$$C_S = \epsilon_i A / T_i \tag{1}$$

where ϵ_i, A, T_i, are permittivity of storage insulator, area of capacitor electrode, and insulator thickness, respectively. Therefore, the cell size reduction through scaling leads to the area reduction and subsequent decrease in capacitance value.

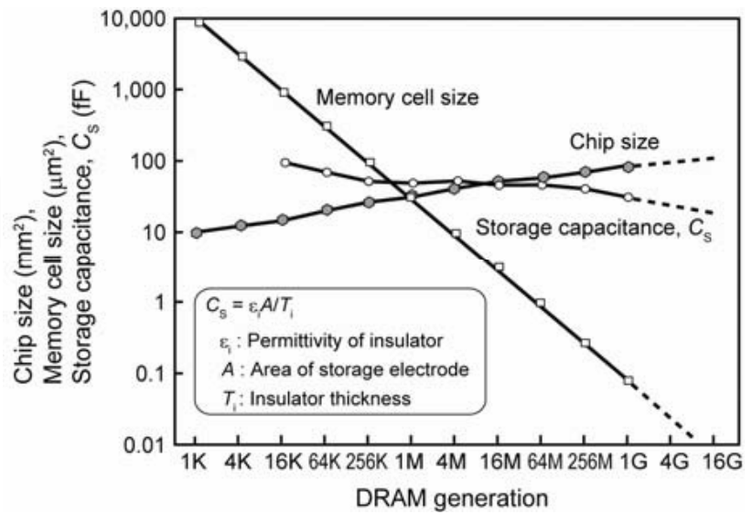


Fig. 3. Memory cell size shrinkage at DRAM in volume production.

To cope with the dilemma as to cell size vs. capacitance, insulator thickness was reduced by a factor of 10 from 100 nm in 1-Kbit to 10 nm in 1-Mbit chips, becoming adversely close to dielectric field breakdown. When the author took a glimpse at some conference presentation from Texas Instruments Inc. in 1974 introducing a highly efficient silicon solar cell with plural steep trenches, as shown in Fig.4 (a), forecasting the upcoming issue of cell size vs. capacitance, he got an idea of a trench capacitor DRAM cell. Even though his job at that time was to characterize the silicon surface with photoemission spectroscopy, his amateur-radio hobby connected the shape of trimmer condenser, which has two coaxial cylindrical opposite electrodes as illustrated in Fig. 4 (b), with the need of the 1-transistor cell. From that idea, he invented a trench capacitor cell and applied for a Japanese patent in 1975 (Sunami and Nishimatsu, 1975). Due to its low score of assessment, this was not applied to any overseas patent.

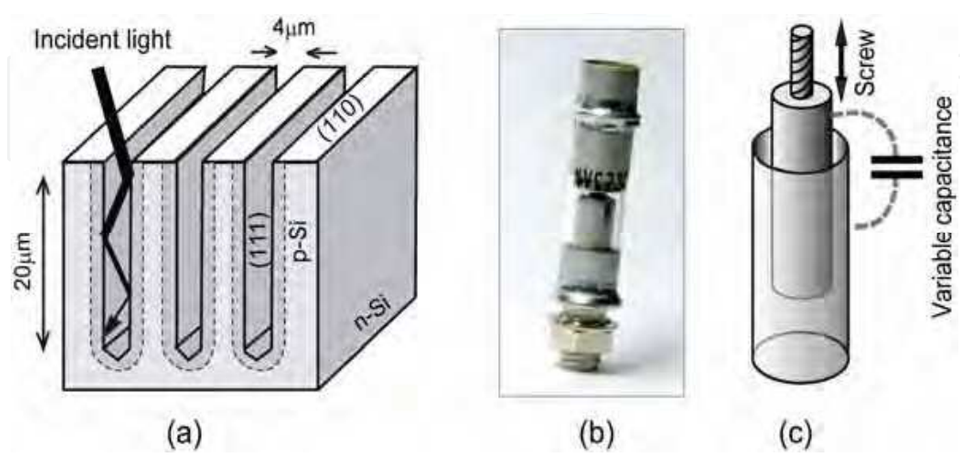


Fig. 4. Hints to create a trench-capacitor DRAM cell concept: proposed solar cell with steep trench, (a), a photograph of trimmer condenser, (b), and its equivalent model, (c).

As Hitachi had won a leader's position in 64-Kbit DRAM products with a 5-V single power supply (Itoh et al., 1980) and folded bit-line arrangement (Itoh, 1975), its research and development group could afford to challenge for novel cell development together with the development of integration processes at 1.3-μm technology node. After several years' development, the first 1-Mbit level trench cell in trial production was successfully implemented and then presented in IEDM (Sunami et al., 1982). The development story is described hereafter.

The memory cell obtained measured 4 μm by 8 μm with a 2.5-μm deep trench. The capacitor insulator is a triple layer of $SiO_2/Si_3N_4/SiO_2$ of which thickness was equivalent to that of 15-nm SiO_2. Resultant capacitance per unit area was 2.2 fF/μm². Then, obtained storage capacitance, C_S with a trench of 2.5 μm in depth and bit-line capacitance, C_B were 45 and 400 fF, respectively with 128-bit folded bit-line arrangement. Resultant C_S/C_B ratio is 0.11. This value is sufficiently large for the stable operation. A scanning-electron micrograph of a cross-section of the cell is shown in Fig. 5.

This first trial 1-Mbit cell array with trenches won a signal voltage of 200 mV at 5-V power supply, as shown in Fig. 6. Since it was empirically recognized that sufficient signal voltage was around 100 mV in those days, an obtained S/N ratio was large enough to obtain stable DRAM operation. Therefore, high immunity to alpha particle hit was being strongly expecxted for coming megabit DRAM products until the time when actual soft-error measurement was made.

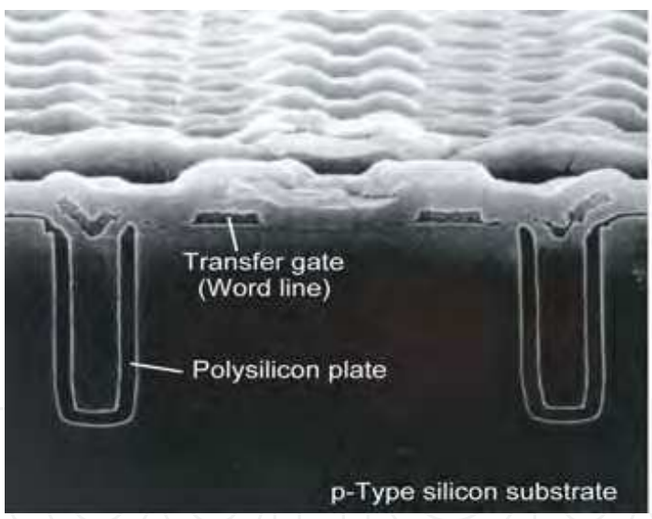


Fig. 5. An SEM cross section of memory-cell array of 1-Mbit DRAM in trial production. The memory cell measures 4 μm by 8 μm.

3.4 Changes of trench cell employment

In a R&D project, 1-Mbit DRAM was a prime vehicle to drive 1.3-μm node MOS technologies, such as lithography, dry etching, film deposition, gate material selection, metallization, etc. except packging. In the course of trench DRAM development, several issues were given birth to. Major ones were

a. degraded oxide uniformity on trench wall, which leads to degradation of oxide integrity,
b. trench to trench leakage which limits further denser packing of cells, and
c. increased soft error which is fatal in application to reliability-conscious computers.

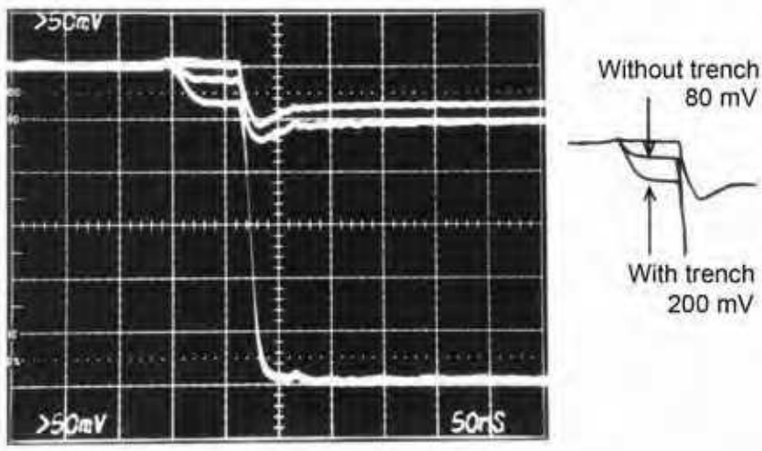


Fig. 6. Output signals of a sense amplifier for a 128-bit folded bit-line cell array with trench of 2.5 μm in depth and that without trench.

Beside these major issues, formation of neat trench shape, avoiding of dislocation formation at the bottom of the trench, high-energy boron implantation into deeper potion of the substrate, uniform capacitor film deposition, polysilicon filling into the trench with phosphorus doping to the polysilicon, etc. should have been solved in a limited period.

a. Oxide uniformity

Crystallographic orientation of trench surface varies resulting in different oxidation rate. It was observed that oxidation rate was higher in order of (110)>polysilicon>(111)>(100). Even though lower oxidation temperature gives rise to more enhanced oxidation rate (Sunami, 1978), this phenomenon still exists at relatively higher temperature range. Thus dielectric breakdown voltage was lowered at the thinnest portion on the trench wall. A transmission-electron micrograph of an experimental result is shown in Fig. 7 in case of 1000°C dry oxidation.

A drastic solution to overcome this problem, it is desirable to utilize chemical-vapor depotion, CVD. An $SiO_2/Si_3N_4/SiO_2$ film was made full use of in trial production. Thickness ratio should be carefully chosen in order to avoid non-volatile memory effect due to the existence of Si_3N_4/SiO_2 interface.

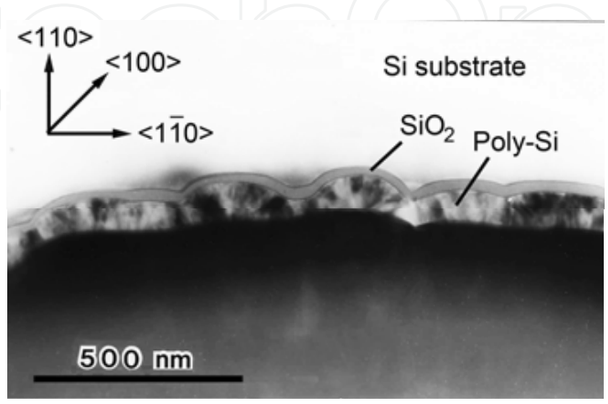


Fig. 7. A transmission-electron micrograph of oxide thickness variation on trench wall with 1000°C dry oxidation.

b. Trench to trench leakage

Another serious problem against further scaling was a leakage current flowing through the deeper portion of adjacent two trenches. The current gradually fills up an empty cell with charges turning "1" into "0". This is a fatal failure for DRAM. This is attributed to a parasitic MOS transistor formed spreading over ajacent two memory cells. Two trenches work as deep source and drain; capacitor plate is the gate; and thick field oxide is the gate oxide. This is regarded as a typical MOS transistor simply causing large punch through current at deeper portion between source and drain.

To outline the leakage current qualitatively, two-dimensional device simulation using CADDET (Toyabe, 1978) was carried out (Sunami et al., 1985). Resultant potential distribution with leakage current flow and a method of leakage current suppression are shown in Fig. 8 (a) and (b), respectively. In the simulation result, one notable fact is that the current flows in the deeper portion of the substrate and a potential mound is located at the substrate surface. These results may be attributable to a field implantation of which peak concentration exists at the surface.

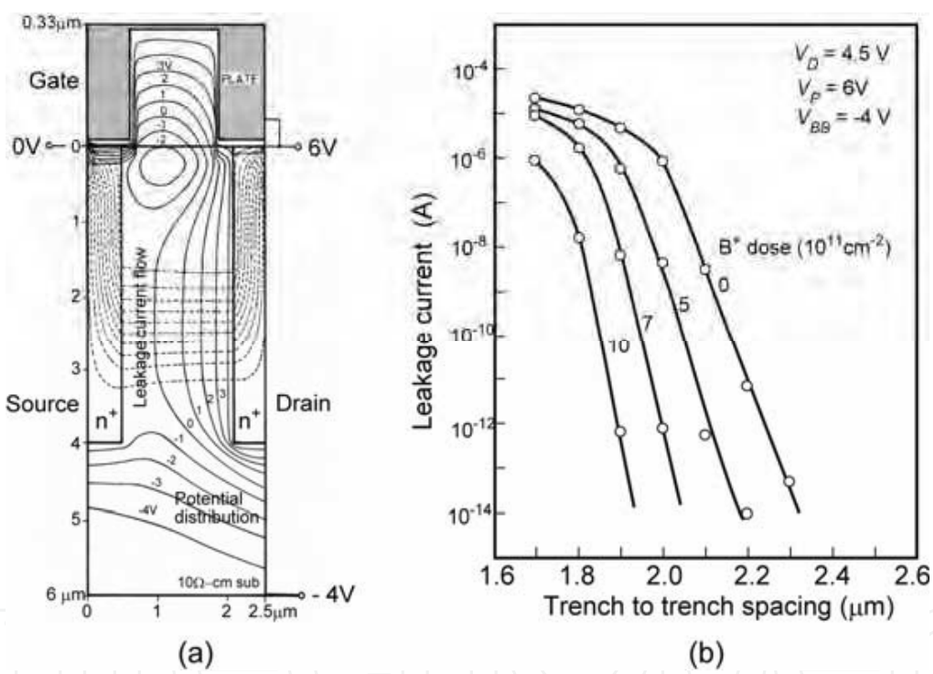


Fig. 8. Leakage current characteristics for two ajacent trenches. Resultant equipotential curves are denoted by solid lines and broken curves are leakage current paths, in (a). A method of leakage suppression with p-type well is shown in (b) using ion implantation with boron.

It is well known that punchthrough stopper with relatively higher dose of p-type dopant can suppress the punchthrough current. As is previously shown in Fig. 8 (b), the leakage current decreases inversely with the increase in a boron implantation dose. Since the impurity concentration of the substrate is $1.5\text{x}10^{15}\text{cm}^{-3}$, boron implantation doses of 1, 5, 7, and $10\text{x}10^{11}\text{cm}^{-2}$ generate accepter concentrations of 1.5, 1.9, 2.1, and $2.5\text{x}10^{15}$ cm^{-3} at 3-μm deep portion between two adjacent trenches. It is noted that even small increase in the concentration can drastically reduce leakage current.

One of radical solutions is to provide a storage node being isolated from the current path in the substrate. Substrate plate or sheeth plate configurations are good candidates which will be referred to hereafter.

c. Soft-error

In the final stage of the development, most serious problem of soft-error was found caused by the alpha-particle hit as shown in Fig. 9. A difference of few orders of magnitude was observed between the planar and the trench cells at cell-failure mode. While, the same performance was observed for both of them in bit-line failure mode. This is because the bit-lines were formed in the same configuration. In this result, it was observed that the trench cell with 40% increase in signal charges provided the same soft-error rate as compared to the planar cell. Even though the trench cell provides stable DRAM operation due to larger signal charges, it loses the advantage of increased signal charges.

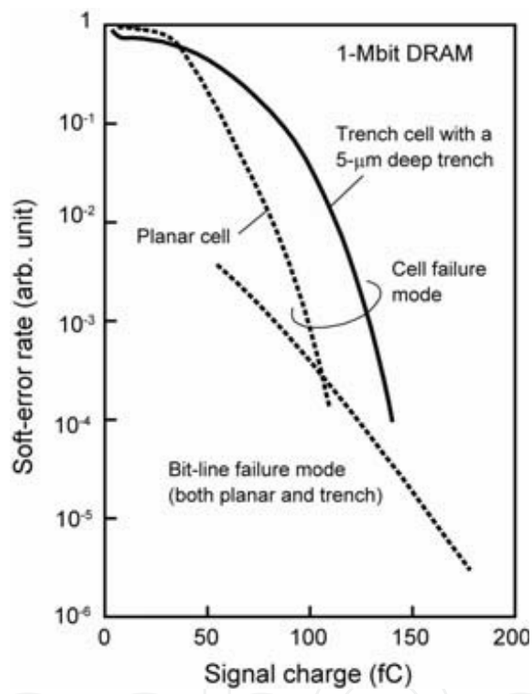


Fig. 9. Measured soft error rates of planar and trench cells.

One alpha particle at maximum 5-MeV energy generates almost one million electron-hole pairs. One million electrons is about 190 fC which is almost equivalent to signal charges stored in one storage capacitor of 1-Mbit DRAM cell. Due to extended depletion layer of the storage capacitor in the trench cell, it "effectively" collects generated electrons, as shown in Fig. 10.

In addition to the soft-error problem, it was predicted that punch-through current between any adjacent two capacitors would soon limit further shrinkage of the cell. That was a serious decision point about whether the trench cell should be improved or abandoned.

In those days, most DRAM manufacturers made efforts to supply their DRAM products to very limited leading mainframe makers. That was a kind of certificate that their products achieved first-grade reliability. The certificate surely made their business fruitful. Even with a half-year delay in product shipment, they might lose their business in the mainframe

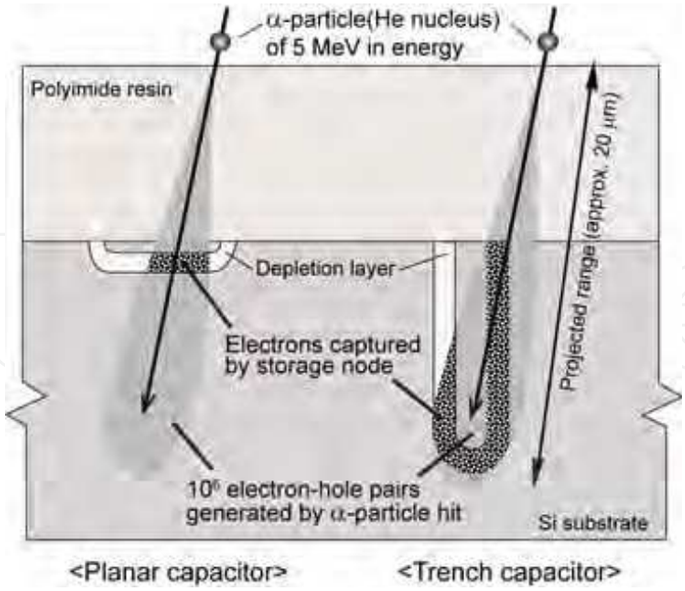


Fig. 10. A model of electron-hole pair generation by an alpha-particle hit.

market during one DRAM generation. There is a clear evidence that a leading maker has changed in each DRAM generation, Intel at 1 K, then, TI, MOSTEK, Hitachi, NEC, Toshiba, Samsung …

Since Hitachi has been a DRAM manufacturer as well as mainframe supplier, it focused keenly on the mainframe application with highest-grade reliability compared to those of personal-use electronic appliances with relatively low reliability. Thus, Hitachi had abandoned the trench cell putting aside several ideas already proposed by the device development group for improved structures to reduce the soft-error problem (Sunami, 2008-a). Additional development was thought to need more than half a year. Since leading mainframe makers accept only a few DRAM suppliers, new product shipment with half-year delay would be fatal.

In the same period, a new configuration of array operation with half-V_{cc} plate (Kumanoya et al., 1985) was proposed as shown in Fig. 11. This has a strong potential of storage-capacitance doubling. As a result, it could prolong the use of conventional planar cell. This proposal had also influenced Hitachi's decision that conventional planar cell should be

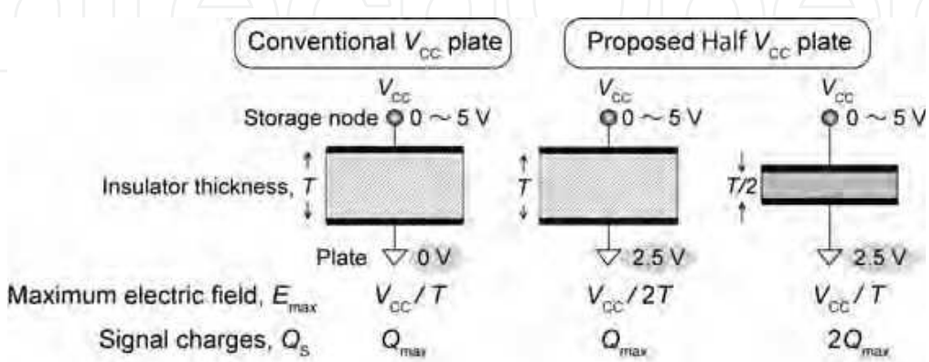


Fig. 11. Half-Vcc plate configuration has a possibility of doubling signal charges keeping maximum electric filed strength applied to capacitor insulator.

applied to 1-Mbit DRAM products. The conventional structure with conventional fabrication technologies are strongly desirable from manufacturability and cost points of view in general.

While, several innovative trench cells had been proposed and then developed to drastically improve soft-error problem in the same development project. A prime key fator was to avoid inflow of charges generated by alpha hit. Those cells were substrate-plate cell (Sunami et al., 1982-a) and sheath-plate cell (Kaga et al., 1988) as shown in Fig. 12. Storage nodes of these cells are surrounded by capacitor insulator being isolated from charges generated in the substrate by an alpha-particel hit. A portion of p-n juction exposed to generated charges is very small clearly illustrated in the figure. The substrate-plate trench cell amazingly improves soft-error tolerance due to its highly shrunk depletion layer.

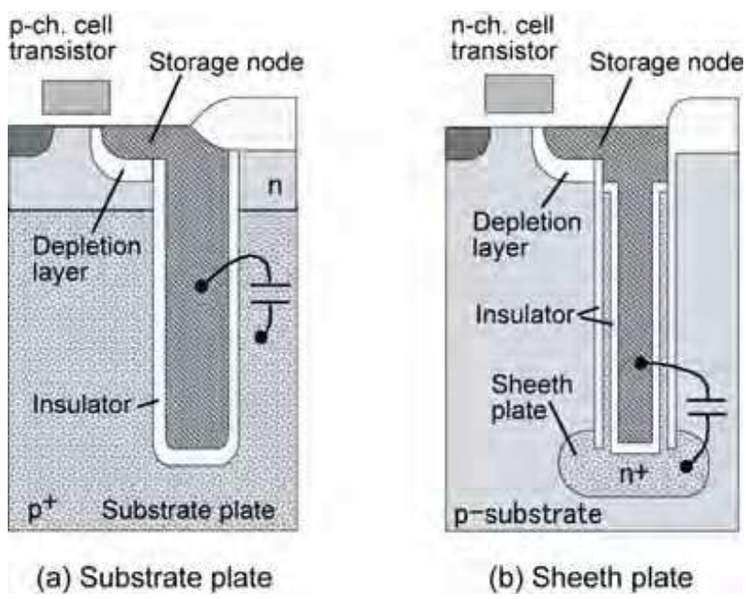


Fig. 12. Proposed DRAM cells to drastically improve soft-error caused by alpha-particle hit. Storage nodes are isolated from substrate by capacitor insulator

Despite alpha-immunity problem, several major manufacturers employed the trench and have been improving the structure until today. Together with the trench, the stacked capacitor cell was also applied in products. In addition to these cell structure innovations, the hemi-spherical grain (HSG) structure (Watanabe et al., 1992) was an inevitable technique to double the storage capacitance due to increased surface area.

3.5 DRAM cell trend

Major advancement in cell innovation is shown in Fig. 13. Cylinder-type stack and substrate-plate trench, both with HSG, are the major cells being manufactured today. These DRAM cell innodations are divided into three phases.

Phase I (1K→1M): Shrinkage of planar area of memory cell together with the decrease in capacitor insulator thickness. Thinning of the insulator finally brought about catastrophic dielectric breakdown of the insulator. Even with utilizing of half-Vcc configuration, planar cell could not survive at 4-Mbit era.

Phase II (1M→1G): 3-D capacitor structure with planar cell transistor. The capacitance does not suffer from planar area shrinkage in principle. Two categories of stack and trench capacitor cells were proposed. In the latter part of the phase II, high-k materials became inevitable to keep capacitance value against cell area shrinkage.

Phase III ((1G→1T): Three-dimensional stack of the capacitor and the cell transistor. This will be described later in section 4.5.

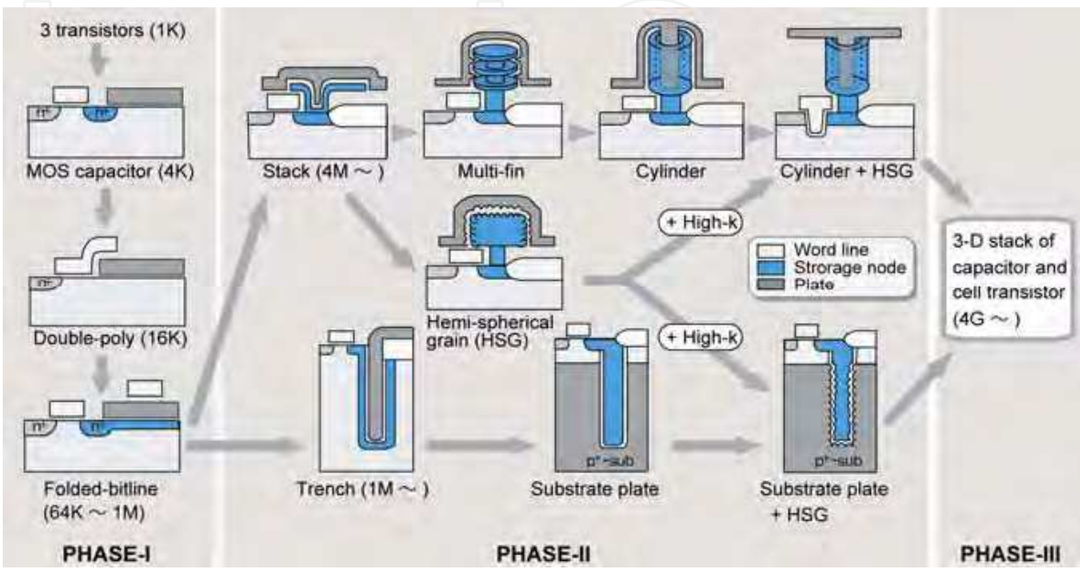


Fig. 13. DRAM cell trend. Phases I, II, and III correspond to planar area shrinkage, 3-D capacitor, and 3-D stack of cell transistor and storage capacitor, respectively.

A typical memory cell of commercially available 1-Gbit level DRAM is shown in Fig. 14 (Sunami, 2008-c). This shows one kind of combination to utilize various technologies. This virtual structure is not necessarily the exact one of commercially available real product.

Extended channel length with trench gate is aiming much less sub-threshold current to keep sufficient refresh time. Relatively low concentration of n-type dopant at junction also provides lower leakage current due to reduced electric filed across the junction. Since it is predicted that there will certainly exist an ultimate limit in size of hemi-spherical grain, diameter of the cylinder will also cease to shrink due to the grain size.

3.6 Material revolution

From 1 K to 1 M, size scaling was the key issue. The storage capacitance value was kept almost the same over several DRAM generations by reducing insulator thickness compensating memory cell shrinkage. Consequently, the reduced thickness made the electric field across the insulator close to 5 MV/cm which was recognized to be the upper limit for keeping insulator integrity and refresh time in DRAM operation. Thus, innovative techniques other than thickness reduction were strongly required.

In response, three-dimensional structures were proposed. From 1 M to 1 G, three-dimensional structure innovation has been achieved as previously shown in Fig. 13. However, as the aspect ratio of the storage capacitor exceeds more than 10, manufacturability becomes a much more serious issue. The final parameter to be handled in the relation expressed in Eq. (1) is permittivity, ϵ_i. Thus, various kinds of high-*k* materials

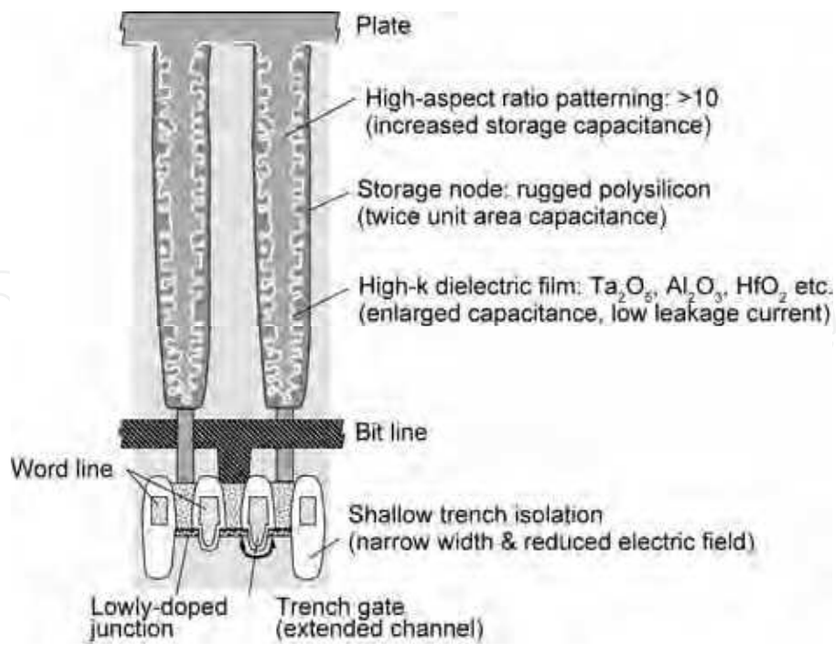


Fig. 14. A typical 1-Gbit level DRAM cell utilizing various kinds of proposed technologies. This may not necessarily be the exact memory cell in commercially available products.

have been developed as shown in Fig. 15. But there is a serious fact that the thinner the thickness is, the less its permittivity is. An empirical equation regarding the relation between leakage current, I_{leak} and barrier height in silicon-insulator system is expressed as

$$I_{leak} \propto \exp[-(m\phi)^{1/2}T], \tag{2}$$

where, m, ϕ, and T are effective mass, barrier height, and film thickness, respectively. Thus, high-k film may not be a unique ultimate solution at this moment. Material revolution with ultra high-k material is solicited to extend DRAM further toward terabit DRAM on a chip.

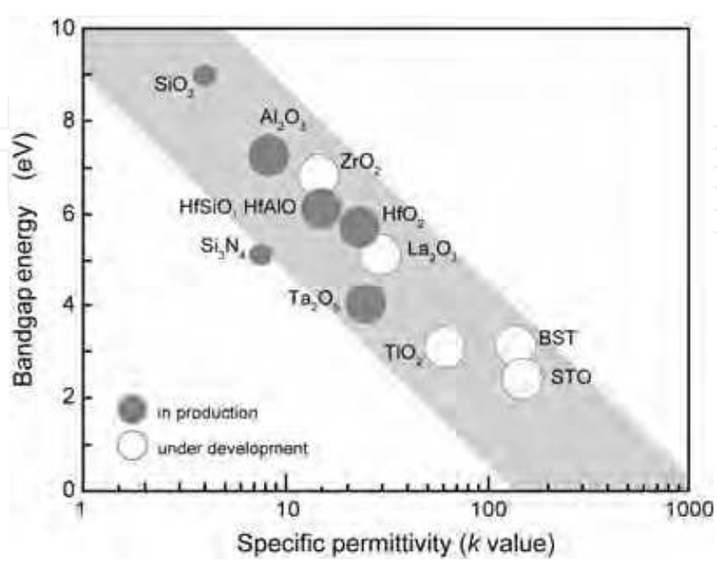


Fig. 15. Relation between bandgap energy and permittivity of high-k dielectric films.

To summarize innovation achieved in the past and requirements to the future, there are three eras for DRAM development.

- 1 K to 1 M ---- dimension improvement: smaller cell and reduced insulator thickness.
- 1 M to 1 G ---- structure or material innovation: stack or trench cell with high-k film.
- 1 G to 1 T ---- 3-D stack: cell transistor and storage capacitor with material revolution.

The final parameter which affects advanced shrinkage of the cell should be the insulator thickness itself. If the insulator is thick enough to fill the internal hole of the trench of the trench cell or cylinder of the stacked cell, the plate of the capacitor cannot penetrate inside the trench or the cylinder, resulting in no capacitor formation (Itoh et al., 1998), as shown in Fig. 16. In this sense, high-*k* films should be thin enough, simultaneously keeping their high-*k* value. This may be the deadlock for realizing smaller cells of the 1-transistor type DRAM cell. Even utilizing cutting-edge high-*k* films at present, 32 or 64-Gbit DRAM will be the biggest capacity on a chip without chip stack. We would like to expect novel main memory candidates in near future.

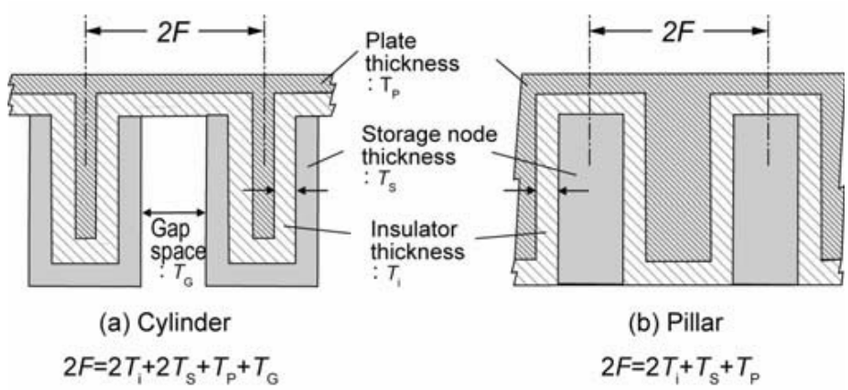


Fig. 16. Relations among several film elements constructing the storage capacitor.

4. Two- and three-dimensional MOS transistors

Since integrated circuits, particularly MOS memory and processor, were introduced to the market in early 1970's, almost four-fold increase in both memory's volume and processor's performance has been continually achieved every three years, as previously shown in Fig. 1. The strongest driving force for the increase is undoubtedly "cost" as previously described in section 3.2. The volume increase has been attained maily by shrinkage of all components on a chip. MOSFET (field-effect transistor) is particularly suitable to the shrinkage because the scaled transistor provides better performance. This transistor's behavior was theoretically analysed (Dennard et al., 1974) and named "scaling principle" later in semiconductor industry.

4.1 Innovation of 2-D transistors

Even though scaled transistor provides better performance, various kinds of problems become more serious in response to the scaling. They are so-called "short channel effects"; drain-to-source breakdown voltage is decreased; hot-carrier immunity gets worse; subthreshold current becomes more harmful against cut-off performance; gate leakage current increases with decreasing of gate oxide thickness; and mobility degradation sacrifices the scaling itself .

To cope with these short channel effects, 2-D transistor structure has been improved, as shown in Fig. 17. The structure has been improved so that electric field in the vicinity of drain is reduced. High electric field results increased leakage current and reduced breakdown voltage of source to drain. Thus DD was developed to reduce the electric filed with more graded impurity profile around n^+ drain. However, the graded impurity profile increases punch-through current in deep portion between source and drain.

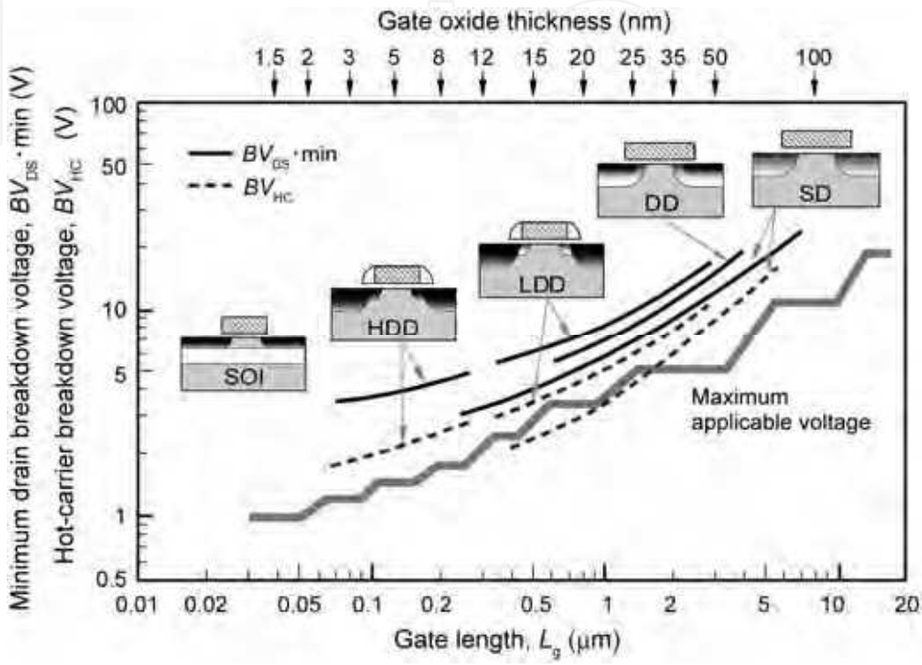


Fig. 17. Improvement of MOS transistor structure regarding source and drain regions. SD, DD, LDD, HDD, and SOI denote single drain, double drain, lightly-doped drain, highly-doped drain, and silicon-on-insulator, respectively.

Then, LDD was developed so as to suppress the punch-through current with graded impurity profile regions which were located only at edges of drain and source, as shown in Fig. 17. Due to relatively higher resistivity associated with the graded impurity profile, LDD's drivability was not satisfactory because of relatively higher series resistance between source and drain. Then HDD was developed to reduce the effect.

Even though these innovations were made, mobility degradation problem still remained. Based on a physical aspect that tensile and compressive strains enhance the electron and the hole mobilities respectively, a strained MOS transistor was proposed (Kesan et al., 1991; Ismail, 1995). Typical strained silicon MOS transistors are shown in Fig. 18.

The strained transistor (a) in Fig. 18 consists of SOI structure with a Si-Ge layer underneath source and drain. Since an overlayer silicon has to be epitaxially deposited on Si-Ge layer, complicated fabrication processes are likely to delay the practical use of it.

As a more practical structure, the usage of compressive and tensile chemical-vapor deposited (CVD) silicon-nitride films was proposed (Pidin et al., 2004), as shown (b) in Fig. 18 . Stresses of about -2 and +2 GPa were successfully introduced into p- and n-channel regions, respectively. Minus and plus signs of stress denote compressive and tensile, respectively. Even though real deposition methods of the films were not disclosed in the meeting, it is well presumed that the tensile strain may be introduced by thermally

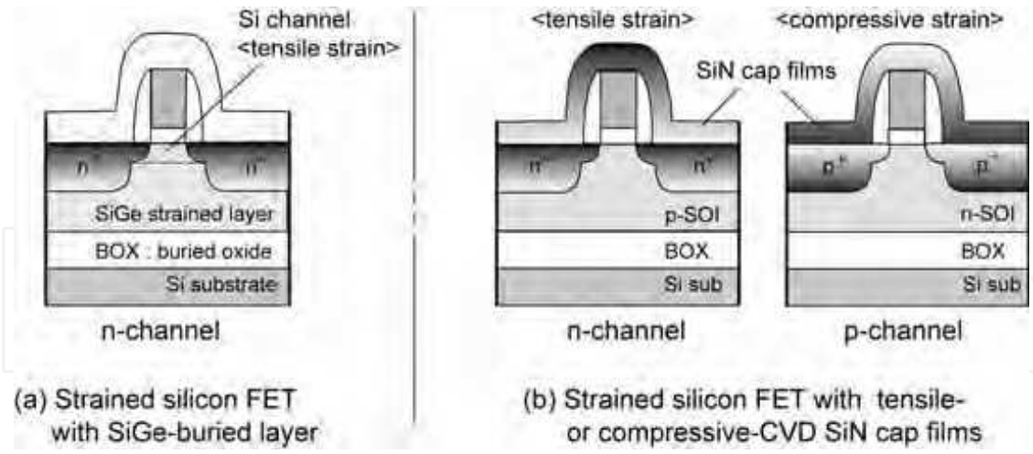


Fig. 18. Typical strained silicon MOSFET's: SiGe buried layer, (a) and CVD SiN cap films, (b).

decomposited CVD whereas the compressive strain may be given by plasma-enhanced CVD. Almost 50% increase in carrier mobilities of both n- and p-channel transistors were obtained.

4.2 Proposals of quasi 3-D transistors

To cope with short-channel effects which will be more and more serious in response to the scaling of conventional 2-D transistors, transistors of which channel was formed on both side walls of a silicon beam, named trench-isolated transistor using side-wall gates, TIS (Hieda et al., 1987) and fully depleted lean-channel transistor, DELTA (Hisamoto et al., 1989) were proposed as shown in Fig. 19 (a) and (b), respectively. Because of horizontal current flow of the transistor, this kind of transistors is called "quasi 3-D" in this article.

In TIS, full side walls were not used, while main channel was formed on side walls of the thin silicon beam in DELTA. The bottom of the silicon beam is fully oxidized with local-oxidation of silicon process (LOCOS), the beam is isolated from silicon substrate like SOI substrate. Advantages of the thin silicon channel were estimated.

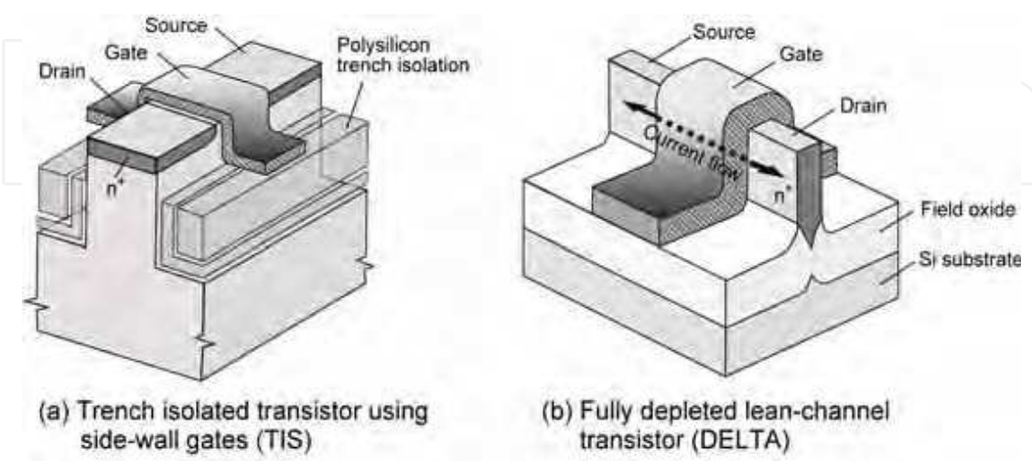


Fig. 19. Proposed quasi 3-D transistors of trench-isolated transistor using side-wall gates (TIS), (a) and fully depleted lean-channel transistor (DELTA), (b)

The author's group has proposed several devices with respect to quasi-3-D structures. One of them is corrugated channel transistor, CCT (Furukawa et al, 2003; Sunami et al, 2004) as shown in Fig. 20. Plural beam channels with {111} surface are formed by a crystallographically preferential etching with tetramethylammonium hydroxide, TMAH, atomically flat channel surface can be formed expecting less mobility degradation by avoiding rough surface of the channel.

The current drivability of CCT is proportional to the number of the beams as shown in Fig. 21. This is suitable for area-conscious applications such as power transistor and/or high-voltage transistor.

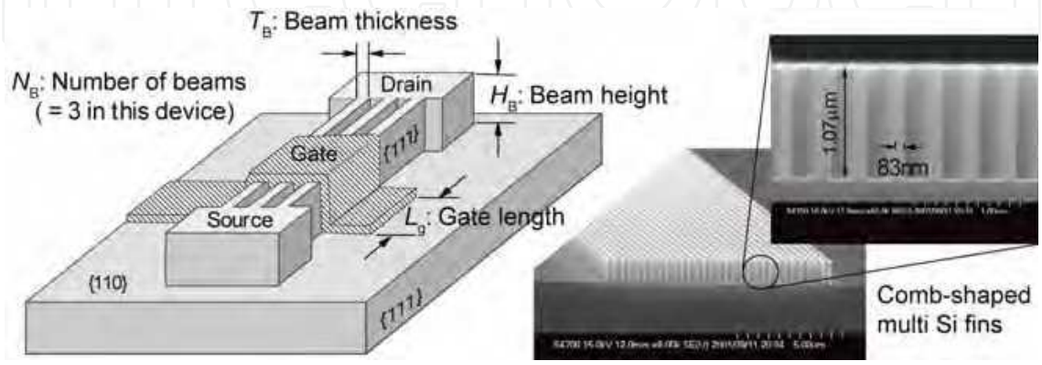


Fig. 20. A corrugated-channel transistor, CCT featuring.

Other proposal is super self-aligned triple gate transistor (Okuyama et al., 2007) as shown in Fig. 22. As two sidewall gates are delineated with an etching mask of a top gate, triple gates are selg-aligned each other leading to much smaller area occupation on a silicon die. One of device performance is shown in Fig. 23. Three gates operate three transistors independently with unified source and drain. At single-gate operation, subthreshold current can be controlled by other two side gates, namely, a variable threshold-voltage transistor can be realized in a certain voltage range.

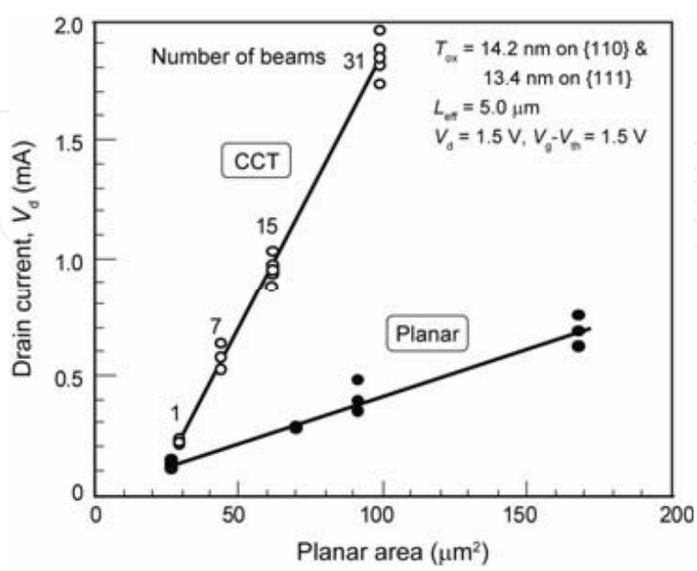


Fig. 21. Drivability of corrugated-channel transistor, CCT in terms of planaer area.

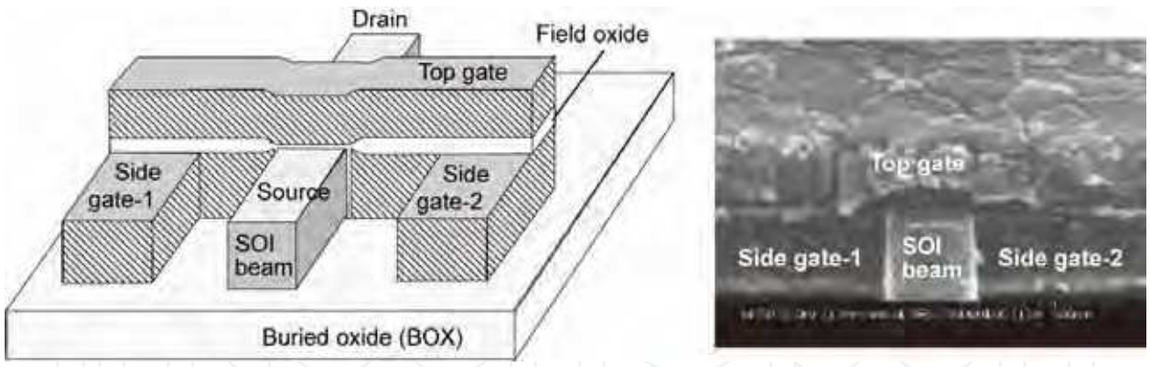


Fig. 22. Super self-aligned triple gate transistor featuring three gates of top gate, side gate-1, and side gate-2 formed in self-aligned manner.

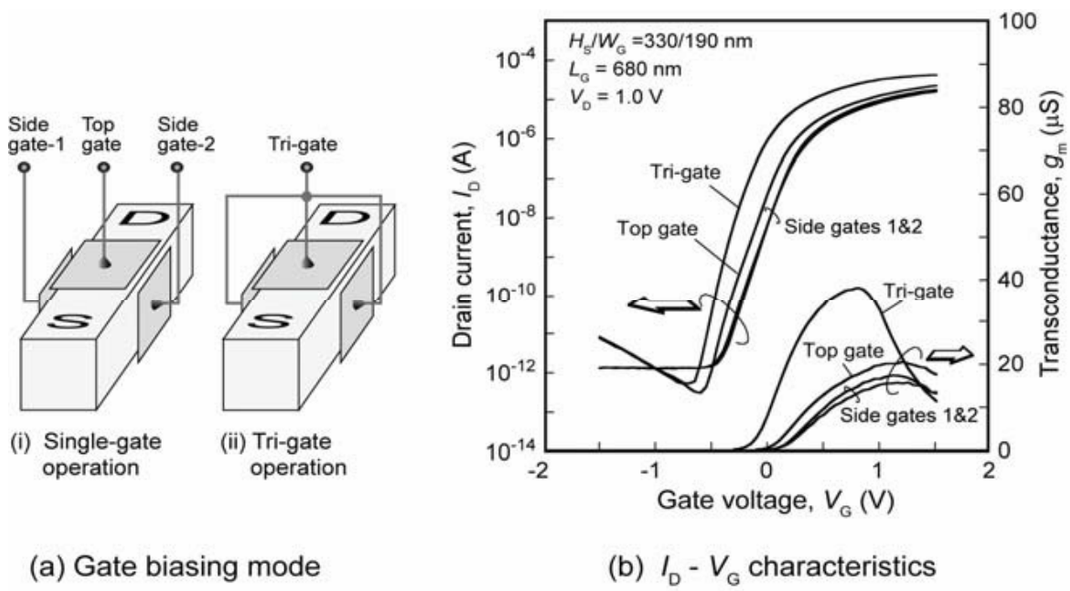


Fig. 23. Drain current characteristics of the triple gate transistor. Three gates provide independent three transistors with a unified drain and a unified source.

In these quasi-2-D transistors, there exist several serious issues caused by the formation of tall and thin steep silicon beam. They are (1) delineation of steep vertical silicon beam, (2) conformal gate material formation, (3) low-resistive source and drain, and (4) low resistive contacts to source and drain. The former two can be solved by advanced lithography with multi-level resist technique, CVD, and dry etching with high material selectivity. The latter two may be achieved by silicidation of silicon beam and wrapped metal contact as shown in Fig. 24.

In the figure, current paths of beam channel transistor are illustrated. It is obvious that longer current paths in relatively high resistivity area are illustrated in top contact as shown in Fig. 24 (a). On the other hand, relatively shorter current paths are formed in wrapped contact as shown in Fig. 24 (b)

Simulated drain currents and transconductances are described in Fig. 25 in case of typical impurity concentration and silicidation (Matsumura et al., 2007). Top contact transistor structure scrifices the advantage of beam-channel transistor to a considerable extent.

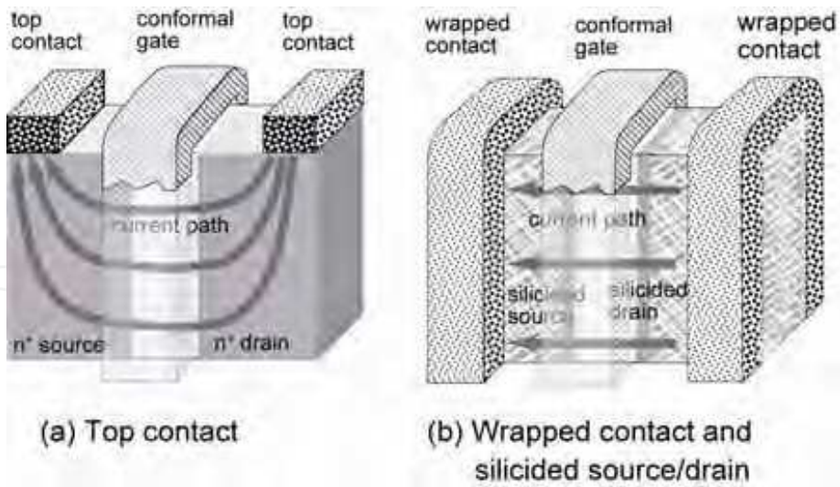


Fig. 24. One of drain current characteristics of the triple gate transistor at two modes of gate voltage application.

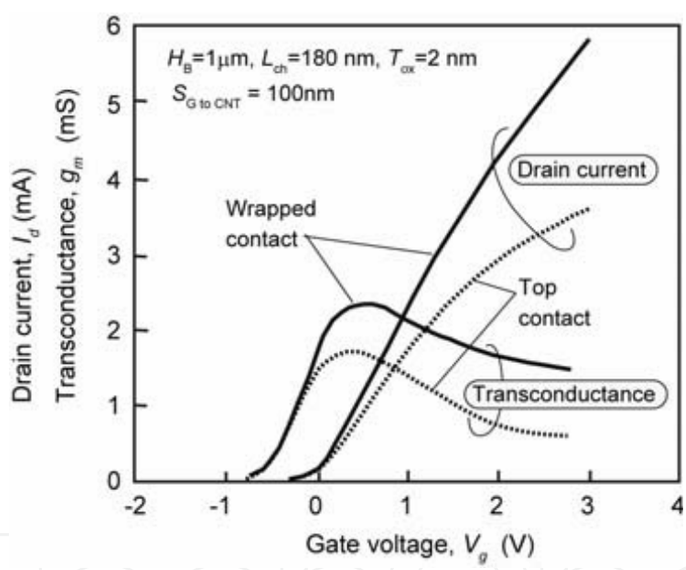


Fig. 25. Simulated drain current and transconductance of transistors with top contact and wrapped contact. Transistor structures are shown in Fig. 24.

4.3 Proposal of 3-D transistors

To summarize quasi-3-D transistors described above, a possible scenario of transistor structure innovation is illustrated in Fig. 26. Transistors with horizontal current flow inside a silicon beam are called FINFET today (Choi et al., 2001). Then, 3-D FET's with vertical current flow will be a next candidate for 3-D LSI.

With respect to the vertical transistor, a few DRAM cells utilizing vertical current flow structure have already been proposed in mid 1980's. They are trench-transistor cell, TTC (Richardson et al, 1985) and surrounding gate transistor, SGT (Takato et al., 1988). However, they are not manufactured in real products yet. One reason is probably that fabrication technologies do not become matured yet in general.

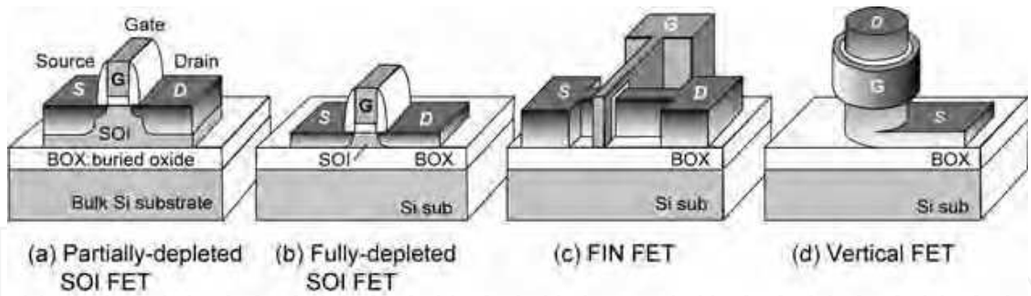


Fig. 26. Recent trend in transistor structure. It is not reported yet in 2009 that both FINFET or vertical FET is already shipped to the semiconductor market.

These structures may be almost the tiniest configuration in one-transistor DRAM cell. A theoretical area of these cells is $4F^2$. F is a feature size of device, in other word, technology node itself. In conventional array configurations, theoretical memory cell sizes of open bit-line and folded bit-line arrangements are $6F^2$ and $8F^2$, respectively. A vertical stack cell as shown in Fig. 27 (c) will be one of the most promising structures in near future.

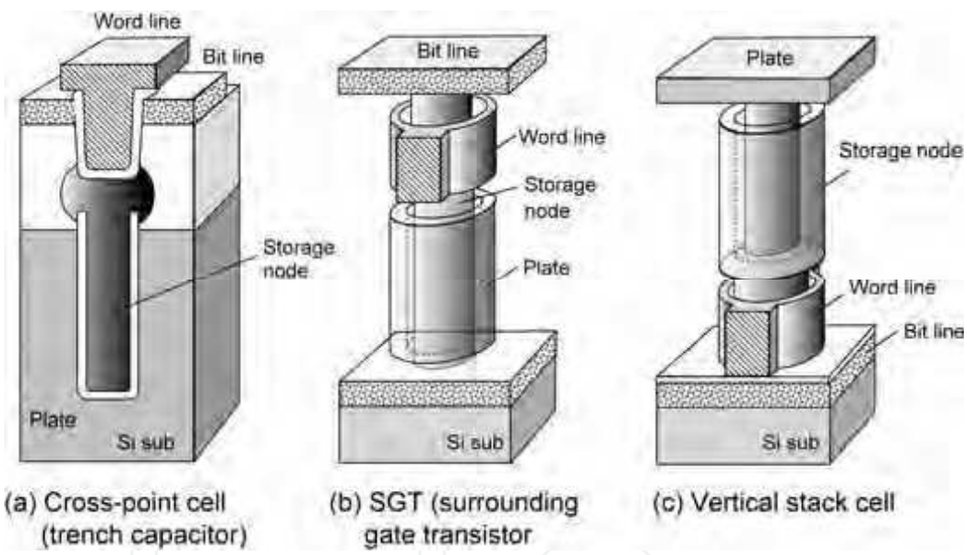


Fig. 27. Proposed vertical cell transistors applied to one-transistor DRAM cell.

4.4 A vertical transistor having a potential of $2F^2$ cell area

The author's group has proposed a super pillar transistor, SPT which has a potential of realizing $2F^2$ DRAM cell (Sugimura et al., 2008). This SPT can double the packing density of DRAM cell as compared to $4F^2$ cells previously shown in Fig. 27. A bird's eye view of SPT is shown in Fig. 28.

Fabrication process folw is as follows. Selected portions of a silicon beam are covered with CVD Si_3N_4 films. Then high temperature oxidation is performed at 1000°C to the extent that the beam is fully oxidized. Portions which are not covered with the Si_3N_4 films are converted into SiO_2 remaining physically and electrically separated silicon pillars. Subsequently, gate oxidation is processed and gate film is entirely deposited. Then, directional dry etching is performed entirely on a wafer remaining two gates located on both sides of the beam as residues associated with the dry etching. The resultant structure is already shown in Fig. 28.

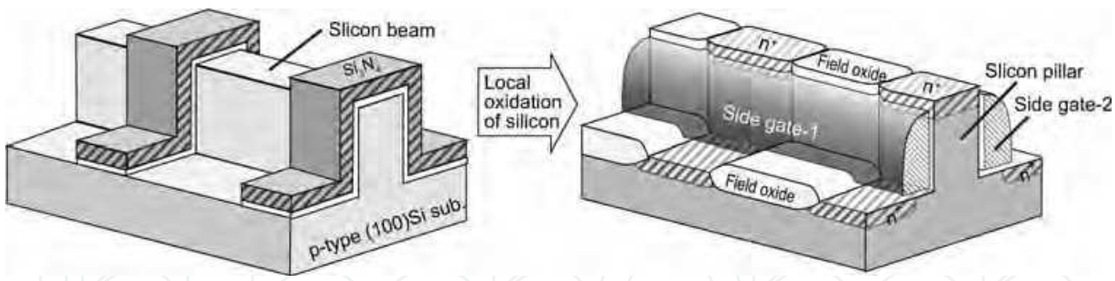


Fig. 28. A fundamental process sequence to fabricate super pillar transistor, SPT. The pillar is isolated with field oxide which is converted from silicon beam itself with well-known local oxidation of silicon, LOCOS technique. Side gate-1 and -2 are self-aligned to silicon and oxide beam.

An SEM plane view of SPT is shown in Fig. 29. Even though the thickness of field SiO_2 film is twice as much as that of silicon beam, removal of the Si_3N_4 film and scrificed oxidation reduce the thickness by a factor of 0.5. Thus the field oxide thickness shown in Fig. 29 is almost equivalent to that of silicon pillar.

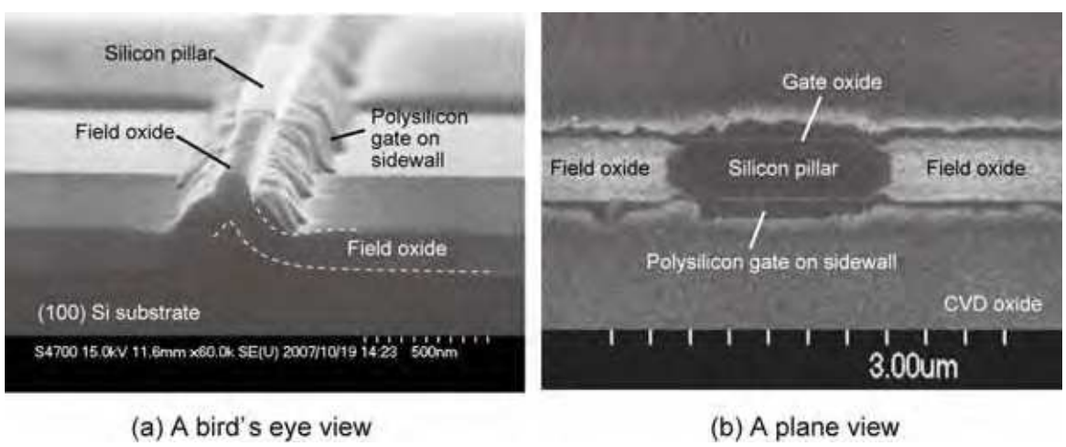


Fig. 29. SEM images of a bird's eye view, (a) and a plane view, (b) of super pillar transistor, SPT. Field oxide is thinned by a factor of 0.5 with a controlled wet etching.

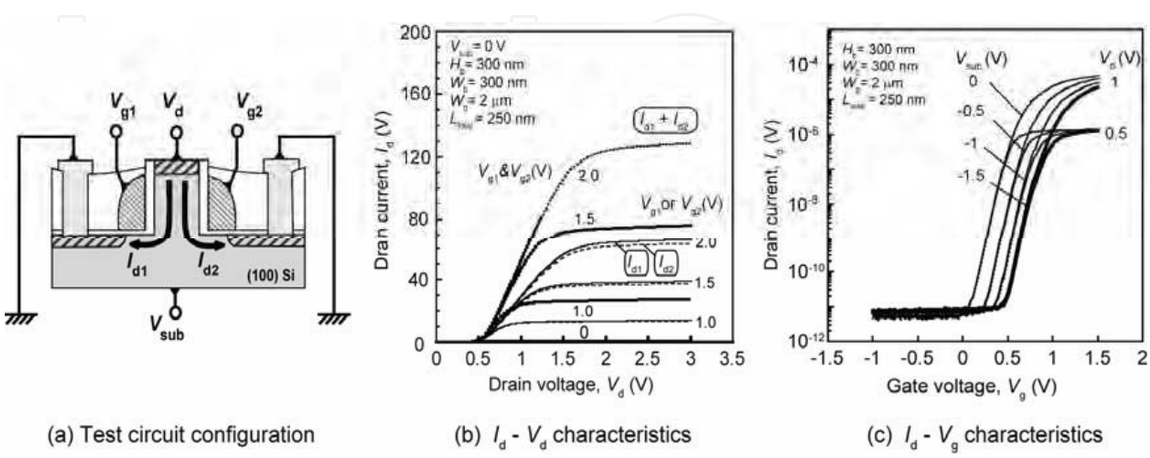
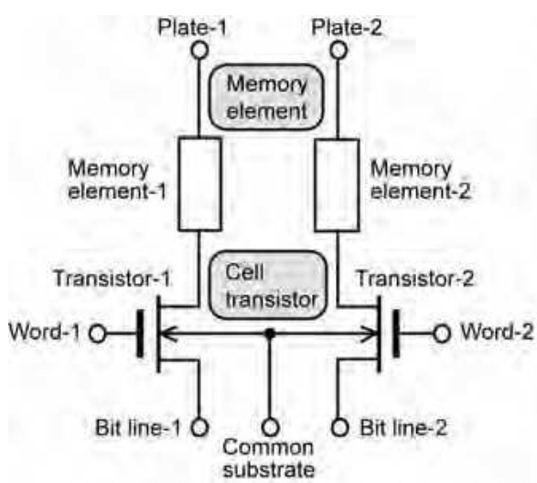


Fig. 30. A test circuit configuration, (a), characteristics of I_d-V_d, (b) and I_d-V_g, (c) for super pillar transistor, SPT.

Side-wall gates on both sides of the pillar make two transistors in one pillar. Typical I_d-V_g characteristics are shown in Fig. 30. Drain currents of I_{d1} and I_{d2} denote those of two sidewall gate transistors. As shown in the figure, two drain currents can be controlled separately.
With additional new technique of forming two capacitors on a pillar, two DRAM cells on a pillar can be obtained leading to $2F^2$ cell. Consequently doubled density of DRAM can be realized at the same technology node.

4.5 Prospect of vertical 3-D transistor

Even though a lot of advantages in vertical 3-D transistor are expected compared to 2-D transistor, there still exists a fundamental limit due to the vertical structure. Except the complexity in fabrication technologies, one of the biggest problems may be practically unchangeable gate length. As an LSI consists of various gate lengths to optimize the performance such as speed/power consumption, chip size, operational margin etc., vertical transistors with single gate length can not be applied to LSI's of processors and ASIC's in particular.
Under these circumstances, one of promising applications may be memory cell array. Cell transistors in a cell array should be identical in order to obtain compact array area and stable operation. Figure 31 proposes possible candidates of super pillar transistor, SPT to memory application. If a certain memory element is chosen, various kinds of memory will be possible. SPT can work as "a universal cell transistor" for almost all memories with one-transistor cell and also can be applied to static memory cell with plural transistors.



Memory element	Memory
(a) Capacitor	DRAM
(b) Phase change	PCM
(c) Resister	ReRAM
(d) Magnetic film	MRAM
(e) New material	New memory

Cell transistor	Memory
(f) Ferroelectric	FeRAM
(g) Floating gate	Flash memory
(h) SiON film	Flash memory
(i) New material	New memory

Fig. 31. Various applications of super pillar transistor, SPT which can be operated as a universal cell-transistor.

In addition to this kind of a cell transistor and a memory element stack, a transistor stack structure is proposed. At present, 16 stack layers of NAND flash memory, named pipe-shaped bit cost scalable (P-BiCS) flash memory, is proposed (Katsumata et al.; 2009), as shown in Fig. 32. As a silicon body of transistors is filled into a hole which is etched after 16 gate-layer stack formation, it is no need for the formation of thin and tall silicon pillar. In this sense, the manufacturability of P-BiCS is expected to be more stable than that of the pillar type in multi-stack memory, however, it is speculated that transistor performance problem exists due to the polycrystalline silicon body.

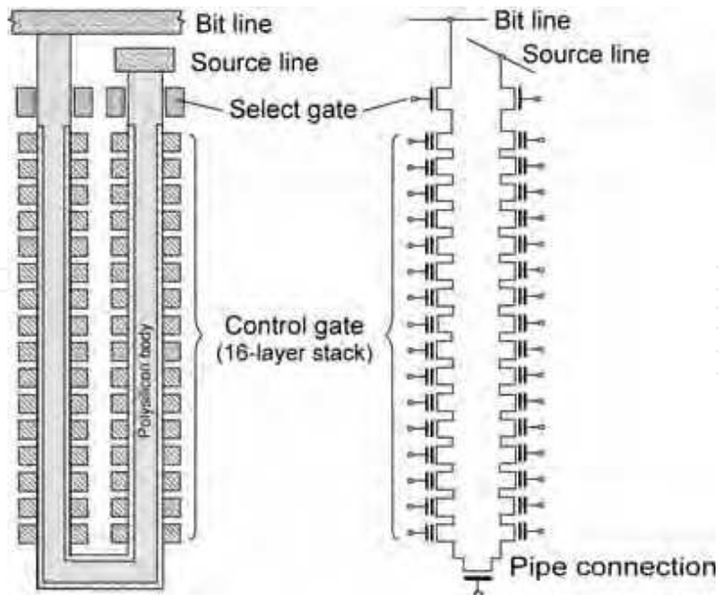


Fig. 32. Proposed 16 layer stack of NAND flash memory named as pipe-shaped bit cost scalable as P-BiCS.

5. Other approaches to 2.5-D stack LSI

A few kinds of 3-D stack of active transistors were extensively investigated in 1980's mainly using laser recrystallization. But they were almost abandoned in the next decade due to poor integrity of overlaid single crystal layer causing much poorer productivity. In place of this active transistor stack, two kinds of chip-stack techniques have been developed as shown in Fig. 33. Flash memory and DRAM are already utilizing bonding-wire connection and 6 to 8 chip stack are now available in flash and DRAM products. An example on a test chip is shown in Fig. 34.

Recently a through-silicon-via type connection has been extensively developed. This provides more flexibility of inter-chip connection and higher productivity due to the batch processing for via formation and inter-via contact. Nevertheless, this may not be a real 3-D stack, because the chip thickness measures tens of 10 μm which is much larger than the device arrangement pitch of tens of 100 nm. Therefore, the chip stack is called "2.5 dimensional" in this article.

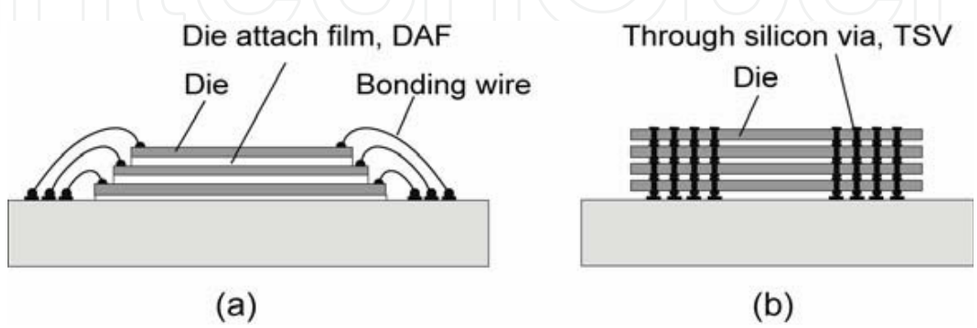


Fig. 33. Two kinds of chip-stack LSI's: bonding-wire connection type, (a) and through-silicon-via, TSV type (b).

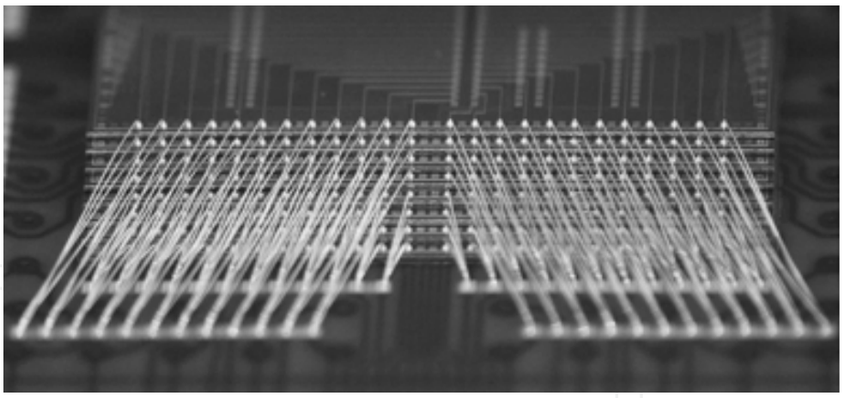


Fig. 34. Eight-layered bonding-wire connection on a test substrare.

6. Conclusion

In response to the ceaseless requirement for extended performance of transistor in LSI, continual scaling has been achieved since early 1970's. Sizes of transistors in products measured 12 μm in 1970 and around 45 nm in 2009. The scaling of device size has been brought about 4-fold increase in memory's volume and processor's performance every three years. Since there existed a limitation of amount of signal charges in DRAM against the cell size scaling, DRAM had first encountered the imitation of the volume size at 1 megabit in mid 1980's. To overcome the limitation, it began to employ a 3-D capacitor structure such as trench capacitor or stack capacitor.

Even with the 3-D structures, its maximum volume of DRAM in a chip is estimated to be 64 gigabit provided that the amount of signal charges stored in a cell must be kept constant against the cell scaling. To solve the deadlock, the employment of an extra high-*k* dielectrics, and a vertical stack of a cell transistor with a capacitor will be inevitable in near future.

Regarding NAND flash memory, multi-stacks of flash transistors have already been proposed. Since flash memory cell consists of one cell transistor in a memory cell and no contact is needed to source and drain in a string of cell transistors, the multi-stack is relatively easier than that of DRAM.

On the other hand, field-effect transistor itself will encounter the ultimate size limit of 5-10 nm. Only about several tens of silicon atoms exist in the channel region of 10-nm transistor. Normal filed-effect operation will be impossible due to fatal short-channel effects in that dimension range. Particularly a ratio of off current to on current becomes worse causing unacceptably large stand-by power consumption.

If the scaling pace is still kept constant, the ultimate limit will be encountered within 15 years. Forecasting the limitation, various kinds of 3-D transistors have been proposed, however, they will still suffer from the short-channel effects same as 2-D transistors. Due to a limitation of invariable channel length of vertical transistor, it will be practical in products that the vertical transistor is employed together with 2-D one in an LSI chip.

To cope with these fundamental limits in miniaturization of devices, various kinds of chip stack will be dominant in LSI products in response to the requirement for smaller package used in personal-use, hand-held products.

7. Acknowledgements

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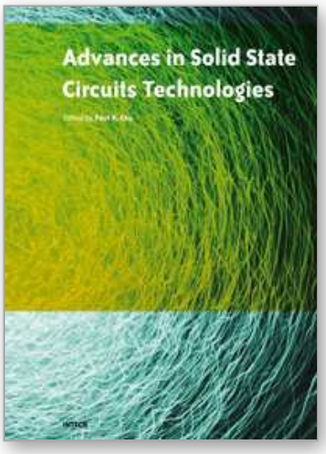

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