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Multi-Mode, Multi-Band Active-RC Filter and Tuning Circuits for SDR Applications

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1. Introduction

The prevalence of wireless standards and the introduction of dynamic standards/ applications, such as software-defined radio, necessitate filters with wide ranges of adjustable bandwidth/power, and with selectable degrees and shapes. The baseband filters of transceivers often utilize a significant portion of the power budget, especially when high linearity is required. Likewise, a widely tunable filter designed for its highest achievable frequency consumes more power than necessary when adjusted to its lowest frequency. Because power consumption is proportional to the dynamic range and frequency of operation, power-adjustable filters have recently gained popularity, as they can adapt their power consumption dynamically to meet the needs of the system.

Dynamic variation in filter attributes (e.g. frequency, order, type) coupled with companies' desire to reuse IP has popularized highly programmable filters. The lowpass-filter cutoff frequencies of several wireless/wireline standards are within the 1–20 MHz frequency range. Many of these standards are irregularly spaced in frequency and do not lend themselves well to standard binary-weighted resistor arrays. In previous designs frequency is solely controlled digitally, and hence, digital circuitry or an ADC is used to tune the frequency of the filters. Gm–C filters offer continuous frequency tunability and can operate at higher frequencies than their active-RC counterparts. MOSFET-C filters can also provide continuous frequency tuning, but both Gm–C and MOSFET-C filters lack good linearity. MOSFET-C filters additionally suffer from reduced tuning range at lower supply voltages; also, in MOSFET-C most of the voltage drop occurs over nonlinear MOSFET triode resistors, which appreciably degrades its linearity. Along these lines, filters with good linearity have been developed that tune on the basis of duty-cycle control in switched-R-MOSFET-C filters; however, duty-cycle control by nature necessitates a discrete-time filter. Active-RC filters, known to have good linearity, have been used for continuous-time programmable filters. Some such filters have narrow frequency ranges, with a few others providing wider but solely discrete ranges. Purely discrete switched resistor tuning limits filter frequency tuning to discrete frequencies determined by the overall frequency range and number of bits used. Tuning to different frequency bands precisely would require very fine resistor stripes to meet precision requirements for the low-frequency end.

Newer technologies offer increased integration with smaller feature sizes, allowing the filter to be on the same chip with other transceiver blocks. This integration especially promotes reconfigurable architectures, as DSPs can be integrated with the transceiver and can control

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the mode of operation. However, as minimum feature size shrinks, supply voltages also reduce, which complicates classical linearization techniques of Gm–C filters. In this respect, active-RC filters possess an intrinsic linearity advantage.

The third generation standards will create a demand for cellular phones capable of operating both in the new wideband and in the existing narrower band systems. Second generation system has a channel bandwidth in range of tens of kilohertz, whereas channel bandwidths of wideband systems are in megahertz range. So the corner frequency of an analog channel select filter must be tunable over at least a decade of frequency. This will increase the power consumption and the area. The proposed multi-mode baseband filter can minimize the area and optimize the power consumption by sharing the capacitors and resistors. And new tuning method can reduce the number of switches in programmable capacitor arrays which can be dominant noise sources.

This chapter is organized as follows. In Section 2, the multi-mode, multi-band active-RC filter architecture is described. Section 3 describes filter tuning circuits. Section IV shows experimental results from a 0.35 μm CMOS implementation and Section V concludes the paper.

2. Multi-mode, multi-band active-RC filter architecture

2.1 Multi-mode, multi-band active-RC low-pass filter

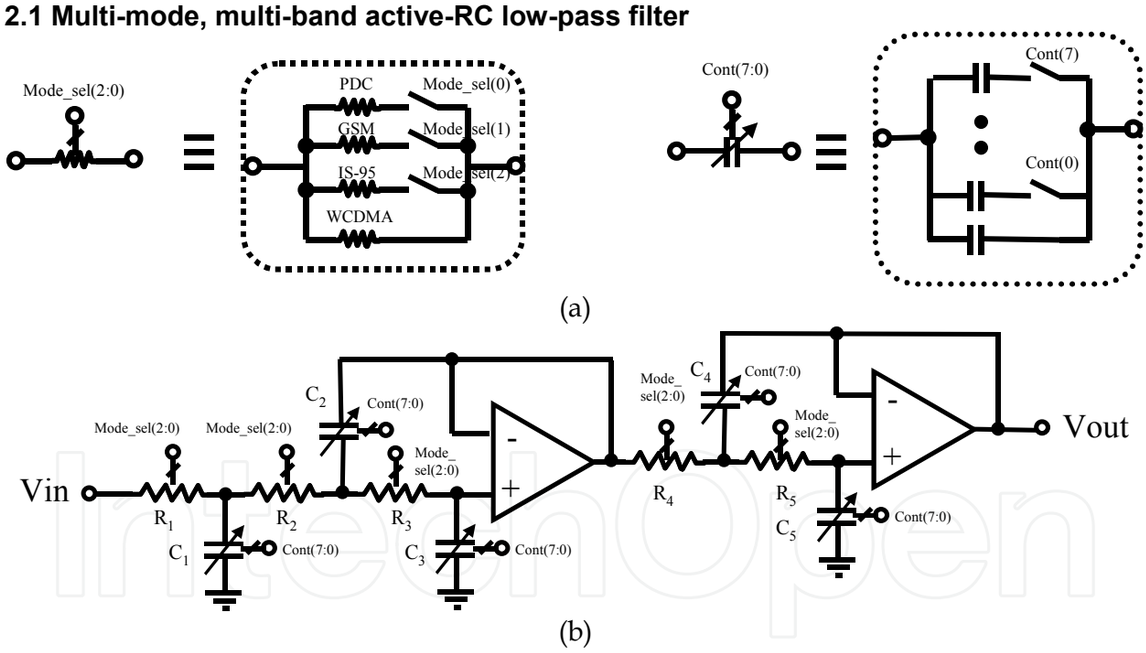


Fig. 1. (a) Resistor matrices and capacitor matrices (b) schematic of the baseband filter.

Fig. 1 shows the designed active-RC 5th-order Chebyshev filter. Resistor matrices and capacitor matrices are shown in Fig. 1(a). Resistor matrics are composed of resistors and switches. Switches are controlled by Mode_sel(3:0), as defined in Table 1. Resistor for WCDMA is not connected to any switch.

The bandwidths of PDC, GSM, IS-95, and WCDMA are 13 kHz, 100 kHz, 630 kHz, and 2.1 MHz, respectively. Mode_sel(3:0) bits are set through the serial interface and represented in thermometer code. The corner frequency was made tunable by using programmable

capacitor matrices. Capacitor matrices are composed of capacitors and switches. The control bits required for each mode are 2-bits. Thus, total number of 8-bits are required. The tuning bits, cont(7:0) are determined from the on-chip tuning block based on the mode. In PDC mode, the low corner frequency leads to large passive components occupying a lot of die area [2]. Because the capacitor matrices dominate the area, capacitors were shared between modes. There are trade-offs between resistor values and capacitor values. When resistor values are reduced to make thermal noise small, capacitor values become large. That leads to a large area. On the other hand, as capacitor values become smaller to reduce the area, the noise level rises. So, capacitor values and resistor values were optimized.

Mode_sel(3:0)	Standard	Bandwidth
"0001"	PDC	13 kHz
"0010"	GSM	100 kHz
"0100"	IS-95	630 kHz
"1000"	WCDMA	2.1 MHz

Table 1. Mode definition and corresponding bandwidths

2.2 Tunable active-RC complex band-pass filter

Fig. 2 shows the Adjacent Channel Interference (ACI) of the PHS system. The nearest interferer is located at 600 kHz, and its magnitude is 50 dB larger than the wanted signal.

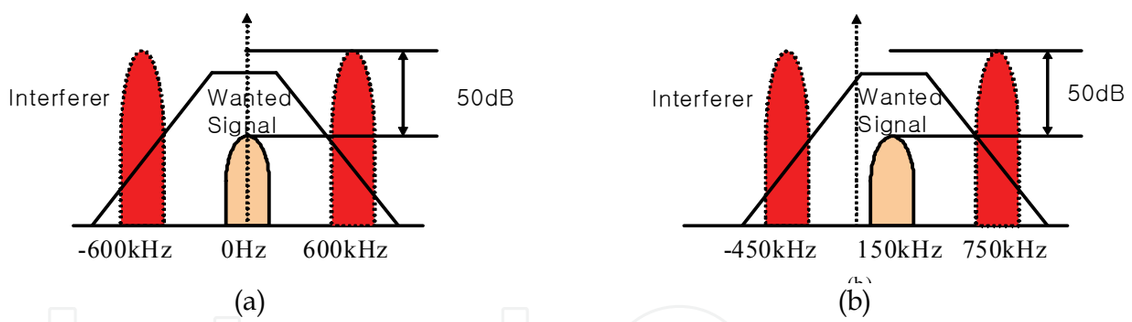


Fig. 2. Characteristic of (a) Lowpass Filter in Direct-Conversion Receiver (b) Complex Bandpass Filter in Low-IF Receiver

As shown in Fig. 2(a), if the direct conversion receiver architecture is used, the interferences are located at ±600 kHz, which can be attenuated by the lowpass filter. However, if the IF frequency is 150 kHz, the interferences are shifted to -450 kHz, +750 kHz, respectively as shown in Fig. 2(b). If the lowpass filter is used, the attenuation characteristic is tighter because the worst case interferer is seemed to be located at 450 kHz. Therefore, the complex bandpass filter whose center frequency is located at 150 kHz is designed for the ACS performance.

The transfer function of the complex bandpass filter is found by frequency translating a low-pass filter.

$$H_{bp}(j\omega) = H_{lp}(j\omega - j\omega_c) \tag{1}$$

The translation of a single pole is given in Eq. (2) and (3)

$$H_{lp}(j\omega) = \frac{1}{1 + j\,\omega/\omega_o} \tag{2}$$

$$\begin{aligned} H_{bp}(j\omega) &= \frac{1}{1 - j\,\omega_c/\omega_o + j\omega/\omega_o} \\ &= \frac{1}{1 - 2jQ + j\omega/\omega_o} \end{aligned} \tag{3}$$

A single complex pole cannot be realized with a real filter. Only complex pole pairs can be realized. The result of Eq. (2) is a single complex pole. The translated version of a single complex pole is also given with Eq. (3). The complex part must just be added to or subtracted from the complex term $2jQ$.

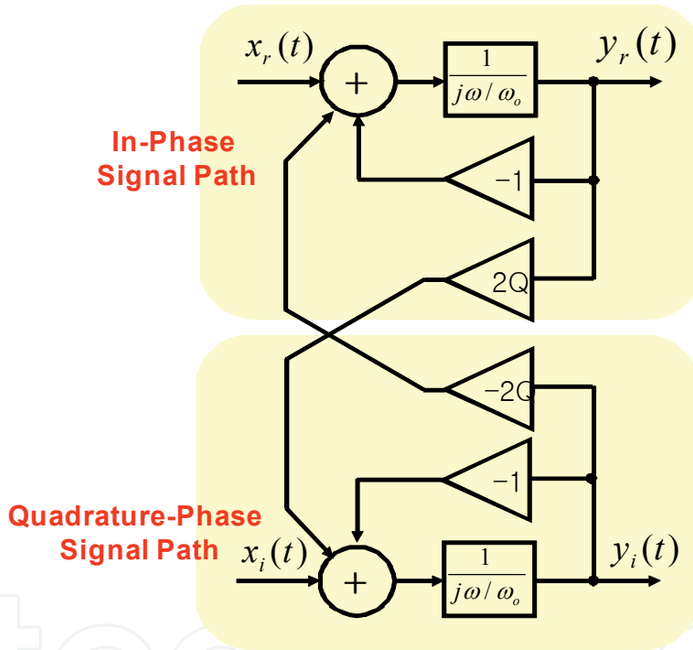


Fig. 3. Block scheme for the realization of a single complex pole.

The realization of for a single pole is given in Fig. 3. It is nothing more than the direct synthesis of the transfer function. Fig. 3 is the full block schematic with building blocks for real signals.

Fig. 4(a) shows the designed 3rd-order Chebyshev complex bandpass filter. The wanted signal is composed of the in-phase signal and quadrature signal, which are separated by the 90° phase. Complex bandpass filter uses both signals to perform the complex operations. As shown in Fig. 4(a), the complex bandpass filter has the in-phase signal path and the quadrature-phase signal path. Internal nodes of each paths are inter-connected to other paths. Therefore, I/Q mismatches is one of the most critical design issues in the complex filter. In this design, because I/Q mismatch compensation scheme is applied, I/Q mismatch is drastically reduced.

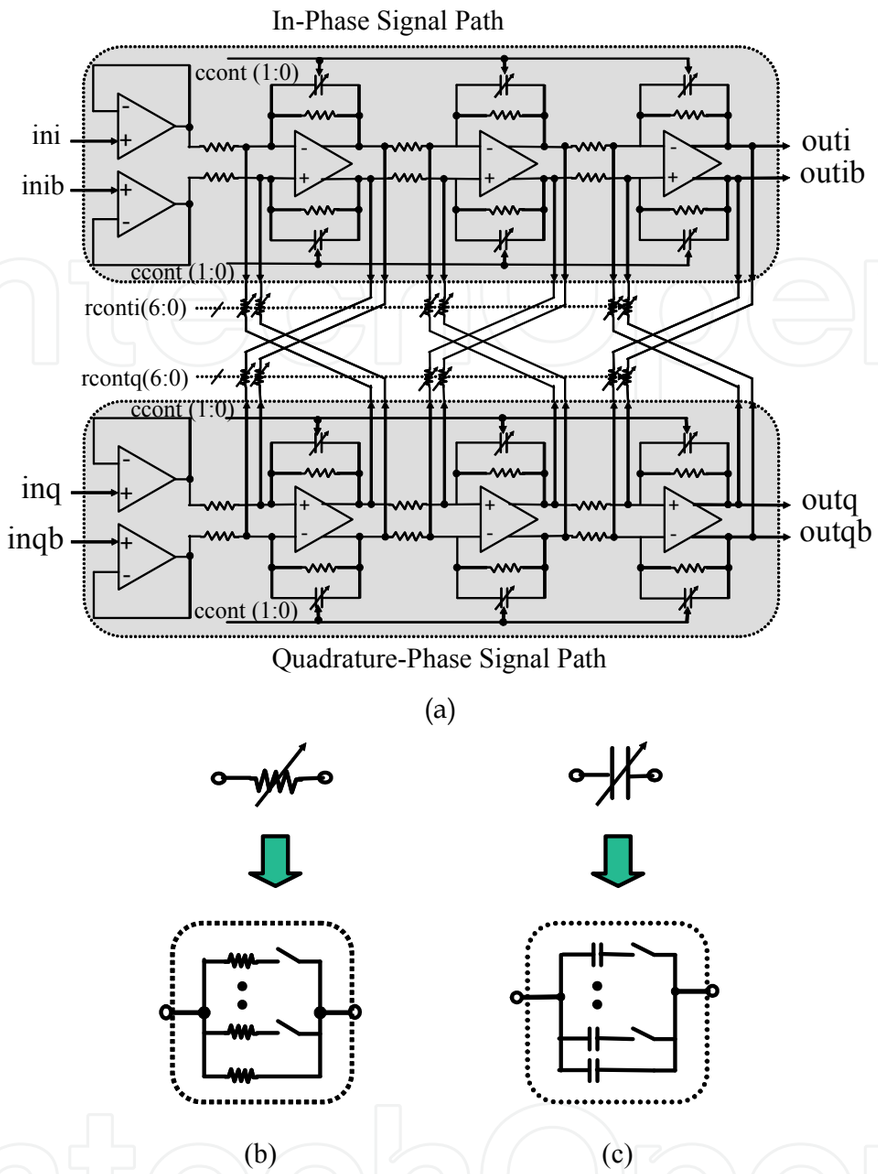


Fig. 4. (a) Schematic (b) resistor arrays (c) capacitor arrays of the complex bandpass filter

Resistor arrays and capacitor arrays are shown in Fig. 4(a). Resistor arrays are composed of resistors and switches. Resistor arrays control the center frequency of the bandpass filter and its control signals, rconti(6:0), rcontq(6:0), are set through the serial interface and represented in thermometer code.

The corner frequency was made tunable by using programmable capacitor arrays. Capacitor arrays are composed of capacitors and switches. The tuning bits, ccont(1:0), are determined from the on-chip tuning block. There are trade-offs between resistor values and capacitor values. When resistor values are reduced to make thermal noise small, capacitor values become large. That leads to a large area. On the other hand, as capacitor values become smaller to reduce the area, the noise level rises. So, capacitor values and resistor values were optimized.

3. Tuning circuit of active-RC filter

Resistors and capacitors are usually varied about ±15% due to the process variation. In continuous time filters, this leads to a large variation of the corner frequency, which in most case, must be compensated by adjusting the component values.
Conventional full analog tuning circuit based on VCO is shown in Fig. 5(a). However, this tuning circuit is not suitable to tune an active-RC filter with programmable capacitor matrices. The output of the loop filter in the PLL is analog voltage, which cannot be interfaced directly with the capacitor matrices.
On the other hand, too many digital bits are required for fine resolution in the conventional full digital circuit shown in Fig. 5(b). Thus, the area and noise level are too high due to many number of switches and capacitor matrices.

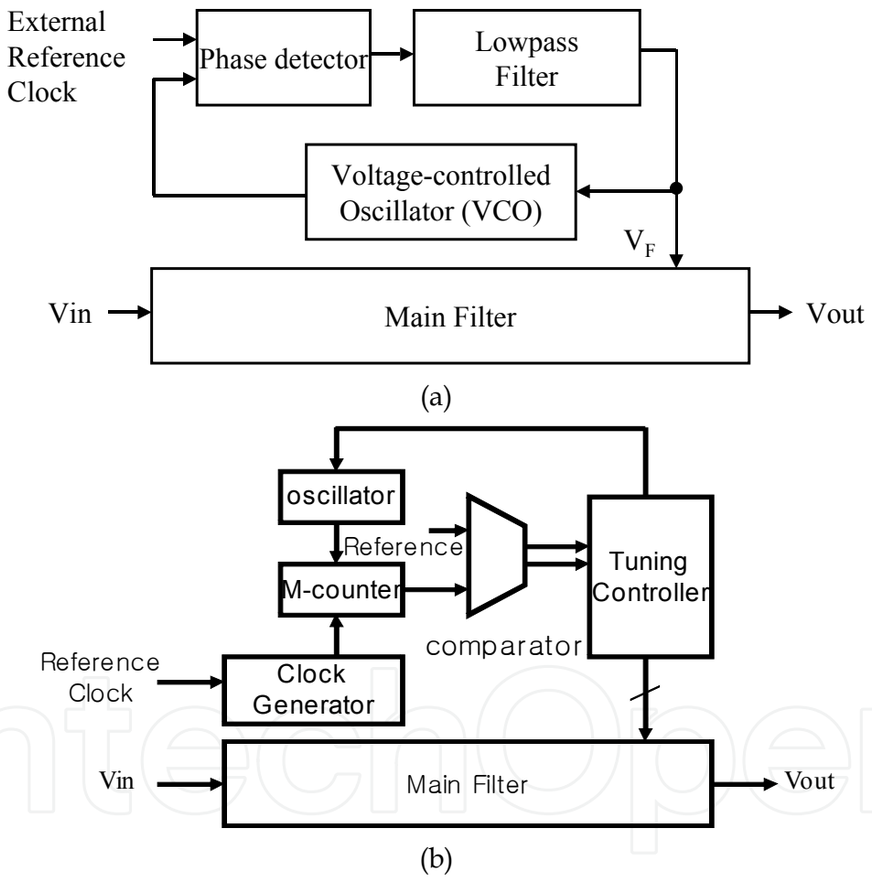


Fig. 5. (a) Full analog tuning method (b) Full digital tuning method.

The concepts of the full analog, full digital and proposed two-step tuning method are shown in Fig. 6(a), (b) and (c), respectively.
The block diagram of the proposed two-step tuning scheme is shown in Fig. 7. The clock generator provides the clocks, clk0, clk1 to coarse and fine tuning controllers. C_{tu} is charged during clk0 is high, and VCOMP is sampled by clk1. Reference voltages for comparators, Vref, Refl, RefH, RefM are generated in the reference voltage generator block. The operation is as follows. Before main capacitor tuning steps, the reference tuning loop is enabled to

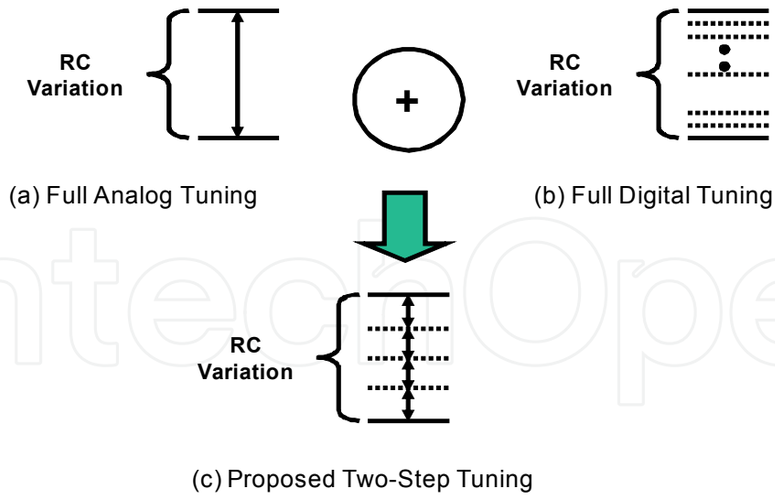


Fig. 6. Concept of (a) full analog tuning method (b) full digital tuning method (c) proposed two-step tuning method.

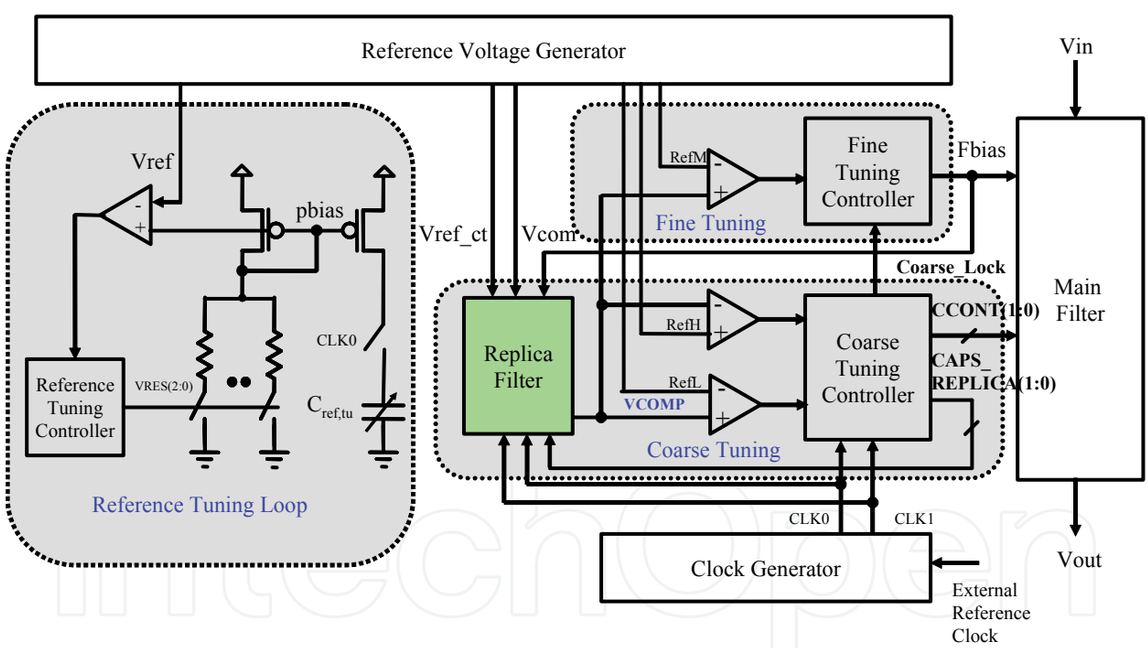


Fig. 7. Block diagram of the proposed two-step tuning method.

compensate the resistor variation. Pbias is compared with Vref, and vres(2:0) is controlled according to the result. When pbias is larger than Vref, resistor load should be smaller, so vres(2:0) is increased. On the other hand, if pbias is smaller than Vref, resistor load should be larger, so vres(2:0) is decreased. Reference tuning is completed when pbias crosses the Vref.

After the reference tuning, main capacitor tuning is done in two-steps, that is, the coarse tuning and the fine tuning.

Fig. 8 shows the timing diagram of the proposed two-step tuning method.

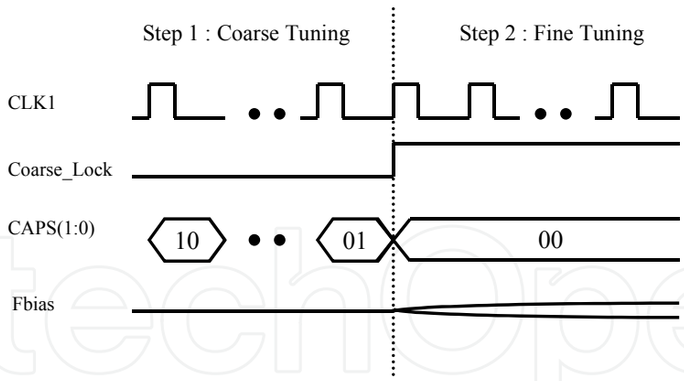
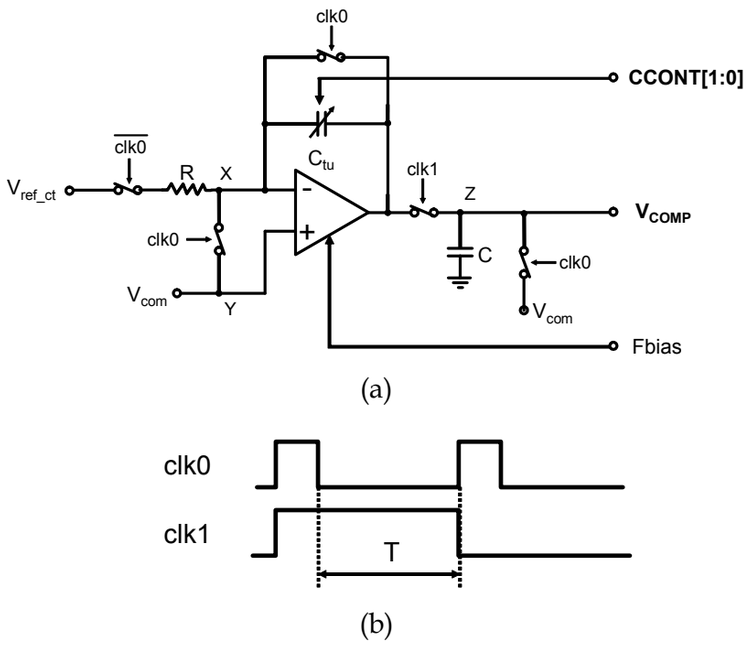


Fig. 8. Timing diagram of the proposed tuning method.



(a)

(b)

Fig. 9. (a) Block diagram (b) timing diagram of the replica filter in coarse tuning block.

Fig. 9 shows the block diagram and the timing diagram of the replica filter in the coarse tuning block. When VCOMP voltage is precharged when clk0 and clk1 are high. When clk0 goes from high to low, the VCOMP voltage is determined as Eq. 4.

$$VCOMP = V_{com} - \frac{1}{RC_{tu}}\left(V_{ref\_ct} - V_{com}\right)T \tag{4}$$

First, CCONT(1:0) are tuned until VCOMP is located between pre-determined ranges. VCOMP is compared with refL and refH. When VCOMP is higher than refH, CCONT(1:0) are increased. Whereas, if VCOMP is lower than refL, CCONT(1:0) are decreased. When VCOMP is located between refL and refH, coarse_Lock signal goes from low to high. Usually, many tuning capacitance levels are required for fine resolution. But, only two bits are sufficient in this design with the two-step tuning method. After the coarse_lock signal is asserted, the corner frequency is tuned by the fine tuning control block.

Fbias controls the tail current of the op-amp. Thus, the DC-gain of the op-amp is changed according to the Fbias voltage. If the DC-gain of the op-amp is infinite, the cut-off frequency does not change. However, because the DC-gain of the op-amp is finite, the cut-off frequency of the filter is changed as the DC-gain of the op-amp changes. Fbias is compared with refM. When VCOMP is larger than refM, Fbias should be increased. On the other hand, Fbias should be decreased when VCOMP is smaller than refM. The range of Fbias is 0.8 V to 1.2 V. The bandwidth of the op-amp is adjustable according to the mode to save the power. And the transistor sizes in the op-amp are designed to be very large to reduce the 1/f noise.

4. Experimental results

4.1 Multi-mode, multi-band active-RC low-pass filter

The multi-mode, multi-band active-RC low-pass filter was fabricated using a 0.35 μm CMOS process. The chip area is 3.8 mm^2 and the supply voltage is 3 V.

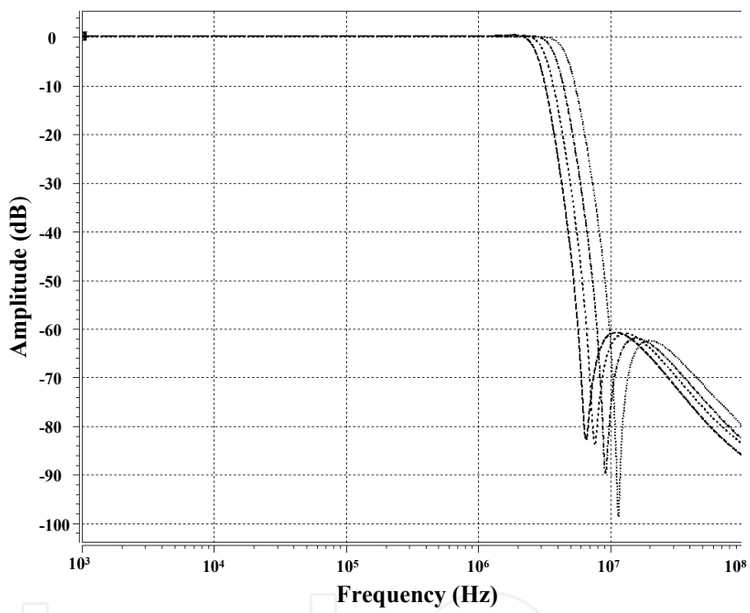


Fig. 10. Amplitude response of the filter in WCDMA mode.

Fig. 10 shows the amplitude response of the filter in WCDMA mode at every code. The cut-off frequency is 2.1 MHz in WCDMA mode. The current consumptions are 5.2 mA, 6.1 mA, 7.1 mA, and 8.4 mA, respectively. The current in PDC mode is less than that of WCDMA mode because the gain and the bandwidth of the op-amp are smaller in PDC mode. The frequency tuning range is from 10 kHz to 3MHz. Out-of-band IIP3 was determined by performing IM3 test. In PDC mode, when two tones of +15 dBm at 20 kHz and 30 kHz are applied, IM3 is –77 dBm. In WCDMA mode, out-of-band IM3 is –68 dBm, when two tones of +14 dBm at 1.8 MHz and 3.0 kHz are applied. Input-referred average passband noise densities of the filter are 250, 130, 85, and 54 $nV/\sqrt{Hz}$ for PDC, GSM, IS-95, and WCDMA, respectively. The passband ripple is less than 0.5 dB in all modes. The stopband rejections are 79, 79, 75, and 75 dB for PDC, GSM, IS-95, and WCDMA, respectively. Table 2 summarizes the performance of the filter.

Technology	0.35 μm CMOS			
Chip area	3.8 mm²			
Supply voltage	3 V			
Tuning range	10 kHz ~ 3 MHz			
	PDC	GSM	IS-95	WCDMA
Current (mA)	5.2	6.1	7.1	8.4
IIP3 (dBm)	28	25	23	21
Noise ($nV/\sqrt{Hz}$)	250	130	85	54
Passband ripple	0.5	0.5	0.5	0.5
Stopband rejection	79	79	75	75

Table 2. Performance summary

4.2 Tunable active-RC complex band-pass filter

The complex bandpass filter was fabricated using a 0.35 μm CMOS process. The chip area is 3.8 mm². The supply voltage is 3 V. Fig. 11 shows the microphotograph.

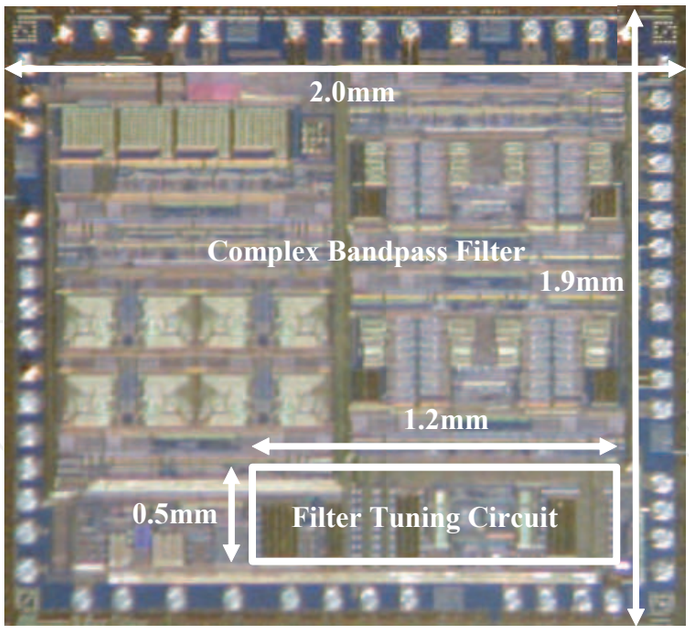


Fig. 11. Chip microphotograph

Fig. 12 shows measured amplitude response of the complex baseband filter, when the temperature is changed from -10°C to 60°C. The cut-off frequency is 150 kHz ± 110 kHz. The cut-off frequency is almost constant as the temperature is changed due to the proposed filter tuning method.

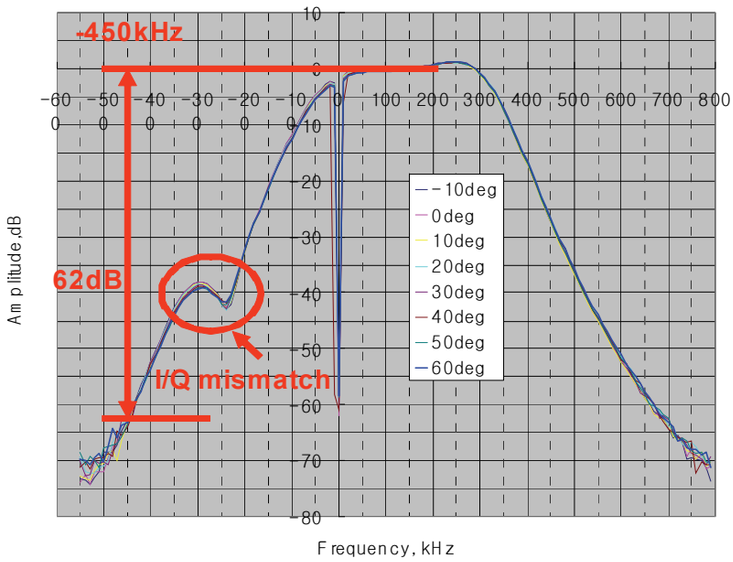


Fig. 12. Measured amplitude response of the complex bandpass filter

The power consumption is 13 mW. The frequency tuning range is 100 kHz, which is the 50% of the signal bandwidth. That is, the cut-off frequency can be adjusted by 100 kHz although it is shifted due to the temperature, the supply voltage, and the process variations.
Out-of-band IIP3 was determined by performing IM3 test. When two tones of -44 dBm at 600 kHz and 1.2 MHz are applied, IIP3 is +25 dBm.

Input-referred average passband noise density of the filter is $85\,nV/\sqrt{Hz}$. The passband ripple is less than 0.8 dB, and the stopband rejection at -450 kHz is 66 dB. Table 3 summarizes the performance of the filter.

Technology	0.35 μm CMOS
Chip area	3.8 mm²
Supply voltage	3 V
Tuning range	100 kHz
Power (mW)	13
IIP3 (dBm)	25
Noise ($nV/\sqrt{Hz}$)	85
Passband ripple	0.8

Table 3. Performance summary

5. Conclusion

The CMOS multi-mode, multi-band low-pass filter and complex baseband filter are presented. Capacitors and resistors were shared to minimize the area. Proposed two-step tuning method can reduce the number of switches and thus, can reduce the noise and the area.

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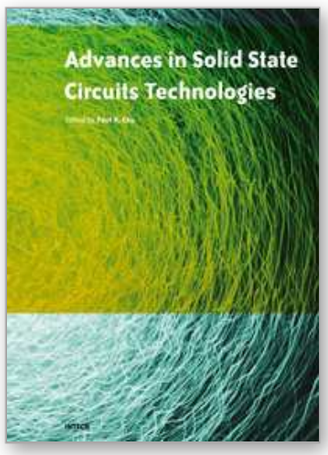

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This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

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