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All-optical flip-flops based on semiconductor technologies

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1. Introduction

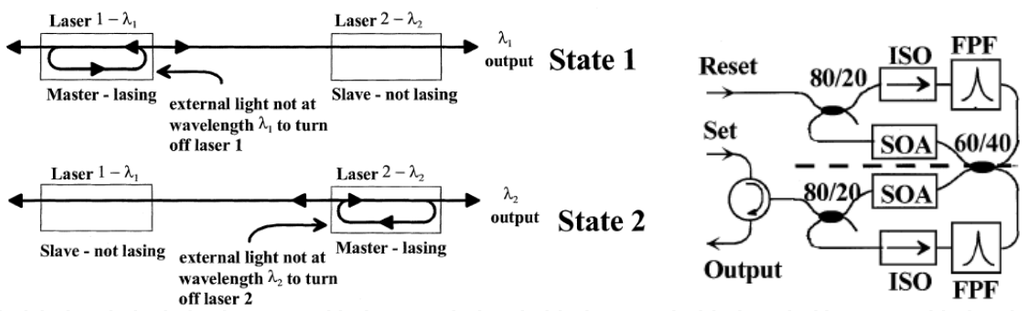
Optical technologies represent the main bet for future communication systems. Among the others, digital subsystems for optical processing are of great interest thanks to their intrinsic properties in terms of bandwidth, transparency, immunity to the electromagnetic interference, cost, power consumption, as well as robustness in hostile environment. Key basic functions are represented by logic gate, logic function, flip-flop memories, optical random access memories, etc.. Research in this field is in its very early stages even if some interesting techniques have been already theoretically addressed and experimentally demonstrated. Here we review the state of the art for all-optical flip-flop based on semiconductor technologies: best result will be highlighted in terms of transition speed, switching energy, complexity and power consumption; we will then discuss some new achievement we have recently reached.

All-optical packet switching seems to be the most promising way to take advantage of fiber bandwidth to increase routers forwarding capacity, being able to achieve very high data rate operations. All-optical flip-flops have been widely investigated mainly because they can be exploited in all-optical packet switches, where switching, routing and forwarding are directly carried out in the optical domain. Some examples concerning optical packet switches are shown in (Dorren et al., 2003; Liu et al., 2005; Bogoni et al., 2007; Herrera et al., 2007), where an optical flip-flop stores the switch control information and drives the switching operation. Former solutions for all-optical flip-flops have been demonstrated exploiting discrete devices (Dorren et al., 2003) or Erbium-doped fiber properties (Malacarne et al., 2007) which suffer from slow switching times and high set/reset input powers. Several integrated or integrable solutions (Hill et al., 2004; Liu et al., 2006) present a switching energy in the fJ range and switching times of tens of ps at the expenses of poor contrast ratios. On the other hand in (Hill et al., 2005) an integrated scheme exhibiting a very high contrast ratio value but with transition times in the ns range is reported. In any case a

trade off between contrast ratio and edges speed must be found as a function of the flip-flop application. Micro-resonators-based bistable element has been demonstrated (Van et al., 2002) presenting high optical operating power, pJ switching energies and microsecond switching times, theoretically reducible down to the order of tens of ps. Making a comparison with electronics, recent large-scale integration (LSI) circuits (Keyes, 2001) show switching energies of 1fJ even though with slower switching speeds. In (Dorren et al., 2003), a solution based on coupled ring lasers is proposed. This solution offers a certain number of advantages: it can provide high contrast ratios between states; there is no difference in the mechanisms for switching from state 1 to state 2 and vice-versa, making symmetric set and reset operations; it presents a large input light wavelength range and a controllable switching threshold. Moreover, considering an integrated version of this kind of flip-flop, through numerical analysis a switching energy in fJ range has been demonstrated.
Here we will describe the above mentioned solutions underlining the main benefits, drawback, limitation and perspectives. We will then present our activities on clocked flip-flops, and an example of their use in an all-optical counter. Finally, we will present an SOA-based flip-flop which is able to switch with very short rising and falling edges, and we use it in a realistic switching operation. Integrability of our solutions is also discussed.

2. State of the art

One of the simplest way that was originally proposed to implement an optical flip-flop includes two coupled lasers (Hill et al., 2001), as depicted in Fig. 1 (a). The system can have two stable states. In state 1, light from laser 1 suppresses lasing in laser 2. In this state, the optical flip-flop memory emits CW light at wavelength λ_1. Conversely, in state 2, light from laser 2 suppresses lasing in laser 1, and the optical flip-flop memory emits CW light at wavelength λ_2. To change states, lasing in the dominant laser can be inhibited by injecting external light with a different wavelength and opportune power. The output pulse of an optical header processor can be used to set the optical flip-flop memory into the desired wavelength. From the theory it also follows that laser driving currents and coupling coefficient determines the required switching light power.
This flip-flop has also been implemented in a ring configuration based on Semiconductor Optical Amplifiers (SOA), as shown in Fig. 1 (b) (Dorren et al., 2003). Two SOAs act as the lasers gain media. Fabry–Pérot filters (FPF) with a bandwidth of 0.18nm have been used as wavelength selective elements. Optical pulses were used to set and reset the flip-flop. The optical spectrum of the flip-flops' output states is shown in Fig. 2.
The switching time between the two lasing modes is inversely proportional to the length of the laser cavities. Thus, in order to allow switching times in the range of picoseconds, an integrated solution has to be adopted. This was realized in (Hill et al., 2004), where a photonic flip-flop based on two coupled micro-ring lasers with dimensions of 20x40 μm^2 was reported, exhibiting a switching time of 18ps and a switching energy of a few fJ.
The micro-ring lasers were fabricated in active areas of the integrated circuit containing bulk 1.55nm bandgap InGaAsP in the light guiding layer. Separate electrical contacts allowed each laser's wavelength to be individually tuned by adjusting the laser current. Passive waveguides connected the micro-ring lasers to the integrated circuit edges (Fig. 3). Micro-ring lasers typically have two inherent lasing modes; laser light traveling in the clockwise (CW) direction, and laser light in the anticlockwise (ACW) direction.



(a) (b)

Fig. 1. (a): Arrangement of two coupled identical lasing cavities forming a flip-flop, showing the two possible states. (b): Implementation of the optical flip-flop memory

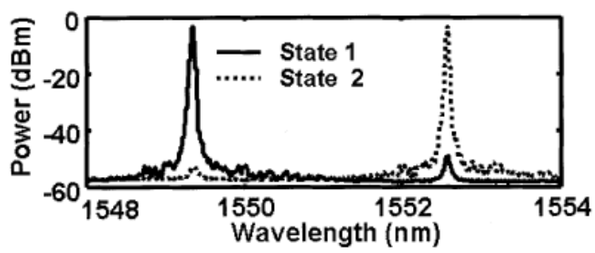


Fig. 2. Spectral output of two states of the optical flip-flop memory.

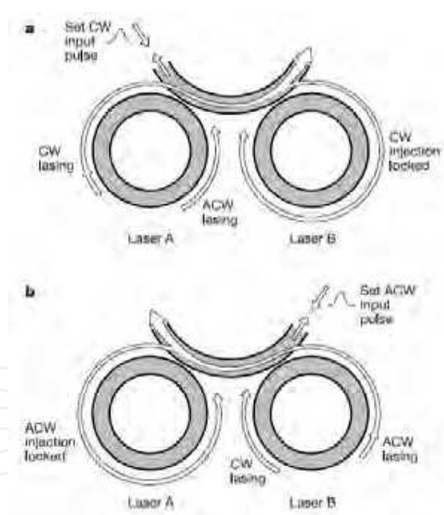


Fig. 3. Two micro-ring lasers coupled via a waveguide to form an optical flip-flop.

In state A, CW light from laser A is injected via the waveguide into laser B. The light from laser A will undergo significant resonant amplification in laser B if the resonant frequencies of the two laser cavities are close. This injected light competes with the laser B self-oscillations for available power from the laser gain medium. If sufficient light is injected into laser B, then the laser B gain will be decreased below threshold. This extinguishes the laser B self-oscillation, and laser A captures or injection-locks (Buczek et al., 1971) laser B, forcing light to circulate only in the CW direction. To set the system in one state or another, light

close to the lasing wavelength and polarization can be injected into the waveguide connecting the lasers. This light will set both lasers simultaneously lasing in either the CW or ACW direction. The different states can be distinguished by the different power levels at the two outputs. The power level at the output associated with the locked laser will be three times that of the other output. Additionally, the lasing wavelengths of the lasers may be different, allowing the states to be distinguished by the wavelength of the light output.

Another scheme recently proposed (Malacarne et al., 2007) exploits absorption and fluorescence of few meters of erbium–ytterbium (Er–Yb)-doped fiber. This solution suffers from slow switching times and high set/reset input powers, and since it doesn't exploit semiconductor devices, it will not be studied in depth here.

In (Liu et al., 2006) a solution that offer the advantage of being fully packaged, was presented. It is based on an hybrid integrated circuit consisting of two coupled Mach-Zehnder interferometers (MZIs), each having one SOA in one arm. The schematic of the circuit is shown in Fig. 4.

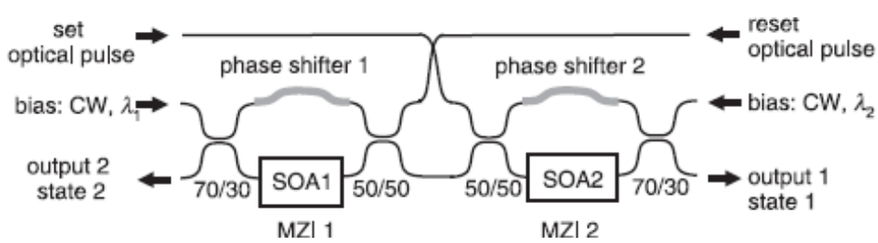
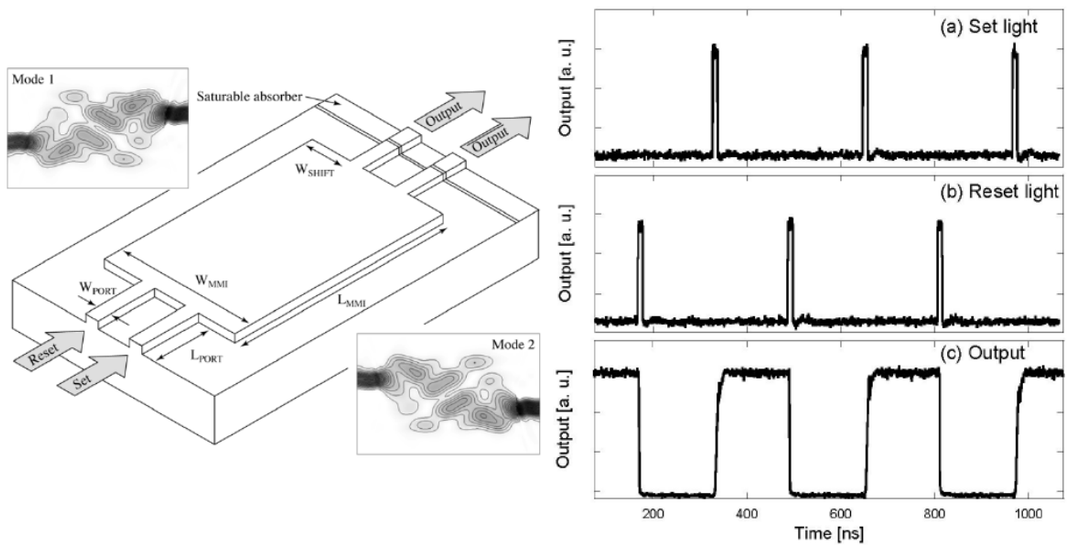


Fig. 4. Schematic diagram of optical flip-flop memory proposed in (Liu et al., 2006).

Each MZI (MZI 1 and MZI 2 in the figure) has an SOA in one arm. A laser emits a continuous-wave (CW) bias light at wavelength λ_1 that is fed into MZI 1. The MZI 1 output is sent into MZI 2, which has the same structure, but biased by a CW light with a different wavelength, λ_2. The system has two possible states: in state 1, the MZI 1 output suppresses output from MZI 2, so λ_1 dominates the output; in state 2, the MZI 2 output suppresses output from MZI 1, and then λ_2 is dominant. When the CW light with λ_1 is injected into MZI 1, MZI 1 is biased in such a way that the light out of MZI 1 goes mostly into the low branch of the 50/50 coupler output. This light then flows into MZI 2 via the 50/50 coupler in MZI 2, and affects the gain and phase shift for light propagating through it. The MZI 1 light perturbs the SOA 2 properties so that the CW bias 2 light (λ_2) propagating through SOA 2 and phase shifter 2 goes mostly into the top output of the 50/50 coupler in MZI 2. Then the CW bias 2 light (λ_1) does not travel into the MZI 1, and does not affect the properties of SOA 1. Actually, the MZI 1 output suppresses output from MZI 2. The states of the system can be switched by sending a light pulse (via Set or Reset port) into the MZI that is currently dominant. This light will switch the MZI output away from suppressing the other MZI, allowing the other MZI then to become dominant.

An optical flip-flop based on two-mode bistability in a multimode interference bistable laser diode (MMI-BLD) has also been reported (Takenaka et al., 2005). A schematic view of the MMI-BLD is shown in Fig. 5 (a). All waveguides including the 2x2 MMI coupler consist of active materials. Saturable absorbers are located at the end of the output ports to obtain hysteresis. The 2x2 MMI is designed as a cross coupler, so that only two cross-coupled lasing modes can exist as illustrated in the insets of Fig. 5 (a). Two-mode bistability between

these two lasing modes will occur due to cross gain saturation and the saturable absorbers if the injection current is within the hysteresis loop (Takenaka & Nakano, 2003).



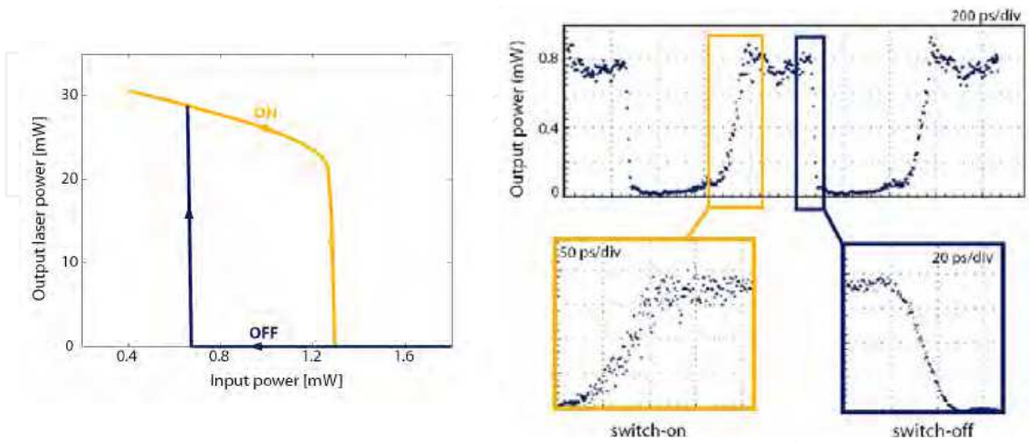
(a) (b)

Fig. 5. (a): Schematic view of the MMI-BLD. Two cross-coupled lasing modes are illustrated in the insets. (b): All-optical flip-flop operation of the MMI-BLD.

A set signal injected into the set port saturates the absorption to Mode 1, causing Mode1 to start lasing. At the same time, cross-gain saturation and the absorption to Mode 2 by the saturable absorber suppress Mode 2. In a similar manner, a reset signal switches the lasing mode from Mode 1 to Mode 2. Therefore, all-optical flip-flop operation is achievable with the MMI-BLD, because external light injection to each input port will select the mode to lase. The corresponding operation, showing the optical power at one of the waveguide output when set and reset pulses are applied is depicted in Fig. 5 (b).

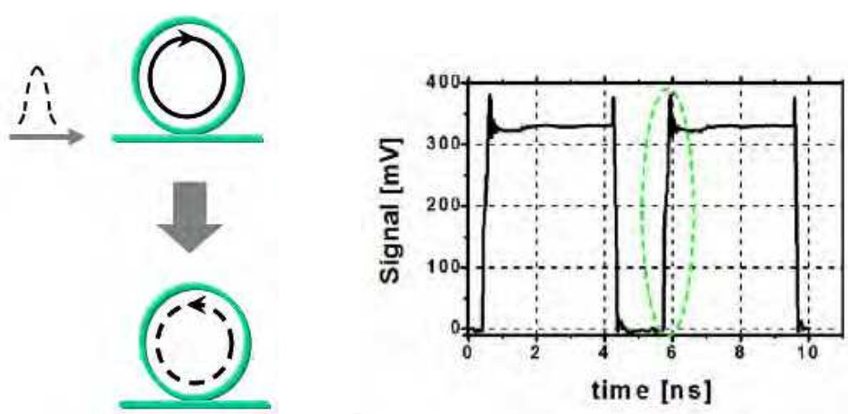
In (Huybrechts et al., 2008) a single DFB laser diode has been used to realize a flip flop. A DFB laser injected with CW light shows two different stable states: one in which the laser is lasing and another one where it is switched off. When the laser is lasing, the gain will be clamped and relatively small. Therefore, the injected light experiences only a small amplification and has almost no influence on the laser light. In the second state, the laser is switched off and the injected light experiences a high amplification. This results in a rising power progression throughout the cavity and therefore a non-uniform distribution of the carriers, known as spatial hole burning. This will affect the refractive index, leading to a distortion of the Bragg reflections in the laser diode. The losses inside the cavity will become higher and the threshold for lasing will rise. Eventually the laser will stay switched off. The two states are equally possible for a range of input powers of the injected light and this gives a bistability in the lasing power (Fig. 6 (a)). This bistability can be exploited to obtain flip-flop operation by injecting short optical pulses: a pulse injected at the same side as the CW light will move the DFB laser out of the hysteresis curve and will switch off the laser; to switch the laser on again, a pulse is injected from the other side, since this will restore the uniformity of the carrier distribution. In the experiment, the set and reset pulses were obtained from an ultra-short pulse source generating 7ps-long pulses. The obtained results

are depicted in Fig. 6 (b). The set-pulses have an energy of 75fJ and the reset-pulses 190 fJ. The repetition rate is 1.25GHz and the switch-on time is 75ps. An almost immediate switch-off time of 20ps has been obtained, which corresponds with the resolution of the optical scope.



(a) (b)

Fig. 6. (a): Bistability of an injected DFB laser as a function of the injected power. (b): Results.



(a) (b)

Fig. 7. (a): Operation principle of the monolithic semiconductor ring laser. (b): Results.

As discussed previously, integrable solutions are preferred since they would allow high-density packaging, with the possibility of reducing costs, power consumption, and operation speed. To achieve these results, researchers are investigating novel technologies in order to reduce as much as possible device dimensions. A possible solution towards this direction is the use of a monolithic semiconductor micro-ring laser (Trita et al., 2009) which shows an intrinsic and robust directional bistability between its CW and ACW propagating modes. If the ring laser is correctly set, injecting a laser pulse in one direction makes the laser emit in that direction (Fig. 7 (a)). Experiments show a switching time of about 20ps for both rising and falling edges, with set/reset pulses of 5ps and 150fJ energy.

Another promising technology is nano-photonics, exploited in the realization of photonic crystals (PCs) and quantum dots (QDs). By combining these technologies one could take

advantage of both the band-gap effect and the highly dispersive property of PCs, and the high-density of state and high nonlinear property of QDs.

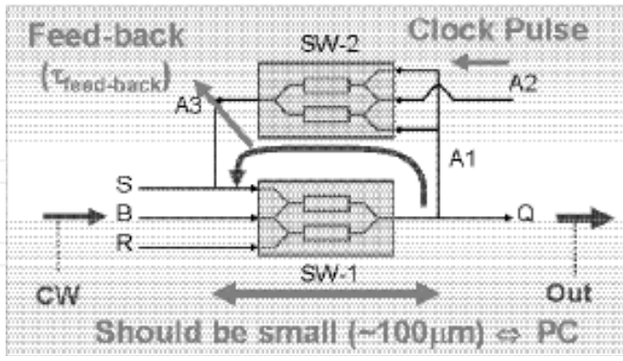


Fig. 8. Schematic diagram of the PC-FF.

A Mach Zehnder-type all-optical flip-flop developed by combining GaAs-based two-dimensional photonic crystal (2DPC) slab waveguides and InAs-based optical nonlinear QDs has been proposed in (Azakawa, 2007). The photonic crystal-based flip-flop (PC-FF) schematic is shown in Fig. 8, and is based on two photonic-crystal-based Symmetric Mach Zehnder (PC-SMZ) switches. The principle of the PC-SMZ is based on the time-differential phase modulation caused by the nonlinear-induced refractive index change in one arm of the two interferometers. 2DPC waveguides are composed of single missing line defects, while nonlinear-induced phase shift arms are selectively embedded with QDs. The mechanism of the third-order nonlinear property is an absorption saturation of the QD caused by a control (pump) pulse. A resultant refractive index change produces a phase shift for the signal (probe) pulse. A wavelength of the control pulse is set to the absorption peak of the QD, while a wavelength of the signal pulse is set in the high transmission range in the 2DPC waveguide with the QD. A single PC-SMZ switch would operate as a pseudo-flip-flop, meaning that the on-state is limited by the carrier relaxation time in the nonlinear material (~ 100ps in the experiment). In order to change the pseudo FF into the normal FF operation, the scheme of Fig. 8 was proposed. An output signal of the PC-SMZ impinges into an optical AND element (which is another PC-SMZ switch) via a feedback loop, where another input pulse, i.e., a clock pulse impinges. An output of the AND element is combined to the set pulse, as shown in the figure. The clock pulse serves as a refresh pulse to expand the on-state period against the relaxation of the carrier, while the feedback signal restricts the clock pulse to be controlled by the set and reset pulses. The feasibility of this idea has been verified only by computer simulation.

3. Flip-flops based on coupled SOA ring lasers: advantages and limitations

In order to investigate advantages and drawbacks of SOA-based solution we consider the setup shown in Fig. 9. The flip-flop consists of two coupled ring lasers emitting at two different wavelengths (λ_1=1550nm and λ_2=1560nm). In each ring, an SOA acts as the gain element, a 0.25nm band-pass filter (BPF) is used to as select the wavelength, and an isolator makes the light propagation unidirectional. Both the SOAs are polarization insensitive

Multi-Quantum Well (MQW) structures with a small-signal gain of 31dB, saturation power of 13dBm and Amplified Spontaneous Emission (ASE) noise peak at 1547nm.

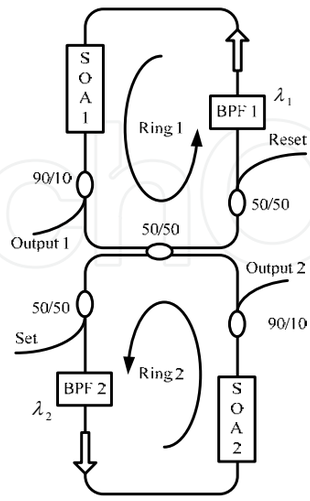


Fig. 9. Experimental Setup of the all-optical flip-flop based on SOAs.

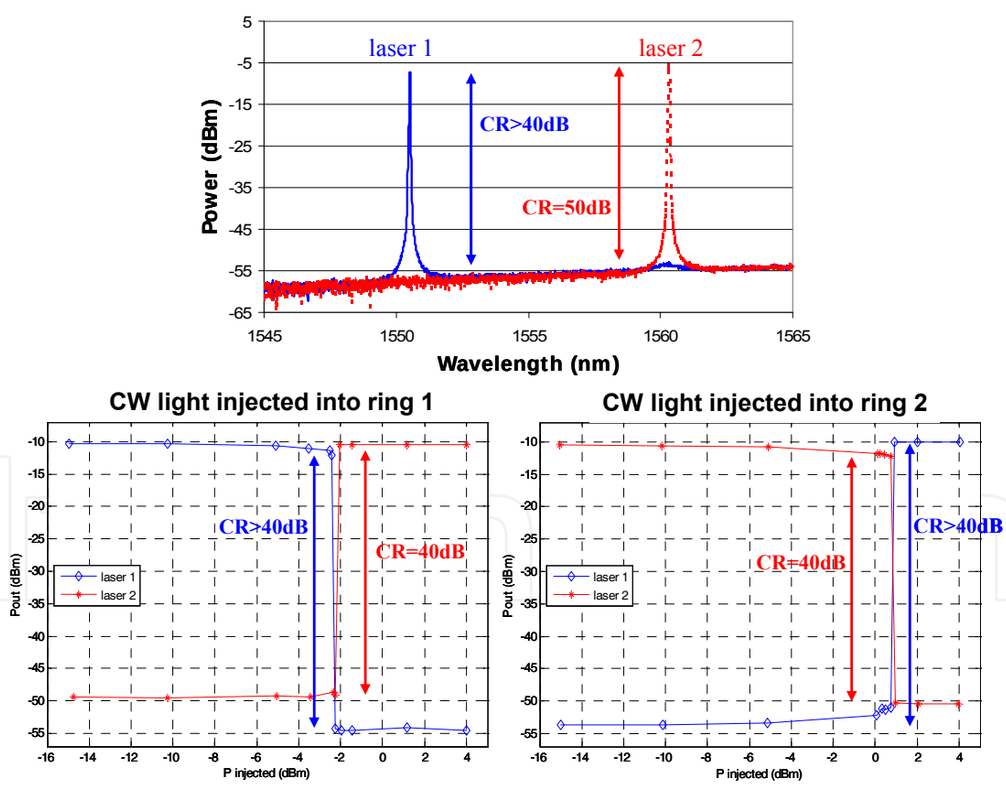


Fig. 10. Top: optical spectra of the two states; Bottom: output power of lasers versus input power injected into cavity 1 (left) and into cavity 2 (right).

The system can have two states. In “state 1”, light from ring 1 suppresses lasing in ring 2, reaching cavity 2 through the 50/50 coupler and saturating the SOA 2 gain. In this state, the

optical flip-flop output 1 emits CW light at wavelength λ_1.In "state 2" light from ring 2 suppresses lasing in ring 1 (saturating SOA 1 gain), and output 2 emits CW light at wavelength λ_2. To dynamically change state, lasing in the dominant cavity can be switched off by injecting external pulsed light with a wavelength different from λ_1 and λ_2 (λ_{IN}=1554.5nm). In Fig. 10 experimental measurements of the two states optical spectra are investigated and a graph of the output power of both the ring lasers, versus the CW input power injected into each cavity is reported. The output contrast ratios are higher than 40dB.

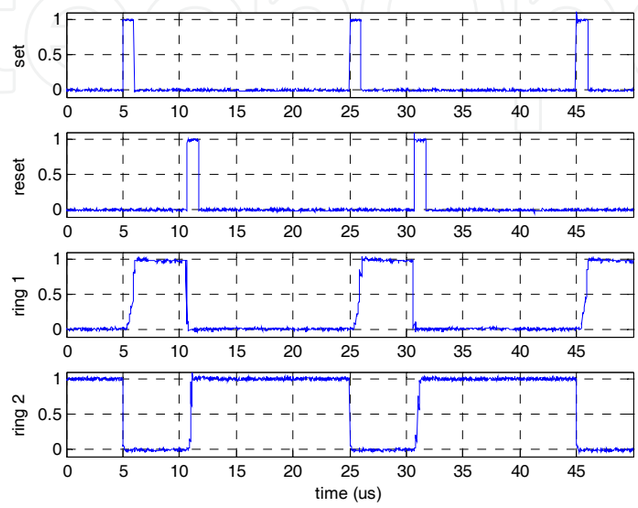


Fig. 11. Experimental results of the all-optical flip-flop output.

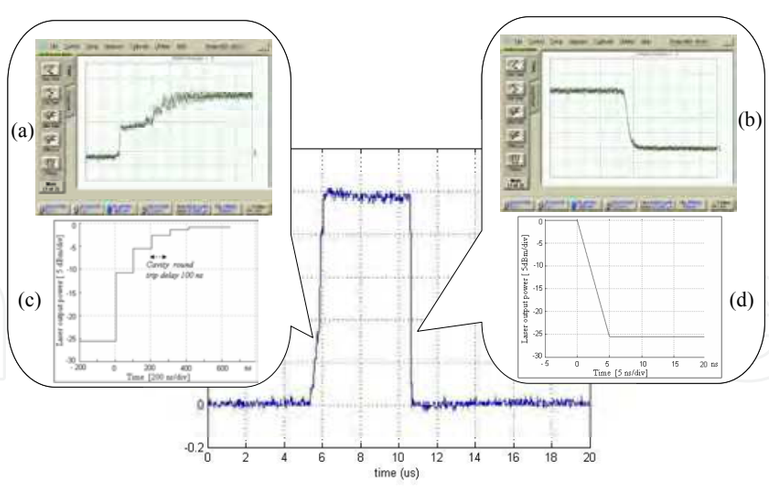


Fig. 12. Measured (a)-(b) and simulated (c)-(d) behavior of the flip-flop output edges.

By injecting two regular sequences of pulses into the set and reset ports, we demonstrate the dynamic flip-flop operation shown in Fig. 11. We experimentally observed that the flip-flop falling time only depends on the edge time of control pulses (5ns in this section), while the rising time is determined by the cavity length and by the length of the fiber between the two SOAs. In our setup, each ring has a cavity length of 20m corresponding to a round-trip time

of about 100ns. Experimental measurements (Fig. 12 (a)) show that the building-up process of one state takes place step by step and each step corresponds to a cavity round-trip time equal to 100ns. The total rising edge behavior lasts several hundreds of ns. The experimental falling edge behavior is shown in Fig. 12 (b), with a transition time of 5ns, equal to the input pulse edge.

Dynamics behavior of the two SOA-based coupled lasing cavities has been analyzed through simulations as well, whose details can be found in (Barman et al., 2007). Assuming the same parameters of the experimental setup (cavity length and cavity loss, injected pulses edge time and average power), as can be observed in Fig. 12 (c)-(d), simulation results for rising and falling edges are in good agreement with experimental measurements, confirming the step behavior of the rising edge and at the same time a falling edge as fast as the input pulse edge. We also simulated an integrated version of this flip-flop, considering 2mm cavity length and 0.5mm SOA length. Results predict 12ps falling time and ~40ps rising time with injected input pulsewidth of 12ps and pulse energy of 15.6fJ, comparable with the results of one of the latest optical flip-flop integrated version (Hill et al., 2004).

4. SOA-based clocked flip-flops

Most of the all-optical flip-flops proposed in literature are non-clocked devices, whose output changes immediately following the set/reset signals, thus they are also referred to as Set-Reset (SR) latch. As a digital device that temporarily memorizes the past input signal and processes it with current inputs, optical flip-flop is expected to be synchronized with a system clock, and to work in a timely programmed mode. Moreover, in some complicated optical computing applications such as optical shift registers or counters, various types of clocked flip-flops are necessary, such as SR, D, T, and JK flip-flops.

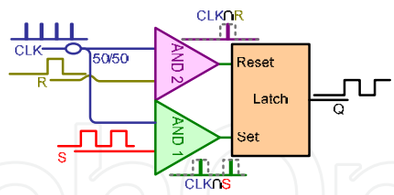
Starting from the basic structure defined in the previous paragraph, here we show clocked all-optical flip-flops including SR, D, T, and JK types, exploiting also AND logic gates based on nonlinear effects in SOA (Wang et al., 2009, a).

4.1 Clocked SR flip-flop

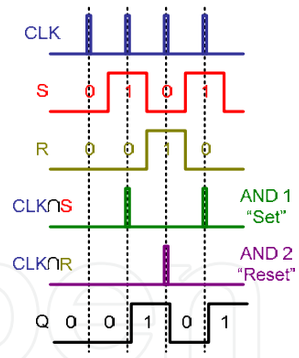
The characteristic table of the set/reset (SR) flip-flop is shown in Fig. 13 (a). If S=R=0, the flip-flop remains at its previous state; if S=1 R=0, it is set to "state 1"; if S=0 R=1, it is set to "state 0". S=R=1 is forbidden since the flip-flop is unstable in this case. The setup of clocked SR flip-flop is shown in Fig. 13 (b): it consists of two AND gates and one SR latch. "AND 1" and "AND 2" perform AND function between the clock pulse and S and R, respectively. The outputs of "AND 1" and "AND 2" are connected to the "Set" and "Reset" ports of the latch respectively. The operation principle of this clocked flip-flop is shown in Fig. 13 (c): when a clock pulse comes, if S=R=0 it can not pass through either "AND 1" or "AND 2", so "Set" and "Reset" ports receive no pulse and the latch maintains its previous state (Q_{next}=Q); if S=1 R=0, the clock pulse can pass through "AND 1" but is blocked by "AND 2", so only "Set" receives a pulse and the latch is set to "state 1" (Q_{next}=1); if S=0 R=1, the clock pulse can pass through "AND 2" but is blocked by "AND 1", so the latch is set to "state 0" (Q_{next}=0). S=R=1 is forbidden since the latch is unstable when "Set" and "Reset" receive pulses simultaneously. The flip-flop is clocked because it only changes state when a clock pulse comes, according to the S and R values at that time. S and R values at any other time are ignored.

S	R	Q_{next}	Comment
0	0	Q	Hold state
1	0	1	Set
0	1	0	Reset
1	1	N/A	Forbidden

(a)



(b)



(c)

Fig. 13. Clocked SR flip-flop: (a) characteristic table; (b) logic circuits; (c) working principle.

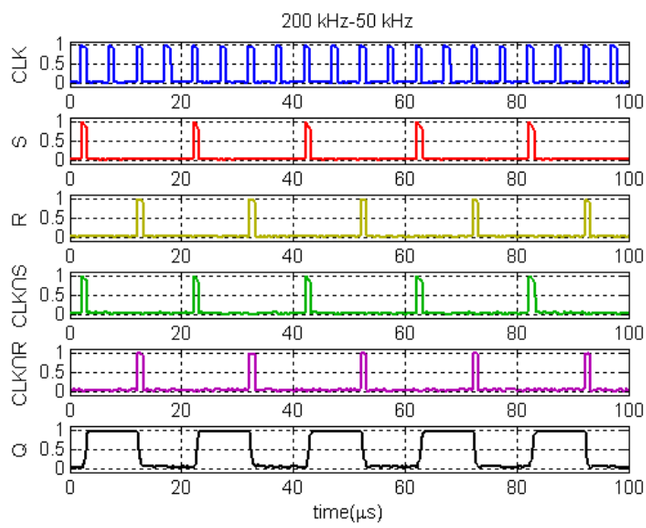


Fig. 14. Clocked SR flip-flop operation.

In Fig. 14 the experimental operation of the clocked SR flip-flop is reported. The clock pulse has a repetition rate of 200kHz with a pulse-width of 1μs. S and R signals also have a pulse-width of 1μs but at a repetition rate of 50kHz, synchronized with the clock. The wavelengths of clock, S and R are λ_{CLK}=1554.1nm, λ_S=1552.5nm and λ_R=1550.5nm respectively, and the outputs of "AND 1" and "AND 2" are at $\lambda_1=2\lambda_S-\lambda_{CLK}$=1550.9nm and $\lambda_2=2\lambda_R-\lambda_{CLK}$=1546.9nm. The flip-flop only responses to the S and R values when a clock pulse comes, but ignores the S and R at any other time, in agreement with Fig. 13 (c).

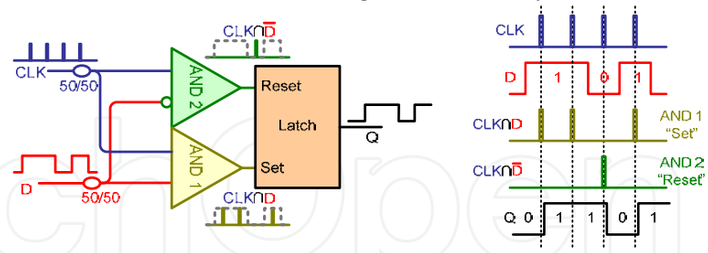
4.2 Clocked D flip-flop

The characteristic table of D flip-flop is shown in Fig. 15 (a). D represents the data signal. If D=0, the flip-flop is set to "state 0"; if D=1, the flip-flop is set to "state 1". The setup of clocked D flip-flop is shown in Fig. 15 (b): "AND 1" gate performs AND function between the clock pulse and D, whereas "AND 2" performs AND function between clock and inverted D. The operation principle of D flip-flop is shown in Fig. 15 (c): when a clock pulse comes, if D=1 it can pass through "AND 1" but is blocked by "AND 2", so only "Set" port receives a pulse and the latch is set to "state 1" (Q=1); similarly if D=0 the clock pulse can

pass through "AND 2" but is blocked by "AND 1", only "Reset" receives a pulse and the latch is set to "state 0" (Q=0). The flip-flop is clocked because it only changes state when a clock pulse comes, according to the D values at that time, but ignores D at any other time.

D	Q_{next}	Comment
0	0	Reset
1	1	Set

(a)



(b) (c)

Fig. 15. Clocked D flip-flop: (a) characteristic table; (b) logic circuits; (c) working principle.

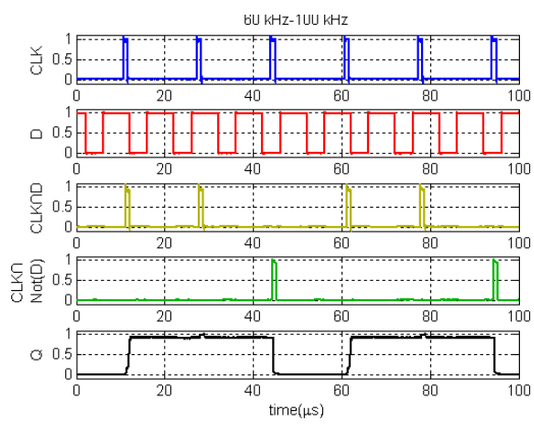


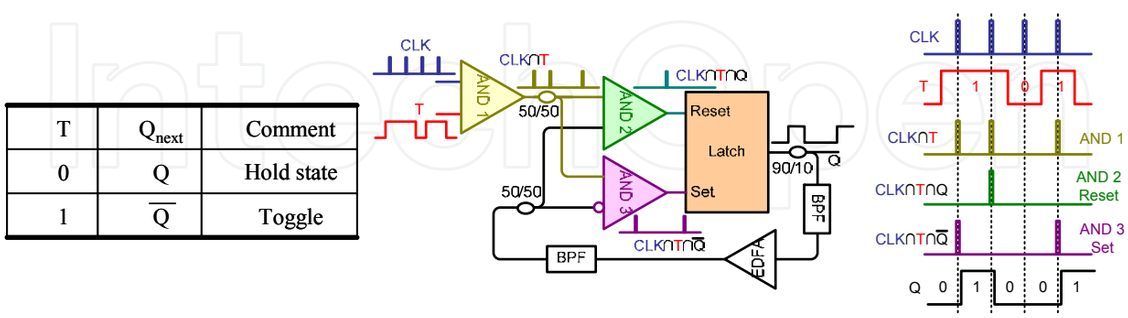
Fig. 16. Clocked D flip-flop operation.

In Fig. 16 clocked D type flip-flop operation is experimentally demonstrated. The clock pulse has a repetition rate of 60kHz with a pulsewidth of 1μs; whereas D has a repetition rate of 100kHz with a pulsewidth of 6μs. The wavelength of clock and D are λ_{CLK}=1554.1nm and λ_D=1552.5nm respectively, so the output of "AND 1" is at $\lambda_1=2\lambda_D-\lambda_{CLK}$=1550.9nm and the output of "AND 2" is at $\lambda_2=\lambda_{CLK}$=1554.1nm, the same with the clock pulse. The flip-flop only responses to the D values when clock pulses come, and therefore is clocked.

4.3 Clocked T flip-flop

The characteristic table of T flip-flop is shown in Fig. 17 (a). T represents the toggling signal. If T=0, the flip-flop maintains its previous state; if T=1, the flip-flop changes its state. The setup of clocked T flip-flop is shown in Fig. 17 (b). Different from SR and D flip-flops, in T flip-flop, the next state is not determined by external control signals, such as S, R, and D, but depends on the previous state, so feedback of output Q is used in T flip-flop to carry out the toggling operation. "AND 1" performs AND function between the clock pulse and T; whereas "AND 2" performs AND between the output of "AND 1" and the feedback output Q. "AND 3" carries out AND function between output of "AND 1" and inverted Q. The operation principle of T flip-flop is shown in Fig. 17 (c): when a clock pulse comes, if T=0 it is blocked by "AND 1", neither "Set" nor "Reset" receives pulse, and the latch remains at its previous state. If T=1, the clock pulse can pass through "AND 1"; then, if Q=1 it can pass

through "AND 2" but is blocked by "AND 3", so only "Reset" receives a pulse and the latch toggles to "state 0" (Q=0); if Q=0 the clock pulse can pass through "AND 3" but is blocked by "AND 2", only "Set" receives a pulse and the latch toggles to "state 1" (Q=1). In this way, the flip-flop is triggered by the clock pulse, changing its state if T=1, or maintaining its state if T=0.



T	Q_{next}	Comment
0	Q	Hold state
1	$\overline{Q}$	Toggle

(a) (b) (c)

Fig. 17. Clocked T flip-flop: (a) characteristic Table; (b) logic circuits; (c) working principle.

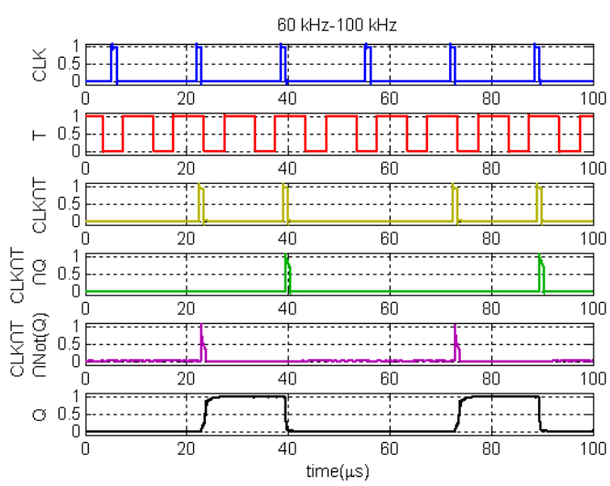


Fig. 18. Clocked T flip-flop operation.

In Fig. 18 clocked T flip-flop operation is experimentally demonstrated. The clock pulse has a repetition rate of 60kHz with a pulse-width of 1μs; whereas T has a repetition rate of 100kHz with a pulse-width of 6μs. The wavelength of clock pulse and T are λ_{CLK}=1554.1nm and λ_T=1552.5nm respectively, so the output of "AND 1" is at $\lambda_1=2\lambda_T-\lambda_{CLK}$=1550.9nm. The flip-flop output, Q, has a wavelength of λ_Q=1549.3nm, so the output of "AND 2" is at $\lambda_2=2\lambda_Q-\lambda_1$=1547.7nm and the output of "AND 3" is at $\lambda_3=\lambda_1$=1550.9nm, the same with the output of "AND 1". The flip-flop is clocked since the state toggling is only triggered when a clock pulse comes and T=1.

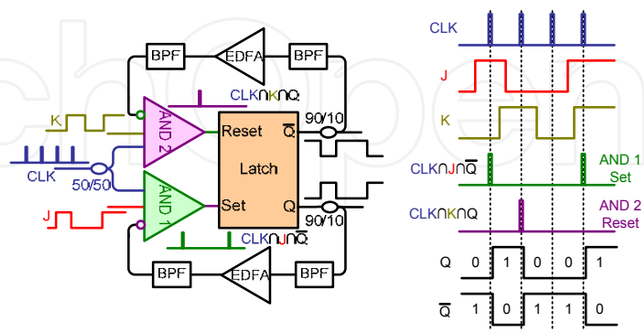
4.4 Clocked JK flip-flop

The characteristic table of JK flip-flop is shown in Fig. 19(a), which could be considered as a

combination of SR flip-flop and T flip-flop. Like SR flip-flop, J and K signals are also used as set and reset signals: J=K=0 makes the flip-flop maintain its previous state; J=1 K=0 sets it to "state 1"; and J=0 K=1 sets it "state 0". However, in SR flip-flop, S=R=1 is forbidden, but in JK flip-flop, J=K=1 is allowed and the flip-flop toggles its state in this condition, like a T flip-flop.

J	K	Q_{next}	Comment
0	0	Q	Hold state
1	0	1	Set
0	1	0	Reset
1	1	$\overline{Q}$	Toggle

(a)



(b) (c)

Fig. 19. Clocked JK flip-flop: (a) characteristic table; (b) logic circuits; (c) working principle.

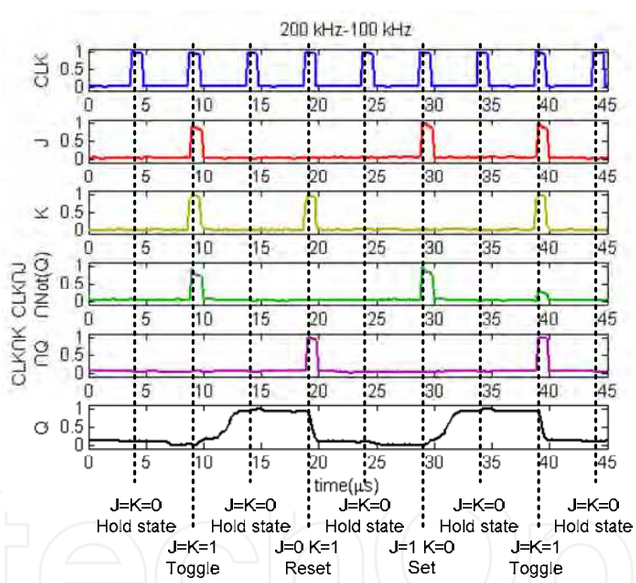


Fig. 20. Clocked JK flip-flop operation.

The setup of clocked JK flip-flop is shown in Fig. 19(b). The two complementary outputs of two ring lasers of SR latch are used as Q and inverted Q respectively. "AND 1" carries out AND function between the clock, J, and inverted Q; whereas "AND 2" carries out AND between the clock, K, and Q. Similar to SR flip-flop, the JK flip-flop can be set and reset by external signals, so CLK∩J and CLK∩K are partially carried out in two AND gates. However, the JK flip-flop can toggle its state like a T flip-flop, so the feedback of Q at previous state must also be taken into account in the two AND gates. When a clock pulse comes, if J=K=0 it can not pass through "AND 1" and "AND 2", so neither "Set" nor "Reset" receives a pulse, and the latch remains at its previous state. If J=1 K=0, the clock pulse is

blocked by "AND 2", but in "AND 1" there are two possible cases. If Q=1 the clock pulse is blocked, so "Set" receives no pulse and the latch will remain at "state 1"; otherwise if Q=0 the clock pulse can pass through "AND 1", and the latch will be set to "state 1". So in the case of J=1 K=0, the flip-flop will be set to "state 1" no matter in which state it was. Similarly, if J=0 K=1, the clock pulse is blocked by "AND 1". But for "AND 2", if Q=1 the clock pulse can pass through, so the latch will be set to "state 0", otherwise if Q=1 the clock pulse is blocked and the latch will stay in "state 0". So the flip-flop will be set to "state 0" no matter in which state it was. Finally, if J=K=1 we also have to consider two cases of Q. If Q=1, the clock pulse is blocked by "AND 1" but can pass through "AND 2", so the latch is set to "state 0"; otherwise, the clock pulse can pass through "AND 1" but is blocked by "AND 2", and the latch is set to "state 1". In both two cases, the flip-flop changes its state, which is called state toggling.

In Fig. 20 clocked JK flip-flop operation is experimentally demonstrated. The clock pulse has a repetition rate of 200kHz and a pulsewidth of 1μs. J and K both quasi-periodic pulse trains, with repetition rate of 100kHz and pulsewidth of 1μs, synchronized with the clock. However, in order to realize all four cases of J=K=0, J=1 K=0, J=0 K=1, and J=K=1, in every 4 periods (40μs) of J and K, there is one pulse missed, as shown in Fig.12. It could be observed that the JK flip-flop operation has a good agreement with Fig. 19(c). The wavelengths of clock, J, and K are λ_{CLK}=1554.1nm, λ_J=1552.5nm and λ_K=1550.5nm respectively, and the wavelength of Q is λ_Q=1549.3nm, so the output of "AND 1" is at $\lambda_1=2\lambda_J-\lambda_{CLK}$=1550.9nm and the output of "AND 2" is at $\lambda_2=2\lambda_K-\lambda_{CLK}$=1546.9nm.

4.5 Three-state flip-flop

Together with clocked flip-flops, another interesting evolution of the basic flip-flop shown in paragraph 3 is the upgrade to multi-state flip-flop. A multi-state memory could in fact extend a 1×2 optical switch to a larger dimension of 1×N, depending on the number of states of the memory.

The setup of the three-state optical memory is shown in Fig. 21 (Wang et al., 2008, a), which consists of three coupled SOA fiber ring lasers operating at three different wavelengths. The memory has three states. In "state 1", only ring 1 is lasing, whereas ring 2 and ring 3 are suppressed; the output light of SOA 1 is split by coupler A into two portions: one portion passes through Path 1 (the dashed red line) and then saturates SOA 3, making ring 3 suppressed; the other portion passes through Path 2 (the dashed green line) and then saturates SOA 2, making ring 2 suppressed. In "state 1", the optical memory emits a CW light at the wavelength of λ_1 from output 1 port. Similarly, in "state 2", only ring 2 is lasing, and the memory emits a CW light at λ_2. Finally in "state 3", only ring 3 is lasing.

To dynamically change the state, three setting couplers are inserted into the ring cavities, each corresponding to a particular state. One pulse injected into set 1 port is split to saturate SOA 3 and SOA 2, and it could not reach SOA 1. Thus ring 2 and ring 3 are both suppressed while ring 1 could lase; the memory is set to "state 1". Similarly for set 2 and set 3.

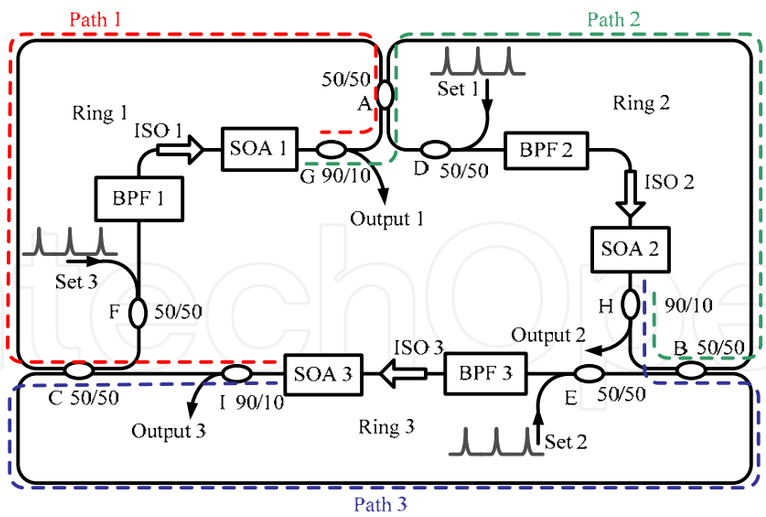


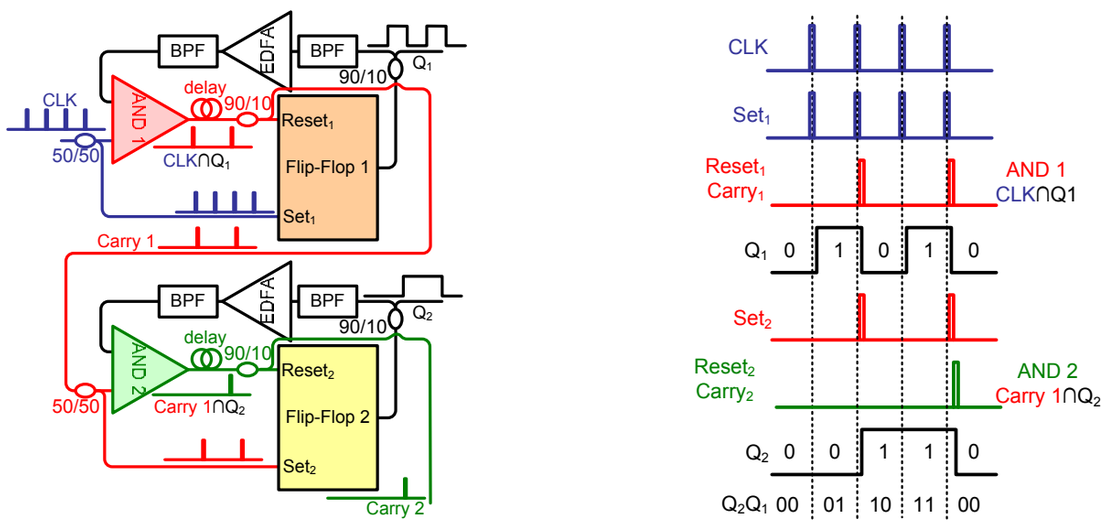
Fig. 21. Experimental setup of three-state all-optical memory

The experiments has shown an "on-off" extinction ratio of 40 dB for each state. The required switching energy is in the order of 12 to 19nJ, depending on the wavelength chosen for the set pulses. In the exploited set-up the ring length of the three cavities is about 42m, giving a rise time of about 210ns, while falling time can be as low as 20ps. Of course, photonic integration will reduce the rise time down to 40ps as well, making GHz switching possible.
By coupling N ring lasers, the scheme could be scaled up to N-state, in which output light of one SOA saturates N-1 other SOAs, requiring higher optical power for stable flip-flop operation. Moreover, N(N-1)/2 couplers would be used to couple N ring lasers together and the cavity length would also be increased. Photonic integration or hybrid integration would be useful to reduce both the cavity loss and the cavity length; and make high optical power and fast switching speed possible.

5. Latch-based all-optical counter

An extremely interesting and promising application of clocked flip-flops is the all-optical counter. As a key component in both areas of optical computing and communication, all-optical binary counter can be used as a finite-state machine in optical computing and can also be used for header recognizing and payload processing in optical packet switching networks. Nevertheless, there are few papers related to all-optical counter (Poustie et al., 2000; Benner et al., 1990; Feuerstein et al., 1991). In (Poustie et al., 2000) an all-optical binary counter based on terahertz optical asymmetric demultiplexer (TOAD) switching gate was demonstrated, which is however not integrable due to the nonlinear fiber loop mirrors in the TOADs. In (Benner et al., 1990; Feuerstein et al., 1991) a counter is presented but it requires optical-to-electrical conversion in the coupler switches. Furthermore, in these reported schemes, due to the lack of optical latch or other memory element, the storage of optical bit is realized by fiber loop memory, which requires precise synchronization of the arrival time of optical pulses and makes the counting speed fixed, depending on the fiber length in the loop memory.

Extending the setup of the above mentioned T flip-flop, we have demonstrated the first SR latch based all-optical binary counter (Wang et al., 2009,b), which is able to work at different counting speeds without the necessity of any reconfiguration or re-synchronization. The SR latch is used for optical bit storage, to memorize the accumulated number of input pulses and to carry out binary modulo-2 addition between the accumulated number and new input pulses. The AND logic gate is used for binary carry signal generation when the input and stored bit are both "1". We also presented two-bit binary counting operation as well as 1/2 and 1/4 all-optical frequency division at different frequencies, and Q-factor measurement is performed to evaluate the signal degradation and confirm the cascadability of the scheme. Finally, the operation speed limitation of clocked flip-flop and the counter is investigated.
The setup of optical counter is shown in Fig. 22 (a), which consists of two cascaded stages. Carry 1 signal from stage 1 is used as the input of stage 2. The latches' output, Q_2Q_1, represent the output of the counter.



(a) (b)

Fig. 22. All-optical binary counter: (a) logic circuits; (b) working principle.

The working principle of the counter is shown in Fig. 22 (b). At first, both latch 1 and latch 2 are in "state 0", Q_2Q_1=00. When the first clock pulse comes, it injects into "Set_1" directly, but since Q_1=0, it can not pass through "AND 1", so only "Set_1" receives a pulse and latch 1 is set to "state 1", Q_2Q_1=01. When the 2nd clock pulse comes, since Q_1=1 it can pass through "AND 1" and reach both "Set_1" and "$Reset_1$" ports. However, due to the fiber delay line, "$Reset_1$" receives the pulse later than "Set_1", so latch 1 is then set to "state 0". The output pulse of "AND 1" is used as "Carry 1" and is injected into stage 2. Since Q2=0, "Carry 1" pulse can not pass through "AND 2", so only "Set_2" receives the pulse and latch 2 is set to "state 1". Now we have Q_2Q_1=10. When the third pulse comes, it is blocked by "AND 1" since Q1=0, so latch 1 is set to "state 1", Q_2Q_1=11. Finally, when the 4th pulse comes, since Q_1=1 it can pass through "AND 1" and reach "$Reset_1$". Due to the fiber delay, "Reset1" receives a pulse later so latch 1 is set to "state 0". Then the output "Carry 1" pulse from "AND 1" injects into stage 2, passes through "AND 2" and sets latch 2 to "state 0". Now the counter returns to the initial state, Q_2Q_1=00, and the "Carry 2" pulse from "AND 2" can be used as the input of next stage. In each stage, the SR latch is used as a memory element to

carry out binary modulo-2 addition and store the current state of the counter; whereas the AND gate is used to generate carry pulse when a clock pulse injects into a stage that has already been in "state 1". Different from the schemes proposed in (Poustie et al., 2000; Benner et al., 1990; Feuerstein et al., 1991), whose bit storage is implemented by fiber loop memory and has a fixed counting speed determined by the fiber length, the counter shown in Fig. 22 utilizes SR latches to memorize its current state, and can work at different counting speeds without the necessity of any reconfiguration or re-synchronization.

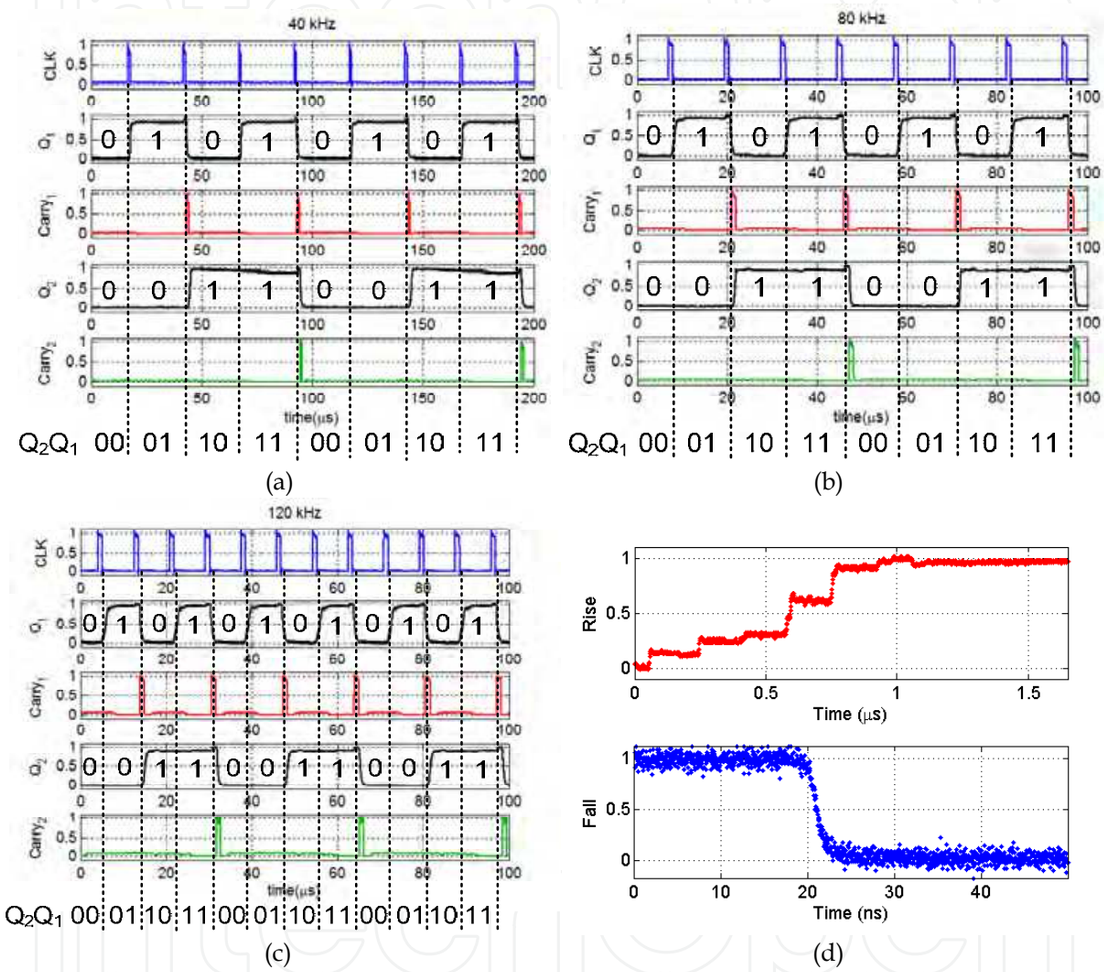


Fig. 23. All-optical two-bit binary counting at three different speeds: (a) 40 kHz; (b) 80 kHz; (c) 120 kHz. (d): transition time of SR latch

Referring to (Wang et al., 2009, b) for all the details of the experiment, Fig. 23 demonstrates that the counter can work at three different counting speeds, 40 kHz, 80 kHz, and 120 kHz without any reconfiguration. It is observed that each time a clock pulse comes, Q_2Q_1 adds 1, from 00 to 01, 10, 11, and finally returns to 00, and when Q_i (i=1,2) changes from 1 to 0 a carry pulse is generated, having a good agreement with Fig. 22 (b). Q_1 and "Carry 1" have a repetition rate 1/2 of the clock; whereas Q_2 and "Carry 2" have a repetition rate 1/4 of the clock. The counter can therefore be used as an all-optical frequency divider.

In principle, by cascading n counter stages it is possible to demonstrate n-bit binary counter which can count from 0 to 2^n-1. However, the cascadability of this scheme is limited by the signal degradation of carry pulses, which mainly comes from the accumulated ASE noise of SOA. To evaluate the signal degradation of carry pulses quantitatively, Q-factor measurement has been carried out. The Q-factors of Q_1 and Q_2 are 16.1 and 19.9 respectively, only determined by the properties of two latches. The Q-factor of "Carry 1" is 17.0, while exploiting an ASE pedestal suppression technique, we obtained "Carry 2" pulse with Q-factor of 15.0, only slightly lower than "Carry 1". These values confirm the good cascadability of this scheme.

In the experiment the operation speed is limited to hundreds of kHz. Since the AND gates are all based on nonlinear effects in the SOA, which have very fast dynamics, the operation speed limitation is mainly due to the switching-on of the SR latch, reported also in Fig. 23 (d). This time depends on the cavity length of fiber ring lasers, and in our setup each ring is about 40m due to the discrete fiber pigtailed implementation. Again, photonic integration is a feasible solution to reduce the cavity length to the range of millimeters, shortening the transition time to <100 ps, and making GHz operation speed possible.

6. Ultra-fast SOA-based all-optical flip-flop

An all-optical flip-flop based on two coupled ring lasers presents a fast falling edge (as fast as the input pulse rising edge), but a slow rising edge (several round-trip times), which mainly limits the flip-flop operating speed for optical packet switching. In this paragraph, using two SOA-based optical NOT logic gates and two identical slow flip-flops, we obtain an optical flip-flop with ultra-fast transition times for both rising and falling edges (Malacarne et al., 2008). The experimental setup is shown in Fig. 24, while the operating principle is described in Fig. 25. Flip-flop 1 is controlled by reset and assistant pulses whereas flip-flop 2 is controlled by assistant and set pulses. Exploiting a 10GHz pattern generator we produce a 16ps-edge pulsed sequence with a pulse-width of 1μs and a repetition rate of 50KHz. Such a wide pulse has been set in order to maintain the gain saturation level into the ring laser to be quenched for several round trip time, allowing to reach a lasing steady condition. The reset pulse is delayed by 10μs (T_{d1}) with respect to the set pulse whereas the assistant pulse is delayed by 15μs (T_{d1}+T_{d2}) with respect to the set pulse. As shown in Fig. 25, a set pulse is firstly injected into ring 3 switching off signal B. Secondly, a reset pulse is injected into ring 1 switching off signal A. Then two assistant pulses are injected into ring 2 and ring 4 simultaneously. They switch off ring 2 and ring 4, switching on ring 1 and ring 3 respectively. Consequently, signals A and B are switched on at the same time. As pointed out above, both signals A and B have a fast falling edge, but a slow rising edge. Exploiting the optical NOT logic gate 1, signal A is inverted in order to obtain signal C, which therefore presents a fast rising edge and a slow falling edge. Since signals A and B are switched on by two assistant pulses simultaneously, the slow falling edge of signal C is almost synchronized with the slow rising edge of signal B, and when they are added together, the slow edges compensate each other in terms of intensity profile. This way, signal D (the sum of signals B and C) has a fast rising edge due to signal C and a fast falling edge coming from signal B. The wavelengths of signals A, B and C are 1550nm, 1558.2nm and 1557.4nm respectively, thus signal D is made of two different wavelengths, as highlighted in Fig. 24, and a tunable filter with -3dB bandwidth of 4.5nm is used to filter and

equalize these two wavelength components. Using NOT logic gate 2, we invert signal D and thus obtain signal E, at the same time convert it to one single wavelength λ_E=1560nm. Signal E is switched on and off by the set and reset pulses respectively, showing fast rising and falling edges.

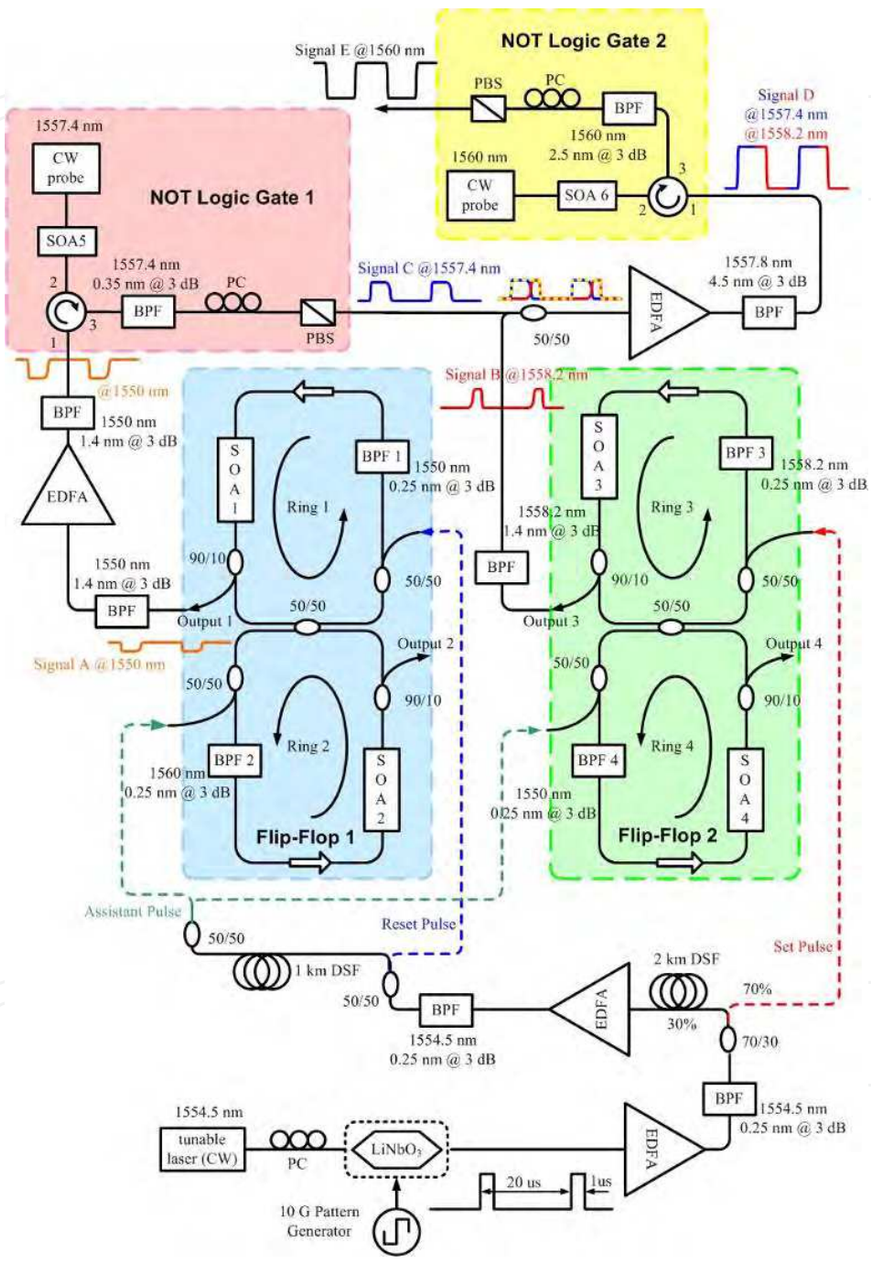


Fig. 24. Experimental setup of the ultra-fast all-optical flip-flop. PC: polarization state controller. Signal A is inverted by NOT logic gate 1 obtaining signal C and added with signal B. Signal D (B+C) is inverted by NOT logic gate 2 obtaining signal E.

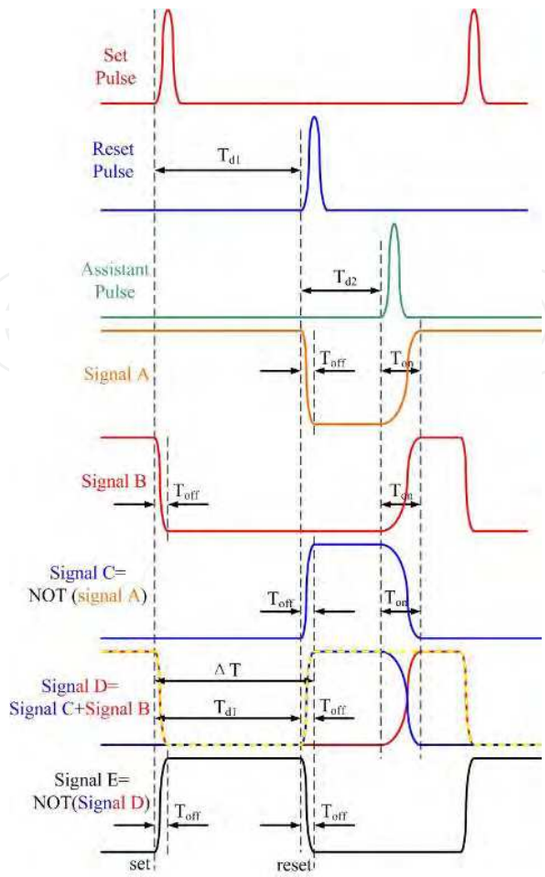


Fig. 25. Working principle of the ultra-fast all-optical flip-flop. Signal A, B, C, D and E. T_{d1}: delay between set and reset pulses; T_{d2}: delay between reset and assistant pulses; T_{on}: rising time; T_{off}: falling time; $\Delta T=T_{d1}+T_{off}$.

The optical NOT logic gates are implemented exploiting cross gain modulation (XGM) in SOAs. Concerning NOT logic gate 1, in SOA 5 a CW probe light counter-propagates with respect to signal A. The gain of SOA 5 is modulated by the intensity profile of signal A through XGM. In particular, when signal A has a low input power, the gain provided by SOA 5 for the CW probe will be high, whereas when signal A has a high power the CW probe will experience a lower gain. Ultimately the CW probe undergoes the gain variations obtaining the inversion of signal A, i.e. signal C.

Signals from A to E are shown in Fig. 26. Since the slow edges of signals B and C do not have a linear behavior, their sum gives rise to a residual peak during the high level of signal D. After NOT logic gate 2 this dynamic is suppressed because of the gain saturation level of SOA 6. CW probe power injected into SOA 6 has been set in order to optimize its saturation level (as CW probe injected into SOA 5). Exploiting input set and reset pulsewidths of 1μs with edge time of 16ps, signal E presents rising and falling times of 18.8ps and 21.9ps respectively, as shown in Fig. 26 (b) and (c) (measured with a total bandwidth of 53GHz), preserving a contrast ratio of 17.5dB. It is possible to obtain a higher contrast ratio just decreasing the CW probe signal powers in SOA 5 and SOA 6, reducing their gain saturation level, with the drawback of slower switching times (Berrettini, 2006, a). Moreover,

integrated coupled ring lasers would experience a round trip time in the ps range (instead of 100ns as in our experiment), allowing to use an injected pulsewidth in the ps range too.

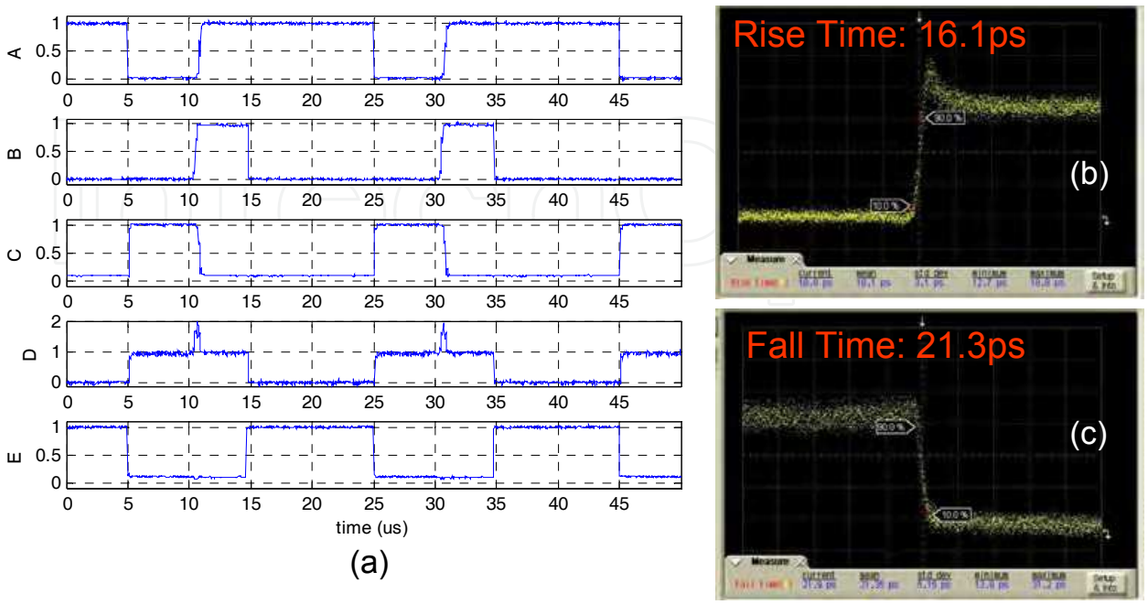


Fig. 26. (a): Signal A, B, C, D and E. Signal C = NOT (signal A); signal D=signal B + signal C; signal E = NOT (signal D). (b)-(c): Signal E rising (a) and falling (b) edges.

7. 10Gb/s switching operation with no bit loss exploiting the ultra-fast all-optical flip-flop

Fast dynamics (rising and falling times of 20ps) and high extinction ratio (17.5dB) make the ultra-fast all-optical flip-flop suitable to be exploited to control a 2×2 SOA-based all-optical switch (Berrettini, 2006, b).

The experimental setup is shown in Fig. 27. The switching operation is based on XGM effect in two different SOAs. Depending on the high or low intensity level of the control signal (pump), in one SOA the gain is strongly reduced while the other SOA is not saturated. The two input signals are generated by splitting a single 10Gb/s Non-Return-to-Zero (NRZ) continuous data stream. The stream is generated by modulating a CW laser at λ_{IN}=1550nm by means of a Mach Zehnder modulator driven by a 10Gb/s pattern generator running in (2^{31}-1)-long PRBS mode. At the same time the ultra-fast flip-flop output is used as pump signal of the optical switch and controls the switch state (BAR or CROSS). The inverted pump signal needed for switching operation is obtained within the optical switch block through signal inversion by means of XGM in an SOA. The data streams average power at the switch inputs are set to -7dBm, while the high pump level is 11.5dBm. We have chosen continuous data streams instead of packet traffic to demonstrate and point out that it is possible to obtain a switching operation without any bit loss, exploiting the 20ps-fast dynamics of the flip-flop. Indeed, as can be observed in Fig. 28, we can confirm a fast switching operation (faster than the 10Gb/s single bit edge), connecting only input 1

(disconnecting input 2) of the switch and visualizing output 1 on a sampling oscilloscope, switching the output data signal on and off within one bit time.

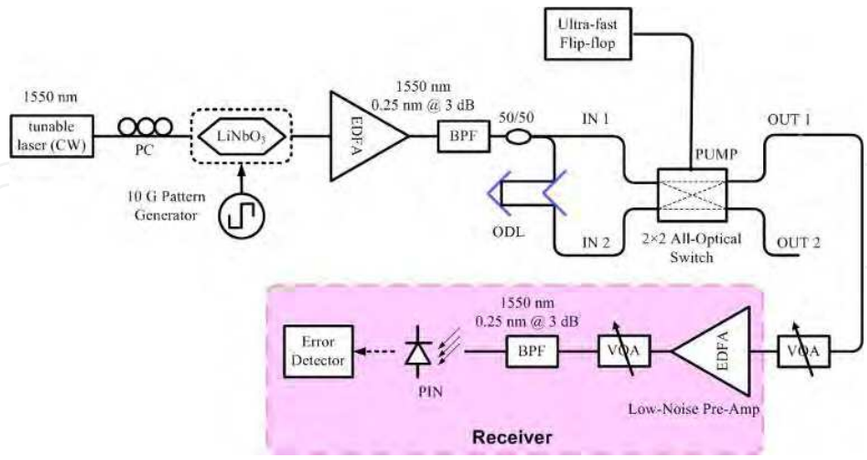


Fig. 27. All-optical switching operation experimental setup using a 2×2 SOA-based optical switch controlled by the ultra-fast all-optical flip-flop.

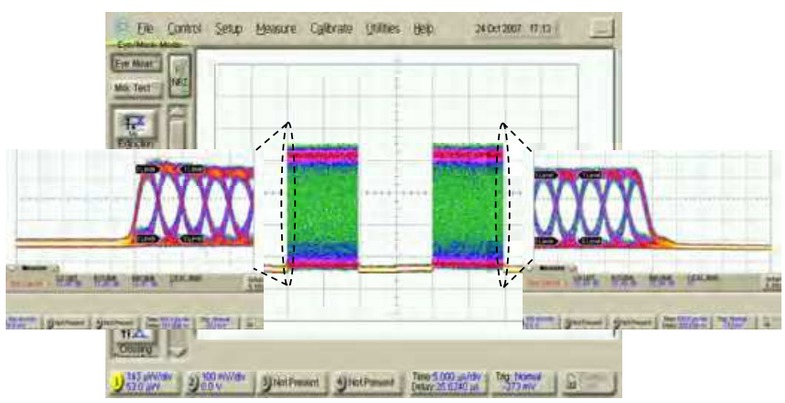


Fig. 28. Output 1 of the 2×2 all-optical switch, when just input 1 is connected (input 2 is disconnected). Insets shows the fast switching-on and switching-off transitions.

Contrast ratio between switched on and switched off signal is about 14dB. This way we avoid any distorted transition bit between switched on and switched off output signals, and vice-versa. Connecting both inputs 1 and 2 of the switch, high or low intensity level of the input pump signal sets the switch in BAR or CROSS state. During BAR state, input 1 of the switch is routed to output 1 (and input 2 is routed to output 2), while during CROSS state input 2 is routed to output 1 (and input 1 is routed to output 2). Fig. 29 (left) shows both input data eye-diagrams and output 1 eye-diagrams in BAR and CROSS configurations, measured by a wide-band photodiode and a sampling oscilloscope. As it can be noticed, the output signal is not affected by pattern effects, showing clearly open eye-diagrams, confirming the effectiveness of the scheme.

Right: (right) shows the BER measurements at output 1 of the switch, in both BAR and CROSS configurations. The used receiver is composed by an optical pre-amplifier with 5dB

noise figure, followed by a VOA, a BPF and a photo-receiver, whose input power is kept constant (by means of the VOA) at -16.7dBm in order to avoid thermal noise. As shown in Right:, making a comparison with the back-to-back case, the maximum penalty at BER=10^{-9} is about 1dB, making the switch driven by the ultra-fast all-optical flip-flop suitable for cascaded schemes.

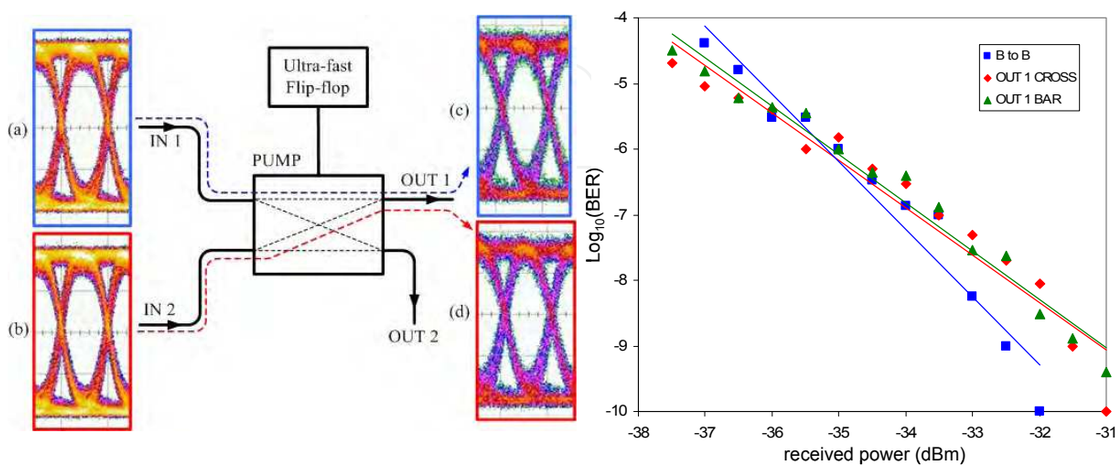


Fig. 29. Left: eye-diagrams of inputs 1 and 2 data frames (a)-(b) and output 1 in BAR (c) and CROSS (d) configurations of the 2×2 all-optical switch. Right: BER curves in the back-to-back (B to B) case and at switch output 1 in BAR and CROSS configurations.

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