# We are IntechOpen,
# the world's leading publisher of
# Open Access books
# Built by scientists, for scientists

## 6,900
Open access books available

## 186,000
International authors and editors

## 200M
Downloads

Our authors are among the

## 154
Countries delivered to

## TOP 1%
most cited scientists

## 12.2%
Contributors from top 500 universities

CLARIVATE ANALYTICS
**BOOK CITATION INDEX**
INDEXED

**WEB OF SCIENCE**™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

# Interested in publishing with us?
# Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

# Multi-Block CMOS LNA Design for UWBWLAN Transform-Domain Receiver Loss of Orthogonality

Mohamed Zebdi, Daniel Massicotte
*Université du Québec à Trois-Rivières*
*(Québec) CANADA*

Christian Jesus B. Fayomi
*Université du Québec à Montréal*
*(Québec) CANADA*

## 1. Introduction

Transform-domain ultra-wideband (UWB) receiver (Hoyos & Sadler, 2006), is a new UWB receiver implementation method, considering a novel approach that utilizes, analog basis expansion of the input signal, followed by parallel sampling of the basis coefficients (Hoyos & Sadler, 2004), to face significant implementation challenges, including achieving sufficient front-end dynamic range, to support desired receiver processing gain, and rejection of large narrowband interferers (NBI), and overcoming channel-induced distortion.

This method enables parallel digital signal processing, and leads to considerable complexity reduction, while still achieve a performance very close to Nyquist rate digital receivers, even when operating at a Sub-Nyquist sampling rate, without significant BER penalty, if the truncation error is negligible compared with the additive noise, or if the incurred SNR degradation can be mitigated by the channel decoder (Hoyos & Sadler, 2006). Since the receiver has $N$ parallel paths, the sampling rate for each path will be $N$ times lower than if, a Nyquist rate time-domain ADC were used to sample the input signal.

If the front-end frequency selectivity of a conventional receiver does not provide the required attenuation of the adjacent frequencies, the remaining unknown and undesired adjacent channel interference, will fold into the signal band. Thus, by using the orthogonality principle in the frequency domain, the transform-domain receiver can select signals with great accuracy, even if strong interferers are nearby.

Unfortunately, there are practical limitations to this solution due, to the limited number of frequency samples that can be taken, because of the complexity in the parallel bank of mixers and integrators needed. This limitation requires us to perform frequency sampling over short time windows, which in turn produces bandwidth expansion due, to convolution in the frequency domain. This frequency expansion implies overlapping (aliasing) in the frequency domain, i.e., loss of orthogonality.

The loss of orthogonality causes the adjacent, as well as in-band, interferers to overlap with the signal of interest producing destructive aliasing. A structure of multipath transform-domain receiver was proposed in (Prakasam et al., 2008). However, this chapter aims at proposing a selective, time-domain UWB, Wireless Local Area Network (WLAN) front-end, employing a direct-sequence architecture (Razavi, 1997), and introducing a multi-block designed Low-Noise Amplifier (LNA), in order to minimise the loss of orthogonality effect in the transform-domain receiver, due to short windowing in parallel sampling of the basis coefficients, during the analog basis expansion of the input signal, while ensuring a better trade-off between, selectivity, linearity, noise figure, and power consumption.

The first topic of this chapter describes the transform-domain receiver architecture, where the analog basis expansion principal of the input signal is briefly introduced. Then, the next topic presents the circuit techniques, including the circuit design and simulations results of the front-end receiver, while the last topic draws the conclusions.

## 2. Transform-Domain Receiver

The transform-domain receiver architecture (Fig. 1), shows the transmitted bit $a_i$ estimation process, from the set of the coefficient $\Phi_n(t)$, provided by the quantized basis coefficients . An estimate of $a$ , namely $\hat{a}$ is obtained via the linear receiver matrix $H$ as:

$$\hat{a} = H \bullet r \qquad (1)$$

In the case of an transform-domain receiver, the linear formulation in (1) includes the Inter-Symbol Interference (ISI) between the received pulses of $\tilde{r}(t)$, so solving the linear filtering problem presented in (1) will perform both signal detection and equalization (Hoyos & Sadler, 2006). Thus, the transform-domain receiver parallelization can be exploited to add robustness to adjacent channel interference, witch would be greatly helpful for the WLAN receivers, occupying the 5-6GHZ frequency band (group #2), in the case of the UWB system standard (Federal Communications Commission, 2002), where the neighboring nodes may be very closes, contrasting with the expensive signal detection and equalization with conventional architectures (Blazquez et al., 2005), (Chen & Chiueh, 2006).

The fundamental difference between the transform-domain receiver front-end and the conventional single ADC architectures is the way sampling of the received signal is performed. Folding of the signal spectrum introduced by the time-domain sampling produces the classical frequency aliasing effect. The adjacent channel interference will fold into the signal band, and may seriously distort the discrete-time representation of the signal, if the front-end frequency selectivity of a conventional receiver does not provide the required attenuation.

Unfortunately, even when we use the orthogonality principal in the frequency domain, witch can select signals with great accuracy, even when strong interferers are nearby, the number of the frequency samples that can be taken is limited, because of the complexity in the parallel bank of mixers and integrators needed (Fig. 1). Thus, loss of orthogonality can be caused by the frequency expansion induced by the convolution in frequency domain, when performing a frequency-domain sampling over short time windows.
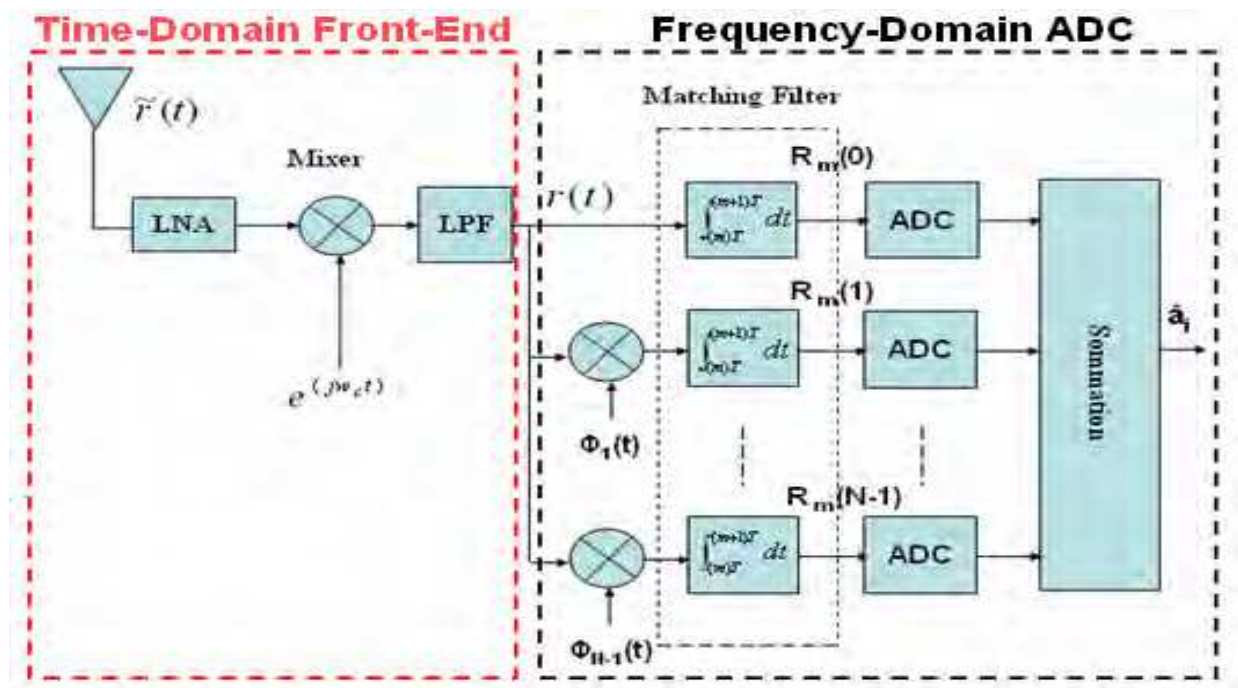
Fig. 1. Mixed-Signal Transform-Domain Receiver Architecture.

Attenuation of the adjacent channel at the front-end of the receiver is critical to avoid catastrophic aliasing after frequency-domain sampling. The aim of this work is to provide a great selective time-domain front-end reception part, for the transform-domain UWB WLAN receiver, in order to minimize the overlapping (aliasing) in the frequency domain caused by the short time windowing limitation.

## 3. Design Techniques

### 3.1 Dynamic Feedback LNA

Several proposals were introduced lately for the design of low-power, UWB CMOS LNA (Park, et al., 2005), (Yu et al., 2006), (Shameli & Heydari, 2006), (Yo & Yoo, 2007). Due particularly to its low input impedance, the common-gate input LNA exhibits an excellent linearity, selectivity, and impedance matching over the common-base LNAs (Cusmai & Brandolini, 2006). This makes it the best candidate to integrate into transform-domain receivers, wherein the selectivity compared to the adjacent UWB groups, would be of a major importance.

Unfortunately, the limited small signal gain and relatively high noise figure (NF) values, constitute serious handicaps for their use. Figure 2 depicts the structure of the proposed, multi-block designed LNA, introducing the dynamic feedback architecture. For linearity purpose, the voltage-voltage feedback is the better way to take advantage of the common-gate LNA.
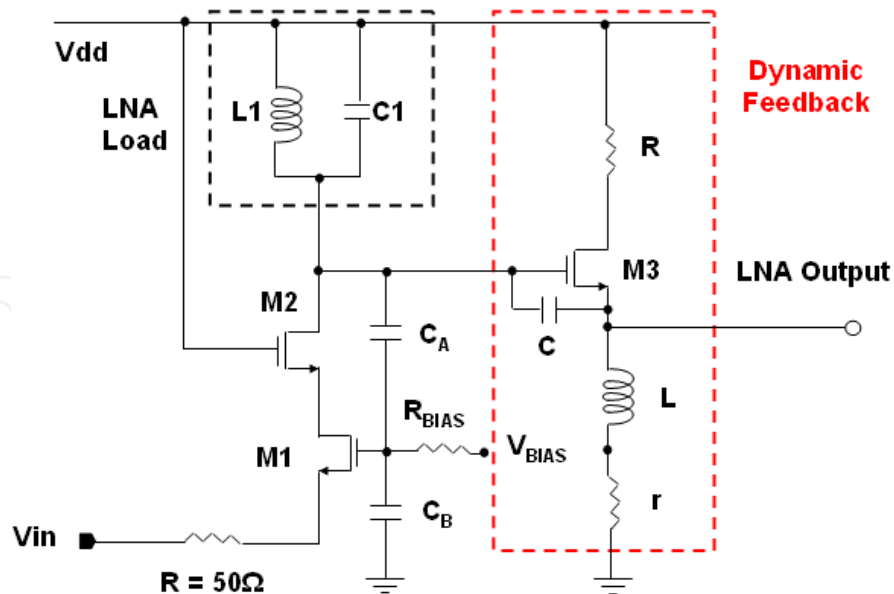
Fig. 2. Dynamic Feedback LNA.

One interesting property of the circuit is its input impedance depends on the loop transfer function. The idea is then synthesizing a single resonance load network, able to simultaneously shape the frequency transfer function, and the input impedance. By inspection of the circuit, and since the marginal wideband gain contribution of the source follower, the input impedance $Z_{in}(j\omega)$ and the frequency transfer function $T(j\omega)$ are given by :

$$Z_{in}(j\omega) = 1/g_m + \alpha.Z_{Load}(j\omega) \tag{2}$$

$$T(j\omega) = \frac{Z_{Load}(j\omega)}{Z_{in}(j\omega)} \tag{3}$$

Where $g_m = g_{m1} // g_{m2}$, is the equivalent transconductance gain introduced by the transistor $M_1$ and $M_2$, $\alpha$ the feedback factor, and $Z_{Load}$ the load impedance. From (2), the input impedance has the same frequency dependence as the load impedance. $\alpha$ is chosen so that $(1/g_m) + \alpha.R_p = R_s$, where $R_p$ is the load resistance at the resonance. Thus, the LNA is easily matched to the source resistance $R_s$ at frequency band of interest.

Furthermore, if the load impedance intentionally presents also a series resonance for filtering purposes, the amplifier input impedance is unmatched at resonance frequency. The resulting power reflection is beneficial, contributing to reduce the signal processed at the interferer frequency. The amplifier load impedance $Z_{Load}$ can be designed to filter out 3–5GHz and 6-10GHz interferers, while amplifying 5–6-GHz WLAN UWB signals and the input impedance is matched to the source in UWB WLAN band only.

On the other hand, the dynamic feedback LNA achieves a significant conversion gain improvement, mainly due initially, to the composed open loop dynamic feedback LNA structure, as depicted in the figure 3, where the $C_2$ represent the equivalent capacitor

between the input and the output of the circuit, and secondly to the inductive load of the feedback circuit, which as will be detailed later on, increases the gain by reducing the LNA to a simple second order circuit with zero at the origin, for certain inductance L values. The small signal gain is then, maximized within the frequency band between the two poles.
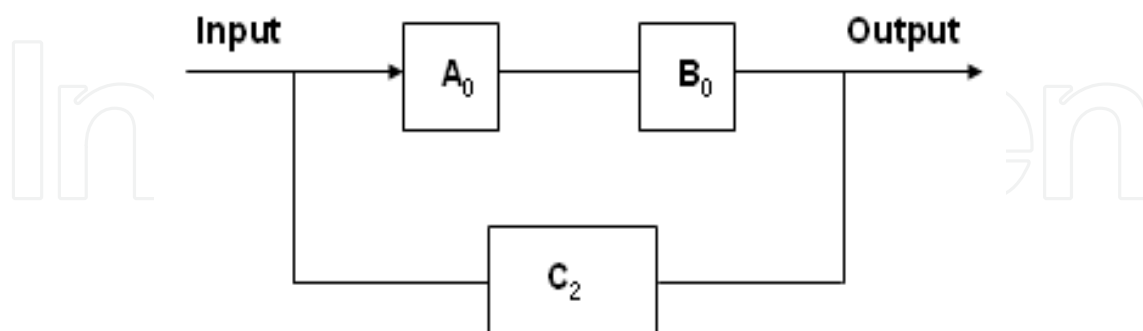


Fig. 3. The Dynamic Feedback LNA Block Diagram.

In the case of the UWB WLAN communication systems, we can maximise the small signal gain by replacing them within the 5-6GHz frequency range. The $M_1$ transistor is biased with 3.8mA, and the load circuit ($L_1C_1$) initially centers the small signal gain at 5GHz, the UWB WLAN lower limit. $C_A$ symbolise the $M_1$-$M_3$ gate-to-gate capacitance (~200fF), where $C_B$ capacitor still in the order of 700fF. The two poles introduced by the dynamic feedback are mainly dependent on the high frequency capacitors of the transistor $M_3$ (Razavi, 2001). Equations (4), (5) and (6) show the source follower high frequency transfer function (Razavi, 2006).

$$\frac{V_{out}}{V_{in}} = \frac{1 + \dfrac{C_{GS3}S}{g_{m3}}}{(aS^2 + bS + 1)} \tag{4}$$

where:

$$\begin{cases} a = \dfrac{R_{s3}}{g_{m3}}(C_{GD3}.C_{GS3} + C_{GD3}.C_{SB3} + C_{GS3}.C_{SB3}) \\ b = R_{s3}C_{GD3} + \dfrac{C_{GD3} + C_{SB3}}{g_{m3}} \end{cases} \tag{5}$$

These equations show that, by introducing two additional poles, a UWB LNA with dynamic feedback is likely to suffer from a chronic instability over all UWB frequency band. In our case, the small signal model of the proposed dynamic feedback circuit is shown in figure 4. Thus, the feedback circuit transfer function can be described as:

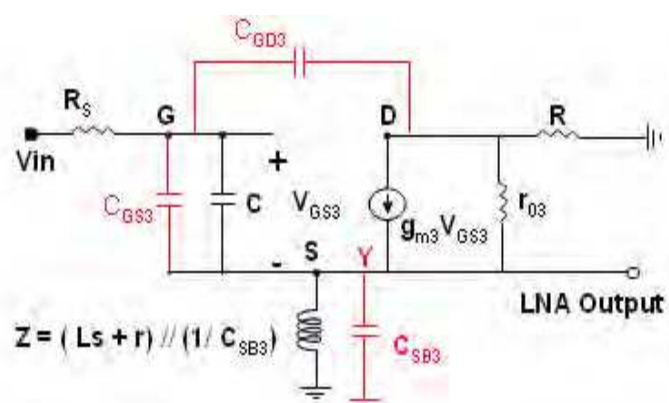$$\frac{V_{out}}{V_{in}}(s) = \frac{r_{03}.Z.(C_2 s + g_{m3})}{[a+b]} \tag{6}$$

Fig. 4. The Dynamic Feedback Small Signal Model.

$$\text{With}: \begin{cases} a = \{R_s(C_2 + C_{GD3})s + 1\}.(Z + R + r_{03}) \\ b = r_{03}.Z.(C_2 s + g_{m3}).(Z + RR_s C_{GD3} s) \end{cases} \tag{7}$$

$$\text{And}: \begin{cases} C_2 = C + C_{GS3} \\ Z = (Ls + r)//(\dfrac{1}{C_{SB3}}) \end{cases} \tag{8}$$

Accordingly, both the impedance $Z$, and the coupling capacitor C are introduced for the LNA gain conversion optimization. On the other part, the dynamic feedback based on a source follower circuit, with an inductive output, allows an inductive behaviour of the feedback circuit input impedance (Fig. 5) witch helps improving the small signal gain too, with more idealized voltage-voltage amplifier circuit (Razavi, 2001). Consequently, the dynamic feedback circuit can also make it possible, to minimize the NF, induced by the purely capacitive feedback circuit proposed by (Cusmai & Brandolini, 2006).
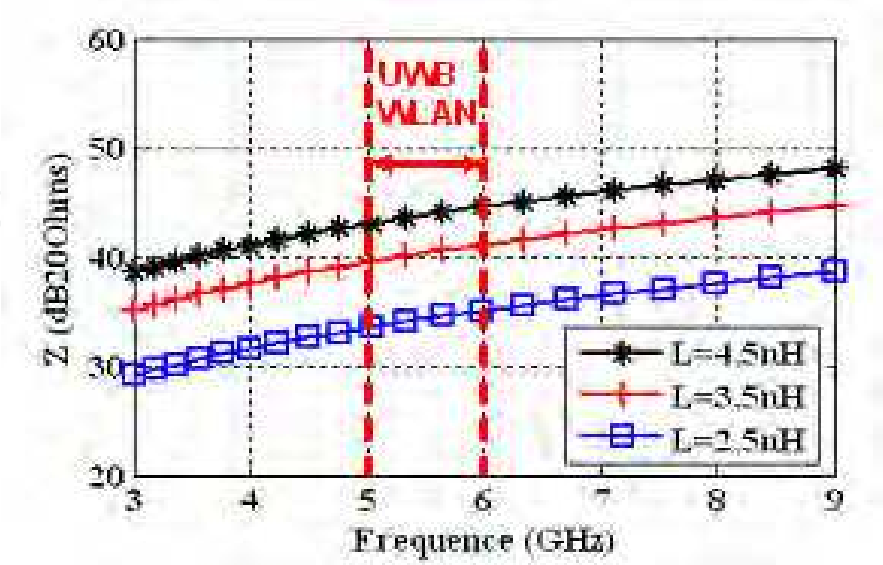


Fig. 5. The Dynamic Feedback Input Impedance.

It's important to note here the marginal dynamic feedback open loop contribution, for the UWB WLAN LNA, in terms of small signal gain (Fig. 6), and NF (Fig. 7), especially at the frequency band of interest. Thus, the small signal gain improvement can be achieved without power noise amplification, witch help improving the NF as needed. The frequency response simulation results suggest that, for a specific inductive load range values L, the closed loop feedback circuit contribution is effectively reduced to a simple zero at the origin (Fig. 8), witch ensures a perfect stability for the LNA circuit, over the entire UWB frequency band. However, for other inductance L range values, the UWB WLAN LNA could become deeply instable, with four poles occupying a larger frequency range (ex. L=1.5nH). The conversion gain can thus be maximized, by introducing an optimum inductance L, and capacitor C values (L=4.5nH, C=0.4pF), until reaching 27dB at 5.65 GHz (Fig. 9), (Fig. 10).
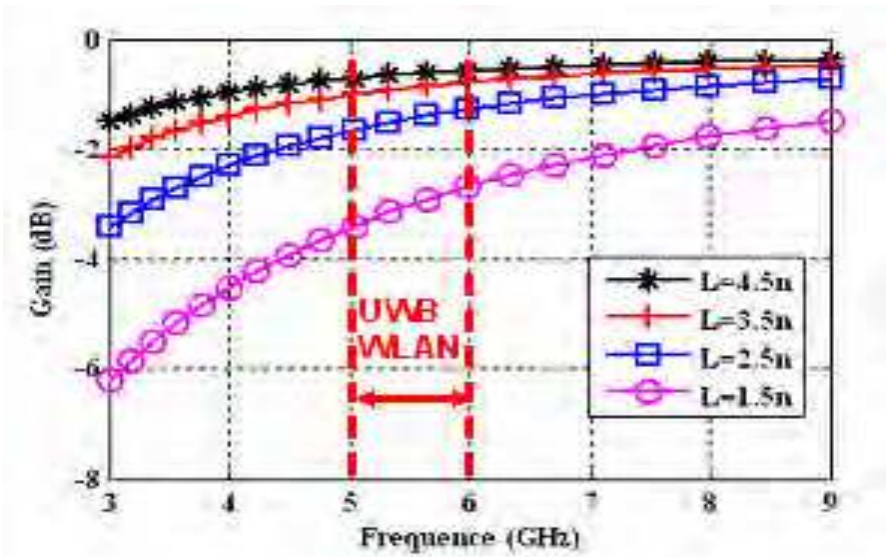


Fig. 6. The Dynamic Feedback Open Loop Gain Contribution.
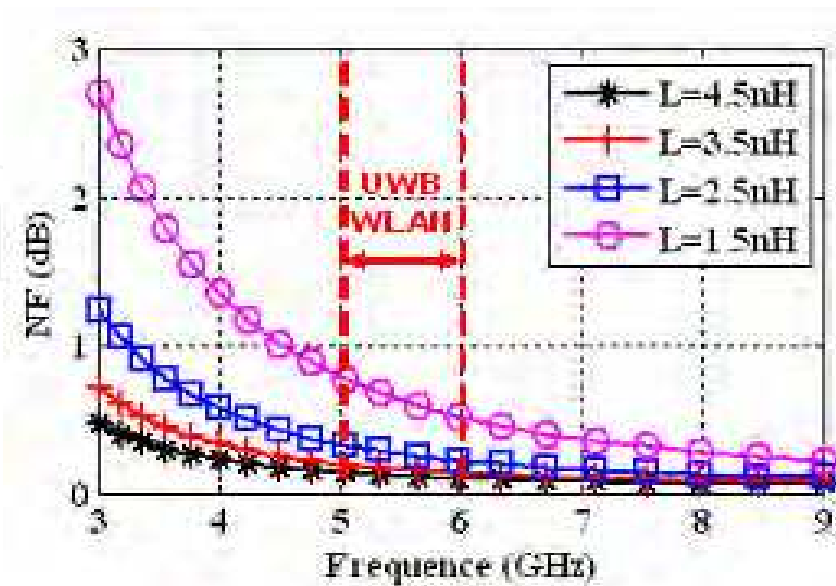


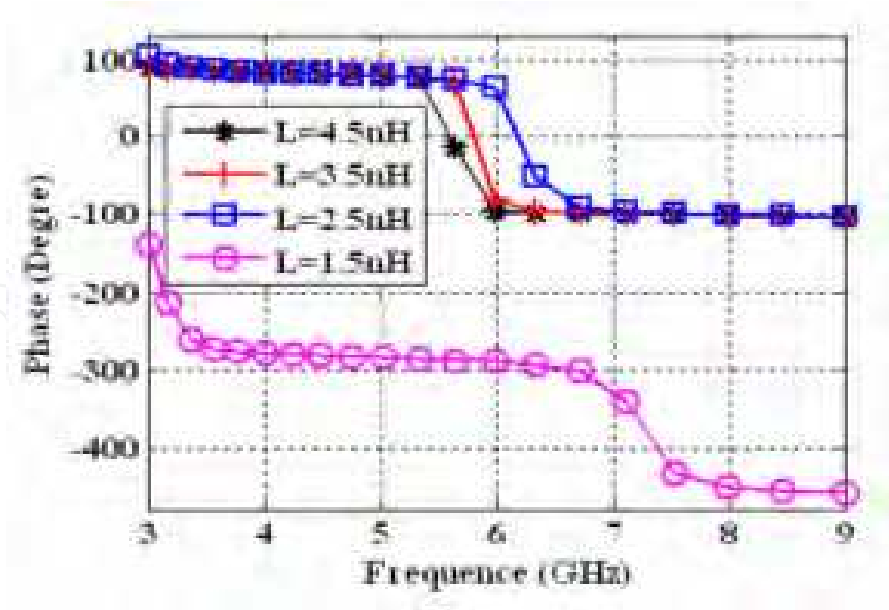Fig. 7. The Dynamic Feedback Open Loop Noise Figure Contribution.
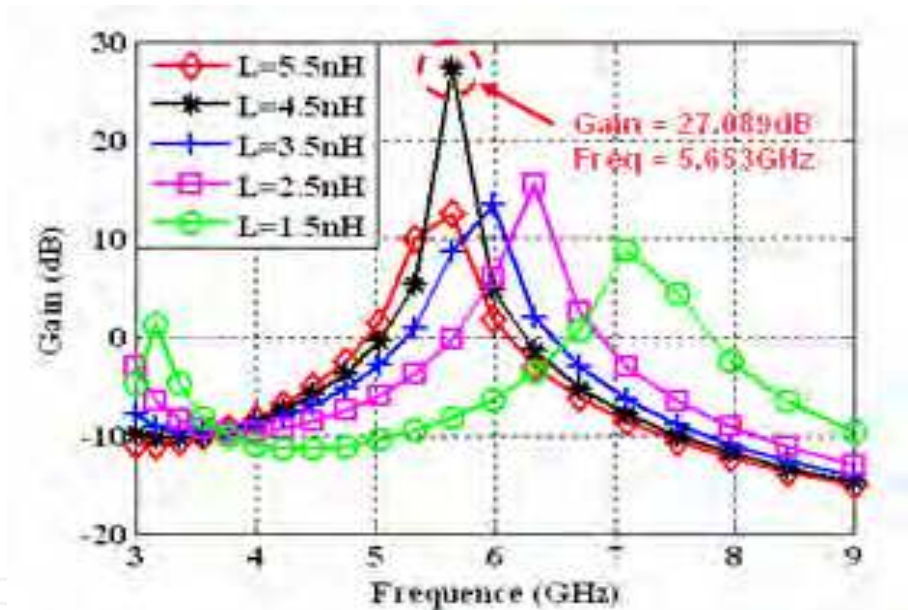
Fig. 8. Dynamic Feedback LNA Phase Simulations.



Fig. 9. Dynamic Feedback LNA Conversion Gain with (C = 0.4pF).

Regarding the noise figure issue, and according to the Friis equation for cascaded stages, the overall noise figure is mainly determined by the first amplification stage, provided that it has sufficient gain. You achieve low noise performance by carefully selecting the low noise transistor, DC biasing point, and noise-matching at the input, and the noise performance is characterized by NF value, defined as the ratio between the input signal-to-noise ratio and the output signal-to-noise ratio (9).
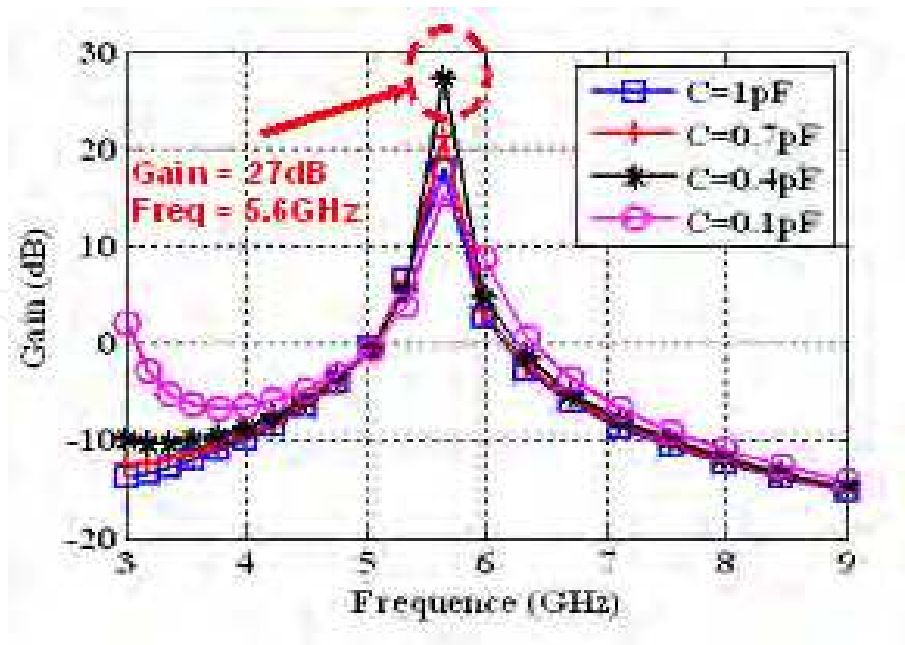
Fig. 10. Dynamic Feedback LNA Gain Conversion Optimization.

$$NF = \frac{\left(\dfrac{S}{N}\right)_{Out}}{\left(\dfrac{S}{N}\right)_{In}} = \frac{N_{Out}}{G_A . N_{In}} \tag{9}$$

Thus, one other advantage when considering the multi-block LNA design methodology, as depicted in (Fig. 2), is the fact that the trade-off between the conversion gain and the noise figure is no longer needed, since, as detailed earlier, the conversion gain could be optimised by properly shaping the over all LNA circuit transfer function. Consequently, the multi-block design LNA circuit noise figure, can be lowered by means of proper input stage circuit, and feedback circuit biasing, considering only the power consumption limitations. Concretely, by introducing a dynamic feedback, with a distinct biasing for the input stage circuit, we actually de-correlate between the available noise power from the source ($N_{in}$), and the available noise power to the load ($N_{out}$), and hence, one can be able to reduce the global NF value. Effectively, the figure 11 shows that, the dynamic feedback LNA noise figure values, vary now from 3.86dB down to 2.78dB in the 5-6GHz frequency range, when considering the inductance optimum value (L=4.5nH), depicted in black curve. As expected, this presents a 0.78 dB average gain with respect to the 4.1dB LNA minimum noise figure, developed by the common-gate made device in (Cusmai & Brandolini, 2006), even when biased at 5mA. However, the dynamic feedback LNA input stage where biased at 3.8mA, with marginal power consumption for its ultra low-power feedback circuit.

In terms of linearity, compared to the LNA circuit proposed by (Cusmai & Brandolini, 2006), the dynamic feedback significant narrow-band conversion gain improvement, was produced at the cost of slight linearity reduction, with a 1dB compression and desensitizing point falling at +1,-2 dBm respectively (Fig. 12), as depicted in (Tab. 1), witch reports the proposed LNA related performances, in comparison with a various recently published UWB

LNAs, including common-source degenerated devices. We also note that, the common-source input stage LNA (Park, et al., 2005), show a poor linearity performance, even with an ultra low-power made devices (Shameli & Heydari, 2006), suggesting that the trade-off between, conversion gain, noise figure, linearity, and power consumption could be relaxed, only when considering a multi-block design methodology, with distinct biasing circuits.
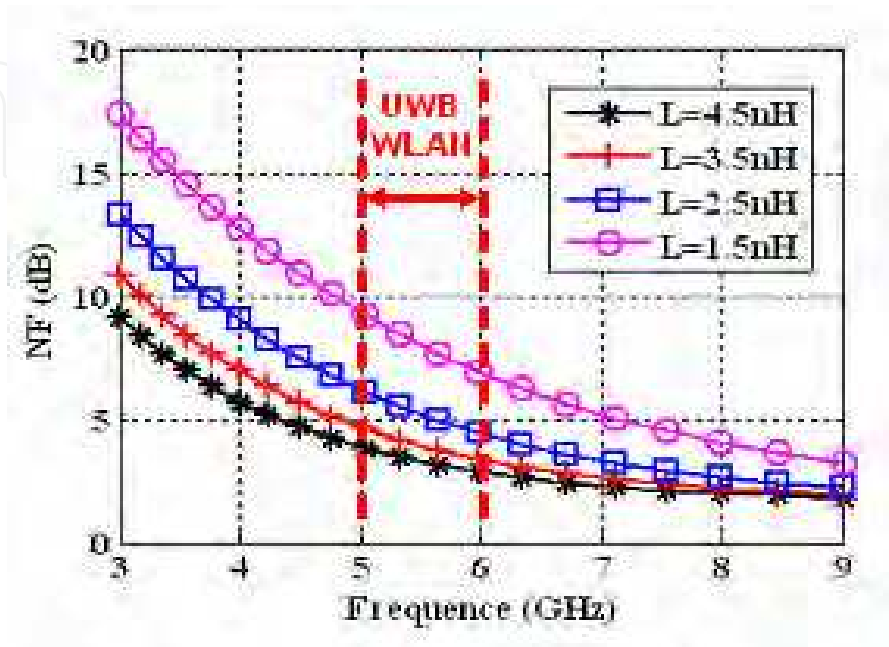

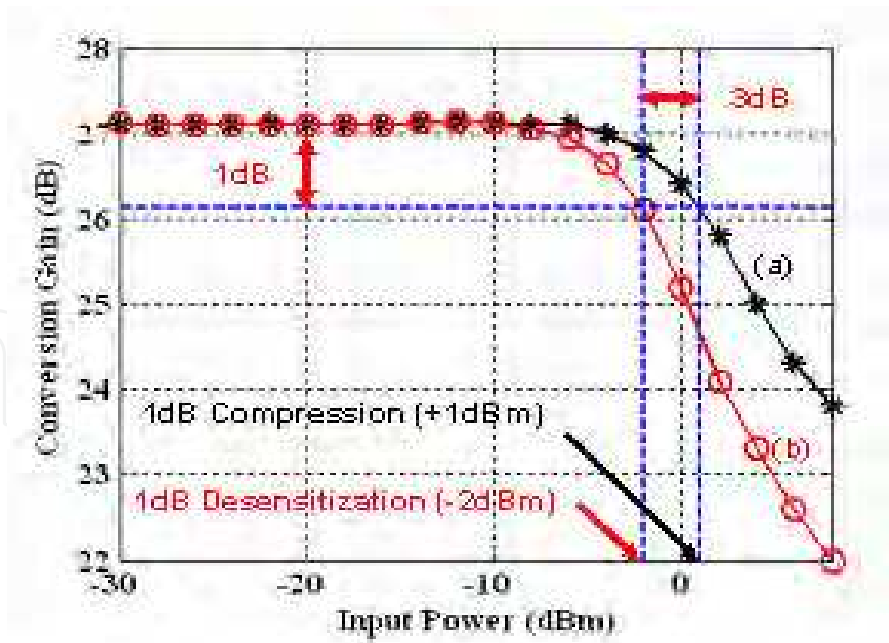
Fig. 11. Dynamic Feedback LNA Noise Figure.



Fig. 12. Dynamic Feedback LNA Linearity Simulations. (a) Gain versus Signal Power. (b) Small Signal Gain versus the Closest Interferer Signal Power (7GHz, Group#3 Signal Power).

|  | Tech. | CG [dB] | NF [dB] | 1dB C.P. [dBm] | 1dB Desensitization [dBm] | Power [mW] |
|---|---|---|---|---|---|---|
| (Cusmai & Brandolini, 2006) | 0.18 $\mu m$ CMOS | 16 | 4.1 | +1.5 | -1.5 | 9 |
| (Park, et al., 2005) | 0.18 $\mu m$ SiGe | 13 | 3.3 | -17 | - | 9.6 |
| (Shameli & Heydari, 2006) | 0.18 $\mu m$ CMOS | 16.8 | 3.9 | -21 | - | 0.1 |
| LNA Fig. 2. | 0.18 $\mu m$ CMOS | 27 | 3.3 | +1 | -2 | 7 |

Table 1. Comparison With Previously Published UWB LNA.

## 3.2 Downconversion Mixer

The choice of a single-balanced mixer instead of its double-balanced alternative is due to the converter would be required after the LNA witch increase the power, and the higher noise introduced by the double-balanced solution.
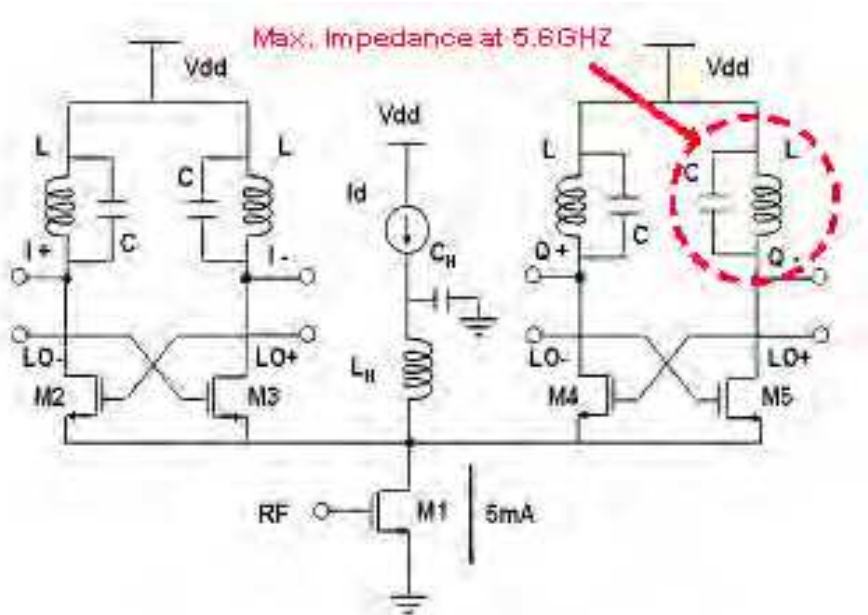


Fig. 13. Quadrature Mixer Schematic.

The mixer schematic is shown in (Fig. 13). A single common-source $g_m$-transistor ($M_1$) injects the RF signal in two single-balanced quadrature commutating pairs. When compared to the conventional solution adopting two separate transconductors, this choice allows a higher switching pair current gain (Sjoland & Karimi-Sanjaani, 2003).

A current source is used to set transconductor and switching stage current independently, in order to lower to DC current in the switching stage, witch leads to a lower noise (Darabi & Abidi, 2003). The inductor $L_H$ extend the commutation bandwidth with benefits to conversion gain, noise and linearity (Razavi, 2007). The bias current of the $g_m$-transistor ($M_1$)

should be higher enough (~5mA) to achieve the desired conversion gain, noise figure and IIP3. The Vgs of the LO switches is set near the $V_t$ to achieve a low bias current, and at the same time ensure that the required LO amplitude remains at a reasonable level (300mVpp) for complete current commutation. The LC circuit present a high impedance at 5.6GHz, such that the output AC current of ($M_1$) will flow into the LO switches. The quadrature mixer achieves 5.8dB CG, 8.8 dB and +1.68 dBm IIP3 at 5.6GHz (Fig. 14).

The DC offset in mixers is a critical parameter for direct conversion receivers, since most of the gain occurs after the downconversion of the input signal and the receiver can be saturated if the offset is too large, but the direct-conversion architecture lends itself to UWB receivers, because static and time varying DC offsets can be easily removed in the adopted OFDM modulation where the subcarrier falling at DC is not used (Batra et al., 2004), and because of the wide bandwidth makes the (1/f) noise less critical.
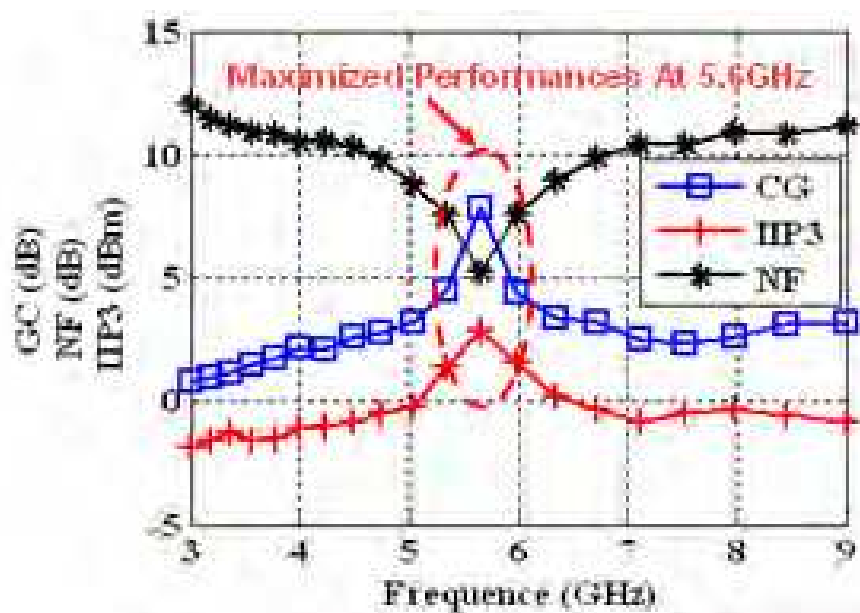


Fig. 14. Quadrature Mixer Frequency Response of CG, NF and IIP3.

### 3.3. Baseband Filter
An SK filter (Razavi, 2006) is designed in conjunction with the above mixer. The core amplifier is a simple low-gain circuit to obtain flat-band behaviour across 300MHz. Consequently, the voltage swings reduction removes the compression bottleneck at the mixer output; however, the loop gain does not force a virtual ground at these nodes. The baseband filter is therefore designed with a 2dB limited loop gain, this is mainly due to the substantial narrow-band conversion gain produced by the downconversion mixer at the 5-6Ghz frequency band, therefore, the later is likely to experience a compression at it's output. Finaly, table 2 reports the proposed selective, time-domain front-end performances, in comparison with the selective UWB front-end presented in (Cusmai & Brandolini, 2006). One can note that, the high interferer rejection developed by the multi-block LNA design methodology; very useful to overcome the UWB transform-domain receiver problem, has been achieved with an excellent front-end linearity, noise figure, and even power consumption performances. Therefore, the front-end subsequent stages design

requirements, were greatly relaxed, when the multi-block LNA design methodology has been introduced.

| | 0.18 $\mu m$ CMOS Selective UWB WLAN Front-end | 0.18 $\mu m$ CMOS Selective Front-end in (Cusmai & Brandolini, 2006) |
|---|---|---|
| Max. Voltage Gain  [dB] | 34.8 | 22.8 |
| Min. NF  [dB] | 6.42 | 5.2 |
| Min. IIP3  [dBm] | -4.35 | -3.5 |
| Current [mA] | 10.9 | 10 |
| Voltage Supply [V] | 1.8 | 1.8 |
| Interferer Rejection [dBc] | -35 | - |
| 1 dB Desensitization [dBm] | -8 | -6.5 |

Table 2. Time-Domain Front-End Performances Summary Comparison

## 4. Conclusion

In this work, a very robust quadrature time-domain CMOS front-end for transform-domain UWB WLAN receiver has been presented, showing 1-dB desensitization point as high as -2dBm, with 27dB narrow-band conversion gain, and 35dBc interferer rejection, witch helps minimizing the loss of orthogonality effect, introduced by the short windowing, in the analog basis expansion of the input signal. The introduced multi-block design LNA, based on highly linear voltage-voltage dynamic feedback topology, filter out the UWB interferers in group #1 and #3, while amplifying the UWB WLAN signal, and shows a better trade-off between linearity, conversion gain, and power consumption.

The downconversion mixer is single-balanced, with the two quadrature pairs sharing the same input transconductor. Further research, will focusing on the implementation of the frequency-domain part of the transform-domain UWB WLAN receiver, where the receiver expands the signal over a basis set, and then operates on the basis coefficients, in order to better use the time-domain front-end performances .

## 5. Referring

Hoyos, S.; Sadler, B. M. (2006). UWB Mixed-Signal Transform-Domain Direct-Sequence Receiver, IEEE Transactions On Wireless Communications, vol. 6, No.8, (August 2006) (3038-3046), ISSN: 10.1109/TWC.2007.051069.

Hoyos, S. et al., (2004). High-Speed A/D conversion for Ultra-Wideband signals based on signal projection over basis functions, Proc. (ICASSP '04), pp. 537-540, ISBN: 10.1109/ICASSP.2004.1326882,  International Conference on Acoustics Speech and Signal Processing, May 2004, Montreal, Canada.

Prakasam, P. K. et al., (2008). Applications of Multipath Transform-Domain Charge-Sampling Wide-Band Receivers, IEEE Transactions on Circuits and Systems –II, vol. 55, No. 4, (April 2008) (309-313), ISSN: 10.1109/TCSII.2008.919480.

Razavi, B. (1997). Design Considerations for Direct-Conversion Receivers, IEEE Transactions On Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 6, (June 1997) (428-435), ISSN: 10.1109/82.592569.

Federal Communications Commission, (2002). Revision of Part 15 of the Commission's Rules Regarding Ultra Wide-band Transmission Systems. [Online].Available: http://www.fcc.gov/Document_Indexes/Engineering_Technology/2002__index_ OET_Order.html.

Blazquez, R. et al., (2005). Direct Conversion Plused UWB Transceiver Architecture, IEEE Proc. (DATE '05), pp. 94-95, ISBN: 10.1109/DATE.2005.122, the Design, Automation and Test in Europe Conference and Exhibition, 2005.

Chen, P.  & Chiueh, T. (2006). Design of A Low Power Mixed-Signal Rake Receiver, IEEE Proc. (ISCAS '06), pp. 2796, ISBN: 10.1109/ISCAS.2006.1693204, International Symposium on Circuits and Systems, May 2006, Island of Kos, Greece.

Park, Y. et al., (2005). A Very Low Power SiGe LNA for UWB Application, ISBN: 10.1109/MWSYM.2005.1516847, IEEE MTT-S International Microwave Symposium Digest, June 2005, Long Beach, CA, USA.

Yu, Y-H.  et al., (2007). A 0.6-V Low Power CMOS LNA, IEEE Microwave and Wireless Components letters, Vol. 17, No. 3, (March 2007) (229-239), ISSN: 10.1109/LMWC.2006.890502.

Shameli, A. & Heydari P. (2006). A Novel Ultra-Low Power (ULP) Low Noise Amplifier Using Differential Inductor Feedback, Proc. (ESSCIRC '06), ISBN: 10.1109/ESSCIR.2006.307603, 32nd European Solid-States Circuits Conference , Sept. 2006, Montreux, France.

Yo, S-S. & Yoo, H-J. (2007). A Low Power Current-reused CMOS RF  Front-end with Stacked LNA and Mixer,  ISBN: 10.1109/SMIC.2007.322780, Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Jan. 2007, Valence, France.

Cusmai, et al., (2006). A 0.18 $\mu m$ CMOS Selective Receiver Front-End for UWB Applications, IEEE Journal Of Solid-State Circuits. Vol. 41, No. 8, (August 2006) (1764-1771), ISSN: 10.1109/ISCAS.2007.377992.

Razavi, B. (2001). Design of analog CMOS integrated Circuits, Boston, MA; Toronto: McGraw-Hill, c2001.

Razavi, B. (2006).  Fundamentals of Microelectronics, B.John & Wiley Sons, Inc. April 2006.

Sjoland, et al., (2003). A merged CMOS LNA and mixer for a WCDMA Receiver, IEEE J. Solid-Sate Circuits, Vol. 38, No. 6, (Jun. 2003), (1045-1050), ISSN: 10.1109/JSSC.2003.811952.

Darabi, H. A. & Abidi, A. (2000). Noise in RF-CMOS mixers: a simple physical model, IEEE J. Solid-Sate Circuits, Vol. 35, No. 1, (Jan. 2000), (15-25), ISSN: 10.1109/4.818916.

Razavi, B. (2007). Design Considerations for Future RF Circuits, Proc. (ISCAS '07), ISBN: 10.1109/ISCAS.2007.377992. IEEE International Symposium on Circuits and Systems May 2007, New Orleans, USA.

Batra, A. et al., (2004). Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a. Mar. 2004 [Online]. Available : https://www.multibandofdm.org .
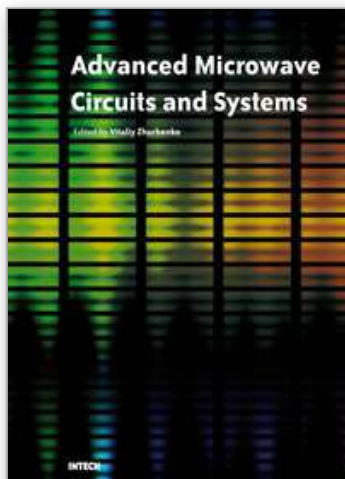
This book is based on recent research work conducted by the authors dealing with the design and development of active and passive microwave components, integrated circuits and systems. It is divided into seven parts. In the first part comprising the first two chapters, alternative concepts and equations for multiport network analysis and characterization are provided. A thru-only de-embedding technique for accurate on-wafer characterization is introduced. The second part of the book corresponds to the analysis and design of ultra-wideband low- noise amplifiers (LNA).

**How to reference**

In order to correctly reference this scholarly work, feel free to copy and paste the following:

# INTECH
open science | open minds