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VLSI Thermal Analysis and Monitoring

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1. Introduction

The rapid evolution in the industry of the integrated circuits during the last decade was so quick that currently it is possible to integrate complex systems on a single SoC (System on a Chip). Due to aggressive technology scaling, VLSI integration density as well as power density increases drastically. As thermal phenomena research activities on micro-scale level are gaining popularity due to an abundance of SoC and MEMS-based applications, various measurement techniques are needed to understand the thermal behaviour of VLSI chip. In particular, measurement techniques for surface temperature distributions of large VLSI systems are a highly challenging research topic. Hence, surface peaks thermal detection is necessary in modern VLSI circuits; their internal stress due to packaging combined with local self heating becomes serious and may result in large performance variation, circuit malfunction and even chip cracking.

One of the important questions in the field of thermal issues of VLSI systems and micro-systems is how to perform the thermal monitoring, in order to indicate the overheating situations, without complicated control circuits. Traditional approach consists of placement of many sensors everywhere on the chip, and then their output can be read simultaneously and compared with the reference voltage recognized as the overheating level.

The idea of the proposed method is to predict the local temperature and gradient along the given distance in a few places only on the monitored surface, and evaluate obtained information in order to predict the temperature of the heat source. Therefore, in the case of an SoC devices, there is no place on the layout for the complicated unit performing computations, but there is also no need for it, as we only want to detect the overheating situations. These peaks are essentials during thermal die monitoring to avoid a critical induced thermo-mechanical stress. Moreover, in most cases, the overheating occurs only in one place.

Due to aggressive technology scaling, VLSI integration density as well as power density increases drastically. For example, the power density of high performance microprocessors has already reached 50W/cm² at 100nm technology and it will reach 100W/cm² at 50nm technology (ITRS, 2003). This evolution towards higher integration levels is motivated by the needs of advanced high performance, lighter and more compact systems with less

power consumption. Meanwhile, to mitigate the overall power consumption, many low power techniques such as dynamic power management (Wu et al., 2000), clock gating (Oh & Pedram, 2001), voltage islands (Puri et al., 2003), dual V_{dd}/V_{th} (Srivastava et al., 2004) and power gating (Kao et al., 1997), (Long & He, 2003) are proposed recently. These techniques, though helpful to reduce the overall power consumption, may cause significant on-chip thermal gradients and local hot spots due to different clock/power gating activities and varying voltage scaling. It has been reported in (Gronowski et al., 1998) that temperature variations of 30°C can occur in a high performance microprocessor design. The magnitude of thermal gradients and associated thermo-mechanical stress is expected to increase further as VLSI designs move into nanometer processes and multi-GHz frequencies.

Nevertheless, the growth of power density dissipated brought a number of critical thermo-mechanical problems. Thus the heat produced in the structure of the VLSI devices is directed towards its edges where it is dissipated by radiation, conduction, or convection. The principal effect of the absence of a good dynamic thermal management is the gradual and continuous degradation of the quality of performance as well as some other direct effects on the life cycle of the electronic systems (Buedo et al., 2002). Thus, an algorithm for the detection and the localization of the thermal peaks is extremely important in order to manage the thermal stress on high density semiconductor devices. These peaks are essentials during thermal die monitoring to avoid a critical induced thermo-mechanical stress.

This study presents a VLSI thermal peak monitoring approach, using GDS, for development of SPTDA algorithm. The proposed algorithm using only two sensor cells will be formulated in a manner to facilitate the development of modular architectures using minimum silicon space in regards of their implementation in VLSI. The architecture selected will be modelled in high level languages, simulated in order to evaluate its performances, and then implemented on a FPGA (Field-Programmable Gate Array). A closed loop of simulation is used in order to evaluate the performances of the architectures proposed at each stage. The proposed architecture of the algorithm will be designed in a modular perspective after the separation of the different elementary functions of the algorithm. Hence the design of SPTDA with flexible modular-based architecture will be presented. The architecture is designed in high level languages such as Matlab™ – Simulink®, simulated, tested using VHDL and synthesized using Xilinx™ ISE (Xilinx, 2009) and Altera™ DSP (Altera, 2009) tools. The simulation and hardware implementation results obtained will be compared to a finite element method (FEM) temperature prediction of the entire GDS method configuration cells.

This chapter will present a packaged VLSI thermal analysis by FEM, thermal monitoring approach using GDS (Gradient Direction Sensors) method. Also the design of surface peaks thermal detector algorithm (SPTDA) with flexible modular-based architecture will be presented.

2. Thermal monitoring by Gradient Direction Sensors method

This part presents the first approach to the method of predicting the temperature of a single heat source on the VLSI device surface. The second approach used concern prediction of the temperature gradient along the given distance in a few places only on the monitored chip-surface. The information obtained will be used to evaluate thermal peak position in order to achieve the temperature of the heat source. This means that we know temperature values in some places on the chip and we try to find the temperature values of the heat sources and eventually predict thermo-mechanical stress distribution in the whole structure.

The proposed algorithm is based on the GDS method for evaluating a single heat source on the chip surface. This method principle of work is explained in details in (Wójciak & Napieralski, 1997). For two sensors, A and C placed in the distance a (Fig. 1), the difference between their output voltages is proportional to the changes of the temperature value along the distance a (Wójciak & Napieralski, 1997). This is true only when the heat source is directly on the line AC for any other cases the values of the angle α has to be taken into account for the proper calculation of ΔT (1).

$$\frac{\Delta T}{\Delta r} = \frac{T_C - T_A}{a \cdot \cos \alpha} \leftrightarrow \frac{V_C - V_A}{a \cdot \cos \alpha} \quad (1)$$

where r is the distance from the heat source. In figure 1, we have:

$$b = \overline{AD}, \overline{AD} \leftrightarrow T_B - T_A \leftrightarrow V_B - V_A \quad (2)$$

$$b + c = \overline{AE}, \overline{AE} \leftrightarrow T_C - T_A \leftrightarrow V_C - V_A \quad (3)$$

In order to obtain the information about angle α we should apply the third sensor. In the simplest case the GDS contains only three temperature sensors placed in distance a (fig. 1)

Fig. 1. The 3 sensors cell $\alpha \in (0^\circ, 30^\circ)$ (Wójciak & Napieralski, 1997)

On the basis of eqs. (2) and (3) and the geometrical dependencies from (fig. 1), eq. (4) is obtained:

$$\tan \alpha \leftrightarrow \frac{2}{\sqrt{3}} \left(\frac{V_B - V_A}{V_C - V_A} - \frac{1}{2} \right) \quad (4)$$

Using the cell we can obtain information on the temperature distribution and partly on the position of the heat source. In order to obtain the temperature value of a single punctual heat source we have to calculate the distance between the sensor and the heat source.

Fig. 2. Problem description and the distribution of the sensors cells

Two sensor cells are required for this purpose (fig2). The cells are placed in a given distance (H) and each of them gives information about the angle α (α_1 and α_2) in the direction of the heat source. Hence, the heat source and cells form a triangle in which the length of one side and values of the angles adjacent to this side are known. This means that we can calculate the distances between the heat source and sensors. Now we can calculate the temperature gradient along the known distance. By adding it to the temperature of the sensor we obtain the temperature of the heat source. Two sensor cells A,B,C and D,E,F are placed in two corners of a monitored layout in the distance H. Hence, the temperature of the heat source can be obtained by equation (5).

$$T_s \leftrightarrow V_s = \frac{H}{a} \times (V_C - V_A) \times \frac{(\tan^2 \alpha_1 + 1) \times (\sqrt{3} + \tan \alpha_2)}{\sqrt{3} \times (1 - \tan \alpha_1 \times \tan \alpha_2) - (\tan \alpha_1 + \tan \alpha_2)} + V_A \quad (5)$$

Figure 2 shows the proposed distribution of the 6 sensors divided into 2 cells located whether on or outside the chip.

3. Algorithmic Design Methodology

3.1 Presentation of algorithmic division

The general flowchart of the proposed SPTDA algorithm is shown in figure 3. It shows some parallelism in computation between the internal variables represented by $\tan \alpha_1$ and $\tan \alpha_2$. This parallelism will be used later in the architectural design in order to optimize the speed of the running implementation. Since successive evaluation of heat source temperature is needed for fast heat-source changes. The algorithm will create 2 triplets of values coming from the detectors. These 2 triplets will be used to calculate the tangents values and estimate R_1 , R_2 and the temperature of the heat source. By dividing the algorithm into its basic arithmetic elementary operations (AEO) we will be able to formulate its data flow graph in order to model the algorithm.

Fig. 3. Flowchart of the SPTDA algorithm

3.2 Architecture modeling using Simulink®

Before modelling the system using Xilinx ISE® or Altera DSP® tools we have to perform a quantification analysis in order to determine the combination of fixed bits that will lead to the minimum quantification error. Due to the fixed number of bits in the fixed point representation, overflow and underflow problems are serious and common. Thus, a set of simulations is required to determine the best fixed point representation. Figure 4 show that a quantification combination of a signed 11.4 and 12.4 bits had great differences with the main function; 13.4 was the turning point, and increasing the number of bits presented no great enhancement to the result. However, it is important to note that the quantification process induce a certain loss of precision. The fixed point specification has to be applied to every operation and even every constant block in a model.

Fig. 4. Results generated using different fixed-point representations

4. Thermal analysis and computational results

4.2 WSI physical structure

In this part we will present steady state and transient thermal analysis of WSI (Wafer Scale Integration) chip junction by FEM approach. It will be used to build models to validate thermal peaks prediction by GDS method. Hence, the geometrical coordinates of the investigated source can be obtained by applying the gradient direction sensors. This way, the possibilities to minimize the thermal peaks in the critical surface areas for BGA (Ball Grid Array) packaged WSI devices can be explored.

Fig. 5. Cross section view of the simulated WSI structure

Fig. 6. Physical position of cell sensors and heat sources on the FEM model

As illustrated in figure 5 (dimensions not respected), the WSI device studied is multilevel structure with simple Si (silicon) substrate covered with different layers, Al (Aluminum), solder ball, and molding compound. The packaging assembly was a ceramic BGA. Once the geometry of the device had been determined and the heat transfer mechanisms quantified, it was possible to model the system using finite element analysis. Using the computer code NISA (Numerical Integrated Elements for System Analysis), a 3-D model was created with more than 100 000 isoparametric thermal shell elements. For the heating computations, this element models the 3-D state of heat flow. For the thermal part, the element has the temperature (T) as the only degree of freedom at each node. Figure 6 shows heat sources and sensors emplacement in the surface of processor. That will enable us to establish in-situ sensor network to achieve the most homogeneous thermo-mechanical cartography. In this study we present a case of WSI structure with internal heat generation. This configuration will enable us to simulate device intense activity and to construct thermal control unit that will ensure a suitable cooling. Moreover, we have to make sure that the temperature device structure variation remains suitable for appropriate induced thermo-mechanical stress. Figure 7 shows position of cell sensors on WSI device for temperature and stress results.

Fig. 7. Schematic position of sensors cell and heat source on WSI device

4.3 WSI Thermal monitoring

In (Lakhsasi et al., 2006) a method has been presented in details, which can be used for mixed fluid-heat transfer approach for VLSI steady state thermal analysis used to analyze IC package problem. However, during thermal analysis the temperature of the chip is determined for typical packages and power levels using fluid boundary conditions to

evaluate equivalent convection coefficient to be applied as a thermal junction BC's. Therefore, the knowledge of the complete temperature field implies the knowledge of the temperature gradients at all times, which is of significance for reliability issues. For the large VLSI device dissipating multiple localized heat sources the single heat source can be considered. As shown in figure 8, fast variations of temperatures in space and in time influence the local peak temperature. Hence, in the case of excessive heating or large amount of power dissipated during short time, the complete transient finite element computations are strongly recommended.

Fig. 8. VLSI device transient thermal analysis dissipating multiple localized heat sources

Fig. 9. VLSI device steady state thermal analysis dissipating single localized heat source

In this study, investigations are done for the simplest case, only six temperature sensors (A,B,C,D,E and F, Figure 2) in the form of two sensor cells and one single power heating source, in order to validate prediction with the 3-D FEM model. The simulations have been carried out for a one source placed at the junction surface level. As expected, the peak temperature profile is located at the centre of the heat source (figure 9). There is subsequent relaxation on temperature gradients through the structure leading to an essentially uniform temperature variation ΔT . The sensor cells can be placed in any way out of the monitored area (different distance H between cell 1 and cell 2), but in some cases adequate placement can simplify the thermal control unit design. In this part the results of thermal peaks can be very useful for indicating overheating situations and critical thermo-mechanical stress occurring in the device structure. Hence, table 1 display a comparison between the temperatures peaks on surface with different implementation under the same conditions.

Thus, the FEM results obtained (Figure 10 and 11) are in full agreement with the GDS predictions.

In this study we use NISA program to construct 3D thermo-mechanical model of WSI device. Furthermore, the application of the finite element method to determine the gradient of temperature that arises in WSI structure is not always simple especially for multi interconnection components such as ball grid array and flip-chip packages. This thermal investigation is based on power loss density distribution (thermal cartography) combined with steady state finite element analysis to predict spatial thermo-mechanical stress at different location in the WSI structure. Therefore, analytical GDS thermal prediction will be compared with FEM method computations.

Detectors Values (°C)			
Detector	Set 1	Set 2	Set 3
V _A	68.655	98.655	75.324
V _B	70.248	100.248	76.324
V _C	71.325	101.325	77.055
V _E	69.365	99.365	75.603
V _F	70.325	100.325	76.540
V _G	72.318	102.318	78.649
Temperature peaks estimated on surface (°C)			
Estimated by	Set 1	Set 2	Set 3
FEM	82.115	115.213	84.632
SPTDA Float	85.320	115.300	85.730
SPTDA Fix	84.060	114.100	84.190
SPTDA Altera	85.630	115.600	85.310

Table 1. Temperature peaks comparisons by FEM and SPTDA

During implementation the fixed-point representation of the SPTDA algorithm was used. After implementation, the same input is directed to the algorithm simultaneously in Simulink® and on the FPGA board. The results are routed back to Simulink®, multiplexed, and projected on the same 2-D graph in order to compare the output. As many simulations and co-simulations have preceded the implementation, the result was expected to be the same as the comparison between the floating and the fixed point comparison. An optimal frequency close to 100 MHZ has been achieved. Furthermore, the VHDL TB (Test Bench) was constructed and the force-file was used to stimulate inputs and to compare with the algorithm predictions. Hence, the set of simulations revealed that the estimations generated by the SPTDA algorithm presented a great concordance with the predictions generated by the Finite Element Method (FEM) presented in (Lakhsasi et al., 2006; Bougataya et al., 2006).

Fig. 10. Temperature distribution according to A-C-axis [C°]

Fig. 11. Temperature distribution according to B-axis [C°]

4.4 Thermal boundary conditions issue

One of the most challenging issues in creating compact thermal models is to use an appropriate set of boundary conditions for generating ‘data’ with a detailed finite element model representing the thermal envelope of the application. The thermal analysis depends on:

- The cooling option (radiators top and/or bottom) applied,
- The location/vicinity and power of its heat-dissipating neighbours,
- The thermal conductivity of the VLSI materials: PCB, heat sink, package, substrate and heat spreader.

In this study we use the NISA finite element program to predict thermal behaviour of the VLSI device structure. A wide variety of boundary conditions can be applied using the FEM software. However, the boundary condition on the vertical sides of the simulation region is somewhat problematic. Placing a fixed boundary condition on these surfaces produces an

incorrect result, unless a very large simulation region is used at the expense of very long simulation run times. A more natural boundary condition is a zero flow condition across these tiny surfaces (adiabatic boundary conditions) as shown in figure 12. The remaining boundary conditions to be defined are on the bottom and top surfaces of the VLSI device, representing the heat sink interfaces. Because the VLSI devices is relatively thin and silicon and solder are good thermal conductors, heat flows happens mainly in the vertical direction, so the boundary conditions in both horizontal directions can be considered adiabatic. The uniform heat removal at the bottom and top is modelled by heat flux exchange coefficient h [$\text{W}/\text{m}^2\cdot^\circ\text{K}$]. The power dissipated by the device is modelled by heat flux produced into the components. The problem formulation is presented graphically in figure 12.

Fig. 12. VLSI device: inside thermal boundary conditions (TBC's) (BC).

5. Thermal stress prediction

If we know the peak temperature along with materials property and boundary conditions we can evaluate the thermal stress using the proposed approach. The algorithm presented herein might prove to be practical comparatively with thermal stress sensors methods especially for applications where the temperature has to be known only in a limited number of points, e.g. the determination of hot spot temperature or on-line temperature monitoring. The thermal stress (excluding the intrinsic one induced by packaging process) in thin films is given by the following expression:

$$\sigma_{th} = (E / (1 - \nu)) \Delta \alpha \Delta T$$

Where $E / (1 - \nu)$ is the composite elastic constant for the different layers and $\Delta \alpha$ the difference in the coefficients of thermal expansion (CTE) between different level of packaging (Kobeda et al., 1989). In (Lakhsasi & Skorek, 2002) a method has been presented in details for calculation of the compressive stress in the silicon level given by:

$$\begin{aligned} \sigma_{xx, max} &\approx -9.63 (E \alpha)_{Si} \Delta T_{in} \quad (\text{Kobeda et al., 1989}) \\ \sigma_{xx, max} &\approx -9.63 (0.15 \times 2.8)_{Si} (102.3 - 81.1) \\ \sigma_{xx, max} &\approx -8.574 \text{ MPa} \end{aligned}$$

However, the induced compressive thermal stress will be combined to the intrinsic one due to the fabrication processes, and the stress due to the mechanical clamping mechanism.

Table 2 gives the thermo mechanical parameters for different materials used in the computation.

Materials	Chip (die)	M	BT Substrate	Solder Ball	Al	Die attach
Young’s Modulus (GPa)	131	16	26(xy), 11(z)	17	70	100
Poison’s Ratio	0.3	0.25	0.39(xz.yz), 0.11(xy)	0.4	0.33	0.25
CTE ppm/°C	2.8	15	15(xy), 52(z)	21	22.4	0.8
Thermal Conductivity W/m.°C	150	65	0.3	50	160	33
Density Kg/m³	2330	1660	1660	8460	2700	3300
Specific heat J/kg. °C	712	1672	1672	957	960	1100

Table 2. Device Materials thermo-mechanical Properties

M e t h o d	Distance Cell 1-cell 2, H (µm)	Source Temp Tmax (°C)	Distance Cell 1-source 1 (µm)	Distance Cell 2-source 1 (µm)
Analytical results by GDS	8000	100.2	10376	10809
3-D FEM model results.	8000	102.3	10148	10984

Table 3. Results comparison between GDS method and 3-D FEM model

The nodal temperatures stored in the thermal part were used to perform a thermal stress analysis of the device structure. It is assumed that the structure is stress-free at 25 °C. The presence of a temperature variation throughout the device structure causes deformation due to thermal contraction and expansion. A thermal stress analysis is performed to calculate these deflections and associated stresses due to the thermal loading. The computation is extended to the whole volume of the device structure.

The present approach may be suitable for large VLSI devices packaging, because it potentially allows the combination and integration of both thermal and mechanical control, in a single unit. As an example, the maximum level of stress generated by intense heating of WSI devices have been evaluated and examined by GDS method. During design and finale packaging of large VLSI devices, in-situ thermo-mechanical control unite must be implemented to ensure the safe fulfillments of their operating conditions. The nature of such interface materials must therefore be considered very carefully during WSI design and packaging. Further research should be focused on elaborating software tools for optimization of temperature sensor positions within the allowed area for an IC designer.

Figure 13 and 14 shows thermal stress profile according to X₁-axis. The peak compressive stress of σ_{xx}= -8.5 MPa is reported around the region of the heat source.

Fig. 13. VLSI thermal stress profile according to X_1 -axis, σ_{xx} = -8.5 MPa Maximum

Fig. 14. VL VLSI thermal stress profile according to X_2 -axis, σ_{xx} = -3.3 MPa Maximum

VLSI layers are very thin and any imperfection in structure may lead to cracking and subsequent shear-initiated delamination at the silicon level. The nature of such interface materials must therefore be considered very carefully in VLSI devices design for intense applications. Depending on the technology requirements and definition of failure, the mechanism of failure may take several forms.

6. Discussion

One of the important questions in the field of thermal issues of VLSI systems and microsystems is how to perform the thermal monitoring, in order to indicate the overheating situations, without complicated control circuits. Traditional approach consists of placement of many sensors everywhere on the chip, and then their output can be read simultaneously (Szekely, 1994) and compared with the reference voltage recognized as the overheating level.

The idea of the proposed algorithm is to predict the local temperature and gradient along the given distance in a few places only on the monitored surface, and evaluate obtained information in order to predict the temperature of the heat source. Therefore, in the case of an SoC devices, there is no place on the layout for the complicated unit performing computations, but there is also no need for it, as we only want to detect the overheating situations. These peaks are essentials during thermal die monitoring to avoid a critical induced thermo-mechanical stress. Moreover, in most cases, the overheating occurs only in one place.

In this chapter, a methodology to evaluate and predict a thermal peak of large VLSI circuit was presented. The important factors contributing to the device's thermal heating were characterized. The monitoring approach reported in this paper can be applied to predict the thermal stress peak of multilevel structures. Surface peaks thermal detection is necessary in modern VLSI circuits; their internal stress due to packaging combined with local self heating becomes serious and may result in large performance variation, circuit malfunction and even chip cracking. Also, in this paper GDS technique was used to develop SPTDA algorithm.

7. Conclusion

This study presented an approach to thermal and thermo-mechanical stress monitoring of VLSI chip. The possibility of evaluating thermal peaks and associated thermal stress distribution all over the monitored area by using GDS and FEM has been shown. Furthermore, this study presented an approach to the application of inverse problem for thermo-mechanical analysis. The thermal peaks of investigated source can be obtained by applying the gradient direction sensors method. The adequate placement of sensors can accurately evaluate the thermal peaks and simplify the thermo-mechanical control unit design. That will enable the chip designer to establish the most homogeneous thermo-mechanical cartography during operation. The cost of the thermal management of WSI device depends heavily upon the efficiency of the chip design. However, heat sources spatial distribution has a significant effect on the WSI device operation. Hence, in-situ thermo-mechanical control unite must be implemented to prevent unexpected pitfalls.

Another aspect presented in this study is related to surface peaks thermal detection in modern VLSI circuits; because their internal stress due to packaging combined with local self heating becomes serious and may result in large performance variation, circuit malfunction and even chip cracking. As an example, in this study GDS technique was used to develop SPTDA algorithm. Several approaches were implemented to achieve a better performance for the SPTDA operation. In (Wójciak & Napieralski, 1997), physical circuit architecture was proposed. However, complicated control components had to be deployed in the circuit which is not suitable for today's constraints regarding area, especially if the control algorithm needs to be placed on-chip, for example, on a sensor network node. Thereby, deploying the SPTDA in sensor network can be made feasible in the future.

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The process of Integrated Circuits (IC) started its era of VLSI (Very Large Scale Integration) in 1970's when thousands of transistors were integrated into one single chip. Nowadays we are able to integrate more than a billion transistors on a single chip. However, the term "VLSI" is still being used, though there was some effort to coin a new term ULSI (Ultra-Large Scale Integration) for fine distinctions many years ago. VLSI technology has brought tremendous benefits to our everyday life since its occurrence. VLSI circuits are used everywhere, real applications include microprocessors in a personal computer or workstation, chips in a graphic card, digital camera or camcorder, chips in a cell phone or a portable computing device, and embedded processors in an automobile, et al. VLSI covers many phases of design and fabrication of integrated circuits. For a commercial chip design, it involves system definition, VLSI architecture design and optimization, RTL (register transfer language) coding, (pre- and post-synthesis) simulation and verification, synthesis, place and route, timing analyses and timing closure, and multi-step semiconductor device fabrication including wafer processing, die preparation, IC packaging and testing, et al. As the process technology scales down, hundreds or even thousands of millions of transistors are integrated into one single chip. Hence, more and more complicated systems can be integrated into a single chip, the so-called System-on-chip (SoC), which brings to VLSI engineers ever increasingly challenges to master techniques in various phases of VLSI design. For modern SoC design, practical applications are usually speed hungry. For instance, Ethernet standard has evolved from 10Mbps to 10Gbps. Now the specification for 100Mbps Ethernet is on the way. On the other hand, with the popularity of wireless and portable computing devices, low power consumption has become extremely critical. To meet these contradicting requirements, VLSI designers have to perform optimizations at all levels of design. This book is intended to cover a wide range of VLSI design topics. The book can be roughly partitioned into four parts. Part I is mainly focused on algorithmic level and architectural level VLSI design and optimization for image and video signal processing systems. Part II addresses VLSI design optimizations for cryptography and error correction coding. Part III discusses general SoC design techniques as well as other application-specific VLSI design optimizations. The last part will cover generic nano-scale circuit-level design techniques.

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