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Power Amplifier Design for High Spectrum-Efficiency Wireless Communications

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1. Introduction

The growing market of wireless communications has generated increasing interest in technologies that will enable higher data rates and capacity than initially deployed systems. The IEEE 802.11a standard for wireless LAN (WLAN), which is based on orthogonal frequency division multiplexing (OFDM) modulation, provides nearly five times the data rate and as much as ten times the overall system capacity as currently available 802.11b wireless LAN systems (Eberle et al., 2001; Zargari et al., 2002; Thomson et al., 2002). The modulation format of the IEEE 802.11a is OFDM (Orthogonal Frequency Division Multiplexing) which is not a constant-envelope modulation scheme; more sensitive to frequency offset and phase noise, and has a relatively large peak-to-average power ratio. These reasons induce the linearity requirements, which are crucial for power amplifier design. Among various linearization techniques, transistor-level predistortion is the simplest approach to implement and can be realized in a small area, which makes it be the most compatible with RFIC implementation.

Conventionally, WLAN has been implemented with multi-chip approach or single chip with processes other than CMOS. For example, the radio frequency (RF) and intermediate frequency (IF) sections are fabricated with GaAs or BiCMOS processes, and the baseband DSP section with a CMOS process. Note that the complexity and cost will be dramatic in a wireless LAN system with hybrid processes, which makes the CMOS process be the most promising approach to achieve high integration level, low power consumption, and low cost for the integration of baseband and RF front-end circuits of a WLAN system.

There are two different modulation schemes employed in wireless communication standards: linear modulation and nonlinear modulation, in which the former one is employed in North American Digital Cellular (NADC) standard whereas the latter one is also called constant-envelope modulation which employed in the European Standard for Mobile Communications (GSM). The main requirements for power amplifiers (PA's) employed in wireless communications are generally high power efficiency and low supply voltage operating at high frequencies. Class-E PA's have demonstrated the potential of high power efficiency whereas due to the operation characteristics, it can only be adopted in constant-envelope modulation applications. The linear modulation scheme, on the other hand can achieve high spectrum efficiency, which is especially suitable for the application of

wireless communications. A power amplifier that can achieve high power efficiency while providing high spectrum efficiency is therefore highly desired. To discuss this issue, in this chapter a class-AB type amplifier in a standard CMOS process is investigated together with the presentation of a transistor-level predistortion compensation techniques.

The main theme of this chapter is aimed at providing the fundamental background knowledge concerned with linear PA design for high spectrum-efficiency wireless communications. Nevertheless, we also present the design considerations of the state-of-the-art linear PA's together with the design techniques operating at the gigahertz bands in CMOS technologies. To conclude the chapter, we investigate a design and implementation of a Class-AB PA operating at GHz for IEEE 802.11 wireless LAN to demonstrate the feasibility.

2. Design Concept of CMOS Power Amplifiers

Conjugate matching is fully understood as making the value of load resistance equals to the real part of the generator's impedance. Since the maximum power will be delivered to the load, however, this delivering power will be limited by the maximum rating of the transistor. This phenomenon can be shown in Fig. 1. For utilizing the maximum current and voltage swing of the transistor, a lower than the real part of generator's impedance is chosen for maximum power transformation.

Fig. 1. Conjugate Matching and Power Matching

The load-line match represents an actually compromise that extracts the maximum power from the power devices, and simultaneously maintains the output swing within the limitation of the power devices and the available DC supply. In a typical situation, the conjugate matching yields a 1-dB compression power about 2dB lower than that can be attained by the correct load line matching (power matching), which means the power device can deliver 2dB lower power than the manufactures specify. So the power matching condition has to be taken seriously, despite the fact that the gain of the PA circuits is lower than conjugate matching at lower signal levels.

Another design concept of CMOS power amplifiers is the knee voltage effect of deep sub-micron CMOS transistors. The knee voltage (pinch-off voltage) divides the saturation and linear operation region of the transistor. Typically, for a power transistor may be 10% or 15% of the supply voltage, and the optimum load impedance is

$$R_{opt} = \frac{V_{max} - V_{Knee}}{I_{max}} \quad (1)$$

Notice that the knee voltage can be as high as 50% of the supply voltage for deep sub-micron CMOS technologies as shown in Fig. 2. Therefore, preventing the CMOS transistor from operating in the linear region doesn't result in the optimum output power. Also, both the saturation and linear operating regions must be considered in determining the optimum output load impedance since a lot portion of RF cycle could be in the linear operating region.

Fig. 2. Knee Voltage of Typical Power Device and CMOS device.

Another issue is the choice of device size of each amplifying stage. A simple class-A amplifier can briefly explain this issue as shown in Fig.3, in which RFC means radio frequency choke with large impedance compared with load impedance R_L .

Fig. 3. Simple circuit of class-A amplifier.

Load impedance R_L is generally equal to 50 ohms and the matching network is tuned to obtain the device maximum output power. When the device output power is reaching to the maximum, the output impedance R_{out} is defined as the optimum load impedance R_{opt} . In a class-A amplifier, the device plays a role of a voltage-dependant current source as shown in Fig.4, in which I_{max} is the maximum available current of the device, I_{min} is the minimum current of the device. V_{max} is the maximum tolerance voltage of the device between drain and source of the device. V_{min} is the knee voltage of the device. V_{dc} and I_{dc} are the DC bias of the device. Therefore, the device voltage swing and current swing are $V_{max}-V_{min}$ and $I_{max}-I_{min}$, respectively.

Fig. 4. I-V Curve of a NMOS device.

The optimum load impedance R_{opt} for maximum AC swing can thus be described as

$$R_{opt} = \frac{V_{max} - V_{min}}{I_{max} - I_{min}} \quad (2)$$

and the output power of the device can be expressed as

$$P_{RF} = V_{rms} I_{rms} = \frac{V_{max} - V_{min}}{2\sqrt{2}} \cdot \frac{I_{max} - I_{min}}{2\sqrt{2}} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad (3)$$

Since DC power consumption is

$$P_{DC} = \frac{V_{max} + V_{min}}{2} \cdot \frac{I_{max} + I_{min}}{2} = \frac{(V_{max} + V_{min})(I_{max} + I_{min})}{4} \quad (4)$$

the power efficiency η is thus given by

$$\eta = \frac{P_{RF}}{P_{DC}} = 0.5 \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{(V_{max} + V_{min})(I_{max} + I_{min})} \quad (5)$$

Theoretically, V_{min} and I_{min} are zeros, and ideal drain efficiency of a class-A amplifier is 50%. However, in fact V_{min} and I_{min} are not equal to zeros, which implies that the drain efficiency should be less than 50%.

3. Power Amplifier Linearization Techniques

Feedback linearization techniques are the most general approaches employed in RF power amplifier design such as in the North American Digital Cellular (NADC) standard, a CMOS power feedback linearization is employed to linearize an efficient power amplifier transmitting a DQPSK modulated signal (Shi & Sundstrom, 1999), in which a reduction of more than 10dB in the adjacent channel interference was achieved according to the experimental results.

Fig. 5 shows a PMOS cancellation transistor-level linearization technique (Wang et al., 2001). The measurement results demonstrate that the amplifier with nonlinear input capacitance compensation has at least 6-dB IM3 (Third-order intermodulation intercept point) improvement in a wide range of output powers compared with the non-compensated amplifier whereas the disadvantages are low power gain and increasing input capacitance.

Fig. 5. Transistor-level linearization techniques – PMOS cancellation.

A miniaturized linearizer using a parallel diode with a bias feed resistance in an S-band power amplifier was also proposed (Yamauchi et al., 1997). The diode linearizer can improve adjacent channel leakage power of 5dB and power-added efficiency of 8.5%. Note that the improvement is based on 32 kb/ps, $\pi/4$ shift QPSK modulated signal at 28.6 KHz offset with a bandwidth of 16 KHz.

A miniaturized “active” predistorter using cascode FET structures was also applied to linearize a 2-GHz CDMA handset power amplifier. The ACPR (Adjacent Channel Power Ratio) improvement of 5dB was achieved (Jeon et al., 2002). Unlike the previously reported predistorters, this “active” predistorter can provide 7 to 17-dB gain which alleviates the requirement of additional buffer amplifiers to compensate the loss of the predistorter.

Another transistor-level linearization technique using varactor cancellation is shown in Fig.6 (Yu et al., 2000), which the approach improves 10-dB spectral regrowth with a low loss at 2GHz. However, the GaAs FET amplifier has AM-PM distortion under large-signal operating conditions due to the non-linear gate-to-source capacitance C_{gs} and the disadvantages are high cost, low integration with other transmitter circuits, and occupy a large PCB footprint.

A complex-valued predistorter chip in CMOS for baseband or IF linearization of RF power amplifiers has been implemented (Westesson & Sundstrom, 1999). By choosing the coefficients for the predistortion polynomial properly, the lower-order distortion components can be cancelled out. Results of measurement performed as two-tone tests at an IF of 200MHz with 1MHz tone separation, using the chip for linearization gives a reduction of IM3 and IM5 with more than 30 and 10dB, respectively

Fig. 6. Transistor-level linearization techniques – varactor cancellation.

Digital predistortion is a technique that counteracts both adjacent channel interference and BER degradation of power amplifiers. By employing digital feedback and a complex gain predistortion present, the experimental results demonstrate that a reduction in out of band spectra in excess of 20dB can be achieved (Wright & Durtler, 1992).

4. Predistortion Techniques for Linearization

Predistortion techniques are popular approaches for linearity improvement in power amplifier design. The concept is placing a black box on the PA input, which consumes little power and provides an acceptable linearity improvement instead of employing more complex circuitry to enhance system linearity. Basically, all predistortion approaches are open loop and can only achieve the level of linearization of closed-loop systems for limited periods of time and dynamic range. Recent research focuses on predistortion techniques offered by DSP. The basic concept is shown in Fig.7, where a predistorter preceding the nonlinear RF power amplifier implements a complementary nonlinearity, such that the combination of the two nonlinearities results in a linearized output signal. In practice, the lower orders nonlinear terms, such as third and fifth, is the most troublesome in communication applications. Even in practical PA models that consist of a couple of lower order nonlinear polynomial terms cannot be accurately estimated.

Fig. 7. Concept diagram of predistortion linearization.

4.1 Analog predistorters

Analog predistorters can be classified into two categories: 'simple' predistorters and 'compound' predistorters. The simple predistorters comprise one or more diodes, and the compound predistorters synthesize the required nonlinear characteristic using several sections to compensate different degree of distortion.

Simple analog predistorters mainly use a nonlinear resistive element such as a diode or an FET device as an RF voltage-control resistor that can be configured to provide higher attenuation at low drive levels and lower attenuation at high drive levels. A simple predistorter linearized RF power amplifier has been developed for 1.95-GHz wide-band CDMA (Hau et al., 1999), in which the amplifier is based on a heterojunction FET and its linearity and efficiency are improved by the employment of a MMIC simple analog predistorter which is shown in Fig.8. Gain expansion is observed when V_c is lower than $-1V$. Insertion loss (IL) is less than 5dB for a gain expansion of 2dB. Phase compensation was obtained from the MMIC predistorter as a result of the use of two inductors.

Fig. 8. Schematic of the MMIC predistorter.

The block diagram of a compound cuber predistortion system is shown in Fig.9, in which the input signal is split into two paths, and recombined in 180° phase shift at the output preceding PA (Morris & McGeehan, 2000). The key point of cuber predistorter is that the distortion terms can be scaled and phase shifted independently from the original undistorted input signal. Since the out of phase path can be set only for the third-order term, only the distortion term can be cancelled. For the reasons, this system is sometimes called a "cuber". However, there is a significant insertion loss in the combiner and splitter. Note that the lower coupling factors into and out of the cuber will result in a few losses in the main path. The independent two paths for high levels of IMD correction need a good gain and phase match.

Fig. 9. Block diagram of a compound cuber predistorter.

4.2 DSP predistortion techniques

This approach is attractive since most modern radio frequency transceivers employ some form of DSP in their baseband processing as illustrated in Fig. 10.

Fig. 10. Baseband predistortion system.

Fig. 11. DSP look-up table predistortion scheme.

A DSP look-up table predistortion system illustrates in Fig. 11. It should be noted that the system employs an input signal delay element to compensate the processing delays in the detection and DSP signal processing. The main limitation of the scheme is the speed of the detection and DSP itself.

The correction signals contain multiple harmonics of the baseband signal in order to perform the necessary predistortion function, which imposes a stringent requirement on the data converters. The precision of the look-up table is an important issue, which it can be implemented either physically or by a suitable algorithm. Moreover, the envelope input sensing is also a difficult task when the input signal throughputs continue rising. Note that a trade-off between the precision of detection process and the number of RF cycles employed to determine the final detector output is existed for the classical envelop detectors.

5. Linearity Improvement Circuit Techniques

Modern communication standards employ bandwidth-efficient modulation schemes such as non-constant envelope modulation techniques to prevent spectral re-growth problem, AM-AM, and AM-PM distortions, which means that some extra circuits for linearization purpose in power amplifier design are required.

Nevertheless, employing a linear PA's is a straightforward approach whereas it is also an inefficient method to meet the requirement of linearity. By taking advantage of the characteristics of high efficiency and applying some linearization techniques, nonlinear PA's may be a promising alternative. In this section, we investigate two transistor-level linear techniques to improve linearity of CMOS PA's namely, one is the nonlinear capacitance compensation scheme and the other is a parallel inductor compensation scheme. These two approaches will be described in the following subsections.

5.1 Nonlinear capacitance compensation technique

A deep sub-micron MOSFET RF large signal model that incorporates a new breakdown current model and drain-to-substrate nonlinear coupling is shown in Fig. 12 (Heo et al., 2000). This model includes a new breakdown current I_{dsB} with breakdown voltage turnover behavior and a new nonlinear coupling network of a series connection of C_{dd} and R_{dd} between the drain and a lossy substrate. The robustness of the new nonlinear deep sub-micron MOSFET model has been verified through load-pull measurements including IMD and harmonics at different termination impedance and bias conditions.

Fig. 12. Equivalent nonlinear model of a deep sub-micron NMOS device (slashed components are bias dependent).

A nonlinear capacitance cancellation technique to cancel the bias dependent input capacitance of the amplifier has been proposed and a prototype single-stage amplifier with a measured drain efficiency of 40% and a power gain of 7dB at 1.9GHz was reported in (Wang et al., 2001). The measured results indicate that the amplifier with nonlinear capacitance compensation has at least 6-dB IM₃ improvement in a wide range of output powers compared with the original amplifier without compensation.

The idea of the nonlinear capacitor compensation technique is that during the drain current clipping when the input signal is large enough to turn device 'on' and 'off', which the dramatical change in C_{GS} will generate distortion since Z_{in} is not keeping constant in signal amplification. The input impedance of the amplifier is approximately (ignore the R_s)

$$Z_{in} = \frac{1}{j\omega C_{in}} = \frac{1}{j\omega(C_{GS} + (1 + A)C_{GD})} \quad (6)$$

in which A is the voltage gain of the amplifier, the relationship of V_{GS} and V_{in} is

$$V_{GS} = \frac{Z_{in}}{Z_g + Z_{in}} V_{in} \quad (7)$$

and V_{GS} is a linear and delayed version of V_{in} on linear amplification

$$V_{GS}(t) = CV_{in}(t - t_0) \quad (8)$$

Note that by introducing a parallel inverse nonlinear characteristic component at the input of the amplifier can reduce the distortion, which a PMOS capacitance can be a good choice to compensate the nonlinearity of NMOS input capacitance. In other words, the input impedance Z_{in} is near a constant for a wide range of V_{GS} due to the inverse characteristic of the PMOS capacitance from the NMOS counterpart. The Behavior of NMOS C_{GS} and C_{GD} in

different operation region is shown in Fig.13 (Razavi, 2000), where W is the width of the NMOS device, L is the effective length of the NMOS device. C_{OX} is the oxide capacitance per unit width, and the overlap capacitance per unit width is denoted by C_{OV} . If the device is off, $C_{GD} = C_{GS} = WC_{OV}$ and the gate-bulk capacitance comprises the series combination of the gate oxide capacitance and the depletion region capacitance.

Fig. 13. Variation of gate-source and gate-drain capacitance versus V_{GS} .

If the device is operating at triode region, such that S and D have approximately equal voltages, then the gate-channel (WLC_{OX}) is divided equally and $C_{GD} = C_{GS} = (WLC_{OX})/2 + WC_{OV}$. On the other hand, the gate-drain capacitance of a MOSFET is roughly equal to WC_{OV} for the saturation mode operation. The potential difference between the gate and channel varying from V_{TH} at the source to $V_D - V_{TH}$ at the pinch-off point results in a non-uniform vertical electric field in the gate oxide along the channel. It can be proved that the gate-source capacitance equals to $(2/3)WLC_{OX}$ (Muller & Kamins, 1986). Thus, $C_{GS} = (2/3)WLC_{OX} + WC_{OV}$. The dependence of a p-substrate MOS capacitance on voltage is shown in Fig.14 (Singh, 1994), in which V_{fb} represents flat-band voltage and V_T represents threshold voltage. In accumulation region (negative V_G), the holes accumulate at the oxide-semiconductor interface. Because holes are majority carriers, the response time is fast enough. As the gate voltage becomes positive, the interface is depleted of holes and attracts minority carriers. The depletion capacitance becomes important in this region. When the device gets more and more depleted, the value of C_{MOS} decreases to $C_{MOS}(\min)$.

At inversion condition, the depletion width reaches its maximum width. If the bias increases further, the free electrons in the p-substrate start to collect in the inversion region, whereas the depletion width remains unchanged with bias. The required excess free electrons are introduced into the channel by electron-hole generation. Since the generation process takes a certain amount of time, the inversion sheet charge can follow the bias voltage only if the voltage change speed is slow. If the variations are fast, the electron-hole generation cannot catch up the variations. The capacitance due to the free electrons has no contribution and the MOS capacitance is dominated by the original depletion capacitance. Therefore, under high-frequency conditions, the capacitance does not show a turnaround and remains at the $C_{MOS}(\min)$ as shown in Fig. 14.

Fig. 14. Dependence of a P-substrate MOS capacitor versus voltage.

5.2 PMOS capacitance compensation technique

As shown in Fig.15, we can use this inverse capacitance characteristic to compensate the nonlinearity of NMOS input capacitance.

Fig. 15. Schematic of the PMOS capacitance compensation PA.

The Hspice simulation results of the NMOS and PMOS input capacitance (C_{gs} and C_{gd}) are shown in Fig.16 (a) and (b), respectively.

Fig. 16(a). Capacitances of C_{gs} and C_{gd} versus V_{gs} for NMOS device ($W=1920\mu\text{m}$, $L=0.18\mu\text{m}$).

Fig. 16(b). Capacitances of C_{gs} and C_{gd} versus V_{gs} for PMOS device ($W=1280\mu\text{m}$, $L=0.18\mu\text{m}$).

The total input capacitance of the NMOS and PMOS devices is shown in Fig.17. Obviously, we can use this inverse capacitance characteristic to compensate the nonlinearity of NMOS input capacitance.

Fig. 17. Total gate input capacitance with PMOS capacitance compensation.

5.3 NMOS diode linearizer technique

The newly proposed approach is the diode linearizer which can be integrated in the PA design. The integrated diode linearizer in HBT PA can effectively improve the gain compression and phase distortion performances from the gate dc bias level (V_{GS}). Notice that the dc bias level decreases as the input power increases. A PA uses an integrated diode-connected NMOS transistor as the function of diode linearizer is shown in Fig.18. A similar technique by using nonlinear capacitance cancellation in CMOS PA designs has been reported in (Yen & Chuang, 2003).

Fig. 18. Schematic of NMOS diode linearizer PA with parasitic capacitors.

For a first-order approximation, the oxide-related gate capacitances C_{GS} , C_{GD} , and C_{GB} of M1 are given by (Massobrio & Antognetti, 1993)

$$C_{GS} = \frac{2}{3} C_{OX} + C_{GS0} W \quad (9)$$

$$C_{GD} = C_{GD0} W \quad (10)$$

$$C_{GB} = C_{GB0} L_{eff} \quad (11)$$

for M1 operating at the saturation mode, in which L_{eff} is the effective channel length, W is the width of the channel, C_{OX} is the gate oxide capacitance, C_{GS0} , C_{GD0} , C_{GB0} are the voltage-independent overlap capacitances per meter among the gate and the other terminals outside the channel region and

$$C_{GS} = C_{OX} \left\{ 1 - \left[\frac{V_{GS} - V_{DS} - V_{TH}}{2(V_{GS} - V_{TH}) - V_{DS}} \right]^2 \right\} + C_{GS0} W \quad (12)$$

$$C_{GD} = C_{OX} \left\{ 1 - \left[\frac{V_{GS} - V_{TH}}{2(V_{GS} - V_{TH}) - V_{DS}} \right]^2 \right\} + C_{GD0} W \quad (13)$$

$$C_{GB} = C_{GB0} L_{eff} \quad (14)$$

for M1 operating at the triode mode, where V_{TH} is threshold voltage.

On the other hand, due to the depletion charge surrounding the respective drain diffusion region embedded in the substrate, the junction capacitance C_{DB} of M2 is given by

$$C_{DB} = \frac{C_j A_D}{(1 + V_{DB} / \phi_j)^{m_j}} + \frac{C_{jsw} P_D}{(1 + V_{DB} / \phi_j)^{m_{jsw}}} \quad (15)$$

in which C_j and C_{jsw} are the capacitances at zero-bias voltage for square meter of area and for meter of perimeter, respectively, m_j and m_{jsw} are the substrate-junction and perimeter capacitance grading coefficients, ϕ_j is the junction potential, and drain-to-gate overlap capacitance C_{DG} of M2 can be described as

$$C_{DG} = C_{DG0} W \quad (16)$$

Notice that the input-voltage-dependent capacitances C_{GS} , C_{GD} of M1 indicated in (12) and (13) increase with an increase of V_{GS} whereas the junction capacitance C_{DB} of M2 described in (15) decreases with an increase of V_{DB} ($=V_{GS}$ of M1). Therefore, with a proper choice of the dimensions of M1 and M2, a near constant total input capacitance can be achieved.

Fig. 19 shows the simulation results of the NMOS gate capacitance (C_{GS} , C_{GD} , and C_{GB}) and the NMOS diode total capacitance at drain (C_{DG} and C_{DB}). The total input capacitance of these two devices has flat curve characteristic at each V_{GS} . Clearly, it also implies the distortion due to the nonlinearity of the input capacitance can be reduced.

Fig. 19. Total gate input capacitance with diode linearizer for TSMC 1.8V RF MOS device.

Also, the P1dB simulation results indicate this diode-linearizer bias technique can improve 2-dB linear gain than the conventional resistance bias approach as shown in Fig.20. Note that the device dimensions of the CMOS PA can reach millimeter scale, which implies that the parasitic capacitances C_{p1} and C_{p2} can degrade the gain and power-added efficiency of the PA due to the large parasitic capacitances (Jeffrey et al., 2001).

Fig. 20. P1dB simulation results of the diode-linearizer bias approach for different diode size.

5.4 Parallel inductor compensation diode technique

CMOS cascode amplifier architecture with the parallel inductor is shown in Fig. 21. Notice that the large device sizes of CMOS PA can lead to large parasitic capacitances, C_{p1} and C_{p2} ,

which degrade the gain and power-added-efficiency of PAs (Jeffrey et al., 2001). In order to increase the power gain of CMOS PAs and reduce the currents required to charge and discharge the parasitic capacitors at these nodes, an inductor, L_{tank} is used across the differential cascode nodes to produce a resonant tank at these nodes. Since the power gain increases, the 1-dB compression point is extended to a higher value and the linearity can be improved by this kind of circuit.

Fig. 21. CMOS cascode amplifier with a parallel inductor.

6. Self-Biased and Bootstrapped Techniques

Self-biased and bootstrapped techniques can relax the design restriction due to hot carrier degradation in power amplifiers and alleviate the requirement of using thick-oxide transistors. Note that the transistors have poor RF performance compared with the standard transistors available in the same process. Fig. 22 shows no performance degradation after ten days of continuous operation under maximum output power at 2.4-V supply voltage (Sowlati & Leenaerts, 2003); (Mertens & Steyaert, 2002).

There are two main issues in the design of power amplifiers in submicron CMOS, namely, oxide breakdown and hot carrier effect. Both of these are even worse as the technology scales. The oxide breakdown is a catastrophic effect and sets a limit on the maximum signal swing on drain. The hot carrier effect, on the other hand, is a reliability issue. It increases the threshold voltage and consequently degrades the performance of the device. The recommended voltage to avoid hot carrier degradation is usually based on dc/transient reliability tests. For production requirements, the recommended voltage is 5%–10% above the maximum allowed supply voltage to guarantee a product lifetime of ten years. For a 0.18- μm process, this leads to a maximum dc drain–gate voltage of 2 volts. CMOS power amplifiers have been reported with the dc voltage below the recommended voltage with the dc RF voltage levels of exceeding the maximum allowed value (Fallesen & Asbeck, 2001). The performance degradation due to hot carrier becomes evident during the first few hours, and the output power of the amplifier decreases in the order of 1 dB after 70–80 hours of continuous operation (Vathulya et al., 2001).

Fig. 22. Output power versus time of continuous operation.

Cascode configuration and thick-oxide transistors (Yoo & Huang, 2001; Kuo & Lusignan, 2001) have been used to eliminate the effects of oxide breakdown voltage and the hot carrier degradation, which allows the use of a larger supply voltage. So far, in cascode power amplifiers, the common-gate transistor has had a constant dc voltage with an ac (RF) ground. Under large signal operation, the voltage swing on the gate–drain of the common-gate transistor becomes larger than that of the common-source transistor. Therefore, the common-gate transistor becomes a bottleneck in terms of breakdown or hot carrier degradation. In (Yoo & Huang, 2001), the 900-MHz 0.2-μm CMOS cascode power stage uses a combination of standard and thick-oxide devices (standard device for the common-source and thick-oxide device for the common-gate). The thick-oxide device is equivalent to a device in 0.35-μm process which can tolerate a much larger voltage. However, a thick-oxide device does not have the same high-frequency performance of the standard device. A cutoff frequency f_t of 26 GHz is typical for thick oxide in a 0.2-μm CMOS compared with its standard device which has a typical f_t of 50 GHz. The thick-oxide device basically provides a lower gain at RF. In a cascode combination of thick and standard devices, the thick device limits the high-frequency performance. In other words, even though we use a more advanced technology (0.18-μm process compared with 0.35-μm process), we cannot exploit the higher frequency performance of the scaled-down devices.

6.1 Conventional cascode power stage

A conventional cascode amplifier is shown in Fig. 23(a), in which transistors M1 and M2 configured as common source (CS) and common gate (CG) amplifiers, respectively. The RF signal is applied to G1. Gate G2 is RF grounded with a dc value of V_{DC} which can be equal to the supply voltage V_{DD} . The dc voltage at D2 is equal to the supply voltage with an RF voltage swing around this value. At maximum output power, the voltage at D2 swings down close to zero and up to twice V_{DD} . In order to increase the efficiency, the voltage can be shaped with the choice of the matching network. In the cascode configuration, transistor M1 has a smaller drain–gate voltage swing. This is because the voltage at D1 is always lower

than voltage at G2 by an amount equal to the gate-source voltage of G2. Consequently, the supply voltage is limited by the breakdown voltage of M2 rather than M1. This can also be observed from Fig. 23(b) which shows the time domain voltage waveforms for this amplifier. In this simulation, the supply voltage is 2.4 V and the operating frequency is 5.25 GHz.

Fig. 23. (a).Conventional cascode amplifier (b).Voltage waveforms versus time for $V_G=0.8V$, $V_{in}=0.8\sin\omega t$, and $\omega=5.25GHz$.

6.2 Self-biased cascode power stage

To overcome the breakdown voltage limitation problem of M2, a self-biased cascode transistor is proposed as shown in Fig.24(a), which it allows RF swing at G2. This enables us to design the PA such that both transistors experience the same maximum drain-gate

voltage. Consequently, we can have a larger signal swing at D2 before encountering hot carrier degradation.

Fig. 24. Operational waveforms of (a).Self-biased cascode amplifier (b).Voltage waveforms versus time for $V_G=0.8V$, $V_{in}=0.8\sin\omega t$, $R_b=0.75K\Omega$, $C_b=2.4$ pf, and $\omega=5.25GHz$.

The bias for G2 is provided by R_b - C_b network, for which no extra bondpad is required. The dc voltage applied to G2 is the same as the dc voltage applied to D2. The RF swing at D2 is attenuated by the low-pass nature of R_b - C_b network as shown in Fig.24(b). The values of R_b and C_b can be chosen for optimum performance and for equal gate-drain signal swings on M1 and M2. As G2 follows the RF variation of D2 in both positive and negative swings around its dc value, a non-optimal gain performance is obtained (compared with a cascode with RF ground at G2). However, as long as both M1 and M2 go from saturation into triode under large-signal operation, the maximum output power and PAE are not degraded. The effect of the self-biased concept is demonstrated in Fig.24(b). Here, the same dimensions of

the devices are used as for the case presented in Fig. 23(b). A reduction of more than 20% in the drain–gate voltage of M2 is actually obtained.

6.3 Boot-strapped cascode power stage

To further extend this idea, we can add a resistive-diode boosting so that the positive swing of G2 can be made larger than the negative swing as shown in Fig. 25(a). By choosing the value of R_d and the size of the diode connected transistor M3, we can specify the threshold voltage at which the R_d –M3 starts conducting and boosting the positive swing at G2. This extra path enables G2 to follow the rise in D2 with a smaller attenuation than the fall in D2. During this transient response, the average charge stored on C_b increases causing R_d –M3 to conduct for a smaller percentage of the duty cycle. The average voltage at G2 increases up to the point where R_d –M3 no longer conducts. In steady state, the R_d –M3 path is off and the positive and negative swings at G2 are equal. Fig. 25(b) shows the drain and gate voltages of transistor M2 versus time for different values of R_d . The voltage swing at D2 is not affected by R_d , and the peak-to-peak swing of V_{G2} depends on R_b – C_b and not R_d . However, as the value of R_d is reduced, the average voltage of V_{G2} increases. In Class-E PA design, the voltage swing can be about three times the supply voltage (with a larger positive swing than negative around supply). In this situation, the bootstrapped cascode configuration can be employed to have the same maximum voltage swings at gate–drain of M1 and M2. Therefore, a larger supply voltage can be applied, resulting in a higher output power. For Class-AB/B design, where the signal has roughly the same positive and negative swings around the supply voltage, the self-biased cascode provides the required swing on G2.

Fig. 25. (a). Bootstrapped cascode power stage. (b). Voltage waveforms.

7. Case Study–Implementation of a 5.25-GHz CMOS Cascode Power Amplifier for 802.11a WLAN

In the case study, we investigate a 5.25-GHz highly integrated CMOS class-AB power amplifier for IEEE 802.11a WLAN. The proposed power amplifier is implemented with a two gain-stage structure which is followed by an off-chip output matching circuit. Moreover, transistor-level compensation techniques are employed to improve the linearity. The power amplifier is designed with an on-chip input matching circuit while the output matching circuit translates the signal power from $50\text{-}\Omega$ to $20\text{-}\Omega$ load resistance. The measured results indicate over 20% power-added efficiency, over 20-dBm output power, and 28.6-dBm output IP3. All the specifications are based on $50\text{-}\Omega$ input impedance at 2.4V supply voltage.

7.1 Introduction

Integration with a CMOS process is the key challenge for the state-of-the-art systems-on-a-chip (SOC) design approach. Conventionally, wireless local area network (WLAN) has been implemented with a multi-chip approach. However, the integration of baseband and RF front-end circuits with a CMOS process is the most promising approach to achieve highly integrated level, low power consumption, and low cost for a WLAN system. A challenging functional block in designing a wireless communication transceiver is the power amplifier due to the trade-offs between supply voltage, output power, power efficiency, and linearity, which the problem may couple with spectrum efficiency and leading to an even more difficult dilemma.

In order to achieve a higher spectrum-efficiency, the new OFDM (Orthogonal Frequency Division Multiplexing) based WLAN standards use non-constant envelope modulation,

which the linearity of the power amplifier is a key parameter as it is closely related to power consumption and distortion. Moreover, class-AB power amplifiers are widely used in wireless transceiver design due to their high efficiency and relatively high linearity. Transistor-level compensation techniques to enhance the linearity of a CMOS power amplifier are investigated in this case study. On the other hand, cascode configuration has been employed to eliminate the effects of oxide breakdown voltage and hot carrier degradation, which allows the use of a higher supply voltage. A self-biased technique with thin-oxide MOS is presented, which it can relax the restriction due to the hot carrier degradation in power amplifiers and alleviate the conventional requirement of using thick-oxide transistors.

7.2 Implementation of a two-stage cascode differential power amplifier

Some transistor-level linearization techniques have been employed in the radio-frequency PA design including nonlinear capacitance cancellation in CMOS PA design, PMOS cancellation, parallel diode with a bias feed resistance, and varactor cancellation. In this case study, a diode linearizer as presented in Section 5.3 is integrated in the proposed class-AB PA design, which it can effectively reduce the gain compression and phase distortion. In order to increase the power gain of the CMOS PA and reduce the current required to charge and discharge the parasitic capacitors of these nodes, the inductor L_{tank} is employed across the differential cascode nodes between drain and source connections, which acts as a resonant tank at these nodes as shown in Fig. 21 of Section 5.4.

The two main issues in the design of power amplifiers in deep-submicron CMOS technologies, namely, the oxide breakdown and the hot carrier effect, which become even worse as the technology scales down. The oxide breakdown is a catastrophic effect and sets a limitation of the maximum signal swing on the drain. The hot carrier effect increases the threshold voltage and consequently degrades the performance of a device. To avoid hot carrier degradation, the operating voltage is usually based on dc/transient reliability tests. For production requirements, the voltage is 5%–10% above the maximum allowed supply voltage to ensure a product lifetime. For a 0.18- μm process, this leads to a maximum dc drain-to-gate voltage of approximately 2V.

Cascode configuration and thick-oxide transistors have been employed to eliminate the effects of oxide breakdown voltage and the hot carrier degradation, which allow the use of a higher supply voltage. Under large signal operation, the voltage swing across the gate and drain nodes of the common-gate transistor becomes larger than that of the common-source transistor. Therefore, the common-gate transistor becomes the bottleneck in terms of breakdown or hot carrier degradation. Since the characteristic of thick-oxide devices is equivalent to a device of 0.35- μm process, a combination of standard and thick-oxide devices (standard device for the common-source and thick-oxide device for the common-gate) can tolerate a much higher voltage, which was demonstrated in the implementation of a 900-MHz, 0.2- μm CMOS cascode power stage.

The power amplifier in this case study operates at 5.15GHz-5.35 GHz frequency band, the maximum output power level is over 20dBm, and drain efficiency is over 20%. Moreover, the power amplifier employs a NMOS device to compensate the nonlinear input capacitance variation. By taking advantage of the NMOS device, the nonlinear capacitance can be compensated to nearly constant in the input of the common source device, which in turn improves the linearity. Miller's capacitance effect has also been alleviated by the

employment of the two-stage cascode differential architecture. Furthermore, the fully differential topology can bring the advantages of even order harmonics suppression and better immunity against noise from power supply and the lossy substrate. Note that for a 0.18- μm CMOS technology, the cut-off frequency f_t exceeds 60GHz, the minimum noise figure NF_{min} is below 0.5dB and a threshold voltage of 0.4V, which is a promising technology to implement a high-frequency PA operating at the frequency band.

On the other hand, a self-biased cascode structure presented in Section 6.2 does not necessitate thick-oxide transistors since it can have a larger signal swing at node D2 before encountering hot carrier degradation and this structure is employed in our power amplifier design to alleviate the hot carrier effect.

(a). Matching Network with Bond-Wire and Pad

The bond-wire can be modeled with the series connection of an inductor and a resistor, which the corresponding inductance and resistance are about 0.8nH/mm and 0.16 Ω /nH, respectively for the diameter of 25- μm bond-wires. Moreover, constructed from a stack of metal6 (20kA in height), via5 (6kA), and metal5 (5.8kA) layers, the pad occupies an area of 80 $\times$ 80 μm^2 , which is equivalent to the series connection of a 625 Ω -resistor and a 0.0625pF-capacitor to ground. Therefore, the bond-wire and pad can be modeled with the equivalent circuit which can be easily matched with a π -type matching network.

(b). Driver Stage

The first stage of the power amplifier is configured at class-A operation to provide the sufficient gain and linearity for the design. The schematic of the stage is shown in Fig.26, which the center frequency is determined by the LC high-pass matching network constructed with L_1 , C_1 , L_2 , C_2 , and parasitic capacitors. L_1 , L_2 , C_{p3} , and C_{p4} perform the inter-stage impedance matching at 5.15GHz-5.35GHz.

Fig. 26. Schematic of the driver stage.

(c). Power Stage

Fig. 27 shows the second stage of the NMOS diode linearizer PA which is configured at class-AB operation to obtain sufficient power efficiency and linearity. The NMOS diode linearizer is constructed with Md_1 , R_3 , R_4 and Md_2 , R_5 , R_6 . The inductor L_t resonates with the parasitic capacitance of the cascode amplifier, which it can improve the intermodulation distortion (IMD) performance.

Fig. 27. Schematic of the power stage.

Due to large AC current swing of the power stage, we employ individual driver-stage and power-stage supply voltages ($VDD1$ and $VDD2$). Note that the interaction between the two supply voltages may lead to unstable operation. The pad can be modeled with a shunt connection of a resistor and a capacitor, and then series connection with an inductor. Fig.28 shows an output-matching network with an output pad.

Fig. 28. Schematic of output matching network.

7.3 Experimental results

The experimental test chip is designed and fabricated with the TSMC 0.18- μm single-poly-six-metal (1P6M) salicide CMOS technology. Fig.29 shows the chip microphotograph, which the chip area is $758\mu\text{m} \times 1741\mu\text{m}$ including the bonding pads. The active components are 1.8V NMOS devices to alleviate voltage stress. The transistors comprise the dimension of $320\mu\text{m} \times 0.18\mu\text{m}$ MOS finger cells.

Fig. 29. Chip microphotograph of the NMOS diode compensation PA.

The driver stage of the power amplifier employs a common-source amplifier with on-chip spiral inductors while the power-stage loads of the power amplifier employ a quarter-wave length transmission line to form an RF choke on PCB to reduce the loss of the output matching networks. The number of fingers of each stage is made large to reduce the polysilicon-gate resistance since the resistance can degrade the RF signal and increase noise. The output paths are the top thick metals to avoid voltage drop and electron migration problems. Output pads are located close to the output devices in order to eliminate extra unnecessary resistance and capacitance.

The internal large AC coupled capacitors are used between power supply buses and the ground buses to form RF virtual ground. The matching and symmetry should be arranged very carefully for the differential structure. Each device cell has dummy transistors on the edges to ensure the same environment of all MOS transistors and square metal-insulator-metal (MIM) capacitors with thin oxide are employed throughout the power amplifier. Moreover, the double guard rings around the spiral inductors prevent substrate noise from other circuits.

Fig. 30 is the measurement setup for the power amplifier, in which a single-ended 5.25-GHz signal is developed by the RF signal generator. The input balun converts a single-ended signal to differential output signals, and applies the signals to the device under test (DUT). The output balun converts the differential signals to a single-ended signal and delivers the resultant signal to the input terminal of spectrum analyzer to analyze the output fundamental power signal and harmonics.

During measurement, the bare die of the CMOS PA has been directly mounted to the ground plane of the lossy PCB to minimize the length of a bonding wire, which reduces the parasitic effects of commercial packages and alleviates the thermal effect. The dielectric

constant of the PCB used in this work was a standard FR4 process with a relative dielectric constant of 4.5.

Fig. 30. Measurement setup for the power amplifier.

Because the poor quality and large current tolerance ability of the standard spiral inductor in CMOS process, the final stage load inductor excludes from the chip. This test chip employs high-frequency inductors and capacitors as the power stage load matching network to improve the efficiency of the PA and overcome the large current issue. Fig.31 shows the measured output signal spectrum of the NMOS diode compensated PA, which it demonstrates a 16.5-dBm output power when the input power is -2dBm. Fig.32 shows the output power versus input power, which the measured P1dB is approximately 16.5dBm. Note that the measured data includes the cable, balun, PCB board, and pad losses for input and output ports and each port has about 4-dB power loss.

Fig. 31. Measured output power of NMOS diode compensated PA when input power is -2dBm.

Fig. 32. Output power versus input power and P1dB.

The power-added efficiency (PAE) is indicated in Fig.33. For a lower input power, the extra power losses from the measurement setup are less important since the power amplifier itself inherently has large power loss. By contrast, for a higher input power, however these extra power losses degrade the efficiency more seriously since the power loss of the power amplifier is smaller. Obviously, the measured PAE is 20.1% when the input power is -2dBm. In order to measure the linearity of the power amplifier, an IM3 two-tone test was performed. Two tones spaced at 160MHz have been applied to the input of the power amplifier. Fig.34 shows the measured output IP3 (OIP3) which is approximately 28.6dBm.

Fig. 33. Power-added efficiency versus input power.

Fig. 34. Measured output IP3.

Table 1 summarizes the measured key performance feature of the power amplifier, which shows comparable performance in terms of linearity and intermodulation distortion under the measurement setup.

Technology	TSMC 0.18-μ m 1P6M RF CMOS
Supply voltage	2.4V
Center frequency	5.25GHz
Maximum output power	20.9dBm
Power-added efficiency	20.1%
@Pout = 16 dBm	
Output P1dB	16.5dBm
Output IP3	28.6dBm
DC current of driver stage	44mA
DC current of power stage	112mA

Table 1. Measured performance summary

8. Conclusion

In this chapter, we have presented the design aspects of the class-AB linear power amplifier. The proposition of the linear power amplifier for high spectrum-efficiency communications in CMOS process technology is mainly due to the integration of a single-chip RF radio. The inherently theoretical high-power efficiency characteristic is especially suitable for wireless communication applications. Moreover, linearization enhancement techniques have also been investigated, which makes the power amplifier be practically employed in high spectrum-efficiency communications.

Finally, in the case study a 5.25-GHz, high-linearity, class-AB power amplifier has been investigated and integrated on a chip in 0.18- μm RF CMOS technology. The CMOS PA uses a NMOS diode to compensate the distortion of the PA. Requirements of the specification have been discussed and translated into circuit designs and simulation results. Experimental results indicate a good agreement with the compensation approach.

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Mobile and wireless communications applications have a clear impact on improving the humanity wellbeing. From cell phones to wireless internet to home and office devices, most of the applications are converted from wired into wireless communication. Smart and advanced wireless communication environments represent the future technology and evolutionary development step in homes, hospitals, industrial, vehicular and transportation systems. A very appealing research area in these environments has been the wireless ad hoc, sensor and mesh networks. These networks rely on ultra low powered processing nodes that sense surrounding environment temperature, pressure, humidity, motion or chemical hazards, etc. Moreover, the radio frequency (RF) transceiver nodes of such networks require the design of transmitter and receiver equipped with high performance building blocks including antennas, power and low noise amplifiers, mixers and voltage controlled oscillators. Nowadays, the researchers are facing several challenges to design such building blocks while complying with ultra low power consumption, small area and high performance constraints. CMOS technology represents an excellent candidate to facilitate the integration of the whole transceiver on a single chip. However, several challenges have to be tackled while designing and using nanoscale CMOS technologies and require innovative idea from researchers and circuits designers. While major researchers and applications have been focusing on RF wireless communication, optical wireless communication based system has started to draw some attention from researchers for a terrestrial system as well as for aerial and satellite terminals. This renewed interested in optical wireless communications is driven by several advantages such as no licensing requirements policy, no RF radiation hazards, and no need to dig up roads besides its large bandwidth and low power consumption. This second part of the book, Mobile and Wireless Communications: Key Technologies and Future Applications, covers the recent development in ad hoc and sensor networks, the implementation of state of the art of wireless transceivers building blocks and recent development on optical wireless communication systems. We hope that this book will be useful for students, researchers and practitioners in their research studies.

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