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Low-Power and Low-Voltage Analog-to-Digital Converters for wearable EEG systems

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1. Introduction

Electroencephalography (EEG) has traditionally placed a vital role in monitoring, diagnosis and treatment for certain clinical situations, such as epilepsy, syncope and sleep disorder; by measuring the patient's brainwaves (Casson et al., 2008). Recently, EEG has also merged as powerful tool for neuroscientist allowing the research of cognitive states and the enhancement task-related performance of an operative through computer mediated assistance (Erdogmus et al., 2005).

During monitoring electrodes are placed on scalp to detect the micro-Volt EEG signals that result outside the head due to the synchronised neurological action within the brain. In practice, long-term EEG monitoring is generally required either inpatient or ambulatory. The conventional EEG systems limit patient mobility due to bulk size because of the battery sized required for the long term operation of the constituent electronics. There is thus a strong need for development of lightweight, wearable and wireless EEG systems operation to enable long-term monitoring of patients in their everyday environment (Yates et al., 2007). In this way, wearable EEG is the evolution of ambulatory EEG units from the bulky, limited lifetime devices available today to small devices present only on the head that record the EEG for long time; however this method demands ultra-low power and low voltage circuit design because of the lifetime of the batteries.

One of the most power consuming building blocks of a wearable EEG front-end is the Analog to Digital Converter (ADC) required to process the signal in the digital domain. Therefore it is necessary an ultra-low power ADC (Yang & Sarpeshkar, 2006) for EEG applications.

This chapter presents the design of two extremely low power consumption ADCs that can be used for a wearable EEG system under a very low supply voltage environment. The architectures used for the converters are:

- A 10 bits second order Switched-Capacitor (SC) Sigma-Delta modulator.
- A 1.5-bit per stage 10-bit pipelined ADC.

To achieve both, the extremely low-power and the low voltage operation, a new design principle based on Quasi-Floating Gate (QFG) MOS transistors has been used. Moreover, the use of a class-AB operational amplifier (opamp) biased in weak inversion allows very low

power consumption achieving the high open-loop gain requirements. The implementations in CMOS technology of data converters for EEG systems presented in this chapter confirm the usefulness of the proposed techniques for low-voltage and low-power applications.

2. EEG signal processing and front-end description

Typical EEG signals provided by the electrodes placed on the scalp are in the range 2-500 μV over a bandwidth of 0.5-30 Hz (Binnie et al., 1982). Present ambulatory systems typically have at least 16 channels and operate for around a day without recharging. Wireless systems offer around 8 EEG channels and last for 12 hours. Sampling frequencies higher than 200 Hz are typically specified, nevertheless the trend in EEG systems is for higher sampling frequencies and more recording channels, being not uncommon currently for inpatient monitors offer sampling frequencies of 1 kHz or more. Modern inpatient systems for epilepsy diagnosis may offer 256 channels (Casson et al., 2008). Furthermore, to avoid spatial aliasing towards 600 channels are needed.

Implementation of a low-power EEG system is not an easy task because of the nature of the signals. The reason is that the scalp electrodes drift with time superimposing a low frequency signal in the order of tens of milivolts (Cooper et al., 1974) to the desired EEG one. Two strategies can be followed to deal with this type of signals:

1. Digitalize the EEG signal and the drift signal together and remove the second one digitally. This signal processing requires a very accurate ADC with more than 20 bits of resolution, which would be very power consuming.
2. Filter the drift signal out in the front-end. This second strategy relaxes the ADC resolution at expense of tightening the requirements of the previous instrumentation amplifier because it is difficult to filter such a low-frequency signal out without affecting the desired one. ADCs being presented in this chapter are thought for this signal processing strategy. Because of the extremely low-power consumption of the ADC, there is more power budget available for the design of the filtering instrumentation amplifier (Yates et al., 2007).

Fig. 1. shows the basic block diagram of the low-power low-voltage front-end for wearable EEG systems. The front-end is made up of:

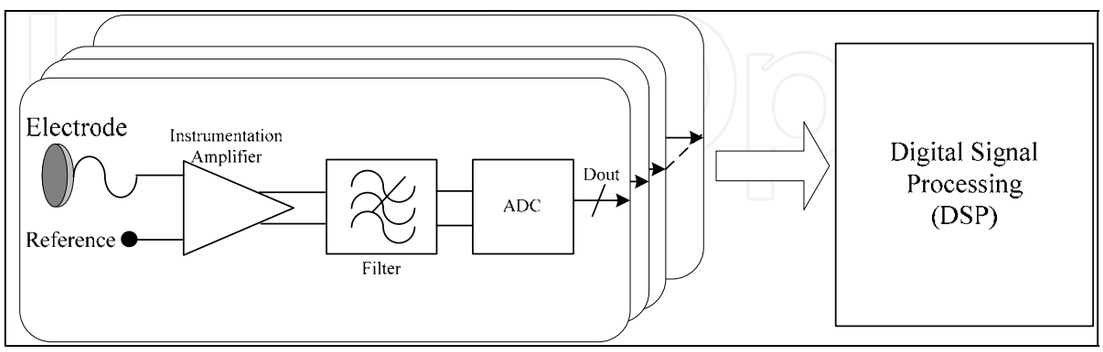


Fig. 1. Front-end for wearable EEG system.

1. An instrumentation amplifier. The instrumentation amplifier performs two tasks. It provides a gain of 175, which is required to accommodate the EEG signal to the

ADC input range. Simultaneously it provides high-pass filtering to remove undesired very low frequency signals hence reducing the effect of the electrode offset drift. Therefore it is possible the use of a moderate resolution ADC. In order to meet the noise specifications, chopper techniques are commonly used in the instrumentation amplifier (Menolfi & Huang, 1999). A chopper amplifier achieves exceptional noise performance and very low offset voltage by upconverting the signal before amplification through modulation with a square wave at chop frequency, f_{ch}. Ideally, the chop frequency is set to a frequency at which the flicker noise is negligible. After amplification at f_{ch} the signal is downconverted to baseband. However, the flicker noise and offset voltage are simultaneously upconverted to the chop frequency, where they can be filtered out (Yates & Rodriguez-Villegas, 2006).

2. An anti-aliasing filter**.**
3. A 10 bit ADC. The fact that the slowly-varying offset due to scalp electrodes' impedance drift is partially suppressed by the instrumentation amplifier allows relaxing the resolution requirements to only 10 bits.

If the volume of the overall device is assumed to be 1cm^3 and half of such volume is reserved for a battery of energy density of 200Wh/l (Casson et al., 2008). For an operation of 30 days without recharging the average power consumption must be less than 140μW. Currently, 20-32 channels EGG systems are preferred. This implies that average power consumption per channel must be less than 5-3μW. The estimated power consumption of the digital signal processing is around 40μW. The power consumption of the entire system is:

$$P = N \cdot P_{ch} + P_{DSP} = N \cdot \left(P_a + P_f + P_{ADC}\right) + P_{DSP} \quad (1)$$

where N is the number of channels, P_{ch}, P_a, P_f, P_{ADC} and P_{DSP} are the power consumption of the channel, instrumentation amplifier, anti-aliasing filter, ADC and DSP respectively. A good design guideline is to reverse 50-66% of the complete analog power consumption (P_{ch}) for the ADC. Thus, a suitable ADC power consumption would be in the range of 3.3-2.5μW per channel for a 20 channels system, and 2-1.5μW for a 32 channel system.

The general specifications for ADCs used in the proposed EEG front-end are summarized in Table 1.

Maximum input frequency	25-100Hz
ADC sampling frequency	>1kHz
Resolution	>9 bits
Input Voltage Range	725mV differential
Supply Voltage	as low as possible (i.e. 1.2V)
Maximum power consumption	3.3-1.5μW

Table 1. General specifications for ADCs used in the EEG front-end.

In this chapter two different 10-bit ADC implementations are presented using a low supply voltage (1.2V).

1. The first ADC is implemented by using a pipelined architecture. Typically such ADC architecture is chosen for intermediate sampling frequencies, but this chapter shows how it is also possible and worthwhile to use a pipelined architecture to design a power efficient ADC for EEG applications.
2. The second ADC uses a switched-capacitor (SC) sigma-delta (ΣΔ) architecture which is commonly used for biomedical applications (Goes et al., 2005), (Lee et al., 2005). The reduced number of operational amplifier of this architecture is an advantage for low-power specifications. However, the input signal bandwidth is limited due to the oversampling operation of ΣΔ ADCs.

Both ADCs have been designed using standard 0.5μm CMOS MOSIS technology. In this technology the MOS transistors have a relative high threshold voltage, V_{TP}=0.96V and V_{TN}=0.67V, which make increase the difficulty of achieve switch linearity and operational amplifiers open-loop gain requirements under a very low voltage supply with classical design techniques. Two strategies were adopted in order to solve these problems:

1. The use of CMOS switches based on quasi-floating gate transistors (QFG).
2. The use of sub-threshold biased class-AB operational amplifiers.

3. QFG transistors

A fundamental issue in SC circuits operating with a very low voltage supply is that not enough overdrive voltage can be provided to the gates of transistors acting as switches (Crols & Steyaert, 1994). In this way, the signal swing and linearity is limited. CMOS switches based on quasi-floating gate transistors are an alternative to the well known clock-boosting techniques and bootstrapped switches (Ramírez-Angulo et al., 2004).

A QFG transistor is a MOS transistor with its gate terminal weakly connected to a DC voltage through a very large resistor. This resistor is used to set the DC operating point of the gate terminal of the input MOS transistor. The resistor can be implemented by means of a MOS transistor in cut-off region.

Fig. 2. shows a QFG nMOS transistor with multiple inputs. A simple ac analysis reveals that the ac voltage at the quasi-floating gate is given by:

$$V_G = \frac{sR_{leak}}{1+sR_{leak}C_T}\cdot\left(\sum_{j=1}^{N} C_j V_j + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B\right) \quad (2)$$

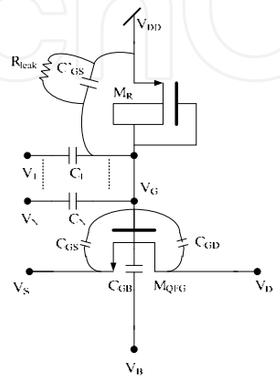


Fig. 2. QFG nMOS transistor.

where C_T is the total capacitance:

$$C_T = \sum_{j=1}^{N} C_j + C_{GS} + C_{GD} + C_{GB} + C'_{GD} \tag{3}$$

The factor $sR_{leak}/(1+sR_{leak}C_T)$ in (2), represents a high-pass filter. In this way, low-frequencies components of the input are filtered out with a cut-off frequency $1/(1+sR_{leak}C_T)$, which can be very low. Therefore, even for very low frequencies, (2) becomes a weighted averaging of the ac input voltages determined by capacitor ratios, plus some parasitic terms. The pull-up resistor R_{leak} sets the gate to a dc voltage equals to the positive rail, to which an ac voltage given by (2) is superimposed. Hence, the gate voltage can become higher than V_{DD}. An exact value of R_{leak} is not required, and its temperature and voltage dependence are not important, provided that R_{leak} value remains large enough not to influence the circuit operation at the lowest frequency required.

3.1 Rail to rail CMOS switch based on quasi-floating gate transistors

In low-voltage SC circuits there are some critical switches that need rail to rail signal swing operation. As the supply voltage is low, not enough overdrive is provided to the gates of transistors used as switches to be turned on over the whole signal range. A simple and very power efficient solution to this problem is the use of a QFG transistor as low-voltage rail-to-rail switch.

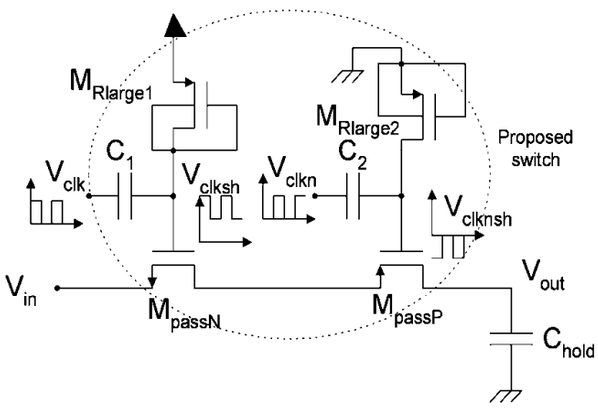


Fig. 3. A low voltage rail-to-rail T/H with a switch based on two complementary QFG transistors.

Fig. 3. shows how a T/H circuit is implemented using a low voltage analog switch based on two QFG transistors (Muñoz et al., 2003). The two complementary QFG transistors, M_{passN} and M_{passP}, are connected in series in order to get rail-to-rail operation.

The gate of M_{passN} is weakly tied to V_{DD} through a large nonlinear resistor implemented by transistor $M_{Rlarge1}$. The gate is also coupled to the clock signal through a small valued capacitor, C_1, so that the clock signal is transferred to the quasi-floating gate. The capacitor performs a level shift of approximately V_{DD}, which allows switching under very low-voltage

restrictions. Note that the switch implemented by M_{passN} is not rail-to-rail because it is not possible to turn off the transistor for input signals near the negative rail. The rail-to-rail operation is achieved thanks to QFG transistor M_{passP} (driven by a complementary clock signal).

3.2 Low-voltage class-AB Operational Amplifier

At low supply voltages the signal dynamic range is reduced and makes not possible the use cascode transistors to get high-gain stages. In this context, two stage class-AB op-amps are the natural choice since they can have low power consumption, rail-to-rail output swing and high gain.

Fig. 4. shows the architecture of the operational amplifiers used in both implemented ADCs (Ramírez-Angulo et al., 2006).

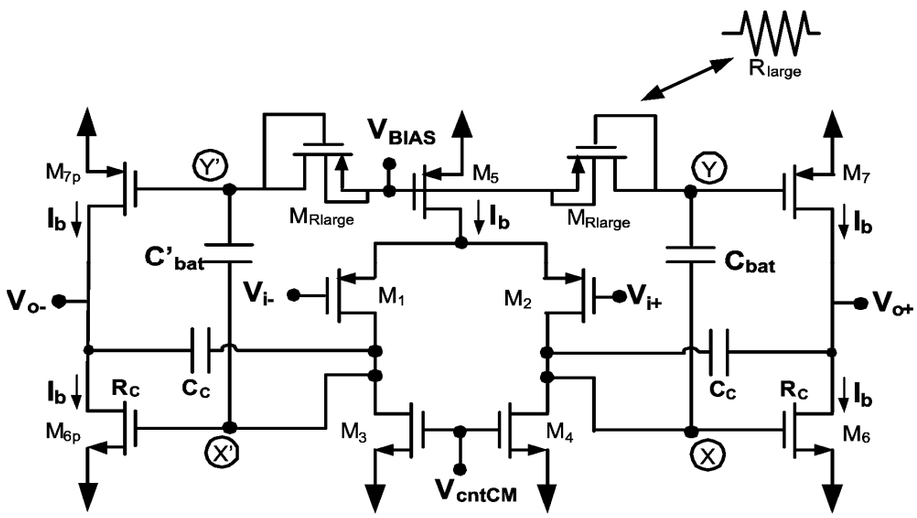


Fig. 4. Implementation of a fully differential Class-AB output stage using QFG transistors.

QFG transistors are used (M_7 and M_{7p}) with the large valued resistor implemented by a minimum size diode connected pMOS transistor M_{Rlarge} , and a small valued capacitor C_{bat}. Under quiescent conditions and given that no DC current flows through M_{Rlarge} the voltage at the gate of M7 is the same as at the gate of M_5 so that the quiescent current in M_5 and M_7 is well controlled and has the same value I_b. Transistor M_6 is commonly sized with W/L dimensions twice as large as those of M_3, M_4 so that the quiescent current in M_6 has also a value I_b. During dynamic operation, when the output of the op-amp is slewing, the voltage at node X is subject to a large change. Given that capacitor C_{bat} can not discharge/charge rapidly through M_{Rlarge} it acts as a floating battery and transfers the voltage variations at node X to node Y. This provides class AB (push pull) operation to the output stage. No additional circuitry to control the desired value of the quiescent output current is necessary due to the large resistor. The value of C_{bat} can be small as transistor M_{Rlarge} is intended to operate as a very large resistive element. The output stage has low supply requirements since it can operate with a supply voltage close to a transistor's threshold voltage:

$$V_{DD_{min}} = V_{GS6} + V_{SDsat2} + V_{SDsat5} \quad (4)$$

Amplifiers have been designed with transistors biased in weak inversion in order to minimize the power consumption and to achieve open-loop gain requirements. Bias current and transistor sizes are set to accomplish the settling requirements. An additional advantage of the used operational amplifier is that it presents enhanced phase margin and higher unity gain frequency as both transistors M6 and M7are active in the class-AB output stage.

4. Design of a low-power low-voltage 10-bit Pipelined ADC for wearable EEG systems

Multi-stage pipelined ADCs are one of the most popular architecture for high-speed applications. They consist of several cascaded stages, called multiplying digital-to-analog converter (MDAC), which contains a sample-and-hold (S/H), a low resolution ADC and a digital-to-analog converter (DAC). A digital delay line is required for output synchronisation to assure the correct operation.

The purpose of this section is to show how it is possible to use a classical power-consuming high-speed ADC architecture for low-power EEG applications by means of a deep understanding of pipelined ADC architecture and design techniques like quasi-static gate transistors. The target is to use this ADC for wearable EEG systems with more than 20 channels and performing simultaneously the analog-to-digital conversion of more than one channel.

Fig. 5 shows block diagram of the presented pipelined ADC. The whole system uses fully-differential architecture without a dedicated front-end S/H and consists of a cascade of 9 fully-differential MDACs stages with 1.5 bits of resolution at 4 kHz of sampling frequency. The last stage is just a 2-bit resolution flash ADC. Bit redundancy is used in order to correct offset errors in the digital domain. Each MDAC stage composes of a S/H, a low-resolution analog-to-digital sub-converter (sub-ADC), a digital-to-analog sub-converter (sub-DAC), and a gain block.

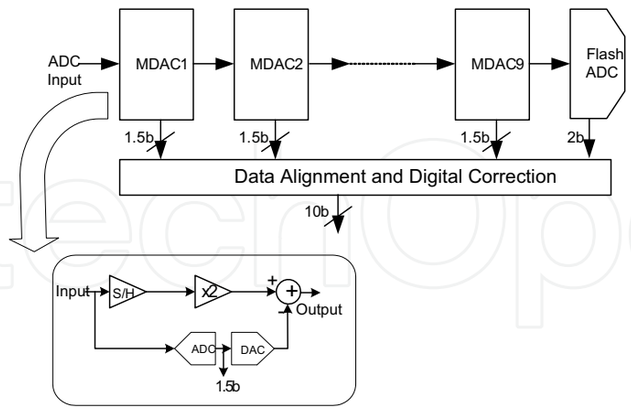


Fig. 5. 10-bit Pipelined ADC architecture.

Fig. 6. shows the architecture of the MDAC stage. In order to achieve low-power and low-voltage restrictions, the input common mode of the operational amplifier is different to the common mode of the input signal. The MDAC stage has two operation phases called *sampling phase* and *amplification phase*. During the *sampling phase* the input of the MDAC is

sampled and stored in both capacitors C_f and C_s. The difference between the input and output common mode of the operational amplifier together with the offset and flicker noise, which were stored in C_m during the previous *amplification phase*, is corrected. During the amplification phase the sub-ADC provides the output bits and decides which signal must be supplied by the multiplexer.

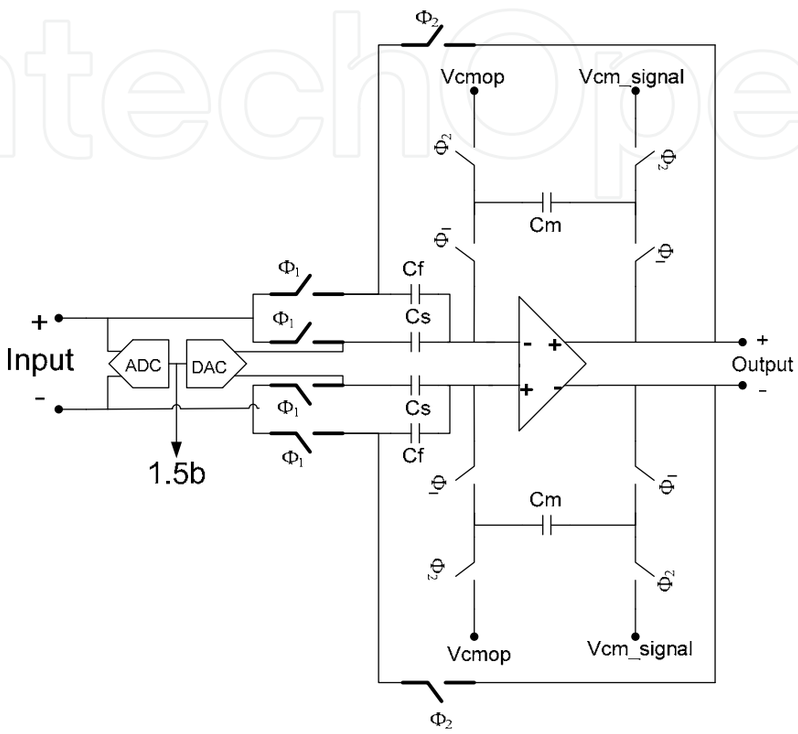


Fig. 6. MDAC architecture (critical switches are highlighted).

The critical switches (that are highlighted in Fig. 6) need rail-to-rail signal swing operation and they were implemented, as it was mentioned before, by means of QFG transistors of Fig. 3. The sampled input is amplified by the factor $1+(C_f/C_s)$, called gain of the MDAC, by connecting the top plate of the capacitor C with the output of the operational amplifier. In a traditional 1.5-bit MDAC stage both capacitor have the same value, so the MDAC has a gain of 2. The transfer function of a MDAC stage is given by:

$$\mathrm{Vout} = \left(1 + \frac{C_f}{C_s}\right) \cdot \mathrm{Vin} + \left(\frac{C_f}{C_s}\right) \cdot \mathrm{D} \cdot \mathrm{Vref} \tag{5}$$

where Vref is the reference voltage of the pipelined ADC, Vin the input voltage of the MDAC stage, and:

$$\mathrm{D} = \begin{cases} -1 & \text{if} \quad \mathrm{Vin} > \mathrm{Vref}/4 \\ 0 & \text{if} \quad -\mathrm{Verf}/4 \le \mathrm{Vin} \le \mathrm{Vref}/4 \\ 1 & \text{if} \quad \mathrm{Vin} < \mathrm{Vref}/4 \end{cases} \tag{6}$$

Only two comparators are required to implement the sub-ADC in a 1.5-bit MDAC stage. The output bits of the MDACs stages are aligned and digitally processed obtaining the final 10-bit output data. Bit redundancy is used in order to correct the comparator offsets of MDAC stages in the digital domain (Gorbatenko, 1966). Due to this redundancy, low resolution comparators can be used with offset up to $\pm\, \mathrm{Vref}\,/2^{B+1}$, being B the bit resolution of the sub-ADC (Cho & Gray, 1994).

The correct operation of a pipelined ADC is fully dependent on which value the output voltage of each MDAC stage is settled at the end of the amplification phase which is processed by next pipeline stage. Errors in the MDAC output voltage limit the performance of the ADC. The maximum voltage error allowed at the output of an MDAC, without degradation in the ADC performance, specifies the MDAC building-blocks requirements. In this way, a deep understanding of the errors at the MDAC output voltage arises in knowledge regarding power saving in the right stage. In this section the error sources in pipelined ADC are described and such description is used to implement a behavioural simulator to obtain the requirements of the building-block of each MDAC stage of the ADC for a required resolution and sampling frequency.

The errors concerning to the value of the output voltage of a MDAC stage can be classified into three different groups:

- Static errors: these errors imply that the output voltage value of the MDAC differs, timely independent, from the ideal one. The dynamic of the MDAC stage is not considered.
- Dynamic errors: these are errors which imply that the output voltage of the MDAC does not achieve the static value in time. In this group, the dynamic of the MDAC is only considered as unique error source.
- Noise

4.1 Static errors in MDAC stages

The first important static error source in pipelined ADCs is the mismatch between the capacitors C_f, C_s of each stage. Considering a mismatch δC between both capacitors, C_f=C, Cs/C_f=1+δC; an error term (ε) appears at the residue voltage in (5):

$$Vout = \left(1 + \frac{C_s}{C_f}\right) \cdot Vin + \left(\frac{C_s}{C_f}\right) \cdot D \cdot Vref + \varepsilon \tag{7}$$

where the error term ε is:

$$\varepsilon = \delta C \cdot (\mathrm{Vin} + \mathrm{D} \cdot \mathrm{Vref}) \tag{8}$$

Another source of error it the finite gain of the operational amplifier. Assuming an open-loop gain of A_0 for the operational amplifier of the MDAC stage the error term of (7) becomes:

$$\varepsilon = \varepsilon_{\mathrm{mismatch}} - \frac{(2+\delta C)}{A_0} \cdot \left(\mathrm{Vout}_{\mathrm{ideal}} + \varepsilon_{\mathrm{mismatch}}\right) \tag{9}$$

where $\varepsilon_{mismatch}$ is the error term written in (8) and $Vout_{ideal}$ is the output voltage of the MDAC stage at the end of the amplification phase when no error sources are considered. This equation shows that low open-loop gain of the operational amplifier increases the errors produced by the capacitor mismatch.

4.2 Dynamic errors in MDAC stages

Error sources related to the speed of the MDAC stage are considered in this section. The first dynamic error source which must be considered is the on-resistance of the switches, which are part of the switch capacitor network of the MDAC. During the sampling phase, the on-resistance of the input switches, together with the capacitors; introduces an error in the sampled input voltage (Carner & Un-Ku). The sampled input voltage at the end of the sampling phase is:

$$Vin_{sampled} = Vin \cdot (1 - \exp(-Ts / 2R_{ON}C)) \tag{10}$$

where R_{ON} and C are the switch on-resistance and capacitance where the analog input signal is sampled, and Ts the clock period. In order to achieve good enough settling, the time constant $R_{ON} \cdot C$ is designed to be several time smaller than the clock period. The drawback is that the equivalent noise bandwidth becomes larger than half of the sampling frequency and aliasing of the sampled noise spectra takes place. Thus, the value of the allowed switch on-resistance is defined in terms of the maximum error allowed in the sampled voltage:

$$\varepsilon_{sampled} = Vin - Vin_{sampled} < \frac{1}{2^{N_{stage}}} \Rightarrow R_{ON} < \frac{Ts}{2 \cdot C \cdot N_{stage} \cdot \ln(2)} \tag{11}$$

where N_{stage} is the required resolution of the stage where the switch is used.
Other dynamic error sources are related to the speed of the operational amplifier. In this way, the slew-rate (SR) of the operational amplifier limits the linear settling time, and a finite unity-gain frequency (GBW) makes the operational amplifier slower. The single-pole model of the MDAC stage shows that the output voltage at the end of the amplification phase is:

$$Vout = Vout_{static} \cdot (1 - \exp(-t_{set} \cdot 2\pi \cdot GBW \cdot \beta)) = Vout_{static}(1 + \varepsilon_{dynamic}) \tag{12}$$

where $Vout_{static}$ is the output voltage when only static error sources are considered (7), β is the feedback factor of the MDAC, and t_{set} is the linear settling time:

$$t_{set} = \frac{Ts}{2} - t_{SR} = \frac{Ts}{2} - \frac{(Vout_{static})}{SR} + \frac{1}{2\pi \cdot GBW \cdot \beta} \tag{13}$$

A two-pole system model for the complete MDAC describes a more accurately the settling behaviour. Considering that the system has a phase margin $\Phi_{m,}$ the damping factor is:

$$\zeta = \frac{1}{2 \cdot \sqrt{\cos(\Phi_m)}} \sqrt{1 - \cos^2(\Phi_m)} \tag{14}$$

and the natural frequency of the system is:

$$\omega_0 = \frac{2\pi \cdot GBW \cdot \beta}{\cos(\Phi_m)} \tag{15}$$

In this way, if $\zeta<1$, the MDAC output voltage at the end of the amplification phase is (Chuang, 1982):

$$\begin{aligned} Vout &\approx V_{SR} + (Vout_{static} - V_{SR}) \cdot (1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\omega_0 \cdot \zeta \cdot t_{set}} \sin(\sqrt{1-\zeta^2}\,\omega_0 \cdot t_{set} + \phi)) \\ &\approx Vout_{static} \cdot \left(1 - \frac{SR}{2\pi \cdot GBW \cdot Vout_{static}}\right) \end{aligned} \tag{16}$$

However, if $\zeta>1$, the MDAC output voltage at the end of the amplification phase is:

$$\begin{aligned} Vout \approx\ & Vout_{static}\left(1 - \frac{1}{2\sqrt{\zeta^2-1}} \cdot \left(\frac{e^{-\omega_0 \cdot \zeta \cdot t_{set} \cdot a}}{a} - \frac{e^{-\omega_0 \cdot \zeta \cdot t_{set} \cdot b}}{b}\right)\right) + \\ & + V_{SR} \cdot \left(\frac{1}{2\sqrt{\zeta^2-1}} \cdot \left(\frac{e^{-\omega_0 \cdot \zeta \cdot t_{set} \cdot a}}{a} - \frac{e^{-\omega_0 \cdot \zeta \cdot t_{set} \cdot b}}{b}\right)\right) \\ & a = \zeta - \sqrt{\zeta^2-1} \\ & b = \zeta + \sqrt{\zeta^2-1} \end{aligned} \tag{17}$$

where V_{SR}, in (16) and (17), is the MDAC output voltage at the end of the slew-rate time:

$$V_{SR} = \frac{A_0 \cdot SR}{2\pi \cdot GBW}\left(1 - e^{-2\pi \cdot GBW \cdot t_{SR}/A_0}\right) \tag{18}$$

Other dynamic error sources are charge injection produced by the switches and clock feedthrough. Errors produced by charge injection can be minimized using dummy transistors in the switches. In addition, both errors are reduced using small transistor in the switches. The errors produced by charge injection and clock feedthrough can be modeled as a common mode offset in fully-differential switched capacitor circuits. This common mode offset is reduced by the Common Mode Rejection Ratio (CMRR) of the system.
Considering the whole error sources in an MDAC stage, the output voltage at the end of the amplification phase can be written as:

$$Vout = Vout_{ideal}(1 + \varepsilon_{static} + \varepsilon_{dynamic} + \varepsilon_{static} \cdot \varepsilon_{dynamic}) = Vout_{ideal}(1 + \varepsilon_{total}) \tag{19}$$

This total error worsens the signal-to-noise ratio (SNR) and will produce total harmonic distortion (THD) of the pipelined ADC. The total error of a MDAC stage can be referred to the input of the ADC. In this way, if the total error of each MDAC is referred to the ADC input, the effective number of bits (ENOB) of the pipelined ADC is:

$$ENOB = \left(20\log\left(\frac{V_{FS}}{2 \cdot \sum_{j=1}^{N} \prod_{i=1}^{j} \varepsilon_{total\,j} / G_i} \right) - 1.76 \right) / 6.02 \tag{20}$$

where V_{FS} is the ADC full-scale, N the number of stages of the ADC, ε_{totalj} the total relative error of the stage "j" and G_i the ideal gain of the stage "i".

4.3 Noise in MDAC stages

The noise in each stage of the pipeline ADC is produced by the switches, the operational amplifier, and the reference voltage generator. As it has been described in the previous section, the unity gain frequency of the operational amplifier and the inverse of the *R C* time must be several times larger than the sampling frequency. The noise suffers from aliasing because the equivalent noise bandwidth, of the sampling network and the operational amplifier, is larger than the Nyquist frequency. However, a MDAC stage has a gain higher than unity which implies that noise contributions to the equivalent input noise are progressively reduced from the first stage to the last stage. In this way, the total input equivalent noise of the MDAC stages is:

$$\overline{Vin_n} = \sqrt{\sum_{i=1}^{N} \prod_{j=1}^{N} \frac{\overline{Von_i}^2}{Gj^2}} \tag{21}$$

$\overline{Von_i}$ being the total output noise of the MDAC stage-*i*. The total output noise of an MDAC stage is the sum of the output referred noise power in sampling and amplification phase. The total output noise of an MDAC is:

$$\overline{Von}^2 = \frac{G^2 kT}{C_{MDAC}} + 4ktR_{ON}BWn_{OPA} + Sn_{OPA}BWn_{OPA} + SnrBWn_{ref} \tag{22}$$

where k is the Boltzmann constant, *T* is the temperature, C is the sum of the capacitance connected to the analog input during the sampling phase, R_{ON} is the on-resistance of the switches connected to the output during the amplification phase, Sn_{OPA} is the output noise spectral density of the operational amplifier, Snr is the noise spectral density of the reference voltage generator, BWn is the equivalent noise bandwidth of the operational amplifier and BWn is the minimum between the equivalent noise bandwidth of the operational

amplifier and the equivalent noise bandwidth of the amplifier which generates the reference voltages.

The complete equivalent input noise power of the whole pipeline ADC is the sum of the equivalent input noise power of the MDAC stages plus the equivalent input noise power of the S/H circuit. Another important noise source in pipeline ADC is the clock jitter. The clock jitter is originated by the phase noise of the clock generator. The noise power produced by the clock jitter when a sinusoidal signal with half full-scale amplitude is:

$$\overline{Vn_{jitter}}^2 = \left(\pi \cdot V_{FS} \cdot f_{in} \cdot \sigma_{jitter}\right)^2 / 2 \quad (23)$$

f_{in} being the input signal frequency, σ_{jitter} the sampling jitter standard deviation of the clock signal.

4.4 Behavioral simulation results

Statistical behavioral simulations were done using MATLAB by means of the equations presented in the previous section to get the minimum restriction of the building blocks and considering the low-power consumption requirement. These behavioral simulations provide the maximum capacitor mismatch (and thus the minimum capacitor values), the open-loop and unity-gain frequency for the operational amplifiers as well as noise restrictions for the reference voltages generator. These basic specifications are summarized in Table 2:

Stage	Capacitor Mismatch (5σ%)	Open Loop Gain(dB)	GBW (kHz)
1	0.5	76	24
2	0.7	73	22
3	1.4	70	21
4	2.25	68	20
5	3.9	64	19
6	6.5	60	18
7	12	58	16
8	21	55	15
9	25	48	10

Table 2. Statistical behavioral simulation results.

4.5. Implementation details

Due to low-voltage supply the use of cascade transistor is not possible to achieve high enough open-loop gain. In this way, only classical two stage architectures can be implemented. In order to increase the linearity of the output stage and the open-loop gain, class-AB output stages have been used. The architecture presented in section 4, Fig. 4., was used for each opamp of the pipelined ADC and following the requirements presented in Table 2. As it was also mentioned before, the transistors of the opamp are biased in weak inversion in order to achieve the open-loop gain requirements with the minimum power consumption.

The sub-ADC, required in each MDAC stage, was implemented by means of two SC comparators, Fig. 7. The SC comparator operates on two non-overlapping clock phases. Thus, during the sampling phase, the analog input voltage is sampled in the capacitors 3C and *C*, while the latch is reset. During the comparison phase, the comparator compares the sampled analog input with the previously sampled reference voltage. The latch provides the digital output whereas the switched capacitor network samples the reference voltage in the capacitor *C* for the following comparison.

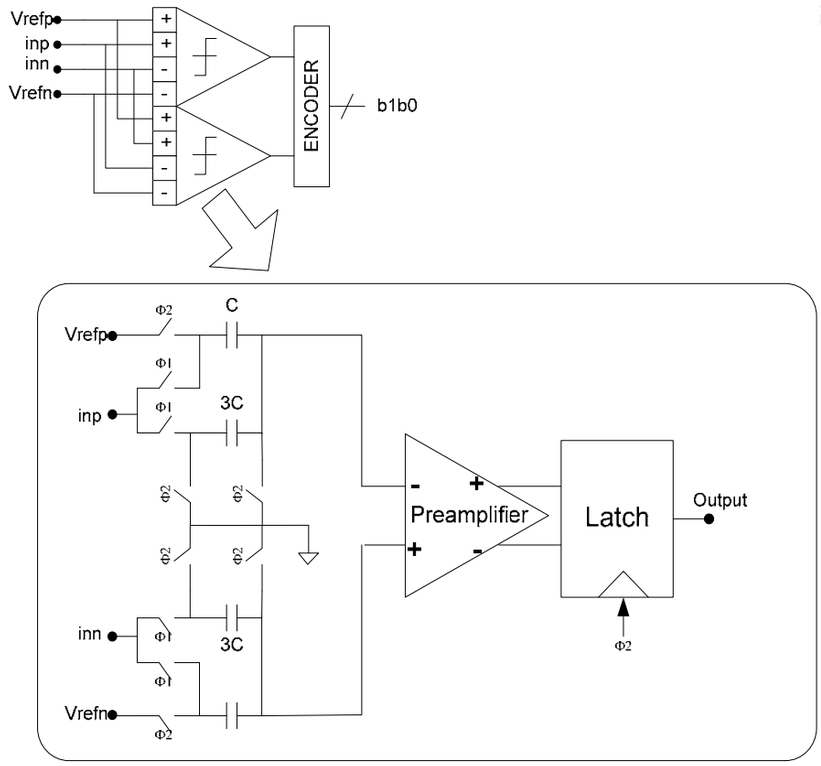


Fig. 7. Sub-ADC architecture.

The ADC was designed using an AMI (MOSIS) 0.5µm CMOS technology with PMOS and NMOS threshold voltages of about V_{TP}=-0.96V and V_{TN}=0.67V respectively. Table 3 summarizes the obtained post-layout simulation results of the complete pipelined ADC when a sinusoidal input signal of a -1dBFS and 93.75Hz is applied. The following figure of merit (FOM) was used:

$$FOM = \frac{P}{2^n f_n} \tag{24}$$

where n is the number of bits, P is the power consumption in Watts and f_n is the Nyquist frequency in Hz.

Sampling Rate	4kS/s
SNR (input 93.75Hz, 0.645Vpp)	61.5dB
THD (input 93.75Hz, 0.645Vpp)	-75.9dB
SINAD (input 93.75Hz, 0.645Vpp)	60.76dB
ENOB	9.8bits
Power Consumption	1.5μW
FOM	0.84pJ/state

Table 3. Simulation results.

Fig. 7. shows the spectrum of the reconstructed analog signal from the digital output bits of the pipelined ADC.
Simulation results are provided which shows 9.8 bits of resolution with 1.2 V supply voltage and only a power consumption of 1.5μW. The power efficiency is of 0.84pJ/state, being the most energy efficient converter of all the biomedical ADCs except (Yang et al., 2006).

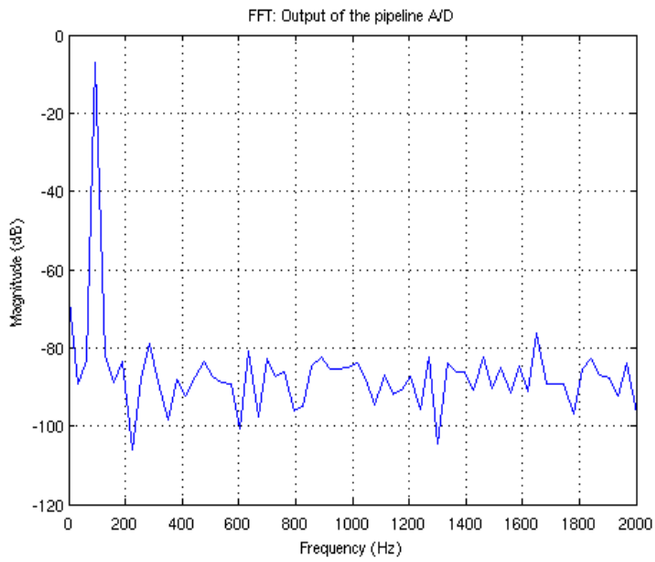


Fig. 8. Simulation results.

5. A 10-bit SC-ΣΔ modulator for EEG applications

Oversampling ΣΔ ADCs are based on the principle that the conversion error can be high-pass filtered and later remove by digital filters. The requirements on the analog parts are relaxed and high-resolutions can be achieved. The drawback is the relative small input signal bandwidth due to oversampling. A ΣΔ modulator consists of an analog filter, continuous or discrete time, and a coarse quantizer enclosed in a feedback loop. Together with the filter, the feedback loop acts to attenuate the quantization noise at low frequency while emphasizing the high frequency noise**.** Thus, the quantization noise is high-pass filtered while the input signal is only delayed. The high frequency noise can be removed by using digital low-pass filter (decimation), and a low-noise output signal is achieved.

A classical implementation of a single-bit second order SC-ΣΔ modulator is shown in Fig. 9. The most important building block in this architecture is the summing integrator.

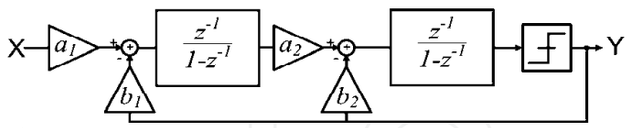


Fig. 9. Second-order discrete-time ΣΔ modulator.

The remaining building blocks in the analogy portion of the modulator are comparator and 1-bit DAC. The comparator circuit acts as a 1-bit ADC that maps its input into one of two digital output codes. The two digital output codes are then mapped back into analog levels by the DAC. If the two output codes of the comparator are defined as ±1/2, then the DAC, neglecting DAC, can be represented simply by gain block.

The ideal output of the second order ΣΔ modulator, when $b_2=2a_1a_2$ and $b_1=a_1$, which guarantee the loop stability; is described by:

$$Y(z) = z^{-2}X(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{25}$$

where E(z) is the quantization noise in the quantizer and X(z) the input signal. Component mismatch, finite open-loop gain of the opamps, thermal noise and incomplete settling are the most important error sources in ΣΔ modulators which degrade the overall ADC performance. As it was previously mentioned, the most important building block of a ΣΔ modulator is the integrator. In this way, the error sources in such block must to be considered. The equation (20) corresponds to the following transfer function for an integrator:

$$H(z) = \frac{a_1 z^{-1}}{1 - z^{-1}} \tag{26}$$

where a_1 is the gain preceding the input to the integrator. Deviations in a_1 from its nominal value in the first integrator alter the noise shaping function of the modulator changing the ADC performance (Boser & Wooley, 1988). In SC ΣΔ modulators, these deviations are mainly a consequence of capacitor mismatch. Larger a_1 means higher gain in the forward path of the modulator and consequently greater attenuation of the quantization noise. However, if a1 is too large (a_1>0.6), the signal amplitudes at the integrator outputs increase rapidly and the system becomes unstable.

The ideal integrator DC gain is infinite. However, due to circuit constrains, the integrator DC gain is limited. This effect is called "integrator leak" and implies that only a fraction "P" of the previous output of the integrator is added to each new input sample. In this way, the DC gain of the integrator becomes:

$$H_0 = \frac{a_1}{1 - P} \tag{27}$$

and the new integrator transfer function:

$$H(z) = \frac{a_1 z^{-1}}{1 - P z^{-1}} \tag{28}$$

The effect of the integrator leak is that limited gain at low frequencies reduces the attenuation of the quantization noise in the baseband increasing the in-band quantization noise.
In a general form, the in-band error power of a ΣΔ modulator can be expressed as (Medeiro et al., 1999):

$$P_{total} = P_Q + P_{noise} + P_{nl} + P_{set} \tag{29}$$

where P_Q is the quantization error, P_{noise} the noise circuit error, P_{nl} the non-linearity error and P_{set} the incomplete settling error. The design of the ADC can be made in such that quantization error is the dominant error source:

$$P_{noise} + P_{nl} + P_{set} << \frac{1}{12} \cdot \left[\frac{2 \cdot Vref}{2^B - 1} \right] \cdot \frac{\pi^{2L}}{(2 \cdot L + 1) \cdot M^{2L+1}} \tag{30}$$

where Vref is the reference voltage, L the modulator order and M the oversampling ratio. Every doubling of the sampling rate will provide L + 0.5 extra bits. The resolution can be increased by increasing the quantizator resolution and the modulator order. A problem with increasing the resolution of the quantizer is that the nonlinearities in the DACs will directly limit the ADC performance. Increasing the modulator order makes the stability of the loop more difficult, especially for order higher than 2.
Usually, the condition expressed in (25) implies a high amount of current consumption. Instead is more efficient to make the design such that $P_Q \cong P_{noise} + P_{nl} + P_{set}$.
In order to obtain an optimum design the following consideration were taken into account:

1. The value of the sampling capacitor at the modulator front-end is selected so that the error due to quantization noise and circuit noise is smaller than the maximum allowed in-band error. The amplifier noise, the switches noise and kT/C noise are the main contributor to the overall circuit noise (P_{noise}).
2. The error contribution due to incomplete settling is made a non-limiting factor by means of a high enough open-loop gain and GBW of the opamps. Anyway, the settling must not be limited by the slew-rate of the opamps. In addition, too high GBW will end ups with unnecessary extra power consumption. The GBW of the operational amplifiers must often be at least an order of magnitude greater than the sampling frequency. However, simulations show that the GBW of the operational amplifiers can be lower (Giustolisi. & Palumbo,2003). A good compromise for the GBW of the operational amplifiers is (Boser & Wooley, 1988):

$$GBW \geq \frac{1 + a_1}{\pi} \cdot f_s \tag{31}$$

3. Critical design parameter of the quantizer implemented by means of comparators must be considered. The speed of the comparator must be high enough for the desired sampling rate, and input offset, input referred noise and hysteresis must be low enough to not degrade the ADC performance.

5.1 ADC architecture and building blocks.

The second ADC implementation that is described in this chapter for EEG purposes is a 10-bit SC-ΣΔ modulator operating with a sampling frequency of 3.2 kHz and a full-scale range of 0.725 V (Lopez-Morillo et al., 2008). A simple and power efficient architecture for high resolution ADCs in the range of biomedical signals is the classical second-order ΣΔ modulator (Fig. 9). The main advantages of this architecture are simplicity, low sensitivity to component mismatch and stability.

System simulations have been performed using MATLAB/SIMULINK based on the models developed on (Boser & Wooley, 1988) and (Rabii & Wooly, 1999). As a result of these simulations (including the main non-idealities such as finite DC gain, bandwidth, and slew-rate of the amplifiers) a set of specifications for the most important building blocks have been obtained. These specifications are summarized in Table 2.

General Specifications	Oversampling ratio	64
	Sampling frequency	3.2kHz
Integrators' coefficients	a_1,b_1	0.25
	a_2	0.5
	b_2	0.25
First integrator's opamp	Output-Swing	2Vpp
	Slew-rate (SR)	15V/ms
	Unity-gain frequency	8kHz
	DC gain	30dB
Clock	Jitter	$0.1ms_{rms}$
Capacitor values	C_{s1}	125fF
	C_{cds}	500fF
	C_{i1}	500fF
	C_{s2}	50fF
	C_{i2}	200fF

Table 4. Specifications for building blocks.

Behavioral simulations show a Dynamic Range (DR) of 72dB with an oversampling ratio of 64, which is enough to achieve the 10 bit resolution. In order to get an unconditionally stable modulator and to maximize the integrators output swing, the coefficients have been chosen as $a_1=b_1=b_2=0.25$ and $a_2=0.5$ (Rabii & Wooly, 1999).

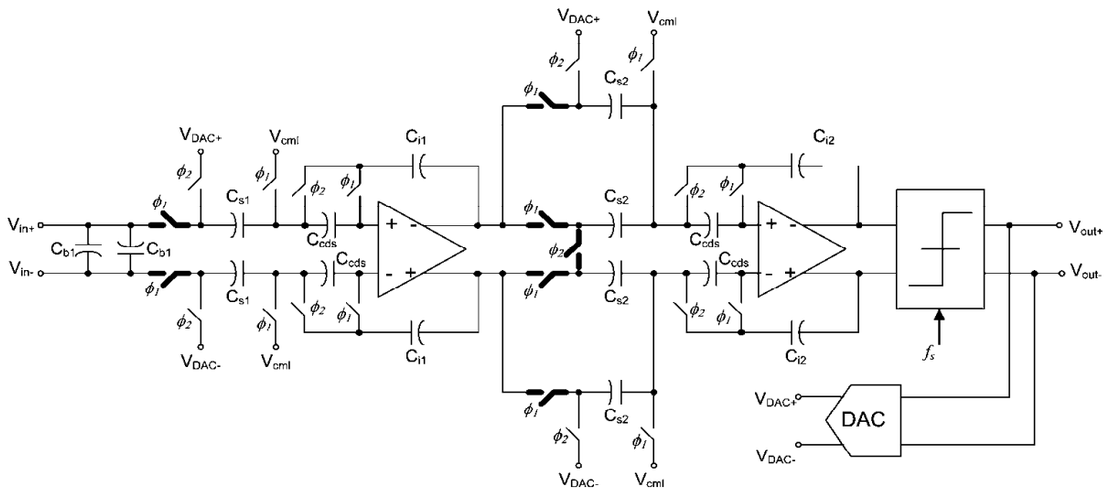


Fig. 10. Implementation of the second-order ΣΔ modulator (critical switches are highlighted).

Fig. 10 shows the SC implementation of the modulator of Fig. 9. The architecture is composed of two correlated double sampling (CDS) integrators, a comparator, and a 1-bit digital-to-analog converter. This implementation has been chosen attending to different implementation issues:

1. Flicker noise: as the desired signal bandwidth of the converter is low, the noise floor is dominated by flicker noise. Correlated Double Sampling has been used in order to shape the flicker noise outside of the signal band (Williams & Wooley, 1994). The basic operation of the CDS integrator is as follows. The amplifier flicker noise and offset is sampled across C_{CDS} during the first clock phase (ϕ_1). During the second clock phase (ϕ_2) the flicker noise and an offset are cancelled by the voltage stored in C_{CDS}.
2. Low-voltage operation: the use of a very low supply voltage introduces several issues that complicate the design of the Sigma-Delta modulator. The first problem to solve is the design of an operational amplifier with a large output swing that achieves sufficient gain and bandwidth. The other critical problem is the need of a rail-to-rail switch. These problems are solved using QFG techniques described in previous section 3 and 4.
3. Low-power operation: the main contributors to power consumption of a ΣΔ modulator are the operational amplifiers. Low-power operation is achieved by means of using the two-stage class-AB opamp based on QFG transistor and biased in weak inversion shown in section 4. Other measure to save power consumption is to minimize capacitor sizes which are limited either kT/C noise or capacitor mismatch specifications.

The 1-bit quantizer has been implemented using the architecture illustrated in Fig. 11. The dynamic latch operates as follows. When the clock ϕ_2 is low, the latch is reset, and its outputs are both pulled high. When ϕ_2 is high the latch enters in the regeneration phase

because M3 and M4 form a positive feedback loop. The power consumption of the comparator is of only 32.5nW during normal operation. Capacitors C_{comp} perform a DC level shifting so that the input common mode voltage of the comparator is of V_{cmCOMP}=900mV. Moreover, by means of C_{comp}, the input signal is sampled at the end of clock phase ϕ_1.

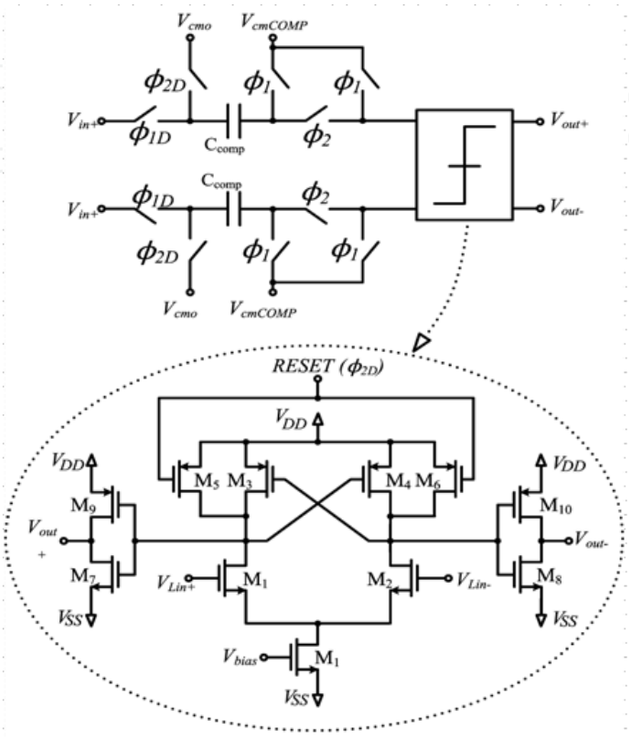


Fig. 11. 1-bit quantizer.

Switches connected to Vi_{n+} and Vi_{n-} are controlled by a delayed clock phase (ϕ_{1D}) in order to remove the input-dependent offset voltage due to the clock feedthrough.
The 1-bit digital-to-analog converter (DAC) has been implemented by switches controlled by the comparator outputs (Fig. 12). In order to maximize the dynamic range, the feedback reference voltages are equals to ±VFS/2, where V_{FS} is the Full-Scale Input Voltage of the ADC.

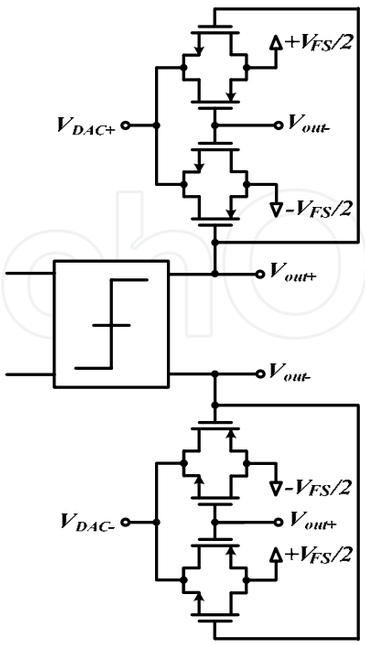


Fig. 12. 1-bit DAC.

5.2 Experimental results.

The Sigma-Delta modulator has been also implemented using an AMI (MOSIS) 0.5μm CMOS technology. The active area of the modulator is of 0.6 mm². A chip microphotograph is shown in Fig. 13. A sinusoidal input of 5Hz and 362 mV amplitude has been used to characterize the dynamic performance. Fig. 14 shows the output spectrum of the modulator, where a SNDR of 62.6 dB is demonstrated. Under these conditions, the power consumption is only of 140nW (90nW of static power consumption).

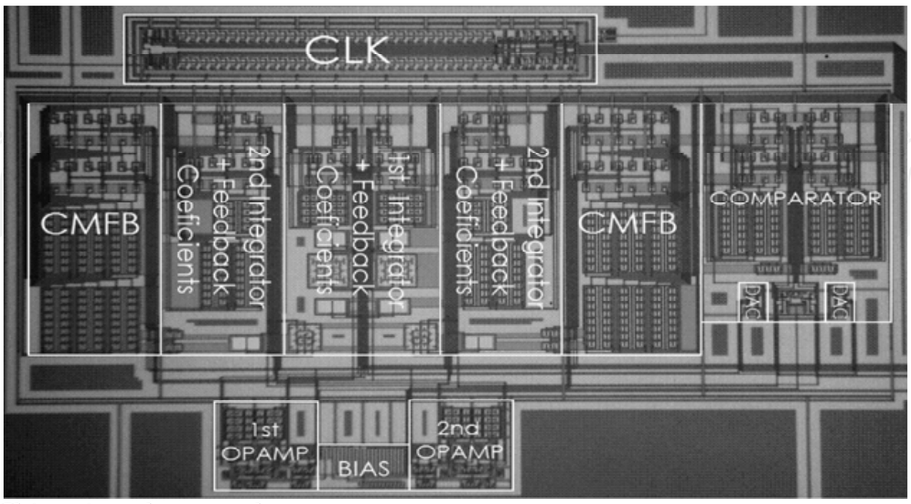


Fig. 13. Chip microphotograph.

Fig. 15(a) shows the SNDR and SNR versus the input amplitude normalized by the full scale input voltage (1.2V amplitude). It can be seen that the dynamic range is 67.4dB, which corresponds to 10.75 effective bits. Furthermore, in Fig. 15(b) the SNDR is shown, using input amplitude of 362mV, versus the frequency of the input signal. We can see that the modulator maintains its performance from DC to 25Hz.

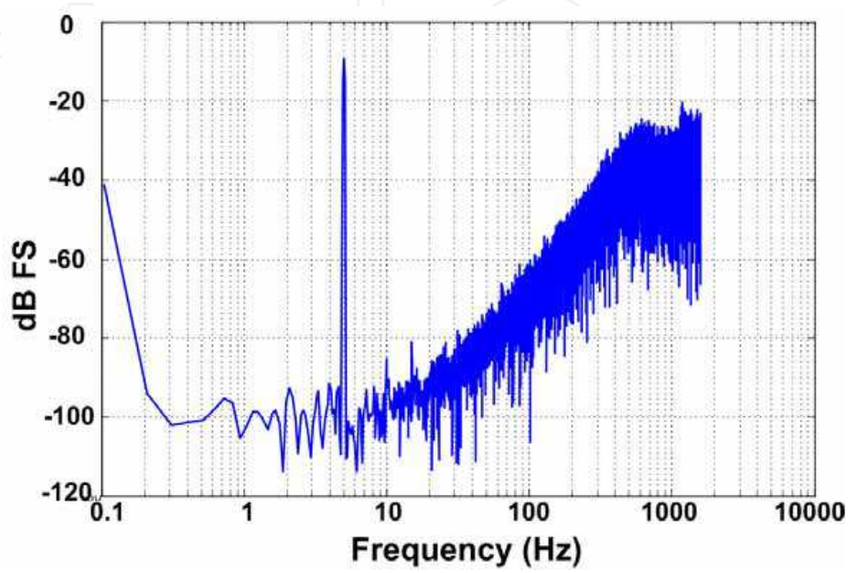
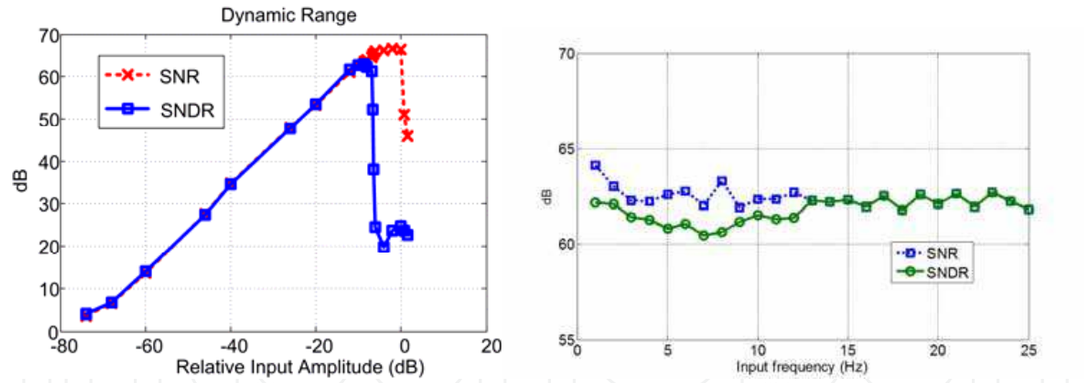


Fig. 14. Output spectrum with an input signal of 362mV amplitude and 5Hz.



(a) (b)

Fig. 15. (a) SNDR and SNR versus the normalized input amplitude. (b) SNDR and SNR vs. input frequency (input signal of 362mV amplitude).

Table 5. summarizes the overall experimental results; (19) was used to calculate the ADC figure of merit.

Technology	MOSIS 0.5μm CMOS
Supply Voltage	1.2V
Full scale input signal	0.362V amplitude
Sampling rate	3.2kHz
Power consumption	140nW
Signal bandwidth	25Hz
ENOB	10.75 bits
Peak SNDR (362mV amplitude and 5Hz)	62.6dB
Peak SNR (950mV amplitude and 5Hz)	66.5dB
DR	67.4dB
Active area	0.6mm²
FOM	1.6pJ/state

Table 5. ADC experimental results.

The reported low-power consumption and measured ENOB makes this ADC suitable for wearable EEG systems. In addition, the low area required makes possible to use this ADC in general purpose biomedical systems were more than one ADC in required.

6. Conclusions

Two 10-bit, low-voltage, low-power ADCs has been designed for wearable EEG systems. Innovative design techniques, circuit architectures based on QFG transistors, are described which allow circuit implementation at very low-voltage supply and low-power conditions. The first one uses pipeline architecture allowing higher input signal bandwidth showing 9.8 bits of resolution during by means of post-layout simulations. The second one uses a second-order SC-ΣΔ architecture with CDS, obtaining in measurements more than 10 bits of resolution.

In addition a deep understanding of the error mechanisms of both ADC architectures have been used to build up a behavioural simulator in order to obtain the design requirements of the ADCs building blocks.

In order to minimize the power consumption a novel weak-inversion biased class-AB operational amplifier based on QFG transistors has been used in both designs in order to achieve high-enough open-loop gain and output-swing under low-voltage conditions. Furthermore, QFG transistors have been used to solve the problem of the high-swing switches.

The presented ADCs have been implemented using MOSIS 0.5μm CMOS technology with high transistor threshold voltages (0.96V for p-MOS transistor). Simulations and experimental results show high enough performance for EEG signal processing with low-voltage supply and low-power consumption.

Table 6. shows a comparative study some of the most recently and relevant published state-of-the-art energy-efficient ADCs for biomedical applications.

Ref	ENOB (bits)	BW (kHz)	Power (μW)	V_{DD} (V)	Tech. CMOS	FOM (pJ/state)
(Yang & Sarpeshkar, 2006)	7.4	23	0.96	1.2	0.18μm	0.12
(Agah et al., 2007)	14	500	38000	1.8	0.18μm	2.3
(Yang & Sarpeshkar, 2005)	10	16	75	3	0.35μm	2.3
This work (Pipelined ADC)	9.8	2	1.5	1.2	0.5μm	0.84
This work (ΣΔ ADC)	10.75	0.025	0.14	1.2	0.5μm	1.6

Table 6. Comparative study of Biomedical ADCs.

We can be observed that the ΣΔ ADC converter described in this chapter is the less power consuming ADC reported so far. In addition, to the best authors' knowledge the energy efficient of both described ADCs are the best of all biomedical ADCs except (Yang & Sarpeshkar, 2006). However, their higher ENOB makes them more useful for modern and high-quality wearable EEG systems.
Finally, we can bring out that this work demonstrate the usefulness of using extensively the QFG technique for the design of very low-power and very low-voltage analog systems.

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Biomedical Engineering can be seen as a mix of Medicine, Engineering and Science. In fact, this is a natural connection, as the most complicated engineering masterpiece is the human body. And it is exactly to help our "body machine" that Biomedical Engineering has its niche. This book brings the state-of-the-art of some of the most important current research related to Biomedical Engineering. I am very honored to be editing such a valuable book, which has contributions of a selected group of researchers describing the best of their work. Through its 36 chapters, the reader will have access to works related to ECG, image processing, sensors, artificial intelligence, and several other exciting fields.

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