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Influence of Immersion Lithography on Wafer Edge Defectivity

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1. Introduction

In semiconductor manufacturing, the control of defects at the edge of the wafer is a key factor to keep the number of yielding die as high as possible per wafer. Using dry lithography, this control is typically done by an edge bead removal (EBR) process, which is understood well. The recent production introduction of immersion lithography however changes this situation significantly. During immersion exposure, the wafer edge is locally in contact with water from the immersion hood, and particles can then be transported back and forth from the wafer edge area to the scanner wafer stage. Material in the EBR region can also potentially be damaged by the dynamic force of the immersion hood movement. In this chapter, we have investigated the impact of immersion lithography on wafer edge defectivity. In the past, such work has been limited to the inspection of the flat top part of the wafer edge, due to the inspection challenges at the curved wafer edge and lack of a comprehensive defect inspection solution. The development of edge inspection & metrology tools now allows us to probe this area of the wafer.
This study used KLA-Tencor's VisEdge CV300-R, an automated edge inspection system that provides full wafer edge inspection (top, side, and bottom) using laser-illumination and multi-sensor detection, and where defects can be classified with Automated Defect Classification (ADC) software. In addition to defectivity capture, the tool performs simultaneous, multi-layer, film edge and EBR metrology, indicating the distance from the wafer edge or wafer top depending on the location of the film/EBR edge. It also can review defects using an integrated, hi-resolution microscope.
In this paper the impact from immersion lithography towards wafer edge defectivity is investigated. The work revealed several key factors related to wafer edge related defectivity control: choice of resist, optimization of EBR recipes, scanner and immersion-fluid contamination, wafer handling and device processing procedures. Understanding the mechanisms of wafer edge related immersion defects is believed to be critical to the successful integration of the immersion process into semiconductor manufacturing.

2. Process control at the wafer edge

In semiconductor manufacturing, control of the process at the wafer edge is a key factor in determining the total number of yielding die on a wafer. The removal of photoresist from

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the wafer backside and edges is especially important to avoid contact between the resist and the scanner stage or wafer handling hardware. Typically, a solvent EBR rinse is the last step in the coating recipe: the combination of a solvent stream from a static nozzle toward the wafer back side and a dynamic nozzle toward the wafer front side dissolves the resist up to a few millimeters from the wafer's outer edge. The desired position of the EBR material edge at top side (the so-called EBR-width) can depend on the coated material (e.g., antireflective topcoat vs. photoresist material) and/or on the layer within the device: for example, a contact hole lithography process might use a slightly different EBR width than the gate process. To increase die yield, it is desirable to have EBR widths that are as small as possible.

Immersion lithography [1-4] has changed the way we view defectivity issues at the wafer edge significantly. During the immersion exposure sequence, the wafer edge is in contact with the water from the immersion hood (IH), introducing additional concerns beyond direct contact of resist with the scanner. First, when the IH is scanning in the EBR region, its movement can damage material edges (Fig. 1a). IMEC's program on immersion lithography found that, for example, photoresist material can partially peel off during the IH pass (Fig. 1b).

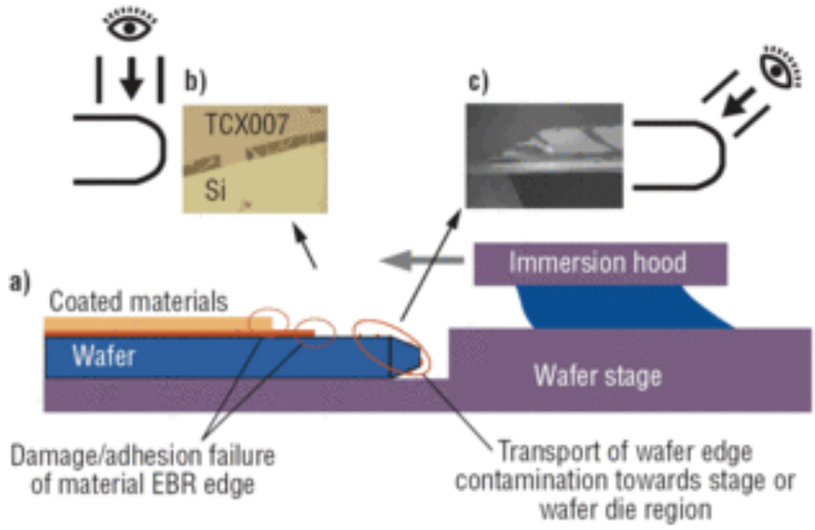


Fig. 1. a) Schematic representation of possible defect issues with immersion lithography; b) example of damaged photoresist material inspected with top-down optical microscope; and c) example of damaged residues at the wafer edge, inspected by tilted SEM (45°).

A second concern involves the cleanliness of the wafer edge outside the EBR edges. The IH pass wets not only the near-edge top surface, but also the curved wafer edge and even part of the bottom surface. Defects can be released from this area and re-deposited either on the wafer or on the wafer stage. In the first case, there will be a direct impact on the wafer defectivity. In the latter case, defects present on the wafer stage can be transported onto wafers in subsequent wafer processing. IMEC's program on immersion lithography found that resist residues left on the curved wafer part by an incomplete EBR step can be damaged by the IH pass, releasing fragments into the system (Fig. 1c).

Traditional defect inspection techniques have serious limitations when monitoring these new issues. Conventional dark field or bright field inspection tools cannot access the wafer edge since these systems typically have an edge exclusion of ~3mm. While microscopy tools can inspect the edge area, they can only give qualitative information with limited sampling.

3. Technology for wafer edge defect inspection

The new measurement system for wafer edge defect inspection (Fig. 2) is based on a laser source directed to the wafer edge surface. Three detectors simultaneously collect the scattered light, the specular or reflected light and the phase difference between different polarization states. As the laser scans the wafer edge surface, each signal can be converted into an image. Each type of defect produces a specific combination of signals from the three detection channels, allowing automated defect classification.

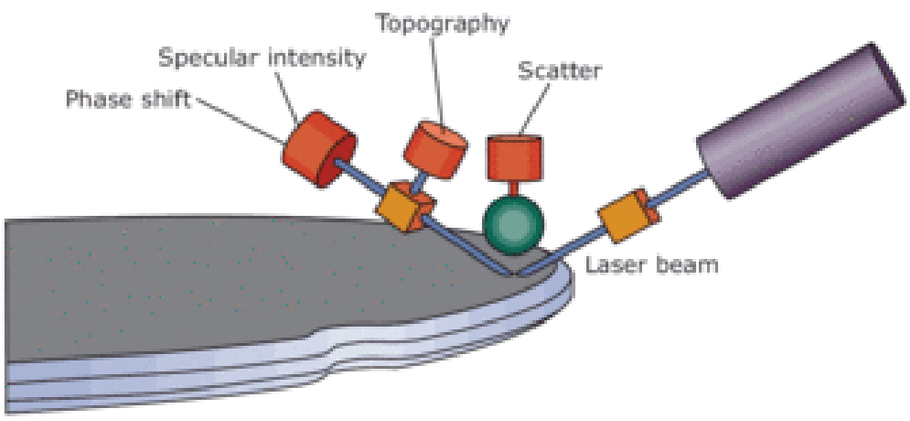


Fig. 2. Schematic representation of the VisEdge measurement principle.

3. Imaging of the wafer edge

Imaging covers the entire edge region including the following areas: ~5mm bottom near-edge, bottom bevel, apex, top bevel, and ~5mm top near-edge. Scanning generates a continuous high-resolution image for the entire wafer edge, which can be represented as a Mercator projection: an unfolding of the wafer edge surface into a flat plane. Excursions in eccentricity and/or in EBR width, which might result in a layer's edge ending on the wrong underlying substrate, can be easily monitored using this kind of inspection.
For wafer edge cleanliness, a high-resolution view of the wafer edge is typically more useful. Here, the images view only a few millimeter of the edge. Figure 3 uses this representation to show resist flakes observed along the apex-bevel regions in the specular channel.

4. Immersion defect process characterization and optimization

As indicated in the introduction, immersion-related defects at the wafer edge can be due to edge damage to the coated material in the EBR area, from the IH passing over this region. On the other hand, defects can be caused by transport of particles present on the bevel. These might be released by forces of the immersion hood, transported by the water in the hood, and re-deposited on the wafer and/or stage. This work focuses on the latter, and in particular on the flake defects observed in past work [5].

5. Edge region flake defects

Flake defects are related to material residues that are present on the wafer edge after coating. Typically, these residues are only present on the apex of the bevel, and therefore are

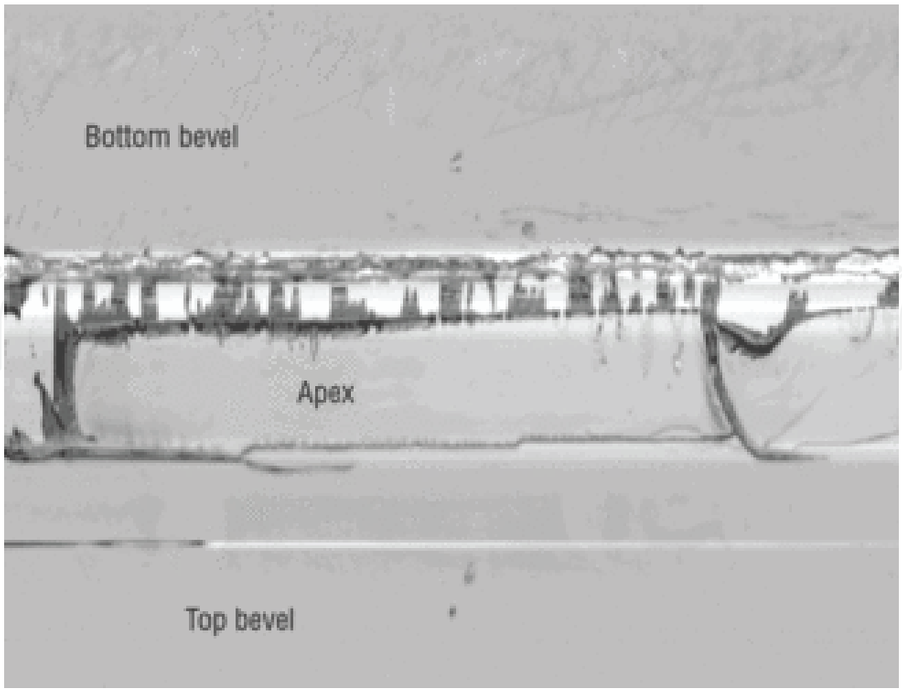


Fig. 3. Example of a specular image using the new technology showing part of the bevel/ apex region. This kind of representation is valuable for the evaluation of wafer edge quality.

difficult to detect by conventional top-down inspection methods. The residues result from a non-optimized EBR process: since the coated material on the wafer edge can be significantly thicker than on the flat top region, an insufficient solvent supply can leave edge residues while the top surface is clean. This phenomenon is more commonly observed with photoresist materials, rather than with BARC and topcoat materials.

The morphology of edge residues can depend on the resist. For some resists, the residue can be quite uniform along the apex. For other resists, large areas of thick residues are combined with areas with thin residues.

Once detected, the problem can be solved by adjusting the EBR recipe. Because making the EBR recipe longer limits the throughput of the immersion cluster, however, fabs try to avoid this adjustment if possible, there is a clear risk of processing wafers with resist residues over to the immersion scanner.

When wafers with resist residues are exposed on an immersion scanner, it is difficult to predict if the IH pass over the edge of the wafer will damage the resist residue, and if (part of) the residues will redeposit on the wafer top-side or on the scanner wafer stage. Tilted SEM review suggested qualitatively that such damage can happen with certain resists.

6. Experimental conditions of edge flake characterization

We experimented with three resists with different chemistries (**Fig. 4**). Sensitivity to edge damage was expected to vary across the three resist types. A dedicated exposure job spatially separated the areas where flakes are expected and where they are not expected. One section, consisting of two rows of 11 fields, was exposed close to the wafer edge at the opposite side of the notch. A similar area of two rows of 11 fields was exposed in the region of the notch. During the exposure of these 2 × 11 sections at both locations near the wafer

edge (Region II), the IH makes continuous up- and down-scans over the wafer edge area, increasing the probability of defect generation. The exposure job was also designed so that on another part of the wafer (Region I, on the right hand side), the immersion hood did not pass over the wafer edge. In Region I, no flake-like defects were expected.

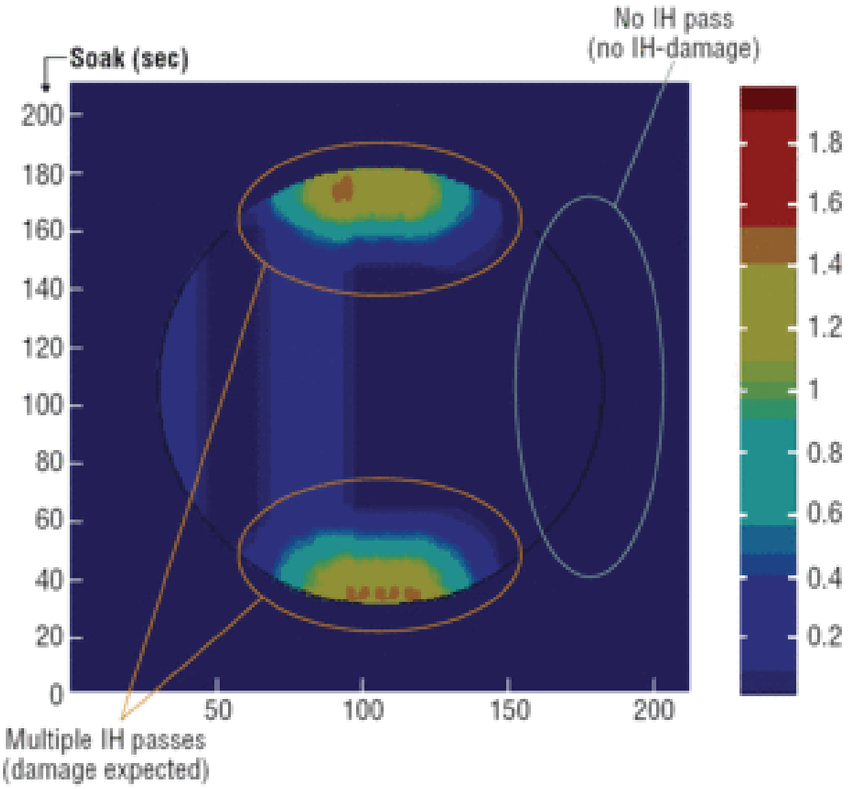


Fig. 4. IH exposure sequence for edge flake characterization.

7. Qualification

The specular images of regions with resist residues clearly showed differences in reflected intensity: dark areas in the resist residues refer to thick layers, while light areas indicate much thinner layers. The results obtained from Resist Type A are detailed below.

We compared the SideScan images of areas where the IH did and did not pass. Figure 5a is a typical SideScan specular image for region I (where the IH did not pass). Differences in thick and thin resist residues are visible, but no fragments of the resist residues are evident. In contrast, in Fig. 5b, taken from Region II, indicated that parts from the thick residue at the bottom of the apex were released. The close-up in the image indicates that some of these edge flakes were re-deposited on the apex closer to the top.

To determine whether any of these edge flakes end up on the top region (where edge die can be damaged), we analyzed the TopScan image of the corresponding areas of Fig. 5a and 5b using the scatter channel, as shown in Figs. 5c and 5d. In Region II, a lot of particles were detected, while in Region I, no particles were observed in the images. This observation was encouraging for further ADC work.

Classification of the edge region flakes was found to vary by the defect location. Re-deposited edge flakes on the apex side were best classified using their signal in the specular

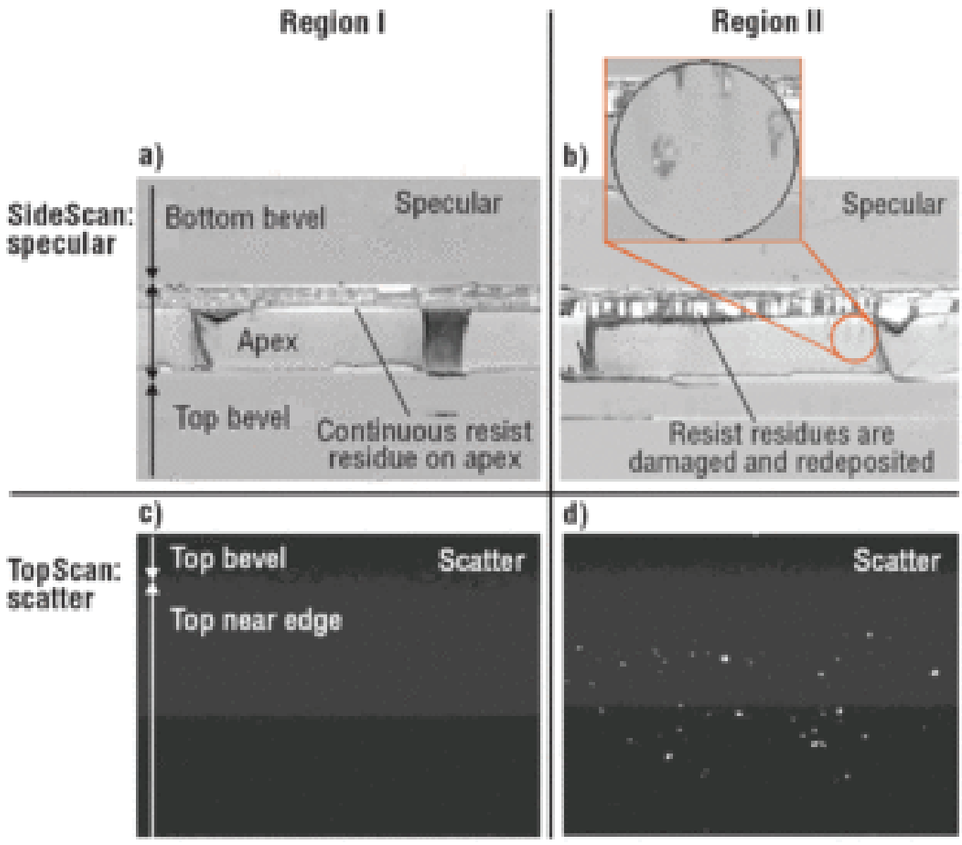


Fig. 5. Specular and scatter images from Region I (a and c) and Region II (b and d) of a test wafer. IH damage is more likely in Region II.

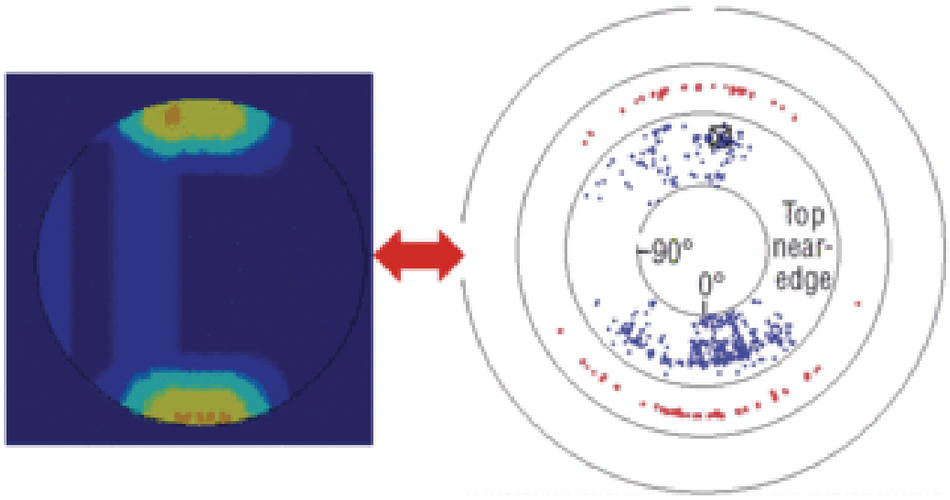


Fig. 6. Immersion characterization (quantification of edge flakes at wafer edge); the flakes on the apex and top near edge can be quantified by composite analysis of SideScan and TopScan signals.

channel of the SideScan image. For re-deposited defects in the top near-edge region, a combination of signals in the specular and scatter channels gave more accurate classification. Once all the measurement parameters for both areas are fixed, they can be combined in a single measurement sequence that provides defect classification and mapping for all the wafer edge areas of interest. (Fig. 6).

8. Immersion process characterization and optimization

Having qualified the inspection to classify and map edge flake defects, we used our results in a design of experiment to improve our understanding of this kind of defect source and its key impact parameters.

As indicated above, Resist A tends to generate flakes when the IH is passing over its edge. The non-optimized coating process left residues for two other resists, resist B and C; however the residue morphology was different.

When the same immersion exposure was used, significantly fewer edge flakes were detected in the near top region for Resist B and C than for Resist A (Fig. 7). Moreover, the residual defects were less confined to the exposure zone, so some of these defects might be caused by coating and wafer handling. In the TopScan images, no clear sign of damage was seen. Clearly the choice of resist chemistry can be important to prevent these kinds of defects.

As indicated earlier, resist residues can be optimized by changing the EBR recipe on the coat track. Resist A showed several hundred defect flakes with the regular (short) EBR sequence. After optimization, this resist achieved defect values similar to the background values obtained with the non-flaking resists B and C.

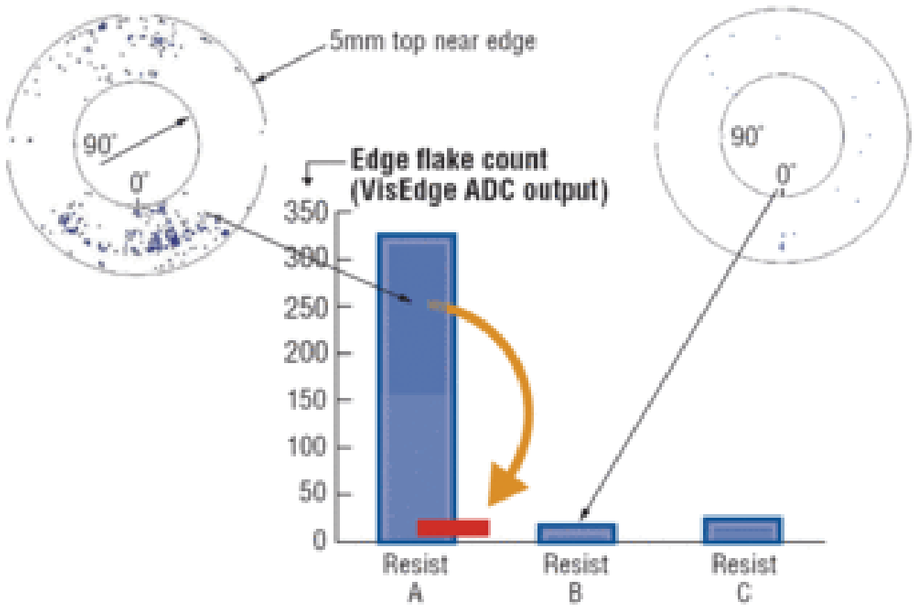


Fig. 7. Edge flake defects as a function of resist chemistry and EBR recipe.

9. Further wafer edge challenges

More kinds of defects besides the edge region flakes can be important in immersion litho. This section discusses other possible defect sources.

10. Wafer handling marks and resist rework process

A variety of artifacts were seen even in fresh Si wafers, primarily on the bevel and apex region. These wafers had very limited processing and handling, but damage was visible in the form of particles in the apex/bevel region. This introduces an additional concern with transport-related artifacts, and illustrates the need for an assessment of wafer edge quality and handling before introduction to the immersion process.

11. Resist rework processes

At IMEC, resist work is typically done by a combination of a dry ashing step, followed by a wet clean. In some cases, rework may be indicated to address an out-of-spec condition. Wafers used for monitoring of focus/dose/CD or overlay processes may be reworked daily. Limited rework typically results in an increased presence of scratches (typically at the lower bottom bevel), and an overall increase in reflectivity variation, indicating degraded surface quality. When wafers are reworked ~10 times or more, the bevel/apex area is much more affected. These defects could pose a risk when the immersion hood is passing over the wafer.

12. Conclusion

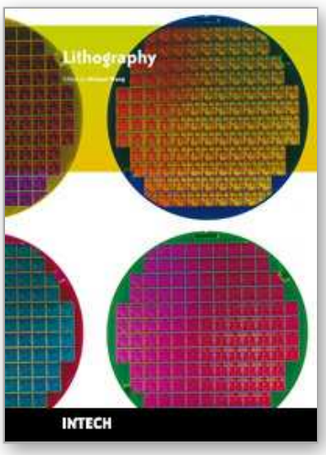
In this paper, we investigated the impact of immersion lithography on wafer edge defectivity. In the past, such work has been limited to inspection of the flat top part of the wafer edge due to the inspection challenges at the curved wafer edge and lack of a comprehensive defect inspection solution. Our study used a new automated edge inspection system that provides full wafer edge imaging and automatic defect classification.
The work revealed several key challenges to controlling wafer edge-related defectivity, including choice of resist, optimization of EBR recipes, and wafer handling.

13. Acknowledgments

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Lithography, the fundamental fabrication process of semiconductor devices, plays a critical role in micro- and nano-fabrications and the revolution in high density integrated circuits. This book is the result of inspirations and contributions from many researchers worldwide. Although the inclusion of the book chapters may not be a complete representation of all lithographic arts, it does represent a good collection of contributions in this field. We hope readers will enjoy reading the book as much as we have enjoyed bringing it together. We would like to thank all contributors and authors of this book.

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