2

Design Considerations for the Digital Core of a C1G2 RFID Tag

Ibon Zalbide, Juan F. Sevillano and Igone Vélez
TECNUN (Universidad de Navarra) and CEIT
Spain

1. Introduction

An EPC Class 1 Gen 2 (C1G2) RFID system is composed of a reader and one or several passive tags. Passive tags obtain the required energy from the radio frequency field emitted by the reader. The forward data link (reader to tag) is embedded in this radio frequency field. The backward data link (tag to reader) is achieved by means of backscattering.
The RFID tag consists of several analog circuits and a digital core. The analog circuits perform tasks such as harvesting the energy from the electronic wave, supplying power, generating a clock signal and signal conditioning. The digital core of the tag performs data detection and implements the logical requirements of the standard.

1.1 Passive long range UHF RFID systems

Fig. 1 shows the basic architecture of a long range Ultra High Frequency (UHF) RFID tag. The antenna receives the signal emitted by the reader. The voltage multiplier rectifies the incoming signal and increments the voltage to charge the supply capacitor C_{supply}. The efficiency of this voltage conversion will depend on the architecture of the voltage multiplier. The supply capacitor is used to supply power to the rest of the tag. The analog front-end creates the signals that the rest of the tag needs to work properly, such as regulated voltages, the clock signal and the reset signal. It performs some kind of demodulation by generating an intermediate signal that can be used by the digital core to detect the received bits. The analog front-end also modulates the load impedance of the tag commanded by the digital core, to backscatter the signal emitted from the reader so that information can be transmitted backwards. The digital core handles the communication protocol and accesses the non volatile memory to retrieve and store data.
Fig. 1 also shows the basic architecture of the digital core of a passive long range UHF tag. The input signal provided by the front-end is evaluated in a symbol detector to detect incoming symbols. A command decoder determines the operation code and the arguments received and it forwards them to a control unit. In the control unit, the finite state machine defined in the standard is implemented to control the communication flow. Moreover, depending on the standard, additional features such as collision arbitration algorithms or integrity checks are performed in this unit. Usually, the number of states of the finite state machine and the integrated additional features define the complexity and functionality of the whole tag. Finally, a transmitter controls the load modulator of the front-end and backscatters the answer to the reader.

Source: Radio Frequency Identification Fundamentals and Applications, Design Methods and Solutions, Book edited by: Cristina Turcu, ISBN 978-953-7619-72-5, pp. 324, February 2010, INTECH, Croatia, downloaded from SCIYO.COM

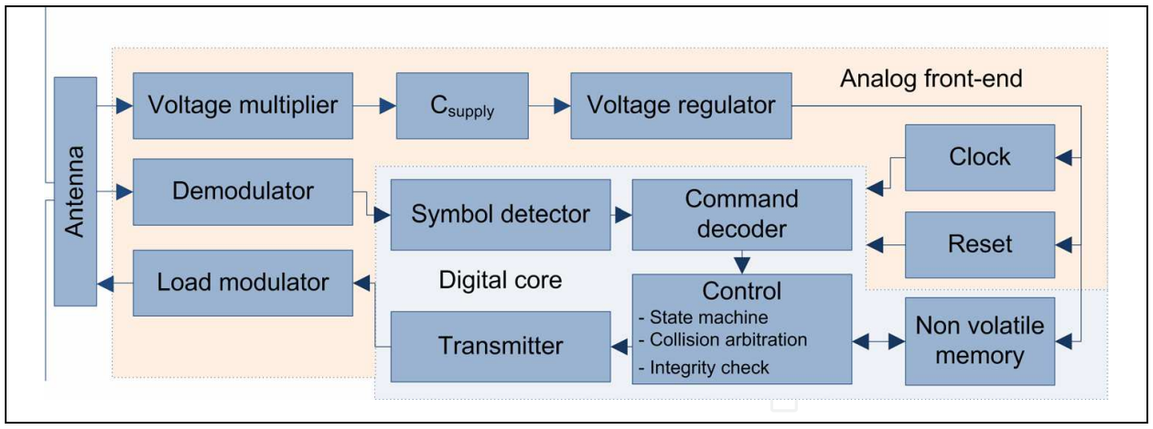


Fig. 1. Architecture of a passive RFID tag.

The C1G2 standard (EPC Global, 2005) has become the main communication protocol of passive long range UHF RFID systems. Given the success of the C1G2 standard, the ISO organization finally adopted it with minor changes as the ISO18000-6C (ISO, 2006). Nowadays, it is the dominant air interface for passive UHF RFID tags, because of its flexible functionality and the compatibility with the whole EPC network. Almost every recent research work concerning passive long range UHF RFID tags uses this communication protocol; e.g.: (Yan et al., 2006; Barnett et al. 2007; Man et al., 2007; Ricci et al., 2008; Zhang et al., 2008; Roostaie et al. 2008; Wanggen et al. 2009). Thus, this chapter is focused in the C1G2 standard. However, the concepts and ideas presented can be extended to other standards.

1.2 Communication range

The communication range of an RFID system is one of the factors that define the scope of its applications. Assuming that the reader is continuously sending a continuous wave (CW), the maximum communication distance between a passive RFID tag and the reader is mainly limited by two factors related to the tag's power consumption: the input power in the tag, and the voltage at the input of the voltage multiplier (Pardo et al., 2007; De Vita et al., 2005).

Input power in the tag

The communication range r is limited by the minimum input power. According to (Pardo et al. 2007),

$$r \leq \sqrt{\frac{P_{EIRP}\lambda^2 G X^2 \eta}{4\pi^2 (R_A^2 + 4X^2)\cdot P_{TAG}}}, \quad (1)$$

where P_{EIRP} is the Effective Isotropic Radiated Power, λ the wavelength, G the tag antenna gain, X the reactance introduced by the load modulator, η the efficiency of the rectifier, R_A the impedance of the antenna and P_{TAG} the tag power consumption. Equation (1) shows that reducing the power consumption of the analog or digital parts increases the communication range.

Voltage at the input of the voltage multiplier

According to (Pardo et al. 2007), there is another constraint due to the minimum voltage at the input of the voltage multiplier. If the threshold voltage required to switch on the voltage multiplier is not achieved, the tag will not start working, no matter the available input power. This constraint is related to the fabrication technology and it is given by

$$r \leq \frac{0.7 Q_{MN} \lambda \sqrt{P_{EIRP} G R_A}}{4\pi V_{tech}}, \quad (2)$$

where Q_{MN} is the quality factor of the matching network and V_{tech} is the minimum voltage at the input of the voltage multiplier. The voltage V_{tech} depends on the technology used. Q_{MN} can be expressed in terms of the equivalent input resistance of the tag as

$$Q_{MN} = \sqrt{\frac{R_P}{R_A} - 1}, \quad (3)$$

where R_P is the equivalent resistance in parallel with C_{supply} that represents the power consumption of the tag. R_P increases as power consumption decreases. Thus, as the power consumption decreases, Q_{MN} increases and a larger communication range is feasible.

Summarizing, the communication range increases when the power consumption of the tag decreases. As detailed in (Pardo et al. 2007), the most restrictive of (1) and (2) sets the actual communication range of the system. However, the relation between power reduction and range improvement is not always constant. The dependence of the communication range on the input power in the tag is stronger than on the voltage at the voltage multiplier. Thus, when the power consumption of the tag is high and (1) limits the communication range, reducing the power consumption of the tag increases notably the maximum communication distance. But when the power consumption goes down, (2) becomes the most restrictive and the range improvement slows down. At this point the technology is limiting the communication more than the power consumption.

A proper design of the tag is required to minimize the power consumption, and move from the section where the power consumption limits the communication range to the section where the technology is the limiter. This way, the maximum communication range for the selected technology can be achieved. As the digital part's power consumption can be comparable to the analog, the reduction of the digital power consumption is very important for the overall performance of the system.

The main goal of the publications focused on C1G2 digital cores is to minimize the average power consumption. Advances in the technology of semiconductors help to reduce the power consumption of integrated circuits. Designers have to work with the technology available at that time. However, there are issues where designers can focus to optimize their designs for a given technology.

The power consumption of the digital core grows with the clock frequency. Thus, designers try to reduce the clock frequency to minimize power consumption. Impinj, a C1G2 tag seller, published a white paper where this value was said to be 1.92MHz (Impinj, 2006). Even though there are some works in the literature that work at 1.92MHz, such as (Wang et al., 2007), most works propose digital cores for other clock frequencies. For example, (Hong et al., 2008) works at 4 MHz, (Man et al., 2007) at 3.3MHz, (Zhang et al. , 2008; Yan et al., 2006) at 1.28MHz and (Ricci et al., 2008) at 2MHz. A study of the constraints on the clock signal of the digital core is needed so that the clock frequency can be optimally selected.

Another approach employed by digital designers to reduce power consumption is power management. Depending on the technology, similar benefits can be obtained in a simpler way by means of clock gating. In either case, the net effect is that the digital core can not be considered to have constant power consumption, but a power consumption profile in time

(Zalbide et al., 2008). The effect of the shape of this power consumption profile in the overall performance (i.e.: communication range) needs to be studied.

1.3 Objectives of the chapter

This chapter performs an analysis of the EPC C1G2 standard to extract requirements of the tag's digital core for proper forward-link data detection and backward-link data backscattering. The EPC C1G2 standard specifies the characteristics of the waveforms employed in the forward-link communication. These characteristics of the waveforms pose requirements on the clock signal used for data detection (wander and jitter of the clock). The backscattering signal is also controlled by the digital core. Therefore, the requirements set by the standard on the backscattering signal constrain the clock signal used in the digital core as well. The chapter reviews some aspects of the operation of the digital core of the tag and presents equations and figures that can be used to select an appropriate clock signal.
On the other hand, the chapter presents methods to analyse the influence of the application of power management techniques in the communication range of the system. The results provide valuable tools to analyse different trade-offs early in the design of a RFID tag.
The chapter is organized as follows. Section 2 describes the architecture of the digital core considered for the study. Section 3 analyses the constraints on the clock signal and Section 4 studies the influence of the power management on the communication range. Finally, the main conclusions are summarized in Section 5.

2. Architecture

Fig. 2 depicts the architecture of a generic C1G2 digital core used as example for this study. The incoming symbols are detected in the symbol detector. The command decoder obtains the operation code and the arguments of the requested operation. In order to avoid a big input buffer, the variable length arguments, such as the selection mask, are processed in the command decoder. The cryptographic functions are also performed in the command decoder making all arguments transparent to the rest of modules. The control module controls the system with a finite state machine and a register bank. The collision arbitration, session management and memory lock are contained in this module. It does the necessary operations accessing the memory and the register bank. Finally, TX, the transmitter, encodes the answer with the required format. For this purpose, a backward link frequency synthesizer is included in the transmitter. The accesses to the tag memory (EEPROM) are handled by an intermediate module memory access. The power management unit, PM, controls the activity of the rest of the modules using the clock gating technique. VEEPROM is a cache memory used to reshape the power consumption profile of the tag (Zalbide, 2009).
For power management, five different working states have been defined. Every working state is optimized to perform a specific operation during the communication. Table 1 shows the relationship of the working states with the modules. Each working state activates the necessary modules to fulfill its functionality and deactivates the remaining modules. Some modules, such as the memory access, are used in various different working states; others are only used in a single working state. The combination of all the working states enables the system to work properly minimizing the activity of its circuitry.
The STRTP state is the initial working state. The tag checks the kill bit, and if it is not killed, the system turns to STDBY state, waiting for the beginning of the forward link data

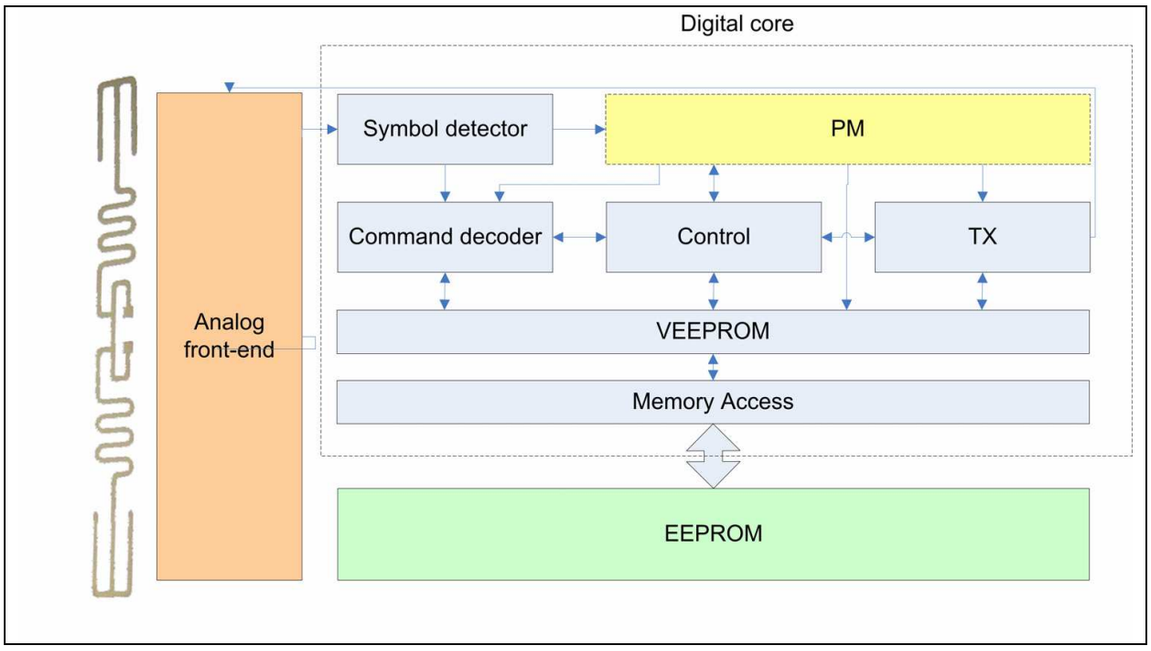


Fig. 2. Architecture of the low power C1G2 digital core.

	Working state				
	STRTP	**STDBY**	**RX**	**CNTRL**	**TX**
PM	ON	ON	ON	ON	ON
Symbol detector	OFF	ON	ON	OFF	OFF
Command decoder	OFF	OFF	ON	OFF	OFF
Control	ON	OFF	OFF	ON	OFF
Memory access	ON	OFF	ON	ON	ON
VEEPROM	ON	OFF	OFF	ON	OFF
TX	OFF	OFF	OFF	OFF	ON

Table 1. Working states of the digital core.

transmission. In this state only the symbol detector is active. When the beginning of a new message from the reader is detected, the command decoder is activated and the working state turns to RX. After receiving the whole message, the working state changes to CTRL, deactivating the command decoder and the symbol detector, and activating the control and the register bank. Finally, in the TX state the response is sent to the reader and the working state returns to STDBY.

Reading from the EEPROM is one of the most power hungry operations that the tag performs. In the design presented in this chapter, the EEPROM is read when a lot of energy is arriving to the tag. Then, the read data is stored in VEEPROM, which is less power hungry. This way, if data from the EEPROM is needed when less energy is available, they can be read from VEEPROM instead of from EEPROM. The introduction of this module allows reshaping the power distribution so that the power peaks caused by the accesses to EEPROM can be moved to less critical time intervals. In exchange, the tag spends more time initializing, as it must copy the data from the EEPROM to the VEEPROM.

3. Analysis of the clock signal requirements

As the power consumption of the digital core grows with the clock frequency, the selection of a minimum clock frequency will maximize the communication range. In the following, a detailed study of the clock signal constraints for C1G2 communication is presented. This study shows that the minimum required clock frequency depends on the characteristics of of the clock signal and the implementation of the transmitter.

The section is organized as follows. First, a model for the clock signal used by the digital core is defined. Then, the operation of the digital core is analyzed together with the specification of the standard. From this analysis, equations that constrain the clock signal parameters are obtained. These equations are computed numerically to find the regions in the clock signal parameter space where the C1G2 standard specifications are satisfied. These results facilitate the definition of the requirements for the generator of the clock signal used in the digital core.

3.1 Clock model

Ideally, the clock signal can be considered as a square wave of period T. The frequency, $f=1/T$, is assumed to be constant and invariable in time. Nevertheless, actual clock sources do not generate perfect clock signals. For instance, if we measure the average clock period over two time intervals in different days or ambient conditions, the results may be different. Moreover, the duration of the clock periods within the same time interval suffers small variations from one cycle to another. For our analysis, we will model the clock signal using two parameters:

Average period, T_a: it is the mean value of the period of the clock signal during a whole inventory round.

Random jitter, ξ_i: it is a random variable that represents the normalized deviation of the clock edges from the edges of the average period.

Thus, the duration of the ith clock period T_i is given by $T_i=T_a+\xi_i$. If the maximum random jitter of the clock signal is annotated as ξ_{max}, then for all i, $T_i \in [T_a \cdot(1-\xi_{max}), T_a \cdot(1+\xi_{max})]$

3.2 Forward link

In the forward link of C1G2 (EPC Global, 2005), a reader communicates with one or more tags by modulating a Radio Frequency (RF) carrier using Amplitude-Shift Keying (ASK) modulation with Pulse Interval Encoding (PIE). The reader transmits symbols of duration $T_S=T_H+T_L$. In each symbol, the signal has maximum amplitude during T_H seconds and minimum amplitude during T_L seconds. $T_L=PW$ for both a data-0 and a data-1. As shown in Fig. 3, in order to transmit a data-0, T_H is set so that $T_S=Tari$. In order to transmit a data-1, T_H is set so that $1.5 \cdot Tari \leq T_S \leq 2 \cdot Tari$.

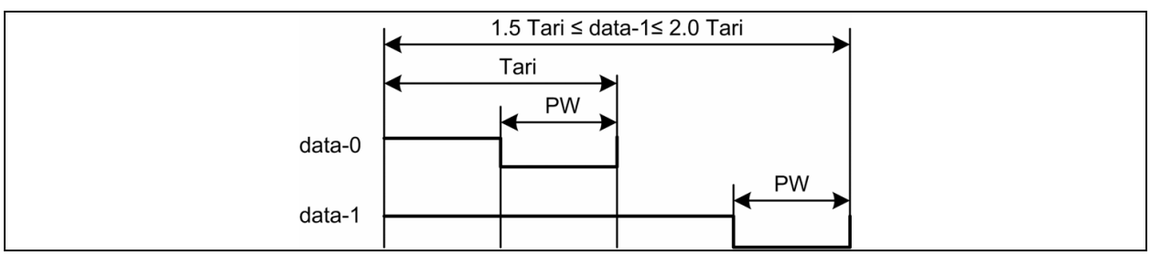


Fig. 3. PIE codification, from (EPC Global, 2005).

The forward data rate is set in the preamble of every command sent by the reader to the tag by means of symbol *RTcal*, as shown in Fig. 4. The duration of this symbol *RTcal* is equal to the duration of a data-0 plus the duration of a data-1. A tag shall measure the length of *RTcal* and compute *pivot*=*RTcal*/2. The tag shall interpret subsequent reader symbols shorter than *pivot* as data-0s, and subsequent reader symbols longer than *pivot* as data-1s.

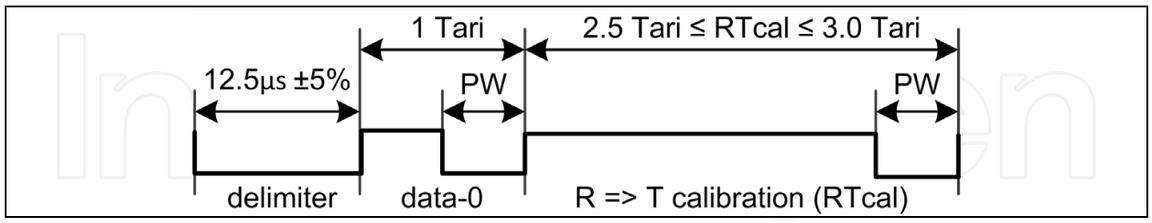


Fig. 4. Forward link calibration in the preamble, from (EPC Global, 2005).

3.2.1 Symbol detection

The front-end of the tag is assumed to have a one bit Analog to Digital Converter (ADC) to convert the envelope of the RF signal to a digital signal. The input to the digital core is assumed to have a high value during T_H and a low value during T_L. The digital core samples the input signal and identifies the incoming symbols by measuring the distance between modulated pulses. It is assumed that one sample is taken every clock cycle.
Given a generic symbol S, its duration will be annotated as t_S. The number of samples obtained when sampling S, n_S, will be in the range defined by equation (4).

$$\left\lfloor \frac{t_S}{T_a \cdot (1+\xi_{\max})} \right\rfloor \le n_S \le \left\lceil \frac{t_S}{T_a \cdot (1-\xi_{\max})} \right\rceil, \tag{4}$$

where $\lfloor \cdot \rfloor$ and $\lceil \cdot \rceil$ are the floor and the ceil functions respectively.

3.2.2 Forward link constraints

For proper operation, the digital core shall be able to detect when its input signal is in the high and in the low states. The duration in the low state, PW, is the shortest one. Therefore, the first constraint is that $n_{PW} \ge 1$. From (4), the first constraint is obtained:

$$\left\lfloor \frac{PW}{T_a \cdot (1+\xi_{\max})} \right\rfloor \ge 1 . \tag{5}$$

The second constraint comes from the fact that in order to detect the data-0 symbol properly, the number of samples obtained from a data-0 symbol has to be lower or equal to n_{pivot}: $n_{data\text{-}0} \le n_{pivot}$, where $n_{pivot} = \lfloor n_{RTcal}/2 \rfloor$. Using (4) to obtain the maximum number of samples for $n_{data\text{-}0}$ and the minimum number of samples for n_{RTcal}, we have,

$$\left\lceil \frac{Tari}{T_a \cdot (1-\xi_{\max})} \right\rceil \le \left\lfloor \frac{1}{2} \left\lfloor \frac{RTcal}{T_a \cdot (1+\xi_{\max})} \right\rfloor \right\rfloor . \tag{6}$$

If the symbol to be detected is a data-1, then we need that $n_{data\text{-}1} > n_{pivot}$. Taking from (4) the minimum number of samples for $n_{data\text{-}0}$ and the maximum number of samples for n_{RTcal}, we obtain the third constraint:

$$\left\lfloor \frac{RTcal - Tari}{T_a \cdot (1+\xi_{\max})} \right\rfloor \leq \left\lfloor \frac{1}{2} \left\lceil \frac{RTcal}{T_a \cdot (1-\xi_{\max})} \right\rceil \right\rfloor . \quad (7)$$

3.3 Backward link

In the backward link, a tag communicates with a reader using ASK and/or Phase-Shift Keying (PSK) backscatter modulation (EPC Global, 2005). The backward link data codification can be either FM0 baseband or Miller. Both the backward link codification and data rate are set by the reader in the last *Query* command. The backward data rate is set by means of the duration of the *TRcal* symbol in the preamble and the Divide Ratio (*DR*) specified in the payload of the last *Query* command.
A tag shall compute the backward link frequency as

$$BLF = \frac{DR}{TRcal} \quad (8)$$

and adjust its response to be inside the Frequency Tolerance (*FT*) and Frequency Variation (*FV*) limits established by the C1G2 standard (EPC Global, 2005). Additionally, the standard sets requirements on the duty cycle of the backward signal.

3.3.1 TRcal symbol detection

The first source of error in the generation of *BLF* is introduced when symbol *TRcal* is detected. The digital core measures the duration of *TRcal* as the number of entire clock cycles comprised inside the backward link calibration symbol, n_{TRcal}. The value of n_{TRcal} will be an integer in the range given by (4). The value of n_{TRcal} is used to compute the number of cycles required to synthesize one cycle of *BLF*. As n_{TRcal} is an approximate representation of the duration of *TRcal*, an error will be introduced.

3.3.2 Backward link frequency synthesis

The accuracy of the synthesized backward link signal depends on how the transmitter is implemented. In the following, we analyze three possible implementations: balanced half-T_{pri} base transmitter, unbalanced half-T_{pri} base transmitter and full T_{pri} base transmitter. A set of backward link constraints result for each of the three transmitters.
For latter use, the following definitions are performed:

- $T_{pri}=1/BLF$ is the period that the transmitter has to synthesize.
- n_{Tpri} is the number of clock cycles inside of a period of the synthesized backward link signal.
- n_H is the number of clock cycles that the transmitter maintains the output signal in high per period of the synthesized backward link signal.
- n_L is the number of clock cycles that the transmitter maintains the output signal in low per period of the synthesized backward link signal.

3.3.3 Balanced half-T_{pri} base transmitter constraints

This is the most straightforward implementation of the transmitter using a synchronous digital circuit design flow. Inside the transmitter, a counter counts $n_H=n_L$ clock cycles, and the output signal is toggled every time the counters finish. As n_H and n_L are the same, the output BLF signal stays the same number of cycles in high and in low, generating a balanced

waveform. Thus, the transmitter needs to computes the number of cycles required to generate a half-T_{pri} pulse. As this value has to be an integer, rounding is performed as shown in equation (9).

$$n_H = n_L = \left\lfloor \frac{n_{TRcal}}{2 \cdot DR} + \frac{1}{2} \right\rfloor \tag{9}$$

And thus, $n_{Tpri}=2n_H$.
The average value of the synthesized backward link frequency will be $n_{Tpri}\ T_a$. Taking from equation (4) the maximum and minimum values of n_{TRcal}, we can write the following two constraints to meet the frequency tolerance requirements of the standard:

$$\frac{DR}{TRcal} \cdot (1 - FT) \le \frac{1}{2 \cdot \left\lfloor \frac{\left\lfloor \frac{TRcal}{T_a \cdot (1 - \xi_{\max})} \right\rfloor}{2 \cdot DR} + \frac{1}{2} \right\rfloor \cdot T_a} \tag{10}$$

$$\frac{DR}{TRcal} \cdot (1 + FT) \ge \frac{1}{2 \cdot \left\lfloor \frac{\left\lfloor \frac{TRcal}{T_a \cdot (1 + \xi_{\max})} \right\rfloor}{2 \cdot DR} + \frac{1}{2} \right\rfloor \cdot T_a}. \tag{11}$$

On the other hand, the frequency variation of the synthesized backward link signal is given by

$$FV = \left| \frac{\frac{1}{T_{pri_k}} - \frac{1}{\overline{T_{pri}}}}{\frac{1}{\overline{T_{pri}}}} \right| = \left| \frac{\overline{T_{pri}} - T_{pri_k}}{T_{pri_k}} \right|. \tag{12}$$

Taking into account that

$$T_{pri_k} - \overline{T_{pri}} = \sum_{i=1}^{n_{Tpri}} T_a \cdot (1 + \xi_i) - n_{Tpri} \cdot T_a = \sum_{i=1}^{n_{Tpri}} \xi_i \cdot T_a \tag{13}$$

and manipulating equation (12), it can be shown that

$$FV = \frac{1}{\left| 1 + \frac{n_{Tpri}}{\sum_{i=1}^{n_{Tpri}} \xi_i} \right|} \le \frac{1}{\left| 1 + \frac{1}{\xi_{\max}} \right|} \tag{14}$$

From the requirements in the standard, we find the frequency variation constraint

$$\xi_{\max} < 0.0256. \tag{15}$$

This constraint is independent from the clock frequency: it only limits the maximum jitter. Finally, the duty cycle requirements are considered. The duty cycle can be expressed as

$$DC = \frac{\sum_{i=1}^{n_H} T_a \cdot (1+\xi_i)}{\sum_{i=1}^{n_H} T_a \cdot (1+\xi_i) + \sum_{i=1}^{n_L} T_a \cdot (1+\xi_i)}. \tag{16}$$

Working on (16), the following equation is obtained,

$$DC = \frac{1}{1 + \frac{n_L + \sum_{i=1}^{n_L} \xi_i}{n_H + \sum_{i=1}^{n_H} \xi_i}}. \tag{17}$$

Introducing the worst case jitter values in (17), the minimum and maximum duty cycles are obtained. Taking the requirements from the standard we have

$$\min(DC) = \frac{1}{1 + \frac{n_L \cdot (1+\xi_{\max})}{n_H \cdot (1-\xi_{\max})}} \geq 0.45 \tag{18}$$

$$\max(DC) = \frac{1}{1 + \frac{n_L \cdot (1-\xi_{\max})}{n_H \cdot (1+\xi_{\max})}} \leq 0.55\,. \tag{19}$$

In this type of transmitter n_H=n_L, and equations (18) and (19) yield the same duty cycle constraint:

$$\xi_{\max} \leq 0.1. \tag{20}$$

3.3.4 Unbalanced half-T_{pri} base transmitter constraints

In this case, we also perform a synchronous digital circuit design flow, but we first compute the value of n_{Tpri} as

$$n_{Tpri} = \left\lfloor \frac{n_{TRcal}}{DR} + \frac{1}{2} \right\rfloor. \tag{21}$$

And then, the values of n_H and n_L are selected as,

$$n_H = \lfloor n_{Tpri}/2 \rfloor \tag{22}$$

$$n_L = n_{Tpri} - n_H\,. \tag{23}$$

The counter in the transmitter counts n_H clock cycles while the output is set to high, and n_L clock cycles while the output signal is set to low.
Proceeding in a similar way to the former transmitter, we find the two frequency tolerance constraints to be

$$\frac{DR}{TRcal}\cdot(1-FT)\le\frac{1}{\left\lfloor\frac{\left\lfloor\frac{TRcal}{T_a\cdot(1-\xi_{\max})}\right\rfloor}{DR}+\frac{1}{2}\right\rfloor\cdot T_a} \tag{24}$$

$$\frac{DR}{TRcal}\cdot(1+FT)\ge\frac{1}{\left\lfloor\frac{\left\lfloor\frac{TRcal}{T_a\cdot(1+\xi_{\max})}\right\rfloor}{DR}+\frac{1}{2}\right\rfloor\cdot T_a}. \tag{25}$$

The frequency variation constraint is the same as for the former transmitter and is given by (20).
In this transmitter, the values of n_H and n_L are different. If we replace equations (22) and (23) in equations (18) and (19), we obtain the two duty cycle constraints.
The backward link signal synthesized with this transmitter has a more accurate frequency. Nevertheless, the duty cycle is worse than in the former transmitter, because the number of cycles that the output signal is set to high and the number of cycles that the output signal is set to low can be different. This generates an unbalanced output waveform.

3.3.5 Full-T_{pri} base transmitter constraints

This approach can be found in (Ricci et al., 2008). Part of the backward link signal synthesis is performed out of the digital circuit synchronous domain of the transmitter as shown in Fig. 5. The transmitter controls a multiplexer, which sets the output BLF signal to '1', '0', 'clk' or '**not** clk'. With this technique, the time granularity needed by the transmitter is T_{pri} instead of $T_{pri}/2$, because the availability of 'clk' and '**not** clk' makes it possible to toggle the input to the load modulator two times per clock cycle. Therefore, the values of n_H and n_L can take values with a precision of a half period:

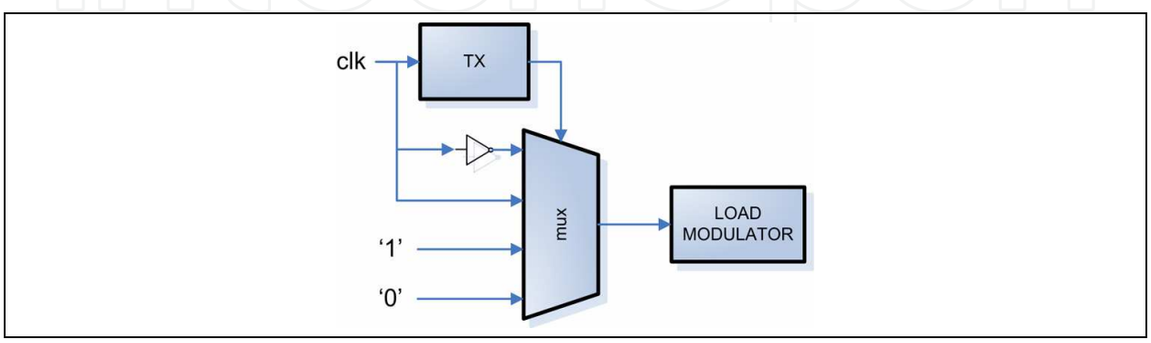


Fig. 5. Full-T_{pri} base transmitter.

$$n_H = n_L = n_{Tpri}/2 \tag{26}$$

where n_{TPri} is computed using equation (21).
The frequency tolerance constraints for this transmitter are the same as for the former unbalanced half-T_{pri} base transmitter and they are given by equations (24) and (25). The frequency variation constraint is equation (20), as for the two former transmitters.
In order to analyze the duty cycle, we define $n_H^{(i)}$ as the number of complete clock cycles that the signal is in high:

$$n_H^{(i)} = \lfloor n_H \rfloor \tag{27}$$

and $n_H^{(f)}$ as a variable that takes the value one when the signal has to be in high for half a clock cycle and cero when not; i.e.:

$$n_H^{(f)} = n_H \bmod 2 \,. \tag{28}$$

Using these definitions, the duty cycle for this transmitter is given by

$$DC = \frac{\sum_{i=1}^{n_H^{(i)}} T_a \cdot (1+\xi_i) + n_H^{(f)} \cdot T_a \cdot (\frac{1}{2}+\xi_i)}{\sum_{i=1}^{n_{T_{pri}}} T_a \cdot (1+\xi_i)} \,. \tag{29}$$

Introducing the worst case jitter values, the minimum and maximum duty cycles are obtained. Then, taking into account the requirements from the standard, we obtain the two duty cycle constraints for this transmitter:

$$\min(DC) = \frac{n_H^{(i)} + \frac{n_H^{(f)}}{2} - (n_H^{(i)} + n_H^{(f)}) \cdot \xi_{\max}}{n_{T_{pri}} \cdot (1+\xi_{\max})} \geq 0.45 \tag{30}$$

$$\max(DC) = \frac{n_H^{(i)} + \frac{n_H^{(f)}}{2} + (n_H^{(i)} + n_H^{(f)}) \cdot \xi_{\max}}{n_{T_{pri}} \cdot (1-\xi_{\max})} \leq 0.55 \,. \tag{31}$$

The accuracy of the backward link signal synthesized with this transmitter is the same as for the former transmitter, but this transmitter has no negative effect on the duty cycle, as the synthesized output signal is balanced.

3.4 Results

In order to comply with all the C1G2 specifications, the clock signal has to fulfil all the presented constraints. As some of these constraints depend on the implemented transmitter type, in the following, the clock constraints are evaluated separately for the three transmitters. The results have been obtained sweeping the range of possible values of all the parameters. *Tari*, *RTcal* and *TRcal* have been swept with a resolution of 1μs for both values of *DR*. The resolution in $1/T_a$ is of 1 kHz and of 0.1% in $\xi_{\max}$.

Fig. 6, Fig. 7 and Fig. 8 show the main constraints for a C1G2 digital core with a balanced half-T_{pri} base transmitter, an unbalanced half-T_{pri} base transmitter and a full-T_{pri} base transmitter, respectively. The results are presented in a two dimensional plot, where the horizontal axis represents $1/T_a$ and the vertical axis represents ξ_{max}. The forward link curve separates the ($1/T_a$, ξ_{max}) combinations that violate any of the forward link constraints from the ($1/T_a$, ξ_{max}) combinations that satisfy all of them. For the backward link, the constraints have been plotted separately, so that we can better see their effect in the clock source requirements. Any combination ($1/T_a$, ξ_{max}) inside the filled area fully complies with all the C1G2 clock requirements. Given a value of ξ_{max}, several ranges of compliant values of $1/T_a$ are found. The clock source implemented in the design has to generate a clock signal whose frequency is inside this range and its jitter is lower than the maximum allowed for the selected range.

If we analyse Fig. 6, we can observe that, for a digital core with a balanced half-T_{pri} base transmitter, it is possible to satisfy the C1G2 specifications with a clock frequency as low as 2.5 MHz. Nevertheless, in order to work in this region, the clock source needs to be very accurate and stable. We propose to work in the range (3.2 MHz-4.3 MHz) with looser requirements for the clock source stability and allowing a maximum jitter of 1%.

An unbalanced half-T_{pri} base transmitter allows synthesizing a more accurate *BLF* than with the balanced half-T_{pri} base transmitter. However, we can observe in Fig. 7 that this gain in accuracy has a negative effect in the duty cycle. As the duty cycle constraints are really restrictive in this case, the minimum clock frequency actually required is much higher than in the previous case. In fact, the clock frequency for such a design has to be higher than 6.4 MHz.

Fig. 8 shows that a C1G2 digital core with a full-T_{pri} base transmitter obtains the best results related to the clock constraints. A wide secure operating region is found at $1/T_a$ = 1.9 MHz with ξ_{max}=0.5%. Moreover, with an accurate enough clock source, it is possible to satisfy the C1G2 clock signal constraints with a clock frequency as low as 1.30 MHz.

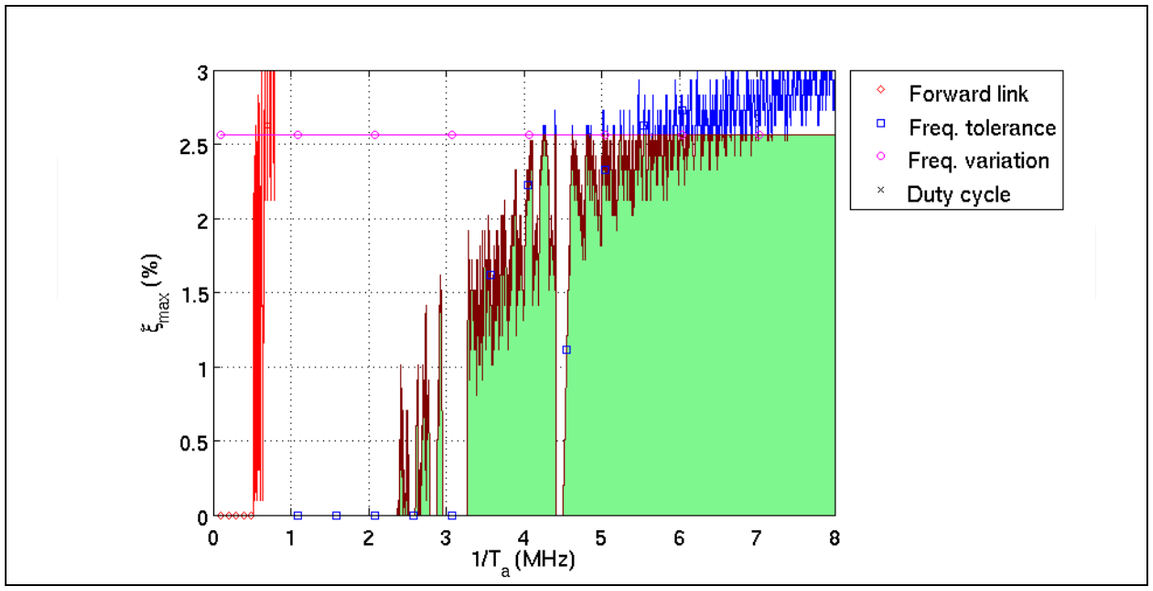


Fig. 6. Clock frequency constraints for C1G2 digital core with a balanced half-T_{pri} base transmitter.

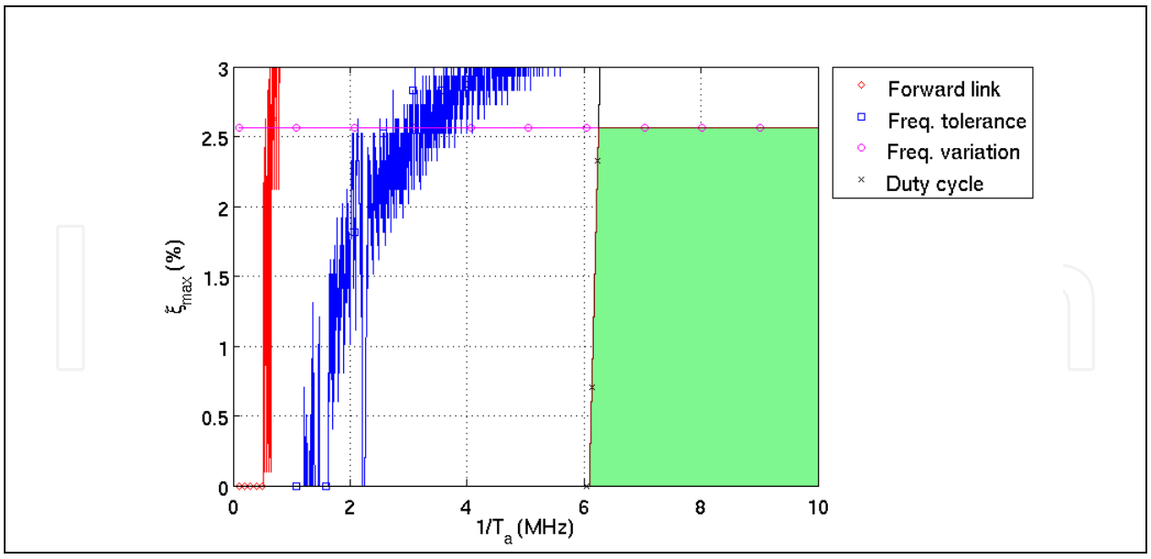


Fig. 7. Clock frequency constraints for C1G2 digital core with an unbalanced half-T_{pri} base transmitter.

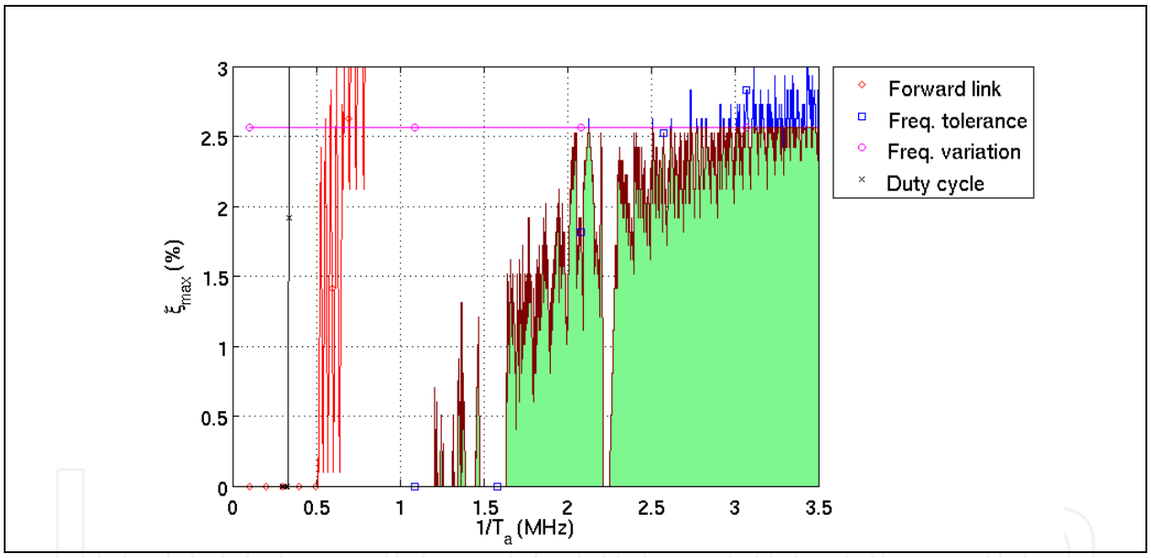


Fig. 8. Clock frequency constraints for C1G2 digital core with a full-Tpri base transmitter.

4. Energetic study

As explained in Section 1.2, the communication range of the system is strongly related to the power consumption of the tag. However, these power constraints are obtained assuming that the reader transmits a constant amount of power and that the tag also consumes power uniformly. None of these assumptions is true when the communication between reader and tag starts. The signal emitted from the reader is modulated, so that there is no continuous energy input at the tag. Moreover, the power consumption of the tag usually changes during the communication process. Thus, it is necessary to perform an energetic study to analyze the real behaviour of passive tags, and to understand the real limitations of the system.

The C1G2 communication protocol specifies that the forward link communication shall be ASK with a modulation depth of 90%, and the backward communication can use ASK or PSK backscattering. During the forward link the RF envelope is modulated with pulses of duration PW as shown in Fig. 9. High PW favours a clear communication. Low PW, instead, minimizes the time periods with no input power. The C1G2 standard defines the limits of acceptable PW values.

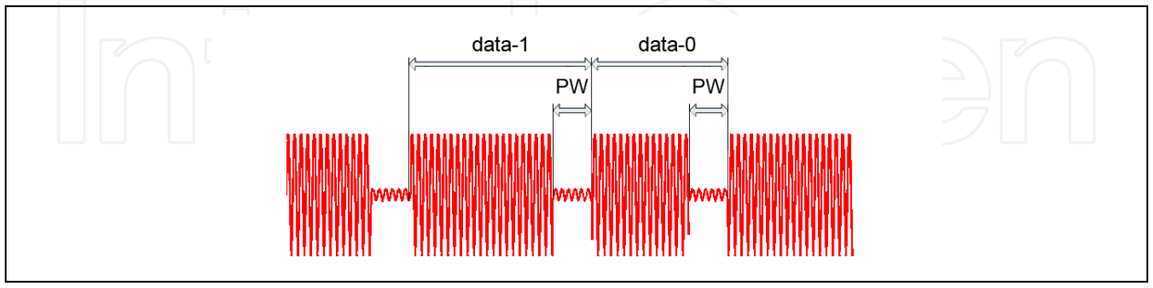


Fig. 9. Modulated RF signal during downlink communication.

Assuming that the power received during PW is negligible, the supply capacitor will supply the energy required by the rest of the tag. This will produce an energy discharge during PW. A similar effect occurs when the tag replies to the reader backscattering the received signal. The modulation in the backscattered signal is produced switching the reflection coefficient of the antenna between two states to differentiate a '0' from a '1'. Thus, the tag can communicate with the reader, but cannot receive all the energy of the input signal. The energetic discharge of the supply capacitor causes a drop in the supply voltage. This voltage drop is related with the discharged energy amount and with the value of the supply capacitor, C_{supply}. As the circuitry of the tag requires a minimum supply voltage to work, energetic constraints can be obtained for the value of C_{supply}. Moreover, the C1G2 standard specifies the minimum charge time of the tag, which also limits the value of C_{supply}.
This section is organized as follows. First, we present the models employed to analyze the energetic behaviour of the tag. An expression is obtained for the constraint on the maximum value of C_{supply} and expressions that can be used to evaluate the constraint on the minimum value of C_{supply} are presented. Next, we describe the methodology to evaluate the constraint on the minimum C_{supply}. Finally, a case study is presented as example.

4.1 Tag model

In order to perform the energetic analysis, a simplified model of the tag is defined. The model is divided into three sub models, each of one representing a specific state of the RFID communication. The first model represents the behaviour of the tag during the charge of the supply capacitor. In this model, it is assumed that the front-end of the tag includes power on reset (POR) circuitry. This POR block is usually included in RFID front-ends in order to switch on the tag only after the supply capacitor has been charged. This way, the tag consumes almost no power during the charge period allowing a faster charge and avoiding uncontrolled activity in the tag due to low supply voltage. The second model describes the energetic behaviour of the tag when the supply capacitor is charged, all the circuits are working and a continuous power is arriving to the antenna. Finally, the third model describes the behaviour of the tag when the input wave is modulated, and times of period with no input power are present.

In order to calculate the available power in the tag, the Friis equation is used to estimate the power available in the antenna, and the power conversion efficiency factor of the tag is applied. The power available in the tag is given by

$$P_{IN} = P_{EIRP} \cdot (\frac{\lambda}{4\pi r})^2 \cdot G_{TAG} \cdot \eta \tag{32}$$

where P_{EIRP} is the equivalent isotropic radiated power emitted from the reader, λ is the wavelength of the operation frequency, r is the communication range, G_{TAG} is the gain of the tag antenna and η is the power conversion efficiency of the tag.
The characterization of the front-end includes the power conversion efficiency η, the power consumption of the tag P_{TAG}, the required minimum supply voltage V_{min} and the maximum allowed supply voltage V_{max}. The front-end creates a regulated voltage at V_{min} to supply the rest of the blocks of the tag. Moreover, the supply voltage is limited to V_{max}, so that the technology does not break.

4.1.1 Charge of C_{supply}

When the reader starts emitting power for the first time, the tag begins accumulating energy in the supply capacitor $C_{supply.}$ During this process, all the blocks of the tag remain switched off, so that all the incoming energy is stored in $C_{supply.}$ The model for this behaviour is shown in Fig. 10. It consists on a power source connected to $C_{supply.}$ This model is a simplified description of the behaviour of the tag during the charge process until the supply capacitor reaches the supply voltage $V_{min.}$ At this point, the POR switches all the modules of the tag on, and the behaviour of the tag changes.

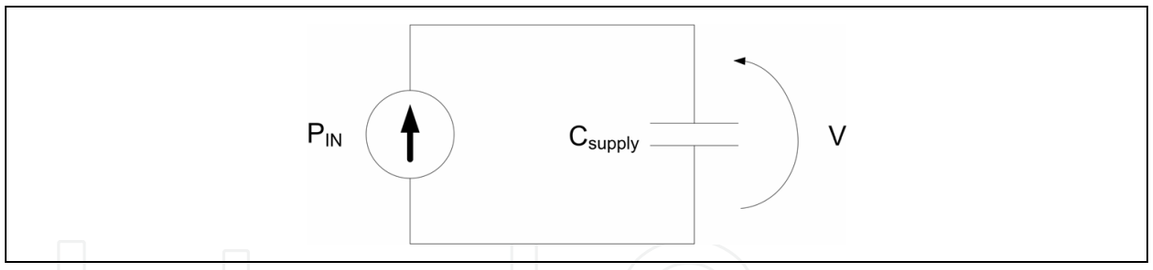


Fig. 10. Tag model during charge process of the supply capacitor.

The energy stored in $C_{supply,}$ is related with the voltage V as follows:

$$E = \int_0^Q \frac{q}{C_{supply}} dq = \frac{1}{2}\frac{Q^2}{C_{supply}} = \frac{1}{2} \cdot C_{supply} \cdot V^2 \,. \tag{33}$$

Given that the energy received during the time period t is equal to $P_{IN} \cdot t$, from (33), the charge time required for a specific C_{supply} to reach V_{min} is obtained as

$$t_{charge} = \frac{C_{supply} \cdot V_{\min}^2}{2 \cdot P_{IN}} \,. \tag{34}$$

Introducing the maximum charge time specified in the standard in (34), and isolating $C_{supply,}$ the maximum C_{supply} constraint is obtained,

$$C_{\max} = \frac{2 \cdot P_{IN} \cdot 1.5 \cdot 10^{-3}}{V_{\min}^2}. \quad (35)$$

This constraint depends on the available input power, and thus, it depends on the communication range between reader and tag.

4.1.2 Tag working with input power

Once V_{min} has been reached, more blocks in the tag are active and, thus, the power consumption of the tag increases. As the supply voltage of the different blocks is regulated, the power consumption of the tag does not change with the supply voltage at C_{supply}. Thus, the power consumption of the tag is inserted in the model as a power source in the opposite direction to the input power source. Fig. 11 shows the model of the tag with all the blocks switched on and receiving constant power from the reader.

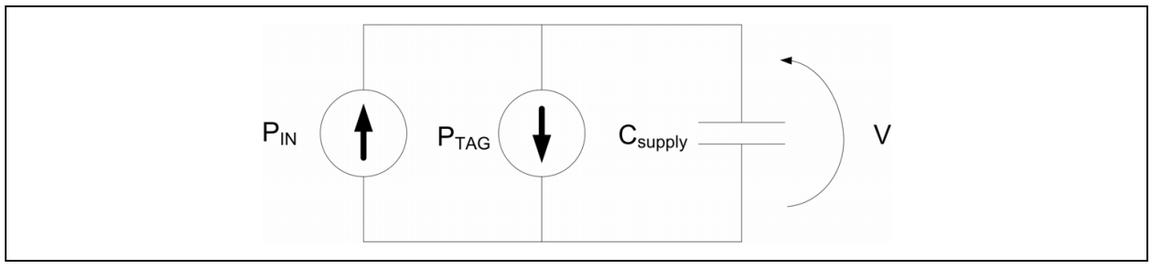


Fig. 11. Tag model receiving CW from the reader.

In this case, depending on the communication range, P_{IN} may be greater or lower than P_{TAG}. If $P_{IN} > P_{TAG}$, V_{supply} still receives some energy and keeps on charging. If $P_{IN} < P_{TAG}$, instead, C_{supply} has to provide the difference, and will discharge slowly. The maximum stable communication range is the one where $P_{IN} = P_{TAG}$. Eventually, this is the power limitation seen in Section 1.2.

Given that at t_0 the supply voltage had a value of V_0, the energy accumulated in the capacitor at this moment was

$$E_{t_o} = \frac{1}{2} \cdot C_{supply} \cdot V_{t_0}^2. \quad (36)$$

Considering a stable situation receiving continuous power from the reader between t_0 and t_1, the available energy in C_{supply} at t_1 is

$$E_{t_1} = E_{t_0} + (P_{IN} - P_{TAG}) \cdot (t_1 - t_0). \quad (37)$$

From (33), (36) and (37), the supply voltage at t_1 is obtained,

$$V_{t_1} = \sqrt{V_{t_0}^2 + \frac{2 \cdot (P_{IN} - P_{TAG}) \cdot (t_1 - t_0)}{C_{supply}}}. \quad (38)$$

4.1.3 Tag working without input power

When the real communication starts, the reader modulates the RF wave. During the modulation, periods of time with no input power exist. The same happens during the

backscattering of the answer. For these periods of time, the model shown in Fig. 12 is used. Both, the forward and backward modulation cause a voltage drop in C_{supply}.

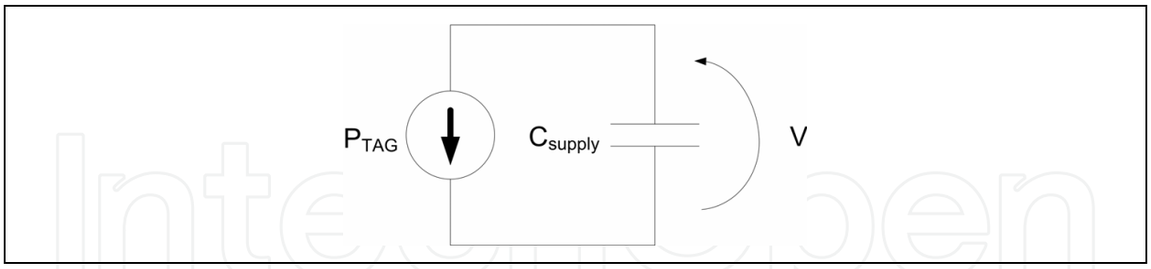


Fig. 12. Tag model receiving no power from the reader.

In this case, considering a stable situation when no input energy is received from the reader between t_1 and t_2, the energy at t_2 is given by

$$E_{t_2} = E_{t_1} - P_{TAG} \cdot (t_2 - t_1) \,. \tag{39}$$

And the supply voltage at t_2 is given by

$$V_{t_2} = \sqrt{V_{t_1}^2 - \frac{2 \cdot P_{TAG} \cdot (t_2 - t_1)}{C_{supply}}} \,. \tag{40}$$

4.2 Methodology for the energetic study

When a communication link is established, the RF wave is modulated in order to transport information, and the input power available in the tag is variable. This can cause a drop in the supply voltage. If the supply voltage drops below a minimum voltage value, V_{min}, the tag operation can fail.

Analysing (38) and (40), we can observe that the supply voltage at a certain instant depends both on C_{supply} and on the power consumption of the tag. When power management techniques are applied to a design, this power consumption can be very variable in time. Additionally, different commands and forward and backward frequencies produce different profiles of power consumption in the time. There will be a certain command and certain forward and backward frequencies that yield the maximum power consumption of the tag, P_{max}. Given a communication distance (or a specific input power in the antenna), a minimum value of the supply capacitor, C_{min}, can be obtained that ensures that the supply voltage does not drop below V_{min} even if P_{max} is consumed.

4.2.1 Estimation of power consumption profile

Given a system $S = \{m_0, m_1, m_2, ..., m_{N-1}\}$ composed by N modules, the power consumption without power-management is given by

$$P_{TOTAL} = \sum_{m_i \in S} P_{m_i} \,. \tag{41}$$

However, when power management is implemented, different working states are defined depending on the activity of each module. In this case, a better characterization of the power

consumption is obtained determining the average power consumption of the design in every working state (WS) as

$$P_{WS} = \sum_{m_i \in WS} P_{m_i} + \sum_{m_j \notin WS} P_{leakage_{m_j}} + P_{m_{PM}}, \quad (42)$$

where m_{PM} is the new power management module introduced to generate the clock gating control signals for the modules. The average power consumption of the different modules of the design can be determined making them work independently at full load.
Combining the power consumption during each working state and the time spent in each of them, the profiles of the power consumption for all possible commands and configurations are obtained.

4.2.2 Selection of the optimum value of C_{supply}

Equation (38) can be used to analyse the voltage drop during the charge and equation (40) during the discharge. The power profile that causes the highest voltage drop is considered to be the worst power profile. The search for the worst case shall consider the different commands and configurations. Given a value of C_{supply}, there is a maximum value of the communication range where the supply voltage does not fall below V_{min} in the worse case. Thus, for each value of C_{supply} the maximum communication range can be obtained.
On the other hand, for each communication range, the constraint defined in (35) sets an upper limit on the value of the supply capacitor, C_{max}. Taking into account the C_{min} constraint caused by the modulation of the RF wave and the C_{max} constraint set by the maximum charge time established by the C1G2 standard, the optimum value of C_{supply} can be selected.

4.3 Case study

In the following example, a front-end which consumes 25 μW and has an efficiency of η =30% is assumed. The voltage limiter of the front-end is assumed to be set to 2.0 V, and the lower limit of the voltage, V_{min} to 1.2 V. P_{EIRP} is set to 2 W, which is the maximum power emission allowed in Europe for RFID communication at the operation frequency of 868 MHz, and G_{TAG} is set to 1 assuming an ideal isotropic antenna. The clock signal has been set to 1.5 MHz and the typical PVT operating conditions have been used.
Using the procedure described in Section 4.2.1, the power consumption in the five working states defined in Table 1 can be obtained. As the activity of the input signal depends on the forward link frequency determined by *Tari*, the actual power consumption of the design in RX working state also depends on the value of *Tari*. Similarly, the activity of the output signal depends on the *BLF* employed. Thus, when presenting any power consumption result of C1G2 digital cores, the configuration of the forward and backward links has to be specified. There is a lack of information about these parameters in the literature, where the results obtained are presented without further specifications.
If we know the power consumption of the tag in each working state for all values of Tari and *BLF*, the power consumption profile of any command can be generated. As an example, Fig. 13 (a) shows the power consumption profile of a *Read* command with *Tari* = 25 μs and *BLF* = 40 kHz. The *Read* command in this example requires that the whole EPC bank (96 bits) is read. It can be observed that the power consumption changes from one working state to another.

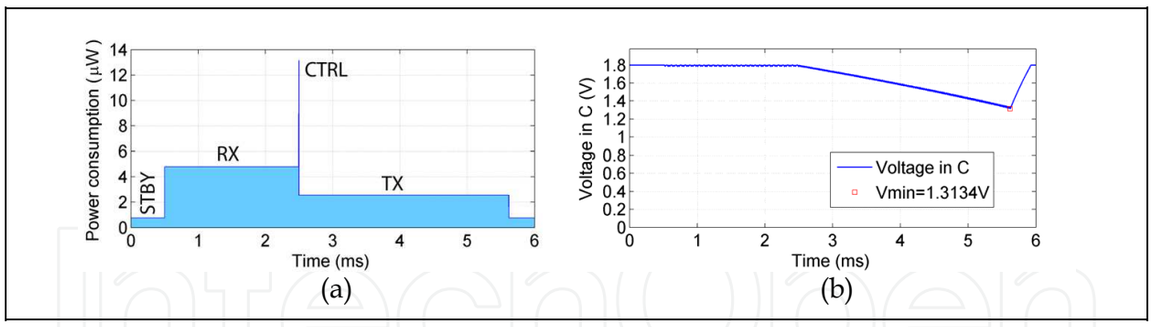


Fig. 13. Power distribution and voltage drop of a *Read* command for *Tari* = 25 μs and *BLF* = 40 kHz.

4.3.1 Worst command

In order to determine the worst command, the power distribution of every command in the C1G2 standard must be obtained, as well as the voltage drop caused by them in the supply capacitor. As an example, for *Tari* = 25 μs and BLF = 40 kHz, Fig. 13 (b) shows the voltage drop caused by the *Read* command. In this case, the time that the tag has to recover energy per received symbol is greater than the recovery time per transmitted cycle. Thus, even though the power consumption in RX is higher than in TX, the voltage drop caused by the reception of the command is smaller than the voltage drop caused by the transmission of the answer.

In our example, the final voltage in the supply capacitor is 1.3134 V. This is the greatest voltage drop in the supply capacitor produced by any EPC command for the design considered in our case study. This is due to the fact that the *read* command of the whole EPC bank is one of the longest commands received by the tag and requires the transmission of the largest amount of data. Thus, in order to characterize our digital core, the average power consumption for a *Read* command requesting the data of the biggest memory bank shall be used.

4.3.2 Worst configuration

The effects of employing different forward and backward data rates shall also be studied. The worst case *Read* command will be used to study the effect of the backward link configuration. However, in this command, the voltage drop caused by the forward link is mostly covered by the voltage drop caused by the backward link. Thus, results for the command with longest forward link communication, *Select*, will be also presented to observe the effects of *Tari*.

Fig. 14 presents the power distribution and supply voltage drop of the worst case *Read* command for *Tari* = 25 μs and *BLF* = 640 kHz. If we compare these results with the ones shown in Fig. 13, we can observe that the power consumption during the TX working state reduces as lower *BLF*s are employed. However, reducing *BLF* makes the communication slower and requires that that tag stays more time in the TX working state. At the end, this produces a bigger voltage drop in the supply capacitor. In order to maximize the communication range of C1G2 RFID systems, a high *BLF* configuration is suggested. However, in order to characterize our digital core, results with the lowest BLF shall be used, i.e.: BLF = 40 kHz.

Fig. 15 shows the power distribution and supply voltage drop of the *Select* command for *Tari* = 6.25 μs and *BLF* = 240 kHz. Fig. 16 presents the power distribution and supply voltage

drop of the same command for *Tari* = 25 µs and *BLF* = 240 kHz. Comparing both configurations, it can be observed that for higher values of *Tari* the power consumption in the RX working state is reduced and, thus, the discharge of the supply capacitor slows down. However, as the forward link frequency is reduced, the time required to transmit the same number of symbols increases. Due to this fact, the supply voltage drop at the end of the operation is greater with a high *Tari*. Thus, the communication range of a C1G2 RFID system may be increased by configuring low *Tari* values. In order to ensure the correct operation of the tag in any case, the characterization of the digital core has to be done with the worst case forward link configuration, which is *Tari* = 25 µs.

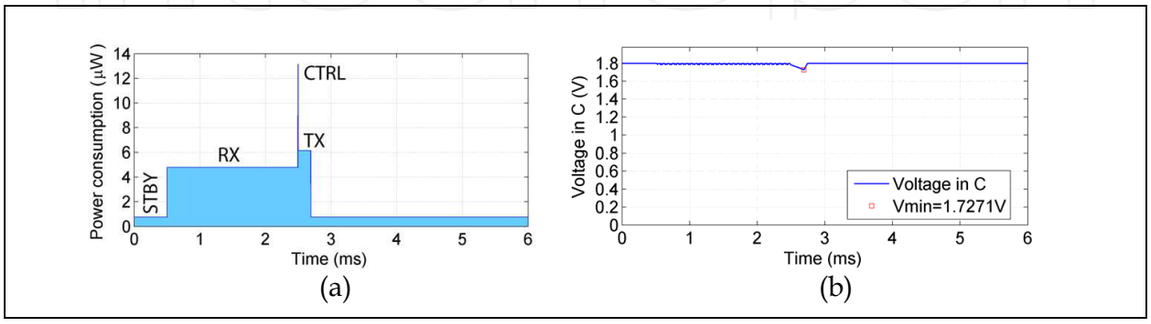


Fig. 14. Power distribution and supply voltage drop of the *Read* command for *Tari* = 25 µs and *BLF* = 640 kHz.

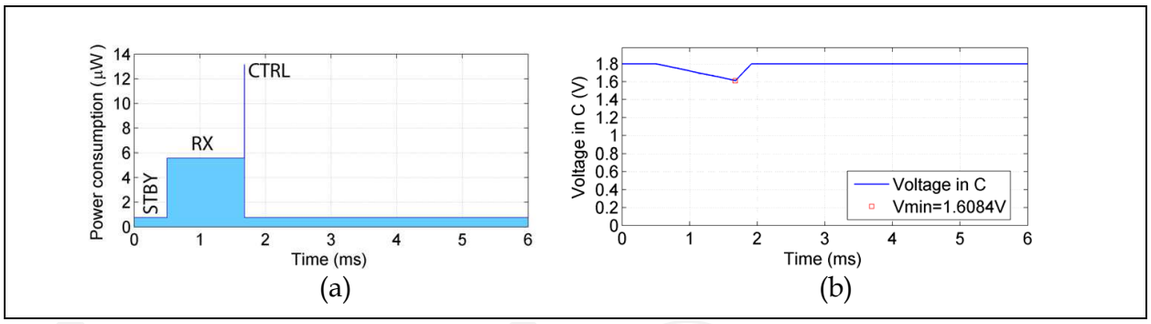


Fig. 15. Power distribution and supply voltage drop of the *Select* command for *Tari* = 6.25 µs and *BLF* = 240 kHz.

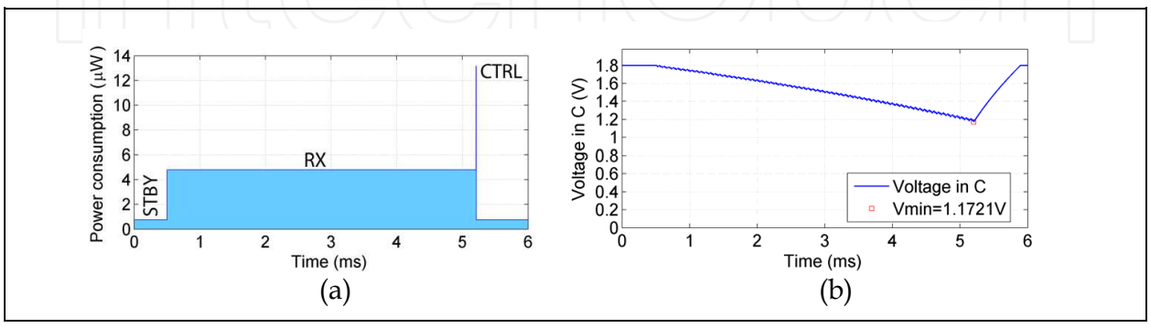


Fig. 16. Power distribution and supply voltage drop of the *Select* command for *Tari* = 25 µs and *BLF* = 240 kHz.

4.3.3 Energetic constraints

For the worst command and worst configuration, the energetic constraints have been calculated using the model described in Section 4.1 and the methodology described in Section 4.2.2. Fig. 17 shows the obtained results for our example. On the one hand, for operation points below the C_{min} constraint line, the supply capacitor is high enough to keep the supply voltage over V_{min}. On the other hand, C_{max} establishes the maximum value of the supply capacitor in order to fulfil the charge time specification. The area that is below both constraint lines is the operative region where the C1G2 standard is completely fulfilled.

In this case, with values of C_{supply} below 0.35 nF, the supply voltage always drops below V_{min}. The maximum communication range is achieved for values of C_{supply} above 90 nF. However, with such a capacity, the C_{max} constraint is violated. C_{supply} =30 nF is the point where both constraints cross. This is the value of C_{min} that maximizes communication distance fulfilling all the energetic constraints.

It can be observed in Fig. 17 that the dimensioning of C_{supply} has a relevant impact on the actual communication range. In this case, the system would work properly with a supply capacitor of 1 nF, but the communication range would be limited by the energetic constraint to 2.8 m. Increasing C_{supply}, the communication range is increased to 3.3 m.

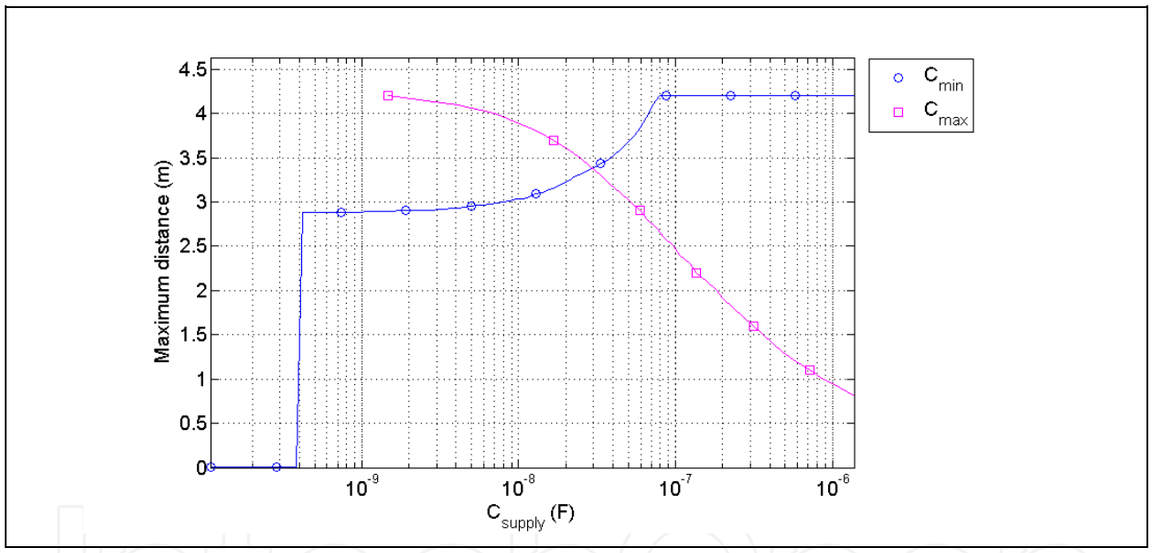


Fig. 17. Maximum distance achievable for different values of C_{supply}.

5. Conclusion

A communication link standard poses many constraints to the clock of the digital core of a tag for proper forward-link data detection and backward-link data backscattering. For the C1G2 standard, the backward link requirements are the ones that set the most restrictive constraints. There are several frequency bands where the C1G2 specifications are fulfilled. Depending on the characteristics of the clock source, such as the average period and the maximum jitter, and on the type of transmitter, the most suitable operation point can be selected using the results presented in Section 3.

In the literature, the average power consumption is usually presented to characterize a tag. However, we have seen in Section 4 that this value is not enough. Due to the energetic

behaviour of the tag, the communication range is also limited by the value of C_{supply}. Moreover, this constraint depends on the profile of the power consumption, which changes from one command to another and from one communication mode to another. In order to obtain a complete characterization of the proposed design, a procedure as the one shown in Section 4.3 shall be followed.

6. References

Barnett R., Balachandran G., Lazar S., Kramer B., Konnail G., Rajasekhar S. & Drobny V. (2007). A passive UHF RFID transponder for EPC Gen 2 with -14dBm sensitivity in 0.13 µm CMOS, *Digest of Technical Papers of the IEEE International Solid-State Circuits Conference,* pp. 582-623, ISBN: 978-1-4244-0853-5, San Francisco (USA), February 2007, IEEE, Piscataway (USA)

De Vita G. & Annaccone G. (2005). Design criteria for the RF section of UHF and microwave passive RFID transponders, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 9, September 2005, pp 2978-2990, ISSN: 0018-9480

EPC Global (2005). Specification for RFID air interface. EPC Global Class-1 Gen-2 UHF RFID Version 1.0.9

Hong Y., Chan C. F., Guo J., Ng J. S., Shi W., Leung L. K., Leung K. N., Choy C. S. & Pun K. P. (2008). Design of Passive UHF RFID Tag in 130nm CMOS Technology, *Proceedings of IEEE Asia Pacific Conference on Circuits and Systems,* pp. 1371-1374, ISBN: 978-1-4244-2341-5, Macao, December 2008, IEEE, Piscataway (USA)

Impinj (2006). Gen 2 Tag Clock Rate - What You Need To Know

ISO (2006). ISO18000-6C, Information technology Radio frequency identification for item management Part 6: Parameters for air interface communications at 860 MHz to 960 MHz, Amendment 1, June 2006

Man A. S. W, Zhang E. S., Chan H.T., LauV. K.N., Tsui C.Y. & Luong H. C. (2007). Design and Implementation of a Low-power Baseband-system for RFID Tag, *Proceedings of International Symposium on Circuits and Systems*, pp. 1585-1588, ISBN: 1-4244-0920-9, New Orleans (USA), May 2007, IEEE, Piscataway (USA)

Pardo D., Vaz A., Gil S., Gomez J., Ubarretxena A., Puente D., Morales-Ramos R., García-Alonso A. & Berenguer R. (2007). Design Criteria for Full Passive Long Range UHF RFID Sensor for Human Body Temperature Monitoring, *Proceedings of IEEE International Conference on RFID,* pp. 141-148, ISBN: 1-4244-1013-4, Grapevine, March 2007, IEEE, Piscataway (USA)

Ricci A., Grisanti M., De Munari I. & Ciapolini P. (2008). Design of a 2 W RFID Baseband Processor Featuring an AES Cryptography Primitive, *Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems, ICECS,* pp. 376-379, ISBN: 978-1-4244-2181, St. Julien's, September 2008, IEEE, Piscataway (USA)

Roostaie V., Naja V., Mohammadi S. & Fotowat-Ahmady A. (2008). A low power baseband processor for a dual mode UHF EPC Gen 2 RFID tag, *Proceedings of International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS*, pp. 1-5, ISBN: 978-1-4244-1576-2, Tozeur, March 2008, IEEE, Piscataway (USA)

Wang J., Li H. & Yu F. (2007). Design of Secure and Low-cost RFID Tag Baseband, *Proceedings of International Conference on Wireless Communications, Networking and Mobile Computing*, pp. 2066-2069, ISBN: 978-1-4244-1311-9, Shangai, September 2007, IEEE, Piscataway (USA)

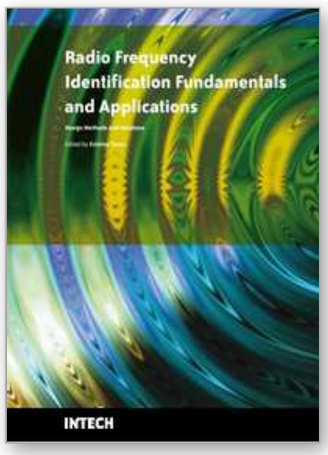
Wanggen S., Yiqi Z., Xiaoming L., Xianghua W., Zhao J. & Dan W. (2009). Design of an ultra-low-power digital processor for passive UHF RFID tags, *Journal of Semiconductors*, Vol. 30, No. 4, April 2009, pp. 045004-1-045004-4, ISSN: 16744926

Yan, H, Jianyun, H., Qiang, L. & Hao. M. (2006). Design of low-power baseband-processor for RFID tag, *Proceedings of the International Symposium on Applications and the Internet Workshops,* pp. 60-63, ISBN: 0-7695-2510-5, Phoenix, January 2006, IEEE Computer Society, Los Alamitos (USA)

Zalbide I., Vicario J. & Vélez I. (2008). Power and energy optimization of the digital core of a Gen2 long range full passive RFID sensor tag, *Proceedings of IEEE International Conference on RFID (Frequency Identification),* pp. 125-133, ISBN: 978-1-4244-1712-4, Las Vegas (USA), April 2008, IEEE, Piscataway (USA)

Zalbide I. (2009). *Design of a digital core for a C1G2 RFID sensor tag*, PhD. Thesis, Universidad de Navarra

Zhang Q., Li Y. & Wu N. (2008). A Novel Low-Power Digital Baseband Circuit for UHF RFID Tag with Sensors, *Proceedings of Solid-State and Integrated-Circuit Technology,* pp. 2128-2131, ISBN: 978-1-4244-2185-5, Beijing (China), October 2008, IEEE, Piscataway (USA)



Radio Frequency Identification Fundamentals and Applications
Design Methods and Solutions
Edited by Cristina Turcu

ISBN 978-953-7619-72-5
Hard cover, 324 pages
Publisher InTech
Published online 01, February, 2010
Published in print edition February, 2010

This book, entitled Radio Frequency Identification Fundamentals and Applications, Bringing Research to Practice, bridges the gap between theory and practice and brings together a variety of research results and practical solutions in the field of RFID. The book is a rich collection of articles written by people from all over the world: teachers, researchers, engineers, and technical people with strong background in the RFID area. Developed as a source of information on RFID technology, the book addresses a wide audience including designers for RFID systems, researchers, students and anyone who would like to learn about this field. At this point I would like to express my thanks to all scientists who were kind enough to contribute to the success of this project by presenting numerous technical studies and research results. However, we couldn't have published this book without the effort of InTech team. I wish to extend my most sincere gratitude to InTech publishing house for continuing to publish new, interesting and valuable books for all of us.

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen