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Power Electronic Converters for Microgrids

Wenlong Ming

Abstract

Power electronic converters are indispensable building blocks of microgrids. They are the enabling technology for many applications of microgrids, e.g., renewable energy integration, transportation electrification, energy storage, and power supplies for computing. In this chapter, the requirements, functions, and operation of power electronic converters are introduced. Then, different topologies of the converters used in microgrids are discussed, including DC/DC converters, single-phase DC/AC converters, three-phase three-wire, and four-wire DC/AC converters. The remaining parts of this chapter focus on how to optimally design and control these converters with the emerging wide-bandgap semiconductors. Correlated tradeoffs of converter efficiency, power density, and cost are analyzed using Artificial Neural Networks to find the optimal design of the converters.

Keywords: power electronics, DC/AC, DC/DC, control, topology, wide-bandgap semiconductor, multi-objective design

1. Introduction

Power electronic converters are essential building blocks in a microgrid, which enable the connection into microgrids of renewable energy resources, energy storage systems, and electric vehicles (EVs), [1–3]. A power electronic converter consists of power semiconductor switches, passive components (inductors, capacitors, transformers, etc.), and a control unit to manage the power conversion and power flow. The main role of power electronic converters is to convert power from one form to another. In addition, power electronic converters can achieve flexible control of active/reactive power fed into the microgrid [4], maximum power point tracking (MPPT) of photovoltaic (PV) cells [5], and wind turbines [6]. The flexible controllability of power electronic converters in microgrids also enables high-level computation and optimization of the microgrid operation and management [7, 8].

Typical power electronic converter-based microgrids are shown in **Figure 1**. This shows a hybrid AC/DC microgrid, which consists of an AC microgrid and a DC microgrid interconnected by an interfacing converter. The microgrid works in grid-connected mode when the utility grid is connected to the AC bus and in stand-alone mode when the utility grid is disconnected.

In an AC microgrid, power electronic converters are used to convert DC power (from PV cells, batteries, EVs, etc.) or variable frequency AC power (from wind turbines) into 50/60 Hz AC power so that the power can be fed into the AC bus and supply loads. In a DC microgrid, power electronic converters are used to convert AC power or DC power with different voltages into DC power with the same
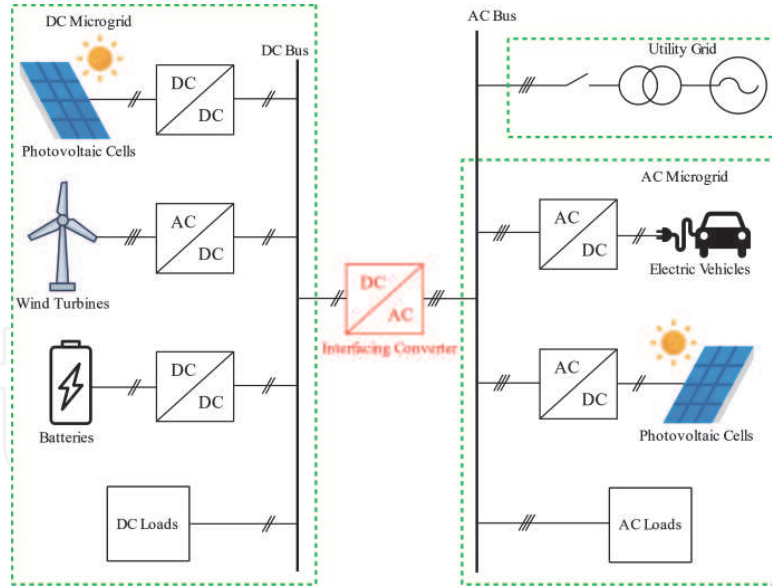
Figure 1.
Power electronic converters in microgrids.

voltage as the DC bus of the DC microgrid. As shown in **Figure 1**, power electronic converters can also be used as the interface between AC and DC microgrids to manage the power flow [9].

Power electronic converters in microgrids use various topologies, according to different applications. Based on the input and output power, power electronic converters can be classified as DC/DC converters and DC/AC converters. DC/DC converters convert the input DC voltages and currents into controlled output DC voltages and currents. DC/AC converters convert DC inputs into controlled AC outputs or vice versa. In microgrids, the DERs can be either DC power or variable AC power.

The control of the power electronic converters ensures that the microgrid functions well in all circumstances [9–11]. In the grid-connected mode when a microgrid is connected to the utility grid, converters in the microgrid operate in grid-feeding mode to provide active and reactive power from distributed generators to the microgrid [12]. In the stand-alone mode when a microgrid is isolated from the utility grid, converters in the microgrid operate in grid-forming or grid-supporting modes to provide AC voltage and frequency support to the microgrid [13]. Besides, converters connected to the energy storage systems and EVs also need to work in battery charging mode to charge the batteries [14]. The different operation modes of power electronic converters require different control algorithms. Converters in the microgrid need to switch between different operations modes according to the status of the microgrid and distributed generators [15, 16].

The design of power electronic converters attempts to meet the system requirements of efficiency, power density, costs, and reliability [17]. However, these factors usually contradict each other. For example, an increase in reliability usually implies higher equipment costs. The power density of a converter can be increased by increasing the switching frequency, which, however, inevitably brings increased switching losses and reduces the overall efficiency. Therefore, tradeoffs must be made between these factors, which requires a multi-objective optimization to find the Pareto-optimal solutions so that the designers can choose the most suitable solution to meet the requirements of a specific application [18].

The rest of this chapter is organized as follows. Firstly, topologies of power electronic converters for microgrids are introduced, including their working principles and applications. Then, an advanced design methodology of power electronic

converters based on multi-objective optimization considering the cost, efficiency, and power density is presented. Finally, the control algorithms of power electronic converters for different operation modes in the microgrid are summarized.

2. Converter topologies

2.1 DC/DC converters

DC/DC converters are used to create either a higher or lower constant DC voltage at the output without being affected by possible fluctuations of the DC input voltage or of the load current. These converters are essential for the operation of devices in various industry areas such as renewable energies, automotive, battery chargers and aerospace.

They use semiconductors that behave like switches that are opened and closed to convert an input voltage level into a different one, applying a series of control signals. Generally, the way the voltage is converted is by forcing energy to be stored in an inductor or capacitor When the polarity is reversed, the energy stored is discharged creating a voltage at the converter output.

Among the different control methods, the most popular one is pulse width modulation (PWM), which regulates the output voltage through adjusting the on and off times of the semiconductors. A Duty Ratio D is defined as the ratio between the on and off time of the semiconductors in a switching period. The output voltage is regulated by controlling the value of D, which is between 0 and 1 [19].

2.1.1 Buck converter

The buck converter is shown in **Figure 2**. creates an output voltage that is lower than the input voltage V_{in}. The average output voltage V_o is a function of the duty ratio according to the expression:

$$V_o = D \, V_{in} \tag{1}$$

The voltage V_o is controlled by varying the duty ratio D of the switch S. This is a linear relationship for ideal conditions. When the switch is on, the diode is reverse biased and so the input current flows through the inductor L. When the switch is off, the diode conducts so the energy stored in the inductor passes through the diode supplying part of this stored energy to the load. The capacitor at the output is used to keep the average value of the output voltage constant [20].

2.1.2 Boost converter

The boost converter in **Figure 3** shows the circuit topology, where the main function is to obtain a higher DC voltage at the output than its input DC voltage. It contains at least one semiconductor switch and elements to store energy.
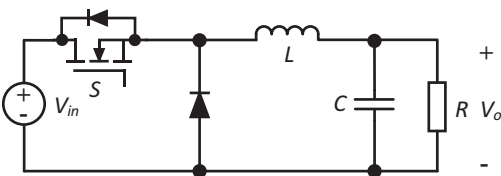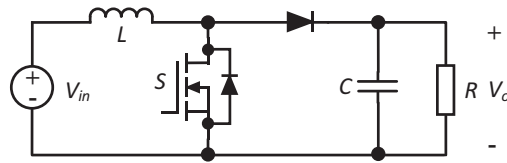

Figure 2.
Buck converter.

Figure 3.
Boost converter.

When the switch S is closed, the inductor stores energy from the source, at the same time the load R is fed by the capacitor (C). When the switch is open, the only path of the current is through the diode, and current flows to the capacitor and the load [21].

$$V_o = \frac{V_{in}}{1 - D} \qquad (2)$$

Since the output voltage is inversely proportional to $(1 - D)$, a higher duty ratio gives a higher output voltage.

2.1.3 Buck-boost converter

A buck-boost converter is used if the desired output voltage may be higher or lower than the input DC voltage.

Figure 4 shows a buck-boost converter, which is a cascaded connection between a buck converter and a boost converter. In steady-state, the ratio between the input and output voltages is the product of the ratios of both converters as:

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D} \qquad (3)$$

When the switch is closed, the input provides power to the inductance and the diode is reverse biased. When the switch is open, the energy stored in the inductance is transferred to the output while the input does not provide power to the load. As in the previous converters, in steady-state the capacity of the output capacitor is large enough so that the output voltage Vo is constant [22]. The output voltage is reversed inside.

2.2 DC/AC single-phase converters

A DC/AC converter also known as an inverter is capable of transforming DC into AC. A single-phase inverter is shown in **Figure 5**. It is often used, for small loads and power supplies.

Single-phase inverters are fundamental parts of solar PV generating systems that convert from DC into AC, allowing the power generated to be supplied to a network with fixed voltage and frequency [23]. Another application is in battery storage
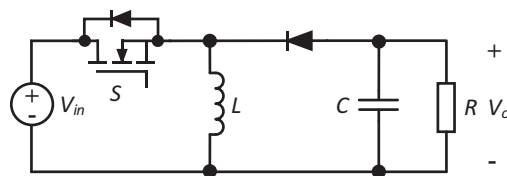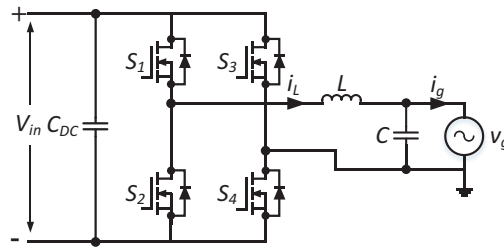

Figure 4.
Buck-boost converter.

Figure 5.
Singe-phase DC/AC inverter.

systems, which are able of accumulating energy for later use when there is not enough solar resource to cover the load demand, using a single-phase inverter to obtain the voltage level and the frequency necessary to be connected to the main grid [24, 25].

Single-phase inverters when connected to the grid under unbalanced conditions, can propagate second-order harmonics from AC to DC side. The power for the grid side P_g is defined as:

$$P_g = V_g I_g = VI \cos^2 \omega t = \frac{VI\left(1 + \cos 2\omega t\right)}{2} = \frac{VI}{2} + \frac{VI}{2} \cos 2\omega t \qquad (4)$$

V_g and I_g represent the grid voltage and current respectively, meanwhile, the angular grid frequency f is defined as $\omega = 2\pi f$. As second-harmonics are present in the DC side, large DC capacitance is required to support second-order ripples [26].

2.3 Three-phase DC-AC converters

The principle for operating three-phase DC-AC converters is similar to that of a single-phase converter. The essential difference is that instead of having a single modulated signal, there are three sinusoidal modulated signals out of phase 120° between them. These signals are compared with a triangular signal for the control of the switches at three phases. The voltage signals obtained in the phases with respect to the neutral are identical to those of the single-phase modulation, but instead of having a single signal, there are three signals out of phase by 120°. Therefore, the same theory can be applied for single-phase converters.

A conventional two-level three-phase inverter consists of six switches generating an output voltage with two values with respect to the negative terminal of the input capacitor as shown in **Figure 6** [27].

The development of 3-level or multilevel technology has been influenced by the development of new wide-bandgap materials for the construction of semiconductors as IGBT and MOSFET, allowing high voltage and current operation and higher switching frequency obtaining lower harmonic distortion at the output [28].
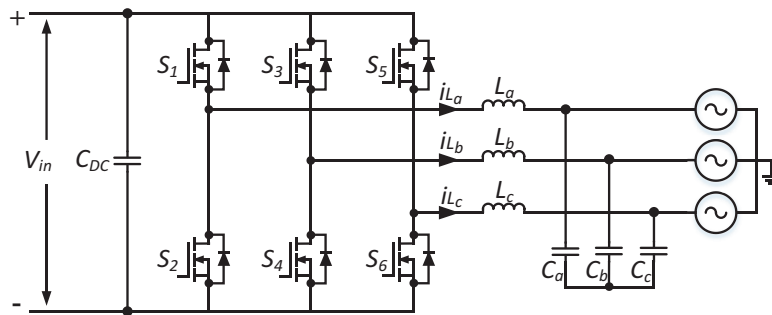

Figure 6.
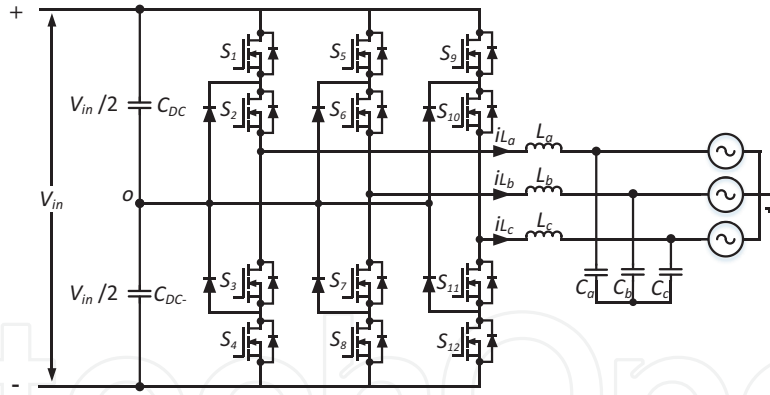*Three-phase two-level DC/AC inverter.*

Figure 7.
Three-phase three-level DC/AC neutral-point-clamped inverter.

A popular three-level inverter is the Neutral Point Clamped Converter. This inverter can be considered as the origin of the recent multi-level inverter and has been widely studied and applied. The topology is shown in **Figure 7**.

In this type of inverter, each leg consists of four switching devices clamped by two diodes. The DC bus voltage is divided by two capacitors connected with the clamped diodes, granting the neutral point (o). The output voltage in each phase can take three levels, $V_{in}/2$, 0, and $V_{in}/2$.

The diodes connected to the midpoint are the elements that set the blocking voltages of the switches to a fraction of the DC bus voltage; therefore, they are the key elements of this topology. This topology can be extended to more levels but the number of switching devices used is greatly increased [29].

2.4 Three-phase four-wire converters

Three-phase four-wire converters consist of three half-bridges that distribute phases A, B, and C, and an additional leg allows the path of the neutral currents.

One of the most attractive applications of these inverters is electric vehicle EV chargers, allowing both charging the EV in the grid to vehicle G2V mode and vehicle to grid mode V2G. The V2G mode can generate an autonomous network by obtaining energy from the EV battery to the grid when there are high energy demands or blackouts, being EV chargers susceptible to power quality problems when there is an imbalance due to loads in the grid [30].

Ideally, the operation of a distribution system is that all the loads that are connected are of the same magnitude which results in the balanced operation of the system. However, any practical system is always operating in unbalanced conditions, leading to overheating, losses and malfunction in transformers, protection systems and cables connected to the network.

Three common topologies being used in microgrids for four-wire systems are Split DC-Link, four-leg three-phase inverter, and independently-controlled neutral leg.

2.4.1 Three-phase four-wire inverter with Split DC-link capacitor

This basic typology consists of only six switches S_1-S_6 as seen in **Figure 8**. containing a neutral point being clamped to the DC bus inverter, resulting in two voltage levels through the DC-link capacitors.

Zero-sequence current causes voltage ripple at the midpoint of the inverter, therefore large capacitors are required to reduce the voltage ripples. To share the
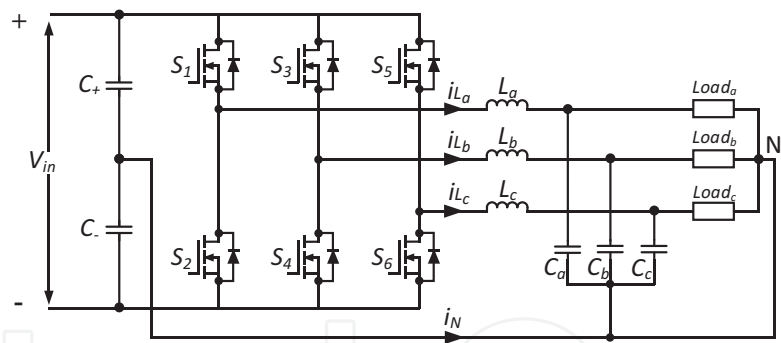
Figure 8.
Three-phase four-wire DC/AC inverter with split DC-link capacitors.

input DC voltage evenly, the voltages of the two divided DC link capacitors must be controlled [31].

One of the disadvantages of this typology is that large neutral currents, are reflected in voltage ripple in the capacitors.

2.4.2 Three-phase four-wire DC/AC inverter with neutral leg

Figure 9 shows the configuration of this inverter, where switches S_1-S_6 feed the ABC phases, while switches S_{N1} and S_{N2} provide the neutral current line. An advantage of this converter is that the capacitor does not need to be bulky to reduce the second-order ripples in the DC-link, but its control strategy is more complex than the previous converter. Additionally, there is a 15% gain in AC output voltage with respect to the DC voltage. As the additional leg cannot be controlled independently, the control complexity of maintaining balanced voltages on the AC lines as well as maintaining the neutral point can be experienced great stress on the DC terminals causing electromagnetic interference (EMI) [32].

2.4.3 Three-phase four-wire DC/AC inverter with an independently-controlled neutral leg

Similar to the three-phase neutral leg inverter, the topology in **Figure 10** is configured with eight switches in total, being S_1-S_6 for ABC phases and S_{N1}-S_{N2} for a neutral current path to the mid-point between the two DC link capacitors. A large amount of capacitance is not required as there are no high current levels through the DC link capacitors.

This topology is highly preferred for use in unbalanced load conditions since the current flowing through the inductor allows the DC link to remain neutral.
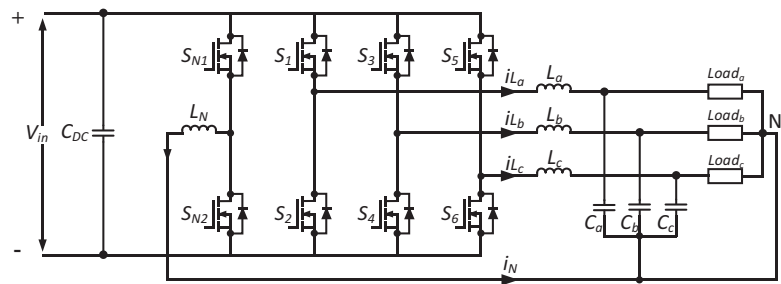

Figure 9.
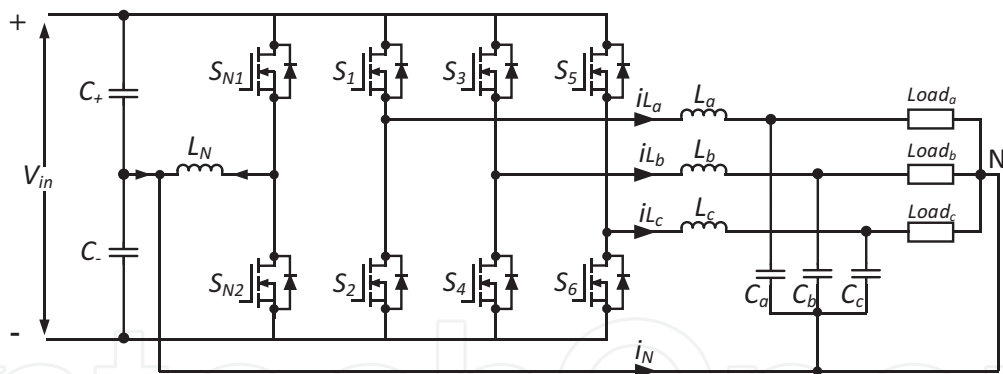*Three-phase four-wire DC/AC inverter with the neutral leg.*

Figure 10.
Three-phase four-wire DC/AC inverter with an independently-controlled neutral leg.

Its control strategy also allows the phases to be controlled independently as well as the neutral leg, avoiding stress on the DC link and other interferences. Another aspect is that by not presenting neutral current through the DC link capacitors; small capacitors can be used and power density will be increased [32].

3. Design of wide-bandgap semiconductors based power electronics converters

3.1 Benefits of wide-bandgap semiconductors

Wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have superior material properties for power electronics compared to conventional Silicon (Si) as shown in **Figure 11**. The semiconductor properties have been characterized by the electric field, energy gap, electron velocity, melting point, and thermal conductivity.

Power switches based on WBG semiconductors have better switching and conduction performance over a wide range of temperatures in comparison to Si-based devices. For instance, they have a faster switching speed, lower switching losses, higher breakdown voltages, and higher operating temperatures. Therefore, WBG devices are considered promising solutions for high-efficient power electronics designs. These properties enabled the devices to achieve better performance for
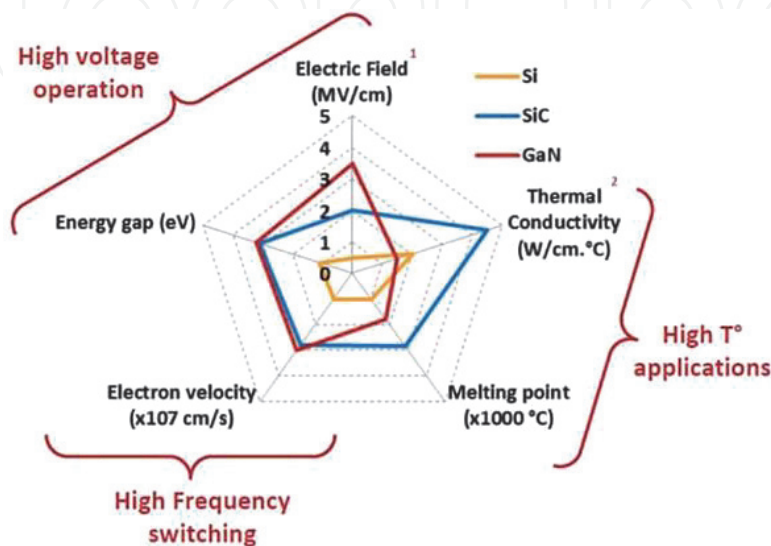

Figure 11.
The properties (and implications for operation) of Si, SiC, and GaN.

applications that require high voltage operation, high temperature, and high switching frequency.

3.2 Design challenges of WBG power converters

A well-designed power electronic converter should have high efficiency, small volume, and lightweight, low cost, and low failure rate. However, the challenge is the trade-off between these performance measures. For example, if a design is focused only to achieve higher efficiency, which impacts the power density, reliability, and cost. The performance parameters must be simultaneously optimized, such as maximizing efficiency while reducing volume, reliability, and cost as much as possible. Typical technical performance measures are efficiency, volume, cost, and reliability as depicted in **Figure 12**. These measures are mainly determined by the design of the converter including selections of topology, modulation scheme, components, and layout. By carrying out the careful design of the converter, the converter will have high power density, as well as reduced volume, weight, and cost.

3.3 Multi-objective design of WBG power converters

Multi-objective design is used to optimize the efficiency and volume of WBG power converters. To achieve this, Pareto fronts are determined. A Pareto front is the absolute limit of performance trade-off for a given set of converter specifications (topologies, control schemes, and components). Detailed mathematical modeling of the converter components is required for determining the Pareto fronts.

3.3.1 Modeling of power loss and volume of the inverter

In a single-phase inverter, the DC-link current is composed of both DC components and second-order ripple current. The second-order ripple current is occurred due to the unbalanced nature of single-phase systems. The conventional DC/AC inverter (see **Figure 5**) requires additional active or passive components to reduce the magnitudes of second-order ripple current. Instead, differential inverters can reduce the ripple current without adding extra components. As a result, Differential inverters are popular solutions for applications where reduction of second-order ripple current is critical and hence the differential inverters are modeled in this study.
Figure 11 shows the GaN switch-based differential inverter topology used to study the multi-objective design. The differential DC/AC inverter topology is
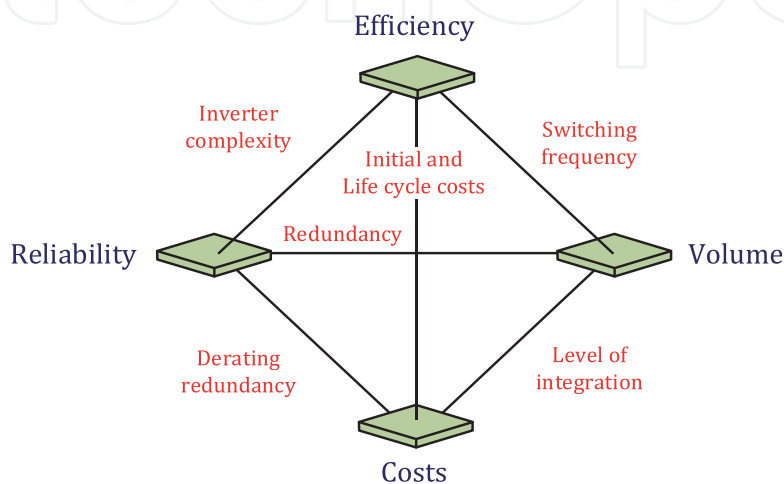

Figure 12.
The trade-off between design and performance parameters.

developed using two bidirectional DC/DC buck converters. In this study, the objectives are to optimize the efficiency and power density of a DC/AC buck inverter. To start with, the efficiency and power density of four major components within an inverter are modeled including the power GaN FETs, inductors, capacitors, and heat sinks. Their efficiency and power density are further determined by the variables including switching frequency f_{sw}, the inductor ripple Δi_L, the switch area A_{sw}, and the junction temperature ΔT_j. Therefore, it is of great importance to model the efficiency and power density based on these variables for each component.

3.3.2 Power GaN FETs

The power loss models of the GaN FETs are based on the on-state resistance $R_{DS,on}$, the output capacitance C_{oss} and the thermal junction-to-case resistance $R_{\theta JC}$ of the switches. The output capacitance C_{oss} represents the parasitic capacitance of the power GaN FETs. The value of C_{oss} is provided in the datasheet of GaN FETs. When the energy is stored into the output capacitor, current discharges through the body diode causes power loss [33]. These variables are scaled by their reference values with respect to the area of the switch. The switching loss of the inverter is the sum of the turn-on and turn-off loss of all the switches [33]. The switching loss of the higher side switches $P_{S_H,sw}(H = 1, 3)$ (see **Figure 13**) is obtained as,

$$P_{S_H,sw} = \frac{V_{in}f_{sw}}{2}\left\{\left(I_{out}\sin(\omega t) + i_{comp} - \frac{\Delta i_{L_a}}{2}\right)(t_{CR} + t_{VF})\right.$$
$$\left. + \left(I_{out}\sin(\omega t) + i_{comp} + \frac{\Delta i_{L_a}}{2}\right)(t_{VR} + t_{CF})\right\} \tag{5}$$

Where, i_{comp} is the second-order current component and Δi_{L_a} is the inductor current ripple. t_{CR} and t_{CF} are the rise and fall times for the current in the switch. t_{VR} and t_{VF} are the rise and fall times for the voltage in the switch.

The switching loss of the lower side switch $P_{S_L,sw}(L = 2, 4)$ can be derived as:

$$P_{S_L,sw} = \frac{V_{SD}f_{sw}}{2}\left\{\left(I_{out}\sin(\omega t) + i_{comp} + \frac{\Delta i_{L_a}}{2}\right)(t_{CR} + t_{VF})\right.$$
$$\left. + \left(I_{out}\sin(\omega t) + i_{comp} - \frac{\Delta i_{L_a}}{2}\right)(t_{VR} + t_{CF})\right\} \tag{6}$$
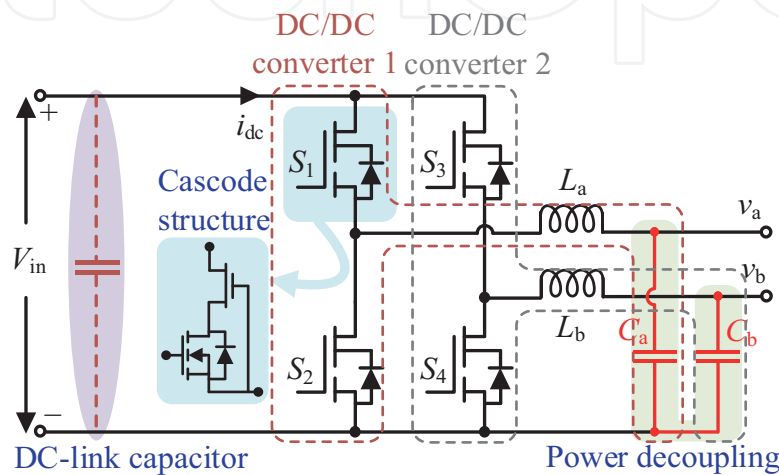

Figure 13.
Structure of a differential DC/AC buck inverter.

From (5) and (6), the total switching losses $P_{tot,sw}$ of the inverter are calculated as the sum of $P_{S_H,sw}$ and $P_{S_L,sw}$. The switching losses of higher side switches depend on the input voltage V_{in}, and lower side switches depend on the diode voltage V_{SD}. Hence, the lower side switches produced lesser switching losses compared to the higher side switches as V_{SD} is much smaller than V_{in}.

The conduction loss depends on the RMS current flowing through the switch $I_{RMS,sw}$, the on-state resistance $R_{DS,on}$ and the change in junction temperature ΔT_j. It will be varied according to the duty cycle of the switches $S_1 - S_4$. After applying the mathematical simplifications, the total conduction loss $P_{tot,cond}$ can be written as:

$$P_{tot,cond} = \left(\frac{R_{DS,on}^* A_{sw}^*}{A_{sw}}\right)\left(1 + \Delta T_j\right)\left\{\left(I_{out}^2 \sin^2(\omega t) + i_{comp}^2 + \frac{\Delta i_{L_a}^2}{12}\right) \right. $$
$$\left. + \left(I_{out}^2 \sin^2(\omega t + \pi) + i_{comp}^2 + \frac{\Delta i_{L_b}^2}{12}\right)\right\} \tag{7}$$

The power losses of the output capacitance C_{oss}, depend on the input voltage and the switching frequency as:

$$P_{tot,C_{oss}} = 2\left(\frac{C_{oss}^* A_{sw}}{A_{sw}^*}\right)V_{in}^2 f_{sw} \tag{8}$$

The reverse recovery loss of the lower side switches is not negligible for cascode devices. The total reverse recovery loss $P_{tot,rr}$ is calculated as:

$$P_{tot,rr} = 2\left(\frac{Q_{rr}^* A_{sw}}{A_{sw}^*}\right)V_{in} f_{sw} \tag{9}$$

The gate losses depend on the switching frequency, the gate-source voltage V_{GS} and the gate charge Q_g. The total gate loss of four switches $P_{tot,g}$ is calculated as:

$$P_{tot,g} = 4\left(\frac{Q_g^* A_{sw}}{A_{sw}^*}\right)V_{GS} f_{sw} \tag{10}$$

In cascode GaN FETs, the current flowing through the body diodes of the lower side switches incur the conduction loss during the reverse recovery time t_{rr} [32]. The total power loss $P_{tot,bd}$ of the body diodes can be written as,

$$P_{tot,bd} = 2V_{SD} f_{sw} t_{rr}\left(I_{out}(\sin(\omega t) + \sin(\omega t + \pi)) + 2i_{comp}\right) \tag{11}$$

The volume of the switches can be calculated as:

$$vol_{sw} = 4h_{sw}A_{sw} \tag{12}$$

Where, h_{sw} is the height of the switch package.

3.3.3 Output inductors

The inductor power loss consists of the core loss and the AC and DC resistance loss which can be expressed as [34].

$$P_{ind} = \left(a_{L1}f_{sw}^{\alpha}\Delta i_{L}^{\beta}\right)_{core\_loss} + \left(a_{L2}f_{sw}\Delta i_{L}^{\gamma}\right)_{AC\_loss} + \left(a_{L3}I_{out}^{2}\Delta i_{L}^{\lambda}\right)_{DC\_loss} \quad (13)$$

Where, a_{L1}, α, and β are the Steinmetz coefficients; a_{L2} and a_{L3} are the constants which are used to approximate the values of DC winding resistance; γ and λ are the real values used to reduce the non-linearity. The approximated inductor volume is calculated as:

$$vol_{ind} = a_{L4}LI_{peak}^{2} + a_{L5}LI_{peak} + a_{L6}I_{peak} \quad (14)$$

Where, a_{L4}, a_{L5}, and a_{L6} are the polynomial coefficients of the inductor which must be a positive value. L is the inductor value. I_{peak} is the peak current of the inductors.

3.3.4 Output capacitors

The power loss of the capacitor is calculated as:

$$P_{cap} = \frac{I_{RMS,C}^{2}\,tan\,\delta}{2\pi f_{2\omega}C} \quad (15)$$

Where, $I_{RMS,C}$ is the RMS current flow through the capacitor, $tan\,\delta$ is the loss factor, $f_{2\omega}$ is the frequency of second-order ripple power and C is the value of the capacitance. The total volume of the capacitors vol_{cap} is calculated as:

$$vol_{cap} = a_{C1}CV_{C}^{2} + a_{C2}CV_{C} + a_{C3}V_{C} \quad (16)$$

Where, a_{C1}, a_{C2} and a_{C3} are the polynomial coefficients of the capacitors which must be positive values. The voltage V_{C} is the voltage across the capacitor.

3.3.5 Heat sinks

The volume of the heat sink is calculated as:

$$vol_{heat\,sink} = \frac{V_{\theta SA}}{P_{D}}\left(\Delta T_{j} - P_{D}\left(\frac{R_{\theta JC}^{*}A_{sw}^{*}}{A_{sw}} + R_{\theta CS}\right)\right) \quad (17)$$

Where, $V_{\theta SA}$ is the volumetric resistance, P_{D} is the power dissipated by the GaN FETs, ΔT_{j} is the temperature difference between the junction and the ambient, $R_{\theta JC}^{*}$ is the thermal resistance from junction to the case of the semiconductor, and $R_{\theta CS}$ is the thermal resistance from the case to the mounting surface of the semiconductor.

3.3.6 Formulation of the multi-objective model

To formulate the multi-objective model, the total power loss $P_{tot,loss}$ and volume vol_{tot} are calculated as:

$$P_{tot,loss} = P_{tot,sw} + P_{tot,cond} + P_{tot,C_{oss}} + P_{tot,rr} + P_{tot,g} + P_{tot,bd} + P_{ind} + P_{cap} \quad (18)$$

$$vol_{tot} = vol_{sw} + vol_{ind} + vol_{cap} + vol_{heat\,sink} \quad (19)$$

Using (18) and (19), the objective function and inequality constraints can be obtained as:

$$\text{minimize } f(P_{tot,loss}, vol_{tot})$$
$$\text{subject to } f_{sw,\,min} \leq f_{sw} \leq f_{sw,\,max}$$
$$A_{sw,\,min} \leq A_{sw} \leq A_{sw,\,max}$$
$$\Delta i_{L,\,min} \leq \Delta i_L \leq \Delta i_{L,\,max}$$
$$\Delta T_{j,\,min} \leq \Delta T_j \leq \Delta T_{j,\,max} \tag{20}$$

From (20), the optimal value of the power loss and volume of the inverters is determined following the iterative process shown in **Figure 14**. The optimized efficiency and power density of the design are then calculated. The outcome of the multi-objective design is the Pareto-front showing the optimized efficiency and power density of the designed inverter.

3.4 Performance evaluation

The multi-objective design approach was implemented in MATLAB/Simulink and examined a 1 kW GaN-based inverter. The performance of the inverter was examined in terms of efficiency and power density. The minimum and maximum values of the design variables used for the multi-objective design are given in **Table 1**. The values of design variables are selected from industrial design standards.

A 900 V GaN FET manufactured by Transphorm was used. A P11T60 series of high current toroid type fixed inductors designed by MPS Industries were used. A MKP1848C series of polypropylene film capacitors from Vishay BC Components
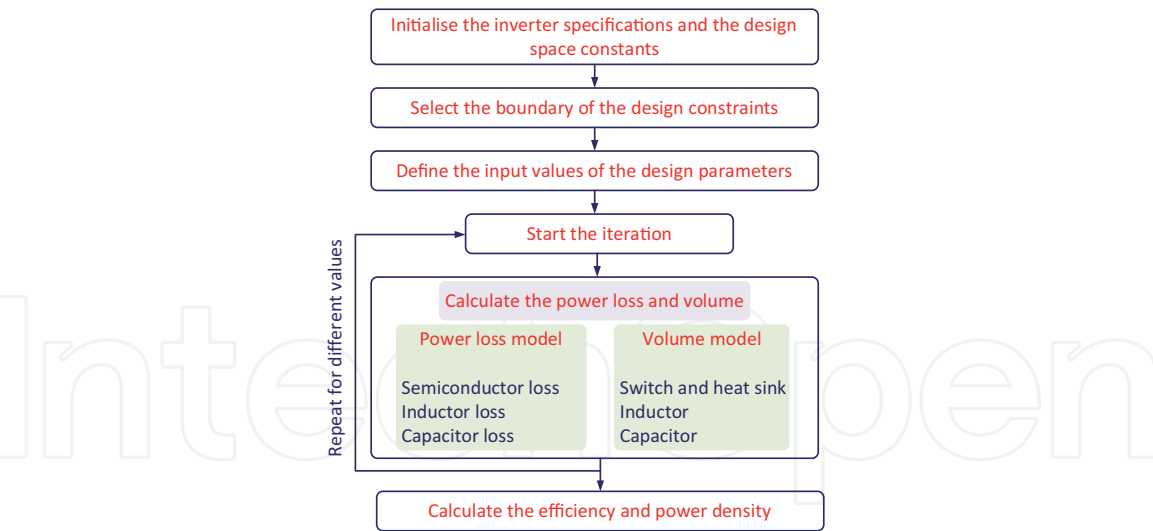

Figure 14.
Flow chart of multi-objective design.

Design variable	Min. value	Max. value
Switching frequency f_{sw}	30 kHz	200 kHz
Current ripple Δi_L	$0.1\, I_{out,max}$	$0.45\, I_{out,max}$
Switch area A_{sw}	$0.94\, A^{*}_{sw}$	$1.07\, A^{*}_{sw}$
Change in temperature ΔT_j	1 °C	25°C

Table 1.
Design constraints of the inverter.

13

was used. The values of the maximum output current $I_{out,max}$, and reference switching area A^*_{sw} are 6.15 A and 45.6 mm^2. The values of the inductor are L = 390 µH, the capacitor is C = 48 µF and the switching frequency is f_{sw} = 100 kHz. These are selected according to the outcome of the multi-objective design approach.

3.4.1 Performance evaluation

The Pareto-front performance of efficiency and power density of the power inverter is generated by the multi-objective design and is given as the green curve in **Figure 15**.

One design based on the Pareto-front performance was chosen to validate the method. The selection of efficiency and power density was made based on different applications. For instance, the selected efficiency and power densities are 98.4% and 4.6 kW/dm3 which are typical for PV inverters. For the corresponding design, the power loss and volume are obtained as 15.93 W and 218.32 cm^3. The breakdown of power loss and volume of each component is given in **Figure 16**. With the total power loss, switches contribute 52%, inductors contribute 33% and capacitors contribute 15%. Likewise, with the total volume, heat sinks and switches contribute 34%, inductors contribute 34%, and capacitors contribute 32%.

3.4.2 Experimental verification

A prototype of the inverter was built using the components sized using the multi-objective design. The prototype is shown in **Figure 17(a)**. The prototype was
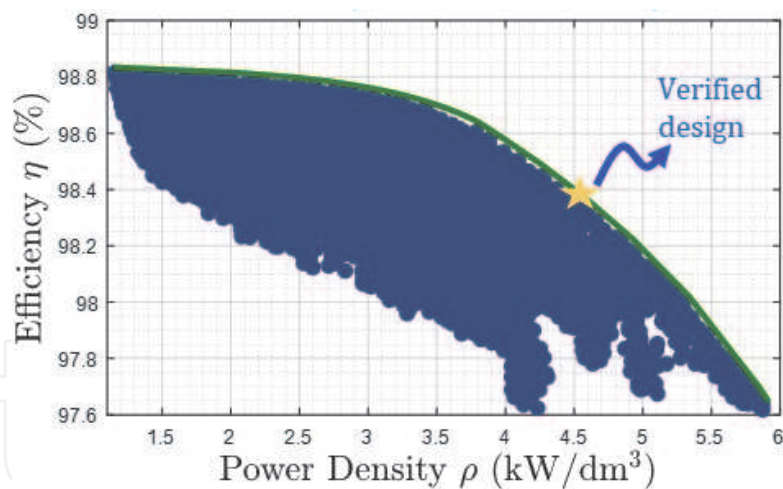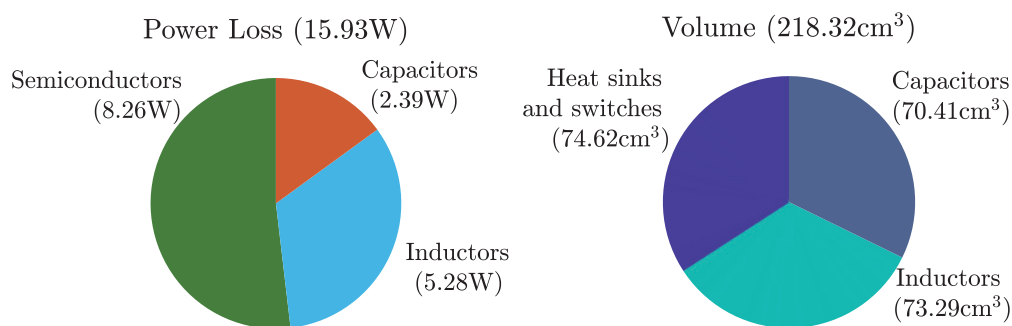

Figure 15.
Efficiency vs. power density.

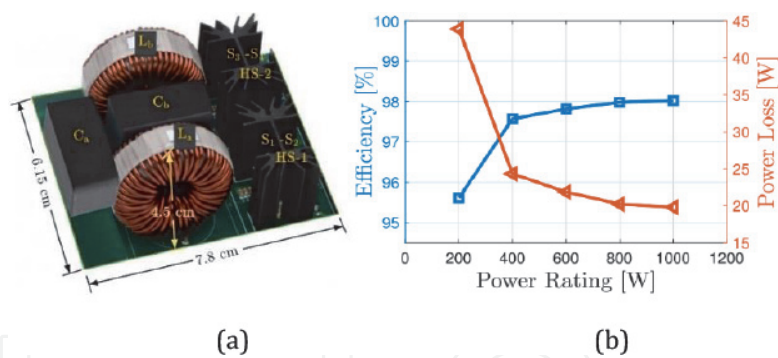**Figure 16.**
Power loss and volume.

Figure 17.
(a) Hardware prototype, and (b) efficiency and power loss.

operated at different output power levels to obtain the efficiency and power loss and the result is given in **Figure 17(b)**. The efficiency was measured by a Yokogawa WT1806E precision power analyzer. It was observed that the maximum efficiency of the prototype is 98.02%. The power density was 4.54 kW/dm^3 from the volume of the inverter which is given in **Figure 17(a)**. Therefore, the efficiency and power density match the results obtained by the proposed design approach in Section 3.4.1. The errors of efficiency and power density obtained from both are only 0.38% and 0.06 kW/dm^3 respectively.

4. Converter control

For the converter system, an important question is how to design a good controller for the system so that the system can run stably while meeting the required performance indicators. In this section, typical approaches to the control of both DC/DC and DC/AC power electronic converters used in microgrids are presented.

The control of converters usually has a hierarchical control structure (see **Figure 18**). The switching-level, converter-level, and application-level control are introduced in this section. For the switching-level control, typical pulse-width modulation (PWM) methods are introduced. For the converter-level control, the
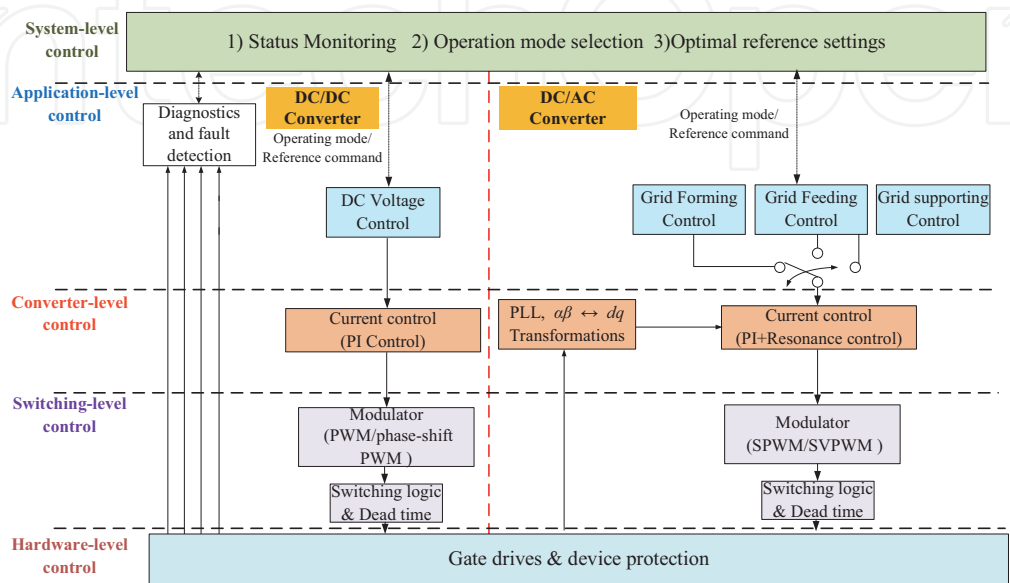

Figure 18.
Hierarchical control of power electronic converters.

design of the current controller is discussed. For the application-level control, control modes used for different applications are discussed.

4.1 Control of DC/DC converters

4.1.1 Switching-level control

PWM is the most used technique to control switching power devices in DC/DC converters. For example, to control a conventional buck DC/DC converter, a modulation wave v_m is generated from the control loop and compared with the sawtooth-wave carrier v_c as shown in **Figure 19**. The driving signal s (0 or 1) is sent to the driver according to (21).

$$\text{If } v_m > v_c, s = 1$$
$$\text{If } v_m < v_c, s = 0 \tag{21}$$

The larger the modulation wave, the larger the duty cycle, and thus the higher the output voltage. For other types of DC/DC converters such as the Dual-active-bridge (DAB) converter, the phase-shift PWM is favored to achieve zero-voltage-switching (ZVS) to reduce the losses [35].

4.1.2 Converter and application-level control

The DC/DC converters are used in the field of DG integration such as solar PV systems [36]. They transfer the power from DGs to DC microgrids. Types of DC/DC converters include buck, boost, and buck-boost converters.

Figure 20 shows a general control schematic for controlling the output voltage of a DC/DC converter. A double-loop controller is used for the DC/DC
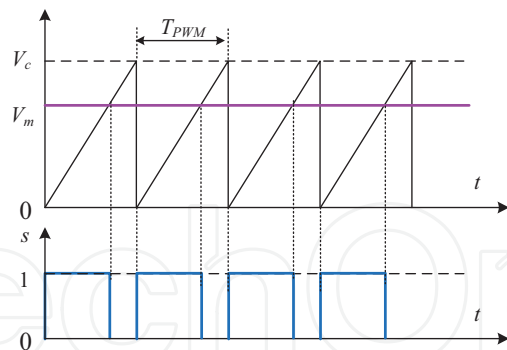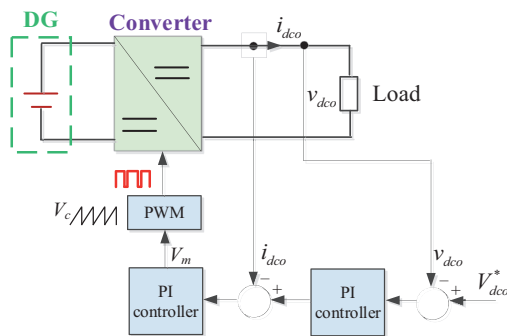
Figure 19.
PWM modulation scheme.

Figure 20.
Output DC voltage control.

converter. The control mode is to control the output DC voltage. The output from the voltage controller is the reference for the current controller. The modulation wave V_m is calculated from the current PI controller. Then, the PWM signal can be generated by the modulator as discussed in 4.1.1 to drive the power electronic switches.

For parallel-connected DC/DC converters in low-voltage DC microgrid. Droop control is also popular for DC/DC converters to achieve autonomous equal power-sharing. A virtual resistance R_V can be used to automatically distribute the power among the parallel converters. The droop curve and the control scheme are shown in **Figures 21** and **22**.

For PV energy integration, the DC/DC converter can be used for the MPPT control [37] as shown in **Figure 23**. A DC/DC converter is connected between the PV array and the load to trace the maximum powerpoint. In this case, the controller controls the input power through an MPPT algorithm. The output of the MPPT algorithm is a DC voltage reference. The input DC voltage of the DC/DC is then controlled according to this reference.

The load at the output side can be the passive load or the active load such as an AC/DC converter for connecting the PV system to an AC grid. In this case, the grid side AC/DC converter is responsible for regulating the DC link voltage.
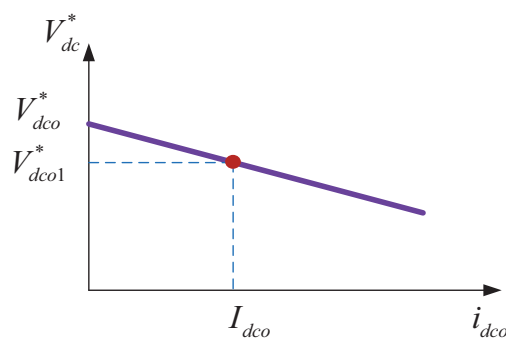

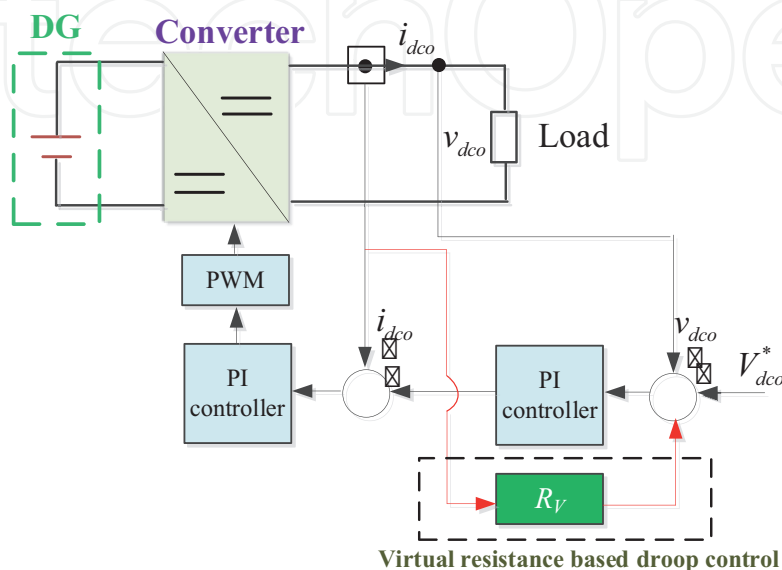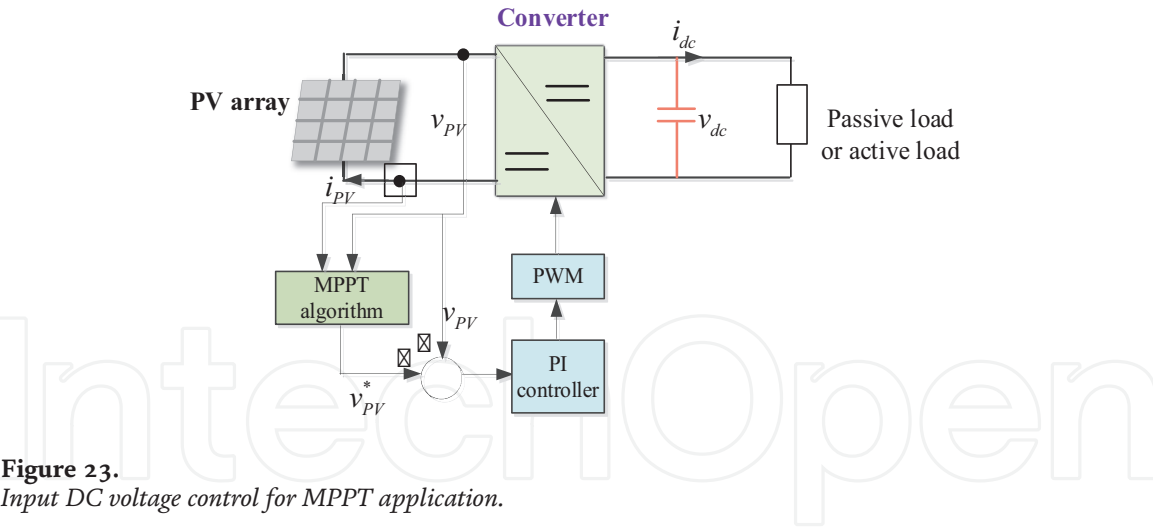**Figure 21.**
Droop cure for virtual resistance-based control.

Figure 22.
Virtual resistance-based control schematic.

Figure 23.
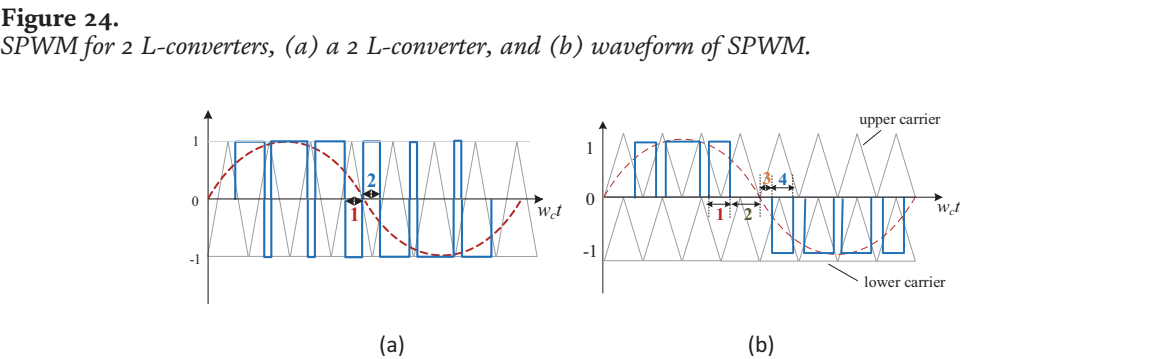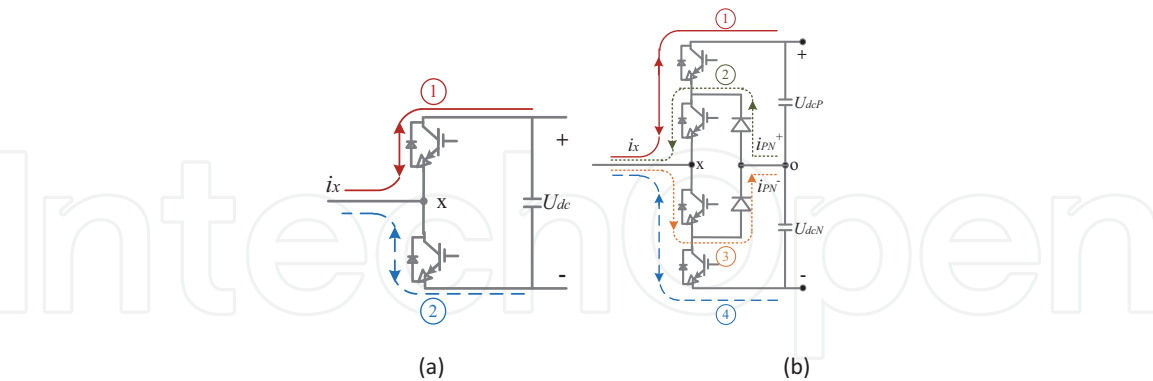*Input DC voltage control for MPPT application.*

4.2 Control of DC/AC converters

4.2.1 Switching-level control

Typical DC/AC converters used for connecting distributed generators (DGs) to the distribution networks are two-level (2 L) and three-level (3 L) converters, as shown in **Figure 24**.

Figure 25(a) and **(b)** show the sinusoidal PWM (SPWM) based modulation for 2 L and 3 L converters, respectively.

For the PWM modulation of 2 L converters in **Figure 25(a)**, the switching on and off of a IGBT device is determined by the comparison between the sinusoidal modulation wave (red dash line) and the carrier (gray triangle wave). For the modulation of 3 L converter in **Figure 25(b)**, the carrier disposition (CD) based modulation is commonly used. The CD modulation algorithm can be further

Figure 24.
SPWM for 2 L-converters, (a) a 2 L-converter, and (b) waveform of SPWM.

Figure 25.
SPWM for 3 L-converters, (a) a 3 L converter, and (b) waveform of SPWM.

categorized as phase disposition (PD) and phase opposite disposition (POD) methods. For the PD modulation, triangle carriers over and down the zero reference have the same phase (as shown in **Figure 25(b)**), whereas the phase of the lower carrier is opposite to the upper carrier for POD modulation. It can be observed that the phase voltage v_{xo} switches between $\frac{U_{dc}}{2}$ and 0 when the modulation wave (red dash line in **Figure 25(b)**) is positive, and between 0 and $-\frac{U_{dc}}{2}$ when modulation wave is negative.

4.2.2 Converter-level control

The decoupled current controller of the converter-level control is shown in **Figure 26**. Through the coordinate transformation from static frame (i.e. abc frame) to the synchronous rotating frame (i.e. dq frame), the active and reactive power is decoupled and can be controlled independently. Also, the control loop presents linear characteristics on the dq frame. Hence, the voltage-oriented vector control strategy is commonly adopted. The dq current controllers are based on PI regulators. The parameters of the PI regulators can be designed based on a second-order transfer function for a linear system. The decoupling terms $-\omega L i_q$ and $\omega L i_d$ are added to decouple the current components at the d-axis and q-axis. Voltage feedforward e_{dq} is used to improve the dynamic performance of the current controller.

For the grid-connected converters, the PLL is required to achieve synchronization to the grid frequency. The design of PLL in the $\alpha\beta$ frame is presented in **Figure 27**. The vector cross product is used to extract the error between the real phase angle of the grid voltage and the estimated phase voltage. The error passes through the PI regulator so that it can be eliminated.

The controller presented in **Figure 26** regulates positive-sequence current and works effectively if the voltage of the connected grid is balanced. However, if the voltage imbalance occurs, both positive-sequence and negative-sequence currents
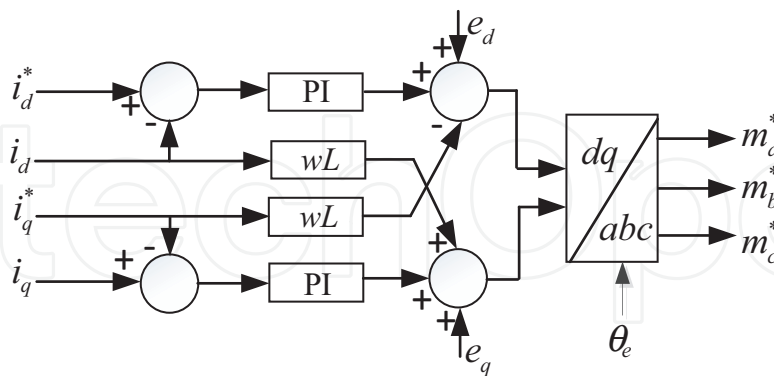

Figure 26.
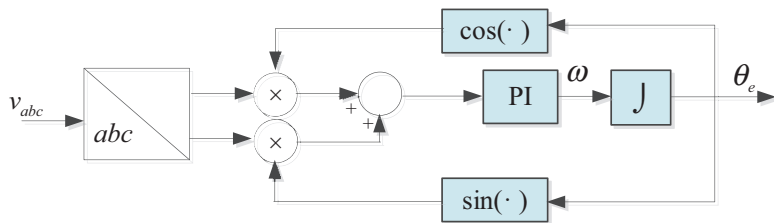*Decoupled current controller at dq frames.*

Figure 27.
PLL for grid synchronization.

will exist. Dual current controller regulating both positive-sequence and negative-sequence currents will be needed as shown in **Figure 28**.

The ultimate objective of using such dual current control to regulate currents of both sequences is to either i) achieve balanced output current [38], or ii) cancel the 2nd order power ripple caused by the interaction of positive-sequence current and negative-sequence voltage [39]. For i), balanced three-phase currents can be obtained by setting negative-sequence current references to zero. However, the interaction of positive-sequence current and negative-sequence voltage will result in a 2nd order power ripple at the grid side although the currents are controlled balanced through i):

$$p = P_0 + P_{c2} \cos(2wt) + P_{s2} \sin(2wt)$$
$$q = Q_0 + Q_{c2} \cos(2wt) + Q_{s2} \sin(2wt) \tag{22}$$

This power ripple could increase odd AC harmonics to the grid. Thus, the approach for ii) is injecting proper negative-sequence current to counteract such a power ripple. The expected injecting currents are expressed as:

$$
\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2}{3}
\begin{bmatrix}
v_{sd}^p & v_{sq}^p & v_{sd}^n & v_{sq}^n \\
v_{sq}^p & -v_{sd}^p & -v_{sq}^n & v_{sd}^n \\
v_{sq}^n & -v_{sd}^n & -v_{sq}^p & v_{sd}^p \\
v_{sd}^n & v_{sq}^n & v_{sd}^p & v_{sq}^p
\end{bmatrix}^{-1}
\begin{bmatrix} P_0^* \\ Q_0^* \\ P_{s2}^* \\ P_{c2}^* \end{bmatrix}
$$

$$
= \frac{2}{3}
\begin{bmatrix}
v_{sd}^p & v_{sq}^p & v_{sd}^n & v_{sq}^n \\
v_{sq}^p & -v_{sd}^p & -v_{sq}^n & v_{sd}^n \\
v_{sq}^n & -v_{sd}^n & -v_{sq}^p & v_{sd}^p \\
v_{sd}^n & v_{sq}^n & v_{sd}^p & v_{sq}^p
\end{bmatrix}^{-1}
\begin{bmatrix} P_0^* \\ Q_0^* \\ 0 \\ 0 \end{bmatrix} \tag{23}
$$

Where, P_{s2}^* and P_{c2}^* are the sine and cosine terms of the 2nd order power ripples. In this scheme, the positive-sequence components $F_{\alpha\beta}^p = \begin{bmatrix} V_{\alpha\beta}^p & I_{\alpha\beta}^p \end{bmatrix}$ and the negative-sequence components $F_{\alpha\beta}^n = \begin{bmatrix} V_{\alpha\beta}^n & I_{\alpha\beta}^n \end{bmatrix}$ need to be extracted from $F_{\alpha\beta} = \begin{bmatrix} V_{\alpha\beta} & I_{\alpha\beta} \end{bmatrix}$. $F_{\alpha\beta}^p$ and $F_{\alpha\beta}^n$ can be obtained by misplaced subtraction as:
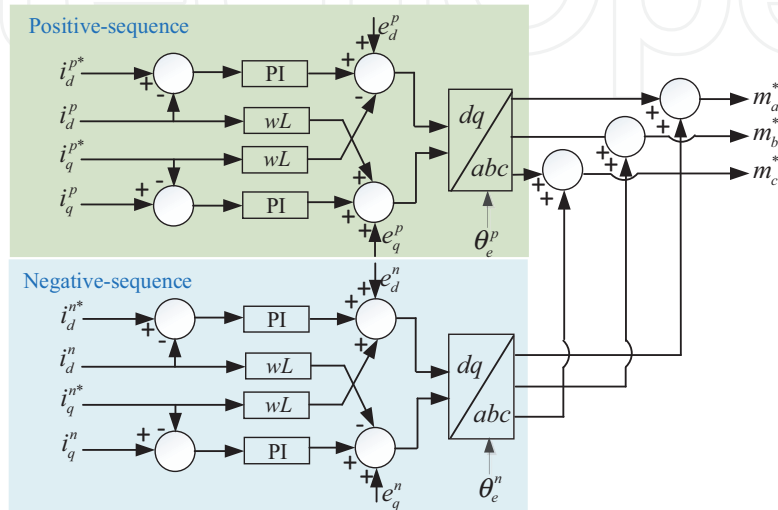

Figure 28.
Dual current controller for positive and negative sequence control.

$$\mathbf{F}^{p}_{\alpha\beta}(t) = \frac{1}{2}\left[\mathbf{F}_{\alpha\beta}(t) + j\mathbf{F}_{\alpha\beta}(t - T/4)\right]$$

$$\mathbf{F}^{n}_{\alpha\beta}(t) = \frac{1}{2}\left[\mathbf{F}_{\alpha\beta}(t) - j\mathbf{F}_{\alpha\beta}(t - T/4)\right] \tag{24}$$

Thus, the phase angles θ^{p}_{e} and θ^{n}_{e} in **Figure 28** can be obtained by phase locking the $V^{p}_{\alpha\beta}$ and $V^{n}_{\alpha\beta}$ separately.

In addition to the current controller in **Figure 26**, more control blocks can be added to reduce the harmonics that are generated by the nonlinear characteristics of converters. For example, carrier-based PWM methods can introduce the odd harmonics (i.e. 5th, 7th, 11th, and 13th), and the DC drift of neutral point voltage can cause even harmonics (i.e. 2nd and 4th). Therefore, the reduction of harmonics is required for converters. This can be achieved using the resonant (RES) controller [40]. The combined PI-RES controller at dq frames is shown in **Figure 29**.

A Nth order RES controller tuned at dq frames can compensate the (1-n)th and (1 + n)th harmonics in the stationary frame. For example, a 6th order RES controller can compensate the 5th and 7th harmonics. More RES controllers can be paralleled with the PI controller according to the compensating requirements.

4.2.3 Application-level control

At the application-level control, the control modes of the converters can be classified into three modes: grid-forming, grid-feeding, and grid-supporting modes [41]. The characteristics of the three modes are illustrated in **Figure 30**.

Converters in grid-forming mode should provide the AC voltage (reactive power) and frequency support (active power) for an AC grid. They act as voltage sources with low output impedance. The grid-forming converters can be also operated without being connected to the main grid.

Converters in grid feeding are operated as current sources and generate constant active and reactive power to the demand. However, as the operation of grid-feeding converters depends on at least one grid-forming converter, this type of converter cannot work without being connected to the main grid.

As for the microgrid, the power capacity of the DGs is limited. Thus, choosing one as the grid-forming converter may not be a good choice. Power-sharing
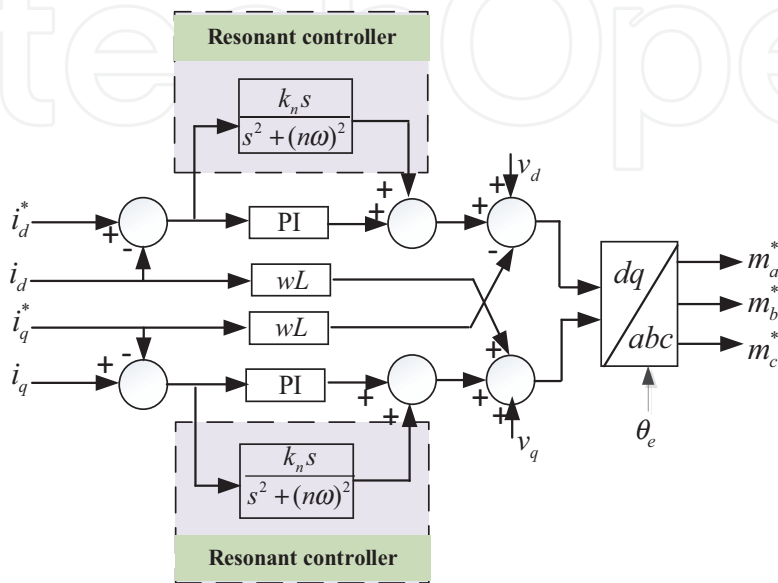

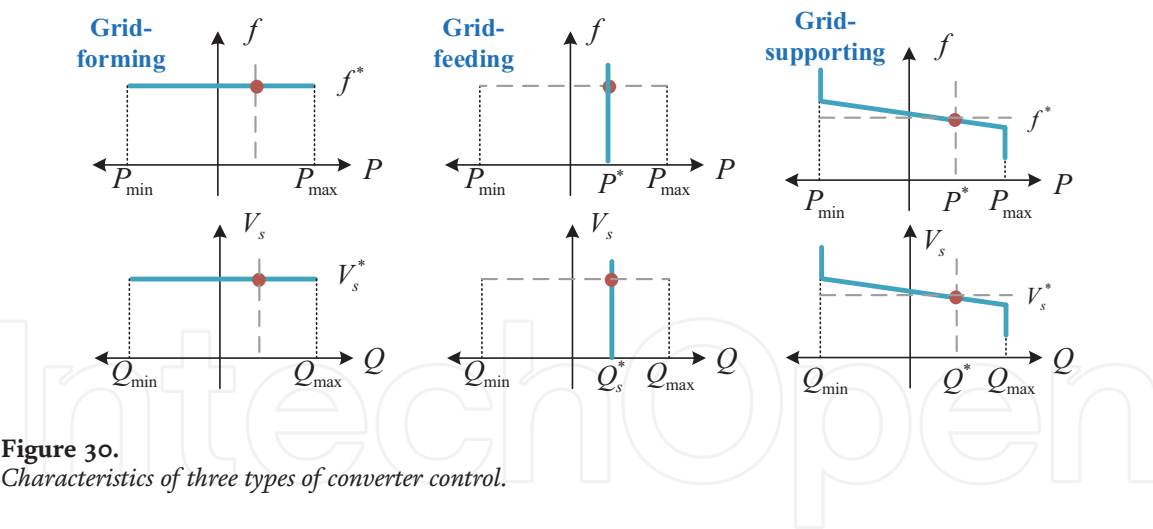**Figure 29.**
PI-RES current controller.

Figure 30.
Characteristics of three types of converter control.

methods to share the burden to each DG are preferred for the distribution networks integrated with renewable energies. To this end, the converters can work under grid-supporting mode and have a joint contribution to the voltage and frequency support. The basic power-sharing methods include centralized methods, master–slave methods, and distribution methods such as the droop methods [42]. The droop methods can automatically distribute the power to the DGs according to the droop curves, thus, communication is not required. Droop control for the grid-supporting converters is a promising power control strategy in the distribution network.

For the grid-forming converter control in **Figure 31**, the reference frequency f_0^* is given for the synchronization. The control is performed at dq frames. Feedback control is used to guarantee that the output voltage is equal to the given value. The outputs from the voltage PI controllers are the references for the current controller as mentioned in the previous section. The grid-forming mode is normally not used when being connected to the main grid, in which condition the grid-forming function is always performed by the synchronous generator of the power plants.

The control schematic for the grid-feeding converter is shown in **Figure 32**. The outer loop is the PI-based active and reactive power control loop. The active power and reactive power are calculated by the measured I_{abc} and V_{abc}. The outputs of the power control loops are the given values of the current control loops. Synchronization is required in this scheme, which is achieved using the PLL. The obtained phase angle θ_e is used for the transformation of voltage and current. The grid-feeding
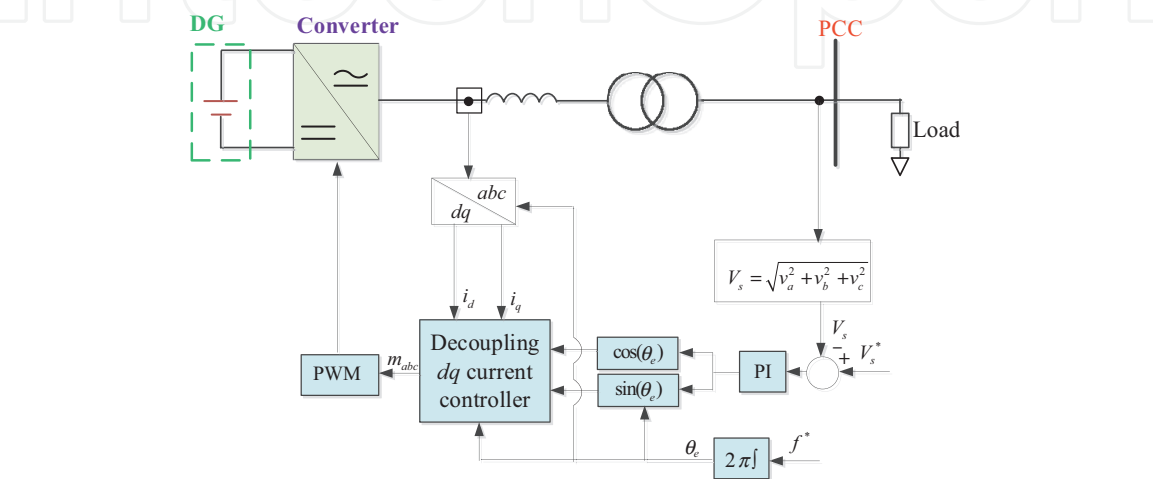

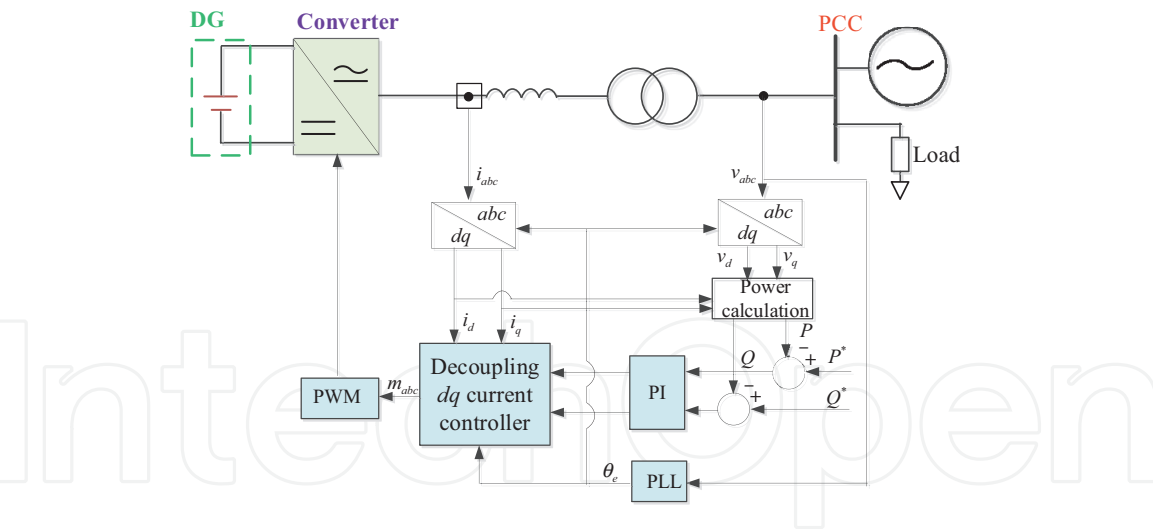**Figure 31.**
Grid-forming control schematic.

Figure 32.
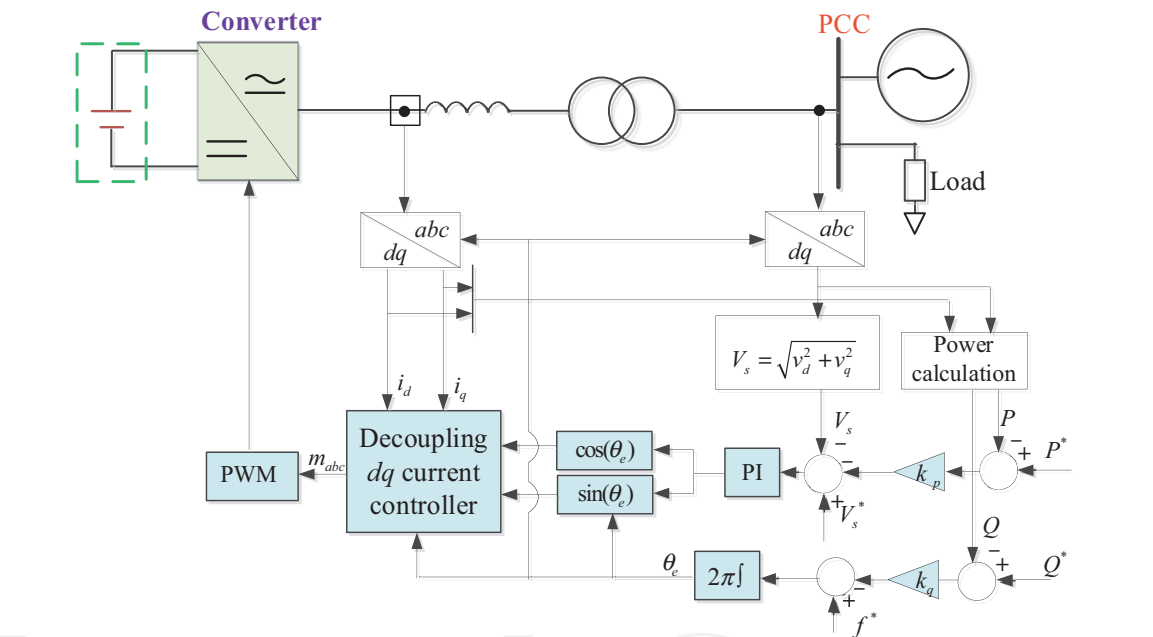*Grid-feeding control schematic.*

Figure 33.
Grid-supporting control schematic.

converter is always fed by the DGs which have more stochastic characteristics such as the PV and wind farms [41].

For the grid-supporting converter shown in **Figure 33**, the control scheme is the combination of the grid-forming and grid-feeding control methods. The $k_{p,q}$ is used to adjust the droop slope. The converter behaves more like a voltage source if $k_{p,q}$ increases. Otherwise, if $k_{p,q}$ decreases, the converter has more characteristics of the current source. The operation points (f^*, P^*) and (V^*, Q^*) in **Figure 33** are regulated by the secondary controller (system-level controller) [41].

5. Conclusion

Renewable energy resources, energy storage systems, and electric vehicles (EVs) are emerging in microgrids. A great many of the new energies are not naturally AC

sources and cannot be connected to the grid. Power electronic converters build a bridge for the connection between renewable energies and microgrid.

Converter types include DC/DC and DC/AC converters. For the DC/DC converters, typical topologies are a buck, boost, and buck-boost converters. For the DC/AC converters, three-phase two-level and three-level converters are most widely used. In particular, the three-phase four-leg converters are used for the unbalanced load conditions. The neutral leg and current are independently controlled so that the dc capacitors can be choosed smaller to achieve lower cost and volume.

WBG devices have been used in the power converters. The design of WBG power converters should consider efficiency, volume, and weight, cost, and failure rate. To maximum these performance indices, the multi-optimization method is utilized. The optimized design solution is found according to the Pareto-front curve. To illustrate the design method, the optimization of efficiency and power density is particularly analyzed and validated through a prototype.

Control is an essential part of the power conversion. The typical control methods are discussed from the switching-level layer to the application-level layer following a hierarchical structure. PWM is a common modulation method. The current controllers are performed on the dq frame to achieve independent control of active and reactive power. Also, different control modes, such as grid-feeding, grid-forming, and grid-supporting control, are presented to accommodate different applications.

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