

# We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

6,900

Open access books available

186,000

International authors and editors

200M

Downloads

Our authors are among the

154

Countries delivered to

TOP 1%

most cited scientists

12.2%

Contributors from top 500 universities



WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index  
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?  
Contact [book.department@intechopen.com](mailto:book.department@intechopen.com)

Numbers displayed above are based on latest data collected.  
For more information visit [www.intechopen.com](http://www.intechopen.com)



# Low Temperature Characterization and Modeling of FDSOI Transistors for Cryo CMOS Applications

*Mikaël Cassé and Gérard Ghibaudo*

## Abstract

The wide range of cryogenic applications, such as spatial, high performance computing or high-energy physics, has boosted the investigation of CMOS technology performance down to cryogenic temperatures. In particular, the readout electronics of quantum computers operating at low temperature requires larger bandwidth than spatial applications, so that advanced CMOS node has to be considered. FDSOI technology appears as a valuable solution for co-integration between qubits and consistent engineering of control and read-out. However, there is still lack of reports on literature concerning advanced CMOS nodes behavior at deep cryogenic operation, from devices electrostatics to mismatch and self-heating, all requested for the development of robust design tools. For these reasons, this chapter presents a review of electrical characterization and modeling results recently obtained on ultra-thin film FDSOI MOSFETs down to 4.2 K.

**Keywords:** Cryogenic CMOS, FDSOI, MOSFET, characterization, modeling

## 1. Introduction

First MOSFET measurements at liquid Helium temperature have been reported as soon as in late 1960s [1–3], leading to some remarkable discoveries like the integer quantum Hall effect [4]. Since then, many works have been published on the electrical characteristics of MOSFETs down to 4.2 K [5–7]. The interest of operating electronic circuits at cryogenic temperatures has been demonstrated a few decades ago, and relies on the performance improvement and/or on the necessity to have electronics in cryogenic environment [5–7]. With the emerging field of quantum computing, for which read-out and control electronics of the quantum bits (qubits) is required in the proximity of the qubit itself, the study of CMOS devices at low and very low temperature, well below 100 K, has received a renewed attention [8–10]. In particular, qubit control requires high-frequency and large-bandwidth signals, as well as low-power electronics to be compatible with the cooling power of modern refrigerators [11–14]. Circuits fabricated from advanced nodes CMOS are good candidates to fulfill the specifications for quantum computing applications [15–18].

Key advantages of operating at low temperatures include the better electrical performance of MOSFETs, with higher carrier drift velocity and so higher on-state

drain current and transconductance, steeper subthreshold slope, lower leakage current [6, 19]. Some works have studied bulk MOSFETs operation at cryogenic temperature emphasizing in particular kink behavior and freeze-out effects in those devices [7, 15, 20–24]. Recently, outstanding characteristics have been demonstrated at 4.2 K on advanced CMOS technologies [19, 25–27], in particular for Fully Depleted Silicon-On-Insulator (FDSOI) [28–32]. Ultrathin film FDSOI devices (with typically silicon thickness less than 10 nm) are immune to kink effects [33], and freeze-out has finally little impact on the DC characteristics of MOSFETs in advanced technologies [34]. Apart from the performance itself of the circuits at these low temperatures, and the figures of merit for analog or digital applications, specific attention to power dissipation has to be brought as well, as the available cooling power is limited in cryostat, and depends of the different cooling stages (typically  $\approx 1$  W at 4 K and less than 1 mW below 100mK) [11].

In that context, FDSOI technology offers a significant advantage over other available technologies, as it allows designing low power electronics, threshold voltage tunability thanks to its back bias ability, and offers low variability due to the undoped channel [35]. Extensive electrical characterization of advanced CMOS devices at deep cryogenic operation, including device electrostatics, carrier transport, mismatch and variability, or self-heating, is thus seriously needed.

Numerical issues appears with the modeling and simulation of MOSFETs at cryogenic and deep-cryogenic temperatures, in particular due to energy  $k_B T$  approaching zero in equations and the extremely small intrinsic carrier density [34, 36]. Besides these difficulties, accurate models must correctly include, among other things, the temperature dependence of the main electrical parameters, such as carrier mobility, saturation velocity, threshold voltage, ... , as well as thermal effects [37, 38]. On the other hand, new physical phenomena appear as the device temperature decreases that need to be characterized and properly modeled [19].

Because these aspects are essential for the development of compact models and robust design tools, this chapter presents a review of recent results obtained on 28 nm FDSOI transistors operated down to deep cryogenic temperatures. More specifically, we first discuss in Section 2 the major device electrical properties in terms of transfer characteristics and MOSFET parameters versus temperature. Then, we describe in Section 3 the self-heating phenomena, which could alter the FDSOI device performances. The matching and variability properties of scaled transistors limiting the analog applications are then addressed in Section 4. The development of compact model necessary for FDSOI circuit design at deep cryogenic temperatures is presented in Section 5. Finally, in Section 6, we illustrate the operation of elementary circuits at very low temperatures regarding inverter delay and oscillator frequency.

## 2. Cryogenic FDSOI device operation

In this section, we present the measurement of the main electrical properties of FDSOI devices operating down to 4.2 K, such as the capacitance and charge control characteristics, the drain current  $I_d(V_g)$  transfer curves as well as the main MOSFET parameters (threshold voltage  $V_{th}$ , subthreshold swing, mobility).

### 2.1 Devices under test

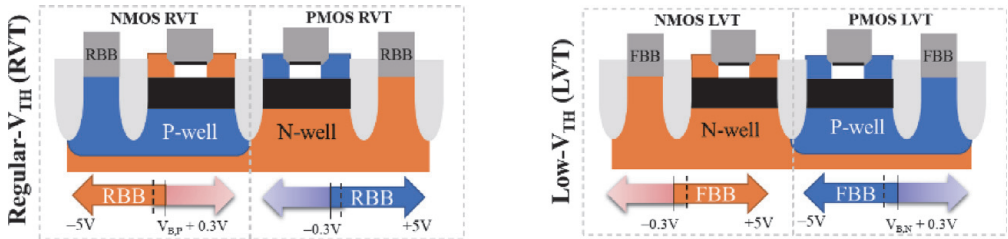
The measurements were performed on 28 nm FDSOI MOSFETs with silicon film thickness  $t_{si} = 7$  nm and buried oxide (BOX) thickness  $t_{BOX} = 25$  nm from STMicroelectronics. NMOS and PMOS transistors were processed from (100)

handle substrate, with  $\langle 100 \rangle$  – oriented channel, and a high- $\kappa$ /metal gate Gate-First architecture (**Figure 1**) [39]. Regular- $V_{th}$  (RVT) and low- $V_{th}$  (LVT) transistors are available through a doped back plane (NWell or PWell, with typically  $N_{A,D} = 10^{18} \text{ cm}^{-3}$ ) below the BOX. Thin (GO1, with equivalent oxide thickness  $EOT = 1.1 \text{ nm}$ ) and thick oxide (GO2,  $EOT = 3.2 \text{ nm}$ ) devices have been characterized using a cryogenic probe station down to 4.2 K.

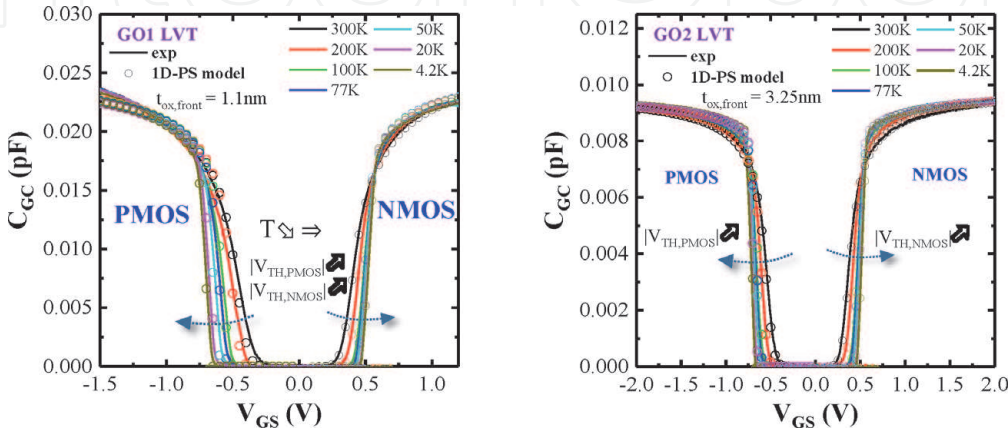
2.2 Capacitance and charge control

The electrostatic charge control of FDSOI devices has been characterized by split C-V measurements with a conventional LCR meter. To this end, the gate-to-channel capacitance  $C_{gc} = dQ_i/dV_g$ , with  $Q_i$  the inversion charge in the channel, has been measured at 500 kHz frequency on large area N and P MOS devices as a function of the front gate voltage  $V_g$  with body bias  $V_b = 0 \text{ V}$  for several temperatures down 4.2 K (**Figure 2**). As can be seen, the  $C_{gc}(V_g)$  curves are almost temperature independent above threshold, whereas a strong improvement of the turn-on behavior is obtained at low temperature, related to the subthreshold slope increase. These characteristics have been well reproduced by Poisson-Schrodinger simulations (see **Section 5.1**), providing precise extraction of front oxide EOT values for GO1 and GO2 transistors [41].

The influence of the AC level ( $V_{osc}$ ) of the LCR meter oscillator used during  $C_{gc}$  measurements at 4.2 K has been studied and is reported in **Figure 3a**. Indeed, due to the strong non linearity of the  $Q_i(V_g)$  curves in subthreshold region at very low temperature, the turn-on behavior of the  $C_{gc}(V_g)$  curve below threshold is not well captured for a too large AC level (here 40 mV, currently used at  $T = 300 \text{ K}$ ). However, for an AC level of 1 mV, getting closer to the thermal voltage  $k_B T/q$  at



**Figure 1.** Schematics of 28 nm FDSOI N- and PMOSFETs with regular- $V_{TH}$  (RVT) and low- $V_{TH}$  (LVT) flavors. Forward and reverse back biases (FBB and RBB) can be applied depending on the doping of the back plane.



**Figure 2.**  $C_{gc}(V_g)$  characteristics (solid lines) for N- and PMOS GO1 and GO2 devices from 300 K down to 4.2 K, at  $V_B = 0 \text{ V}$ . the  $C_{gc}(V_g)$  1D-PS modeling is shown in symbols (frequency = 1 MHz, AC level = 40 mV,  $W = L = 9 \text{ }\mu\text{m}$ ). After Cardoso et al. [40].

4.2 K, where  $k_B$  is the Boltzmann constant and  $q$  the magnitude of the electron charge, the turn-on behavior of  $C_{gc}(V_g)$  below threshold is well accounted for. These results can be well modeled by integrating the ideal  $C_{gc}(V_g)$  curve over one period of the AC signal, providing the measured capacitance  $C_{gc,meas}$  as follows [42]:

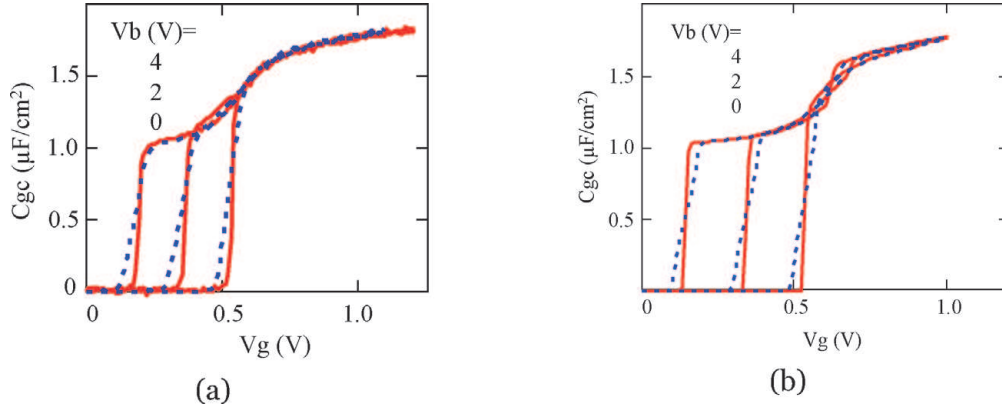
$$C_{gc,meas}(V_g) = \frac{1}{T_p} \int_0^{T_p} C_{gc}(V_g + \delta V_g(t)) dt \quad (1)$$

where  $\delta V_g(t) = V_{osc} \cdot \sin(2\pi t/T_p)$  is the AC signal of period  $T_p$  (Figure 3b).

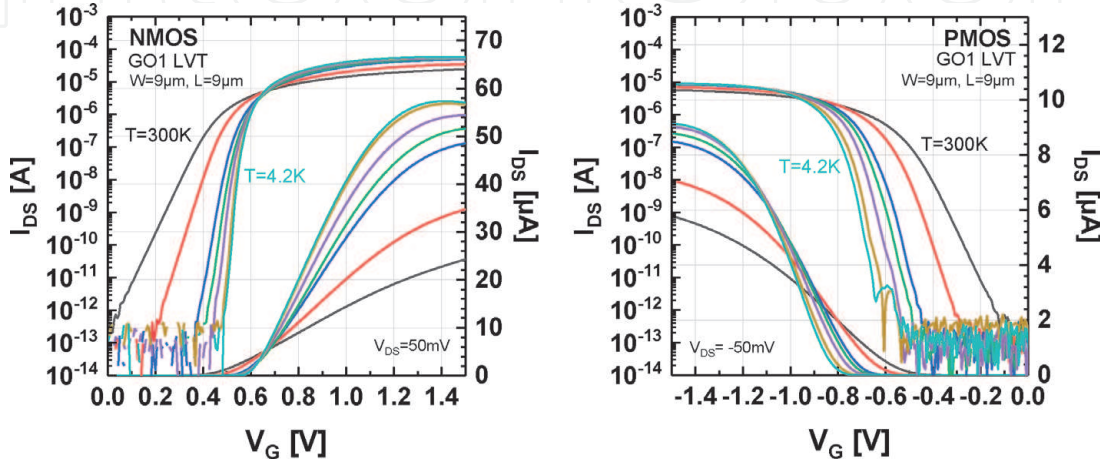
### 2.3 Drain current characteristics, threshold voltage and subthreshold slope

The  $I_d(V_g)$  transfer characteristics of same devices have been measured in linear region ( $V_d = 50$  mV) for various temperatures and are shown in Figure 4. As usually observed in cryo-electronics for bulk CMOS devices [7], the drain current above threshold is highly increased due to mobility improvement of both electrons and holes, resulting from the suppression of phonon scattering. Similarly, the turn-on behavior of the curves below threshold is greatly improved as the temperature is lowered.

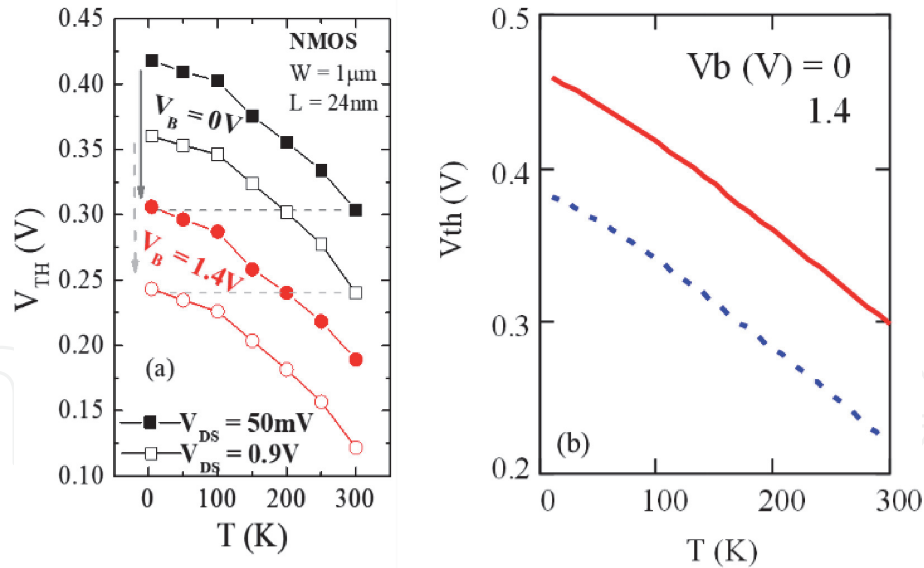
The threshold voltage  $V_{th}$  of the devices has been extracted by the constant current method (*i.e.*  $V_g$  for which  $I_d = 10^{-7} \times W/L$ ) and typical variations with



**Figure 3.** Experimental (a) and modeled (b)  $C_{gc}(V_g)$  characteristics for NMOS GO1 devices ( $W = L = 10 \mu m$ ) at 4.2 K for two AC levels: 40 mV (red solid lines) and 1 mV (blue dashed lines).



**Figure 4.**  $I_d(V_g)$  characteristics for GO1 N and P MOS devices for various temperatures obtained in linear region ( $V_d = 50$  mV).



**Figure 5.**  
 (a) Experimental  $V_{th}$  extracted on NMOS GO1 transistor ( $W = 1 \mu m$ ,  $L = 24 nm$ ) as a function of  $T$  at  $V_{DS} = 50 mV$  and  $0.9 V$ , and at  $V_b = 0 V$  and  $1.4 V$ . (b) Modeled  $V_{th}$  vs.  $T$  for  $V_{ds} = 50 mV$  and  $V_b = 0$  and  $1.4 V$ . After Cardoso et al. [43].

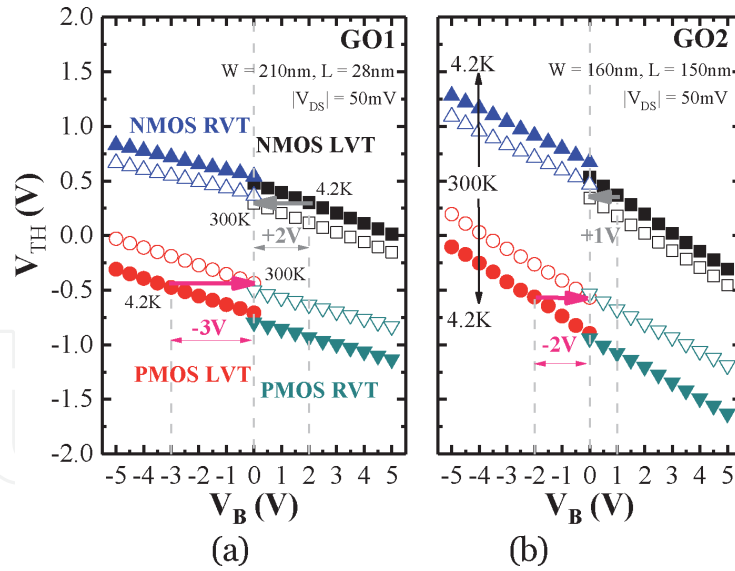
temperature are shown in **Figure 5a**. As in bulk MOS devices [7],  $V_{th}$  increases as the temperature is reduced, here with sensitivity around 0.7 to 1 mV/K. It should be mentioned that in FDSOI devices with undoped film as in our case, the  $V_{th}$  variation with  $T$  is not explained by the temperature dependence of the Fermi level in the silicon film as for bulk MOS devices [44]. Actually, a simple model for  $V_{th}$  read by constant current method can be derived assuming a single subband for the inversion layer with a critical inversion charge density  $n_{th}$  as:

$$V_{th} = V_{sth} + \frac{q \cdot n_{th}}{C_{ox}} + \frac{C_b \cdot (V_{sth} - V_b)}{C_{ox}} \quad (2)$$

with  $V_{sth} = V_0 + \frac{k_B T}{q} \cdot \ln \left( \frac{n_{th}}{e^{k_B T} A_{2D}} - 1 \right)$  being a threshold surface potential associated with a given constant inversion charge density  $n_{th}$  (here  $10^{10}/cm^2$ ), and where  $V_0$  is a constant,  $A_{2D}$  the 2D subband density of states,  $C_{ox}$  and  $C_{box}$  respectively the front gate oxide and the buried oxide capacitance and  $C_b = C_{box} \cdot C_{si} / (C_{si} + C_{box})$  the body to front channel coupling capacitance. As can be seen from **Figure 5b**, a good qualitative agreement between model and experiment can be achieved with Eq. (2).

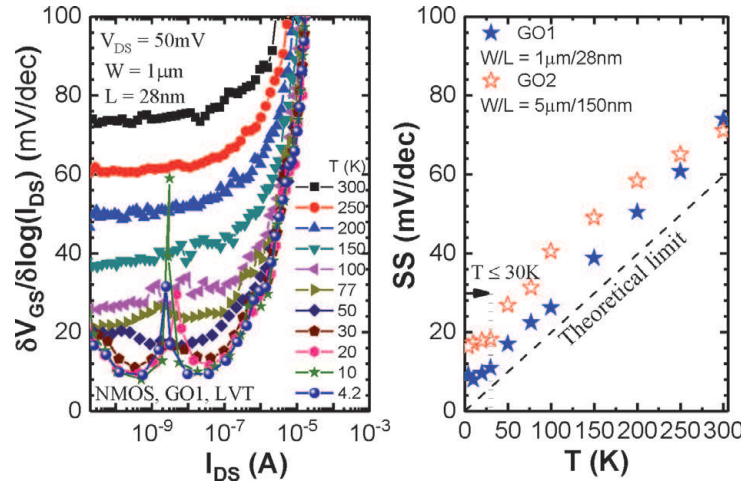
An important feature of FDSOI devices is the strong  $V_{th}$  control allowed by the back bias, which is not possible in FinFET and NW architectures, and very limited in bulk MOS devices [7], especially in forward biasing. Typical dependence of  $V_{th}$  with back bias are illustrated in **Figure 6** for both P and N MOS FDSOI devices of various flavors and gate oxide thicknesses (GO1 and GO2), at  $T = 4.2 K$  and  $T = 300 K$ . As can be seen from this figure, it appears that the threshold voltage control with back biasing ( $\Delta V_{th} / \Delta V_b$ ) is insensitive to temperature down to cryogenic conditions, and that  $V_{th}$  can be decreased to values close to zero volt. Interestingly, this makes it possible to operate the FDSOI devices at deep cryogenic temperatures with very small supply voltage ( $\approx 0.1-0.2 V$ ), enabling low power dissipation.

Another important parameter in FET operation is the so called subthreshold slope,  $S = d \ln(I_d) / dV_g$ , or its inverse the subthreshold swing SS, which characterizes the turn-on efficiency of the MOSFET below threshold. Typical subthreshold swing SS (mV/dec) variations with drain current in weak inversion region are shown in



**Figure 6.**

Measurements of  $V_{th}$  vs.  $V_b$  for N- and P-type, RVT and LVT, GO1 (a) and GO2 (b) MOSFETs, at 300 K and 4.2 K,  $V_{DS} = 50$  mV. As  $T$  is decreased,  $V_b$  can be used to shift  $V_{th}$  back to its value at room temperature. After Cardoso et al. [40].



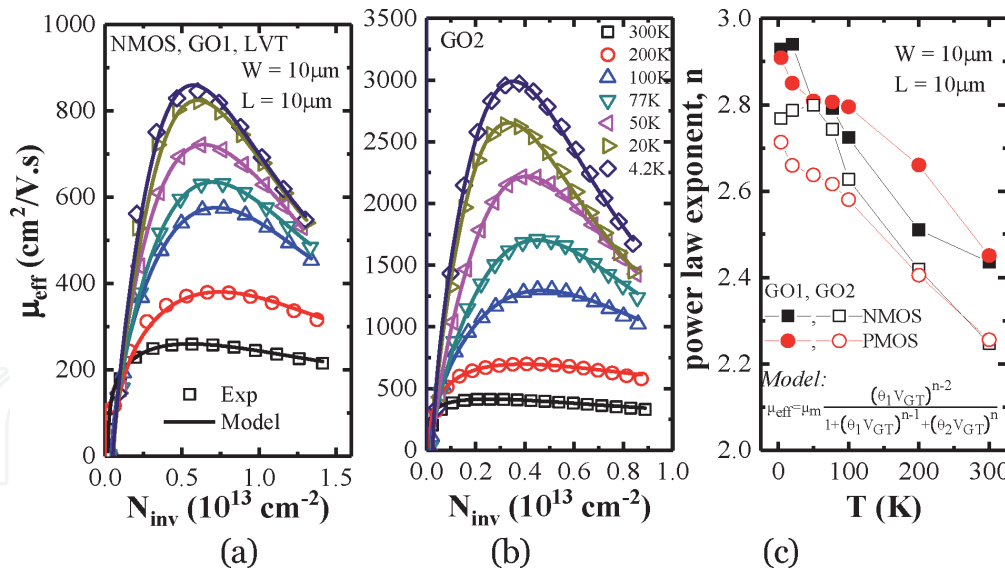
**Figure 7.**

Extracted subthreshold current vs.  $I_d$  (a) and  $SS$  vs.  $T$  (b) for NMOS LVT from 300 K to 4.2 K. After Cardoso et al. [45].

**Figure 7a**, revealing a plateau from which an average subthreshold swing can be extracted and plotted versus temperature (**Figure 7b**). Indeed, the subthreshold swing  $SS$  is varying linearly with temperature down to 25-30 K before plateauing around 10-20 mV/decade at deep cryogenic temperatures. The  $SS(T)$  linear behavior is usual for all FET devices and simply related to the Maxwell-Boltzmann statistics prevailing in weak inversion where  $SS = kT/q \cdot (C_{ox} + C_b + C_{it})/C_{ox}$ ,  $C_{it}$  being the interface trap density capacitance [7]. The  $SS(T)$  plateau is generally attributed to the presence of an exponential tail of subband states, likely due to potential-fluctuations-induced disorder [46–48] and that minimizes the drain current turn-on efficiency at deep cryogenic temperatures.

## 2.4 Carrier mobility

Finally, the effective carrier mobility  $\mu_{eff}$  is investigated as being a driving parameter of MOSFET in linear region. In **Figure 8a** and **b** are illustrated typical mobility variations with inversion charge  $N_{inv}$  as obtained by split C-V method in



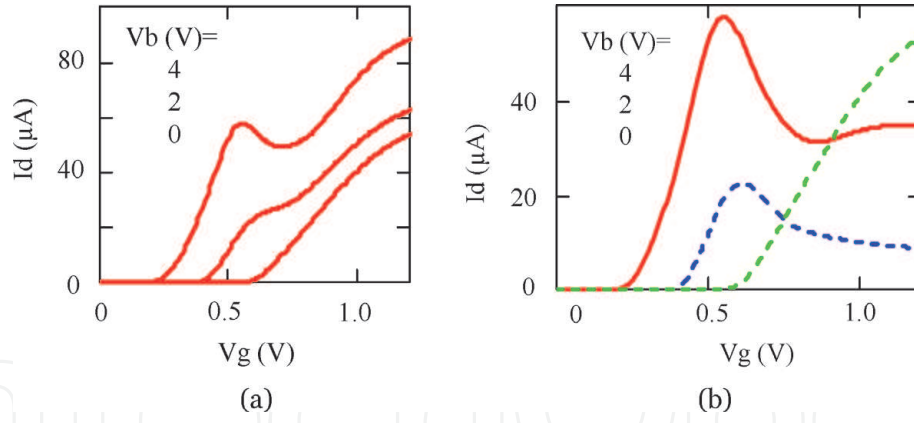
**Figure 8.**  
 Experiments and analytical model of  $\mu_{eff}$  vs.  $N_{inv}$  for NMOS GO1 (a) and GO2 (b), varying  $T$ , power law exponent (c) vs.  $T$  for N and PMOS. After Cardoso et al. [49].

such FDSOI MOS devices for various temperatures. As can be seen, there is a strong improvement (up to 10 times) of the maximum mobility with temperature lowering due to phonon scattering reduction [7]. As already found for bulk Si MOSFET [7], the effective mobility exhibits a bell-shaped behavior with inversion charge at low temperature, where the mobility is limited by combined Coulomb and surface roughness scattering processes. As also shown in **Figure 8**, the mobility can be well fitted by an empirical model inspired from bulk MOSFET results and written as:

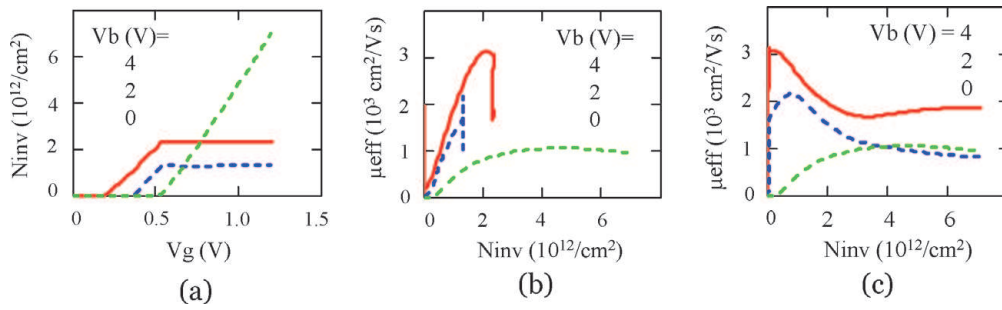
$$\mu_{eff} = \mu_m \cdot \frac{\left(\theta_1 \cdot \frac{Q_i}{C_{ox}}\right)^{n-2}}{1 + \left(\theta_1 \cdot \frac{Q_i}{C_{ox}}\right)^{n-1} + \left(\theta_2 \cdot \frac{Q_i}{C_{ox}}\right)^n} \quad (3)$$

where  $\mu_m$  stands for an amplitude mobility value close to the maximum one,  $\theta_1$  and  $\theta_2$  are the first and second order attenuation coefficients and  $n$  is a power law exponent varying between  $\approx 2$  and  $\approx 3$  as the temperature is changed from 300 K down to 4.2 K, as illustrated in **Figure 8c**. It should be noted that this mobility law vs. inversion charge will be useful for compact modeling purpose (see **Section 5**).

As was already mentioned, a specific feature of FDSOI devices is their operation in forward back biasing condition, enabling a significant lowering of the threshold voltage as illustrated in **Figure 9a** for  $T = 4.2$  K. Interestingly, for sufficiently large  $V_b$ , the drain current measured at low  $V_d$  and very low temperatures (here  $T = 4.2$  K) is increasing above back channel threshold before to decrease significantly and then to increase again well above front channel threshold. Actually, this decrease of the drain current just happens when the front channel is opening and has been attributed to a reduction of the mobility due to remote inter-subband scattering (IS) as well explained in [50]. To better understand this behavior, we have computed the drain current of the back channel after subtraction of the front channel component, taken as being the one in absence of back channel formation i.e. when  $V_b = 0$  V (see **Figure 9b**). This assumption has been validated by Poisson-Schrodinger simulation (not shown here). Doing the same with  $C_{gc}(V_g)$  characteristics for various  $V_b$ 's, the inversion charge in the back channel has also been computed after integration of capacitance vs.  $V_g$  as is usual in split C-V technique (**Figure 10a**). As a result, note that the back channel charge is plateauing after the



**Figure 9.** a)  $I_d(V_g)$  characteristics at 4.2 K for various  $V_b$  ( $= 0, 2$  V, 4 V) and b) Back channel  $I_d(V_g)$  curves after subtraction of front channel component also shown in green dashed line.



**Figure 10.** a)  $N_{inv}$  vs.  $V_g$  for Back channel for  $V_b = 2$  V, 4 V. Green curve shows  $N_{inv}(V_g)$  for front channel at  $V_b = 0$ . b) Back channel  $\mu_{eff}$  vs. back channel  $N_{inv}$  and c) Back channel  $\mu_{eff}$  vs. front channel  $N_{inv}$  for  $V_b = 2$  V, 4 V. Green curves show front channel  $\mu_{eff}$  vs. front channel  $N_{inv}$  at  $V_b = 0$  V.

opening of front channel. The effective mobility in the back channel has been computed and plotted versus inversion charge density in the back channel or versus the front one as shown in **Figure 10b** and **c**. As can be seen,  $\mu_{eff}$  first increases with the back channel inversion charge density before to decrease as the back channel charge saturates (**Figure 10b**). Instead,  $\mu_{eff}$  in back channel decreases with the front channel inversion charge, which clearly indicates that the opening of the front channel is responsible for the back channel mobility decrease. This is precisely the signature of remote inter-subband scattering, which happens when carriers in the back interface 2D subband can interact with the front interface 2D subband. In this situation, some carriers at the back interface can experience scattering mechanisms in the front interface due to the overlap of the back and front subband wave functions. It should be mentioned that this phenomenon of inter-subband scattering is canceling out when the temperature is increased ( $T > 50$  K) due to thermal broadening as well as when the drain voltage is increased due to the averaging over the channel of the conductance by integration over space [50].

### 3. Self-heating phenomena

In FDSOI devices or multi-gate field effect transistors like FinFETs and nanowire FETs, low thermally conductive materials such as the buried oxide (BOX) or the thin Si layer constituting the channel hinder the dissipation of the heat generated in the drain side. Consequently, the channel temperature can significantly rise when the device is in ON operation. This self-heating effect (SHE) can in

turn severely affect the device performance, by reducing the carrier mobility, shifting the threshold voltage [51] or degrading the device reliability [52, 53], with implications to IC design. SHE has been widely studied for room temperature operation of circuits [54]. The thermal effects play a more fundamental role in cryogenic electronics – operating at various temperature stages with different available cooling powers –, as the temperature increase due to SH can be of the same order or even higher than the ambient temperature [55]. Furthermore, at very low temperature (well below 1 K), the cooling power drops down drastically (typically, 1 W at 1 K, 1 mW at 100mK) and thermal management thus becomes an additional constraint.

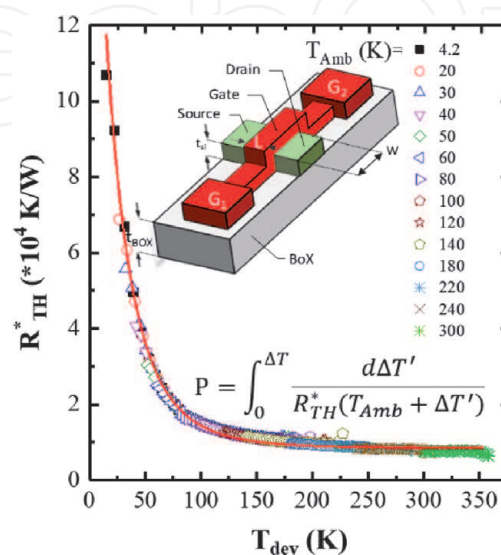
In this regard, the study of self-heating effects at cryogenic temperatures provides valuable information for performance optimization. In addition, to be accurate at cryogenic temperatures, models must take into account these thermal effects, as the device temperature can deviate significantly from the ambient one.

### 3.1 Self-heating characterization technique

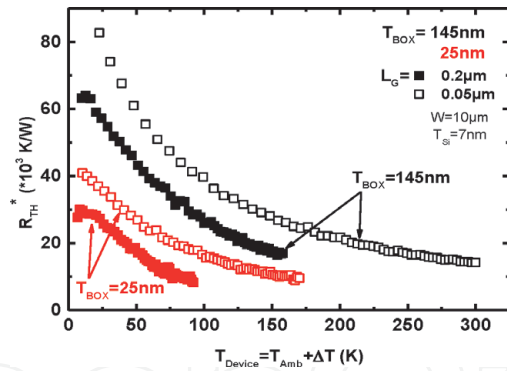
The experimental evaluation of self-heating was performed by using the conventional DC technique based on gate resistance thermometry [56]. In this method, the gate dielectric layer is thin enough to assume that the temperature of the channel is equal to that of the gate electrode. Inset of **Figure 11** shows the typical 2-terminal gate structure that we used to measure the gate resistance  $R_G$ .  $R_G$  is measured between two contacts G1 and G2 using an LCR-meter. By varying the ambient temperature  $T_{amb}$  from 4.2 K up to 300 K, we record the change in the electrical gate resistance as a function of the input power  $P = I_{DS} \times V_{DS}$ . The temperature increase  $\Delta T$  is deduced from  $R_G$  values at zero power (and so without SHE). Then the differential thermal resistance,  $R_{TH}^* = \partial \Delta T / \partial P|_{T_{amb}}$  can be defined. This differential thermal resistance relates the change of  $\Delta T$  due to a change in power dissipation  $P$  at a given  $T_{amb}$  [55].

### 3.2 Study of thermal resistance

In **Figure 11** we have plotted the differential thermal resistance measured on an ultrathin film FDSOI transistor ( $t_{Si} = 11$  nm) as a function of the device temperature



**Figure 11.**  
 (symbols) Differential thermal resistance  $R_{TH}^*$  measured as a function of the device temperature  $T_{device} = T_{amb} + \Delta T$  from 450 K down to 4.2 K, with a corresponding numerical fitting curve (line).

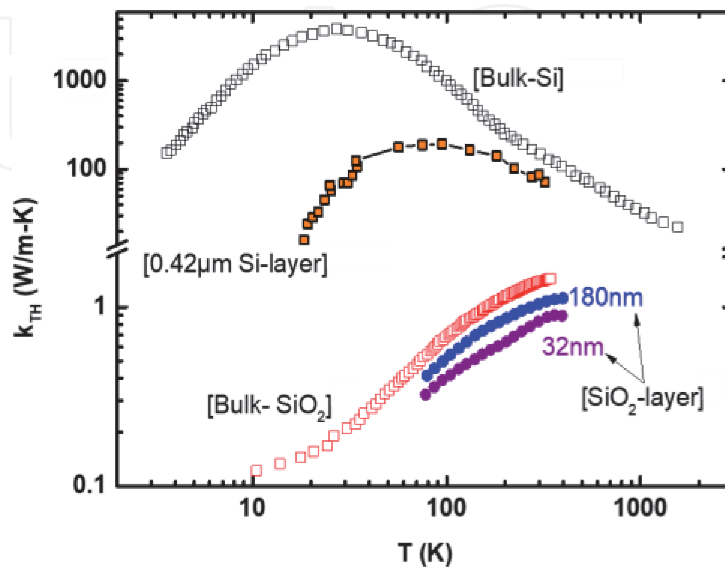


**Figure 12.** Thermal resistance  $R_{TH}^*$  versus device temperature, for wide and ultrathin FDSOI MOSFETs. After Triantopoulos et al. [55].

defined as  $T_{device} = T_{amb} + \Delta T$ . All the  $R_{TH}^*$  data acquired for various ambient temperatures and dissipated power values merge into a single  $R_{TH}^*$  versus  $T_{device}$  curve, which thus provides a complete description of the temperature dependence of the thermal resistance for a given device. The thermal resistance depends mainly on the device geometry  $W$  and  $L$ , as well as on the BOX thickness, but not significantly on the Si film thickness in the 7 nm to 24 nm range typical of FDSOI devices (**Figure 12**) [55].

Our results show that in thin film devices, the thermal resistance  $R_{TH}^*$  of the device is strongly temperature dependent, especially at very low temperature, as illustrated in **Figures 11** and **12**. As the device temperature decreases from 300 K down to 4 K,  $R_{TH}^*$  is multiplied by 3 to 6. In FDSOI devices, the BOX tends to confine the heat in the channel, and therefore the total thermal resistance depends on both the thermal conductivity of Si and SiO<sub>2</sub>, which have different temperature dependence and magnitude (**Figure 13**).  $R_{TH}^*$  follows the temperature dependence of the inverse of the silicon dioxide thermal conductivity in the whole range of explored temperatures [57].

Besides considerations over the dominant thermal path in the device, the  $R_{TH}^*$  vs.  $T_{device}$  plot can be used into thermal model in order to reconstruct the channel

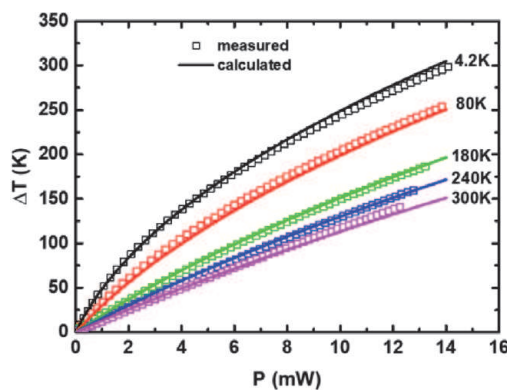


**Figure 13.** Thermal conductivity data versus temperature for bulk and Si-layer compared to that for bulk and SiO<sub>2</sub>-layer. After Triantopoulos et al. [55].

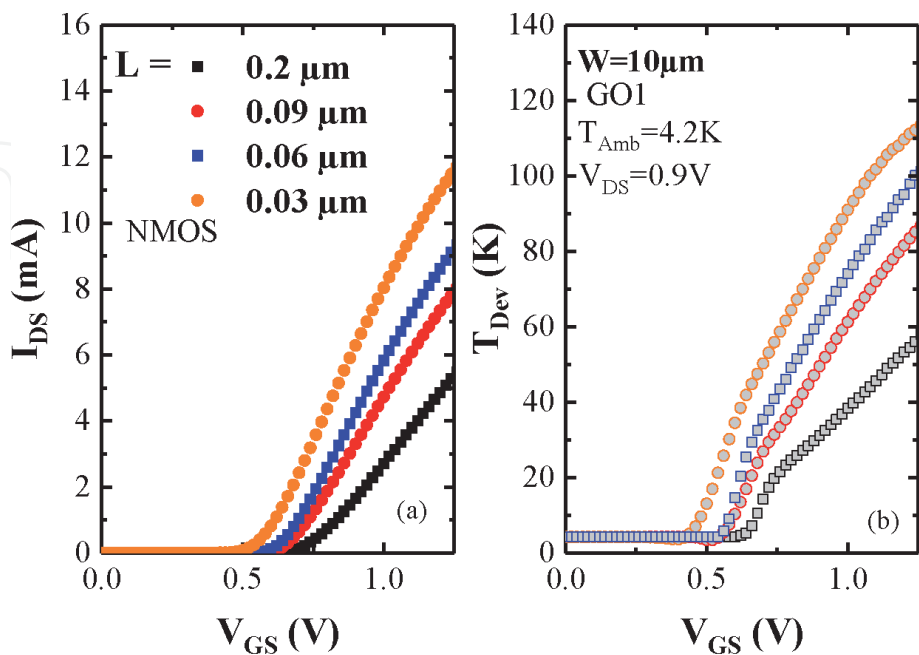
temperature increase  $\Delta T$  as a function of operating ambient temperature  $T_{amb}$  and input power  $P$  using the following expression,

$$P = \int_0^{\Delta T} \frac{d\Delta T'}{R_{TH}^*(T_{amb} + \Delta T')} \tag{4}$$

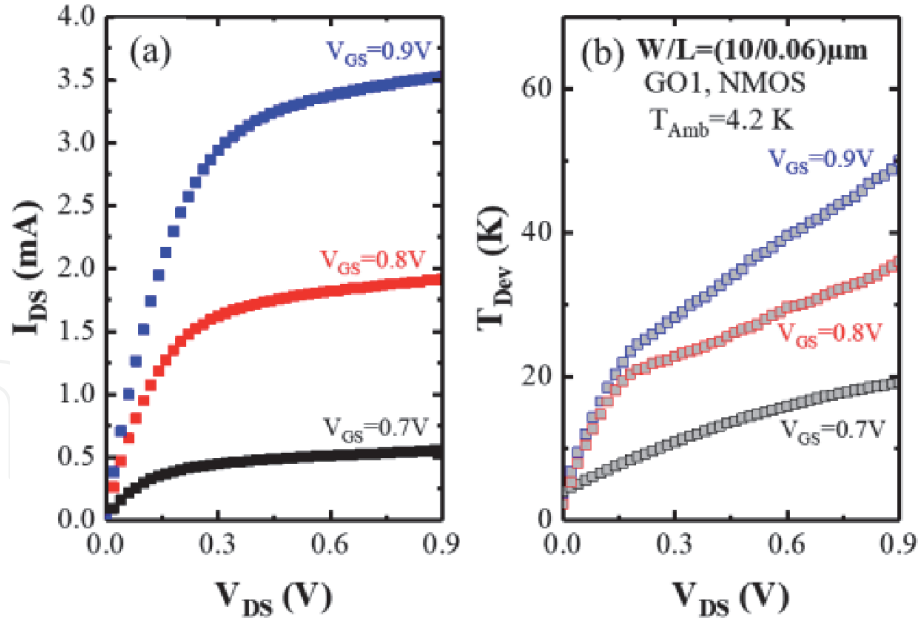
Substituting a given analytical expression of  $R_{TH}^*(T_{device})$  in Eq. (4) the value of  $\Delta T$  at each  $T_{amb}$  and for each value of dissipated power can be calculated (Figure 14). This leads in particular to a nonlinear temperature increase of the device with the dissipated power. In this specific low temperature environment, the device temperature can significantly increase and thus highly deviate from the ambient temperature, depending on the applied gate and drain voltages, as illustrated in Figures 15 and 16.



**Figure 14.** Calculated channel temperature increase  $\Delta T$  (line) as a function of the dissipated power  $P$  using Eq. (4) and a fitting expression for  $R_{TH}^*(T_{dev})$ . Experimental data (symbols) are also shown for a direct comparison. After Triantopoulos et al. [55].



**Figure 15.** (a)  $I_{DS}$  vs.  $V_{GS}$  measured on NMOS at  $T_{amb} = 4.2$  K and  $V_{DS} = 0.9$  V for different gate lengths, and (b) corresponding device temperature,  $T_{dev}$  vs.  $V_{GS}$ .



**Figure 16.**

(a)  $I_{DS}$  vs.  $V_{DS}$  measured at  $T_{amb} = 4.2 K$  on NMOS with  $L = 60 nm$  for different  $V_{GS}$  values, and (b) corresponding  $T_{dev}$  vs.  $V_{DS}$ .

## 4. Mismatch and variability properties

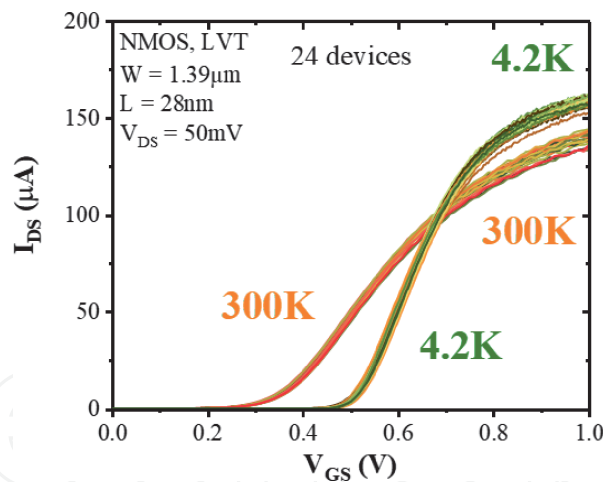
The device mismatch is a key property to be known for the development of transistor compact models and the design of electronic circuits [58–60]. This section presents variability results obtained on FDSOI MOSFETs down to 4.2 K. To this end, an integrated on-chip matrix of individually addressable transistors has been used to increase the sample size statistics.

### 4.1 Devices under test

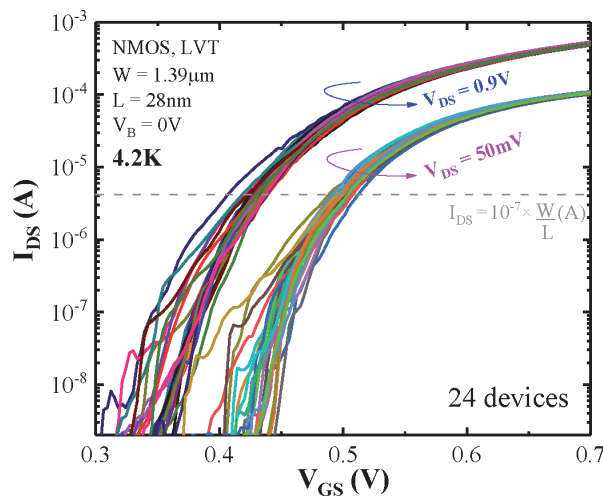
The measurements were performed on both N- and P-type transistors fabricated using the same 28 nm FDSOI technology as those described in **Section 2.1**. In order to provide statistical analysis on variability and mismatch at low temperature, matrices of transistors were produced with integrated addressability in an approach similar to [61]. An automated measurement system was implemented thanks to the on-chip multiplexed arrangement. The device chips were wire-bonded on a chip carrier connected to a printed circuit board (PCB) and mounted on a dipstick to reach 4.2 K in a liquid helium bath. Each die comprises 512 matched pairs of MOSFETs (256 pairs of RVT plus 256 pairs of LVT) addressable through 10-bits selection ( $2^{10} = 1024$  transistors).

### 4.2 Threshold voltage variability

**Figure 17** shows typical drain current  $I_d(V_g)$  characteristics for short channel N-type MOS transistors, at 300 K and at 4.2 K. Twenty four devices were measured for each MOS type at low drain voltage ( $|V_d| = 50 mV$ ) to illustrate device variability. In **Figure 18** the logarithmic scaled  $I_d(V_g)$  emphasizes the subthreshold oscillation variability at low and high drain voltage ( $V_d = 50 mV$  and  $0.9 V$ ), at 4.2 K. The oscillations observed in the subthreshold current are a known signature of short channel MOSFETs operating at deep cryogenic temperatures, and could result from the presence of impurities in the channel [63, 64]. The threshold voltage was



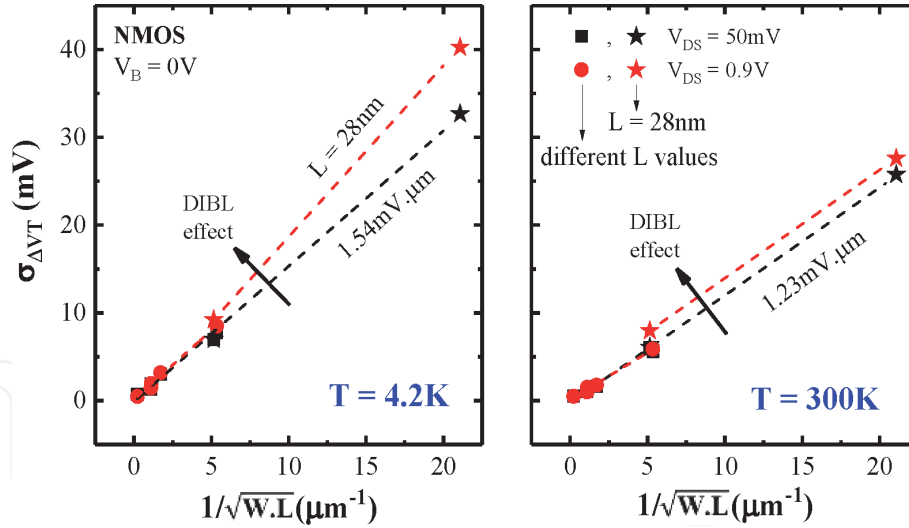
**Figure 17.**  
 $I_d(V_g)$  curves for 24 short channel ( $L = 28$  nm) N-type LVT MOSFETs at 4.2 K and 300 K, at  $V_d = 50$  mV. After Cardoso et al. [62].



**Figure 18.**  
 $I_d(V_g)$  curves for 24 short channel ( $L = 28$  nm) N-type LVT MOSFETs at 4.2 K, at  $V_d = 50$  mV and 0.9 V. After Cardoso et al. [62].

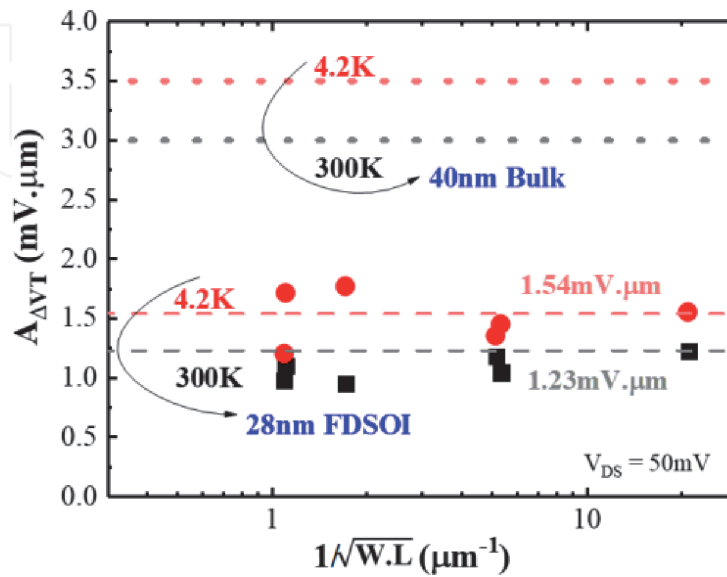
extracted following the constant current criterion, at  $I_d = 10^{-7}$  W/L (A). Such current level represents the standard value used for  $V_{th}$  extraction, and it is well above the region where the oscillations are mainly identified, as highlighted in **Figure 18** by a dashed line.

**Figure 19** shows the Pelgrom plots of the standard deviation of  $\Delta V_{th}$ ,  $\sigma_{\Delta VT}$ , for NMOS devices (similar results have been obtained for PMOS). It can be seen that  $\sigma_{\Delta VT}$  well follows the area scaling linear dependence with respect to  $1/\sqrt{W \cdot L}$  at 4.2 K, as it is the case at 300 K, for all channel dimensions explored in this study ( $1 \mu\text{m} \leq L \leq 28$  nm,  $80 \text{ nm} \leq W \leq 25 \mu\text{m}$ ). This result does not reveal any specific variation with channel width and channel length due to e.g. line edge roughness (LER) for such geometries. From 300 K to 4.2 K, the extracted linear slopes,  $\Delta\sigma_{\Delta VT}/\Delta(1/\sqrt{W \cdot L})$ , indicates that the threshold voltage mismatch performance degrades by  $\approx 25\%$  for NMOS and PMOS, at  $|V_d| = 50$  mV, when temperature is decreased from 300 K down to 4.2 K. Since the metal gate granularity and the local charges in the gate dielectric are the main sources of threshold voltage variability in FDSOI technology [65], the slight increase of  $\sigma_{\Delta VT}$  at 4.2 K may likely be attributed to the increase of interface charge density [63]. Moreover, in **Figure 19**, it can be seen that short channel MOSFETs ( $L = 28$  nm) exhibit higher threshold voltage variability at high drain bias ( $V_d = 0.9$  V), which could be due to Drain Induced Barrier Lowering (DIBL).



**Figure 19.** Pelgrom plot of threshold voltage variability  $\sigma_{\Delta V_T}$  for NMOS at  $V_d = 50\text{ mV}$  and  $0.9\text{ V}$ ,  $4.2\text{ K}$  (left) and  $300\text{ K}$  (right). After Cardoso et al. [62].

**Figure 20** shows the threshold voltage individual mismatch parameter,  $A_{\Delta V_T} = \sigma_{\Delta V_T} \cdot \sqrt{W \cdot L}$ , plotted as a function of  $1/\sqrt{W \cdot L}$ , for  $28\text{ nm}$  FDSOI transistors studied in this work and  $40\text{ nm}$  bulk MOSFETs from [61], at  $300\text{ K}$  and  $4.2\text{ K}$ . Despite  $A_{\Delta V_T}$  degradation at low temperature, FDSOI remains highly competitive compared to bulk technology, mainly due to the suppression of random dopant fluctuation (RDF) induced variability in FDSOI. In **Figure 20**, it can also be observed that  $A_{\Delta V_T}$  does not exhibit higher values for the short channel MOSFETs (i.e. high  $1/\sqrt{W \cdot L}$  values), for which subthreshold oscillations have been observed at low temperature (**Figure 18**). This means that such oscillations do not have a significant impact on the threshold voltage variability, mainly because they occur below the drain current level where the threshold voltage is extracted, as discussed before.



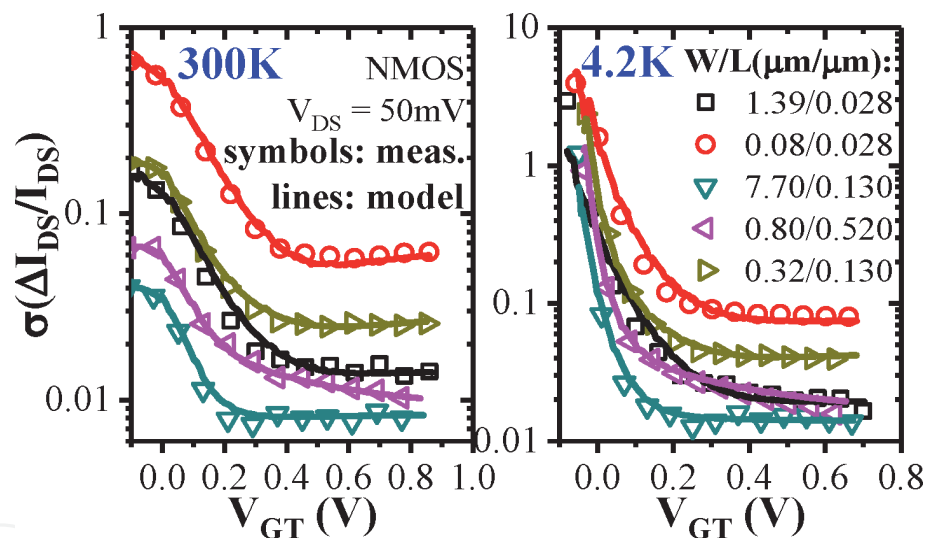
**Figure 20.**  $A_{\Delta V_T}$  versus  $1/\sqrt{W \cdot L}$  for NMOS, at  $V_d = 50\text{ mV}$ ,  $4.2\text{ K}$  and  $300\text{ K}$ . dashed lines indicate the extracted linear slope values from the Pelgrom plots. Dotted lines show typical  $40\text{ nm}$  bulk CMOS technology data [61]. After Cardoso et al. [62].

4.3 Drain current variability

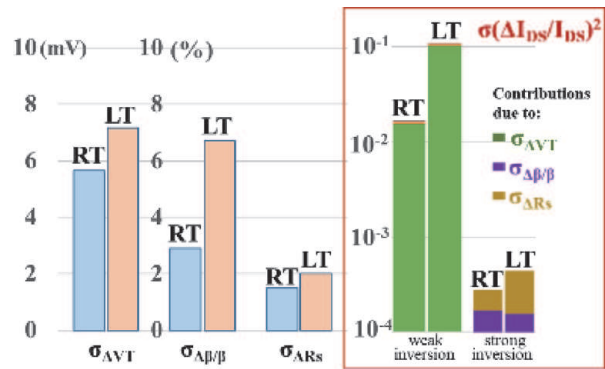
The drain current variability,  $\sigma(\Delta I_d/I_d)$ , has also been directly measured on the 28 nm FDSOI transistors studied here and their variations with gate voltage over-drive are shown in **Figure 21** for 300 K and 4.2 K. As is usual,  $\sigma(\Delta I_d/I_d)$  is maximized below threshold before to decrease in strong inversion, where it might slightly increase again due to the contribution of access resistance  $R_s$  variability [66]. Actually, these variations can be very well fitted by the model of Eq. (5) developed for room temperature:

$$\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \left(\frac{g_m}{I_d}\right)^2 \cdot \sigma_{\Delta V_T}^2 + (1 - g_d \cdot R_s)^2 \cdot \sigma_{\Delta \beta/\beta}^2 + g_d^2 \cdot \sigma_{\Delta R_s}^2 \tag{5}$$

where  $g_m$  is the transconductance and  $g_d$  is the output conductance. In this model, the drain current variability is controlled by three matching parameters related respectively to the threshold voltage,  $\sigma_{\Delta V_T}$ , the gain factor  $\sigma_{\Delta \beta/\beta}$  ( $\beta = W/L \cdot C_{ox} \cdot \mu_0$ , with  $\mu_0$  being the low-field carrier mobility) and to the access resistance  $\sigma_{\Delta R_s}$ . Typical matching parameters extracted from the drain current modeling, as well as their respective contributions are summarized in **Figure 22**. It indicates that there is a slight degradation of variability at low temperature and that the matching



**Figure 21.** Measured and modeled  $\sigma(\Delta I_d/I_d)$  variations with  $V_{gt} = V_g - V_{th}$ .  $\sigma_{\Delta R_s}$  varies from 0 to 8% of  $R_s = 377 \, \Omega \cdot \mu m$  ( $T = 300 \, K$ ) and  $266 \, \Omega \cdot \mu m$  ( $T = 4.2 \, K$ ). After Cardoso et al. [45].



**Figure 22.** Summary of matching performance and respective parameter contributions at 300 K (RT) and 4.2 K (LT) for NMOS ( $W = 1.39 \, \mu m$ ,  $L = 28 \, nm$ ). After Cardoso et al. [45].

is mainly dominated by threshold voltage variability in weak inversion and by gain factor and access resistance mismatch at strong inversion.

## 5. Device compact modeling approach

In previous sections, we focus our efforts on understanding individual device physics and variability at cryogenic temperature. In this section, we present typical Poisson-Schrodinger simulation results for the capacitance and charge control in FDSOI structures operated down to deep-cryogenic temperatures and their application for building up an analytical compact model for charge and drain current in FDSOI MOSFET including back biasing effect.

### 5.1 Poisson-Schrodinger simulations

Poisson-Schrodinger (PS) simulations were conducted after solving self-consistently the Schrodinger and Poisson equations given below:

$$H(\psi) = E \cdot \psi \quad (6)$$

$$\nabla(\epsilon_r \nabla V) = -\frac{q \cdot n(x)}{\epsilon_0} \quad (7)$$

with  $H$  the Hamiltonian,  $E$  the system energy,  $\psi$  the electron wave function,  $\epsilon_0$  and  $\epsilon_r$  the vacuum and relative silicon permittivity,  $n$  the carrier density as a function of position  $x$  in the Si channel depth. The electrical potential  $V$ , the subband energies  $E_{i,j}$  and wave functions  $\psi_{i,j}$  for valley  $j$  and level  $i$  are numerically calculated in a FDSOI structure for given front and back gate voltages. Then, the electron density is obtained after summing the different valleys and subband contributions as:

$$n(x) = \sum_{j=1}^2 \sum_{i=1}^{i_{max}} g_j A_{2D,j} k_B T \psi_{i,j}^2(x) \cdot F_0 \left( \frac{E_f - E_{i,j}}{k_B T} \right) \quad (8)$$

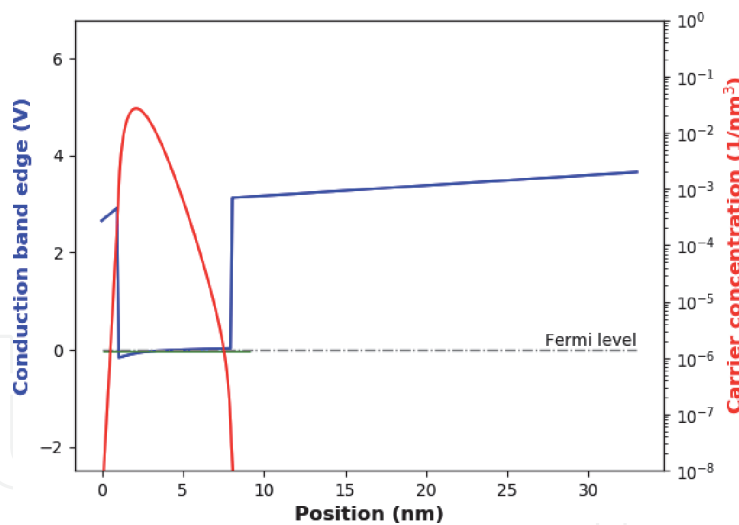
where  $k_B T$  is the thermal energy,  $F_0$  is the zero-order Fermi-Dirac integral function,  $E_f$  the Fermi level,  $E_{i,j}$  the subband energy,  $g_j$  the valley degeneracy, and  $A_{2D,j}$  the 2D density of states of valley  $j$ .

It should be noted that in order to compute the PS equations down to very low temperature (1 K), special truncation caution has been taken to avoid numerical overload in the  $F_0$  Fermi integral function accounting for Fermi-Dirac statistics. PS simulations were also possible at 0 K by replacing the  $F_0$  Fermi-Dirac integral function by a Heaviside function, thus mimicking the fully degenerate metallic statistics.

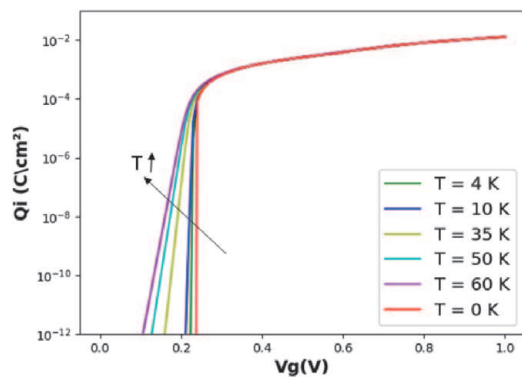
The 1D FDSOI structure used for PS simulation is depicted in **Figure 23**, showing the band diagram across the stack and typical electron density profile in the channel obtained at  $T = 4$  K for a given bias condition.

**Figure 24** demonstrates the variations of the inversion charge  $Q_i$  in the Si film as a function of front gate voltage  $V_g$  with  $V_b = +3$  V, obtained from PS simulations for various temperatures between 0 K and 60 K. A strong increase of the subthreshold slope with temperature dropping can be noticed, reaching infinity at  $T = 0$  K, which is an interesting feature for transistors operating at such low temperatures.

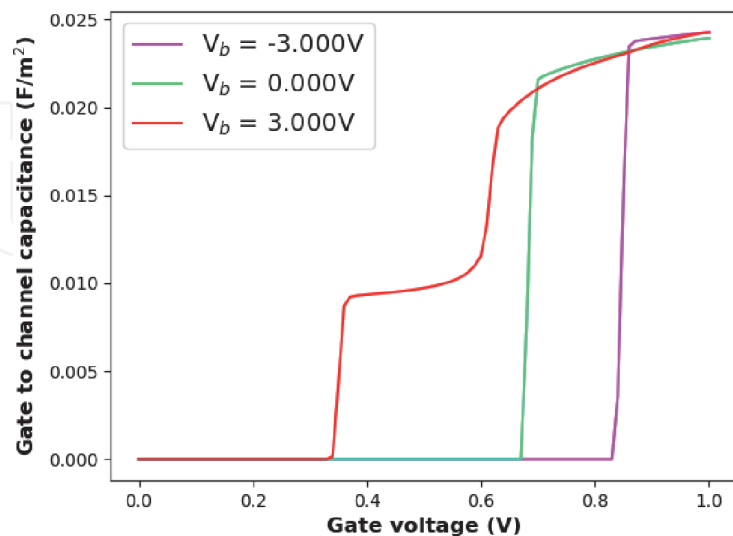
**Figure 25** shows the inversion charge control by field effect through the variations of the gate-to-channel capacitance  $C_{gc}(V_g) = dQ_i/dV_g$  with front gate voltage



**Figure 23.**  
Typical band diagram and electron distribution from PS simulation for a FDSOI structure ( $V_g = 1$  V,  $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 7$  nm,  $V_b = 0$  V,  $T = 4$  K). After Aouad et al. [41].



**Figure 24.**  
Inversion charge  $Q_i(V_g)$  calculated for different temperatures ( $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 7$  nm,  $V_b = +3$  V). After Aouad et al. [41].



**Figure 25.**  
 $C_{gc}(V_g)$  curves for different back biases  $V_b$  ( $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 10$  nm,  $T = 4$  K). After Aouad et al. [41].

for various back gate biases  $V_b$ . The onset of the back inversion channel for  $V_b = +3$  V is evidenced by an additional plateau in the  $C_{gc}(V_g)$  curve, followed by the front channel opening. This effect clearly demonstrates the capacitive coupling,

through the silicon channel, between the front gate and the back channel inversion layer, which leads to a lower capacitance.

The impact of temperature on the  $C_{gc}(V_g)$  characteristics is shown in **Figure 26**, clearly revealing the rounding of the curves with temperature rise above  $T = 10$  K.

## 5.2 Compact modeling

Following the PS simulation results, an analytical model has been established considering that front and back channel charges can be evaluated separately at each interface within a single subband approximation with energy level of a triangular potential well [41]. The coupling between the front and back channels is realized owing to the silicon channel capacitance  $C_{si}$  and the charge sheet approximation with Fermi-Dirac statistics.

In this case, the charge conservation equations at front and back interfaces are expressed by:

$$V_g = V_{fb} + V_{s1} + \frac{qN_{inv1}}{C_{ox}} + \frac{C_{si} \cdot (V_{s1} - \Delta V(F_1) - V_{s2} + \Delta V(F_2))}{C_{ox}} \quad (9)$$

$$V_b = V_{fb} + V_{s2} + \frac{qN_{inv2}}{C_{box}} + \frac{C_{si} \cdot (V_{s2} - \Delta V(F_2) - V_{s1} + \Delta V(F_1))}{C_{box}} \quad (10)$$

where the front and back interface 2D charge densities read,

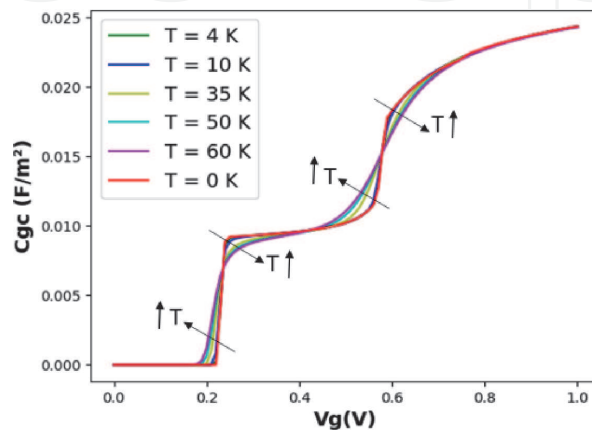
$$N_{inv1,2} = A_{2d} \cdot k_B \cdot T \cdot F_0 \left[ \frac{V_{s1,2} - V_0 - \Delta V(F_{1,2})}{k_B T} \right] \quad (11)$$

where  $V_{s1}$  ( $V_{s2}$ ) is the front (back) interface surface potential,  $C_{ox}$  ( $C_{box}$ ) the front (back) oxide capacitance,  $C_{si}$  the silicon film capacitance. The front and back electric field are given by:

$$F_1 = (V_g - V_{s1} - V_{fb}) / 3t_{ox} \quad (12)$$

$$F_2 = (V_b - V_{s2} - V_{fb}) / 3t_{box} \quad (13)$$

with the Airy subband potential shift  $\Delta V(F) = K \cdot |F + F_0|^{2/3}$  with  $K = 1.75 \times 10^{-5} \text{ V}^{1/3} \text{ cm}^{2/3}$  [67]. As the film quantization effect is dominating when



**Figure 26.**

$C_{gc}(V_g)$  curves for different temperatures ( $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 10$  nm,  $V_b = +3$  V). After Aouad et al. [41].

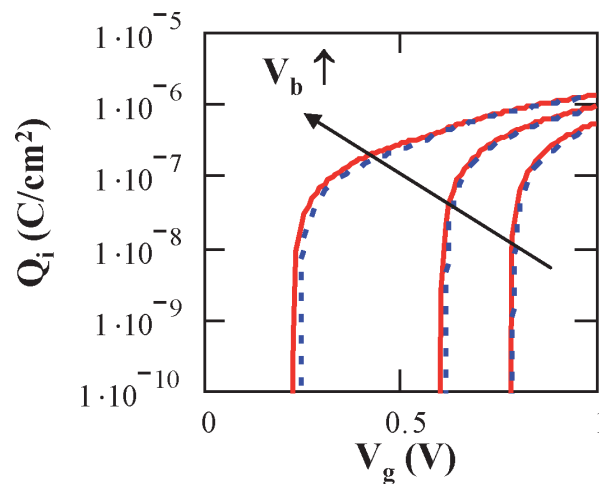
the electrical field approaches zero, an offset field  $F_0$  is added to the electric field to account for the flat band quantum confinement [41].

Typical  $Q_i(V_g)$  and  $C_{gc}(V_g)$  characteristics obtained by this Airy-based analytical model are presented in **Figures 27** and **28**, along with the PS simulation results. As can be seen, the compact model provides a good agreement with PS data, emphasizing its physical consistency in terms of charge and capacitance.

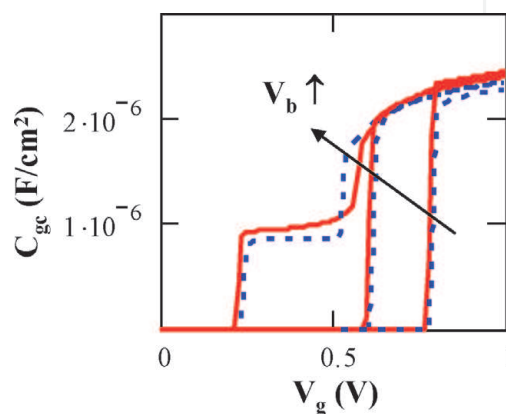
The total drain current in the channel can then computed, within the gradual channel approximation, by integrating the channel conductance between source and drain for the front and back channel and by adding their contribution as:

$$I_d = \frac{W}{L} \int_0^{V_d} \mu_{eff1}(Q_{i1}) \cdot Q_{i1}(V_{s1} - U_c) \cdot dU_c + \frac{W}{L} \int_0^{V_d} \mu_{eff2}(Q_{i2}) \cdot Q_{i2}(V_{s2} - U_c) \cdot dU_c \quad (14)$$

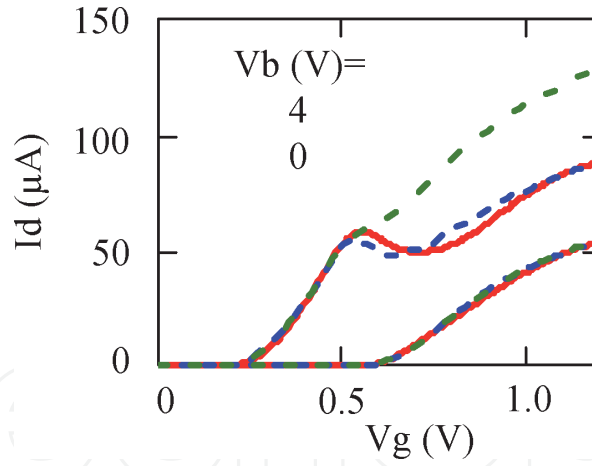
where  $U_c$  is the quasi Fermi level shift between source and drain common to both channels,  $Q_{i1,2} = q \cdot N_{inv1,2}$  are the front and back inversion charges obtained from Eq. (11) and  $\mu_{eff1,2}$  are the front and back channel effective mobility evaluated separately using Eq. (3). In absence of inter-subband scattering, the drain current calculated using Eqs. (3) and (14) does not exhibit a decrease for  $V_b = 4$  V when the front channel is opening, in contrast to the experimental results discussed in **Section 2.3** (see **Figure 29**). Inter-subband scattering can be taken into account



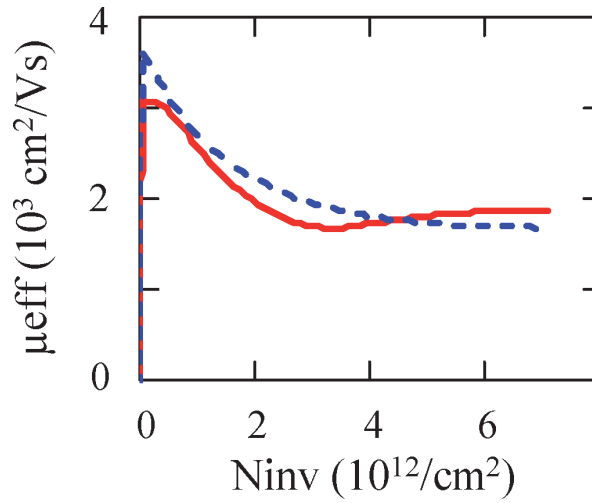
**Figure 27.**  $Q_i(V_g)$  curves obtained from PS simulations (solid lines) and analytical modeling (dashed lines) for various  $V_b = -3, 0, +3$  V ( $T = 4$  K,  $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 10$  nm). After Aouad et al. [41].



**Figure 28.**  $C_{gc}(V_g)$  curves obtained from PS simulations (solid lines) and analytical modeling (dashed lines) for various parameters  $V_b = -3, 0, +3$  V ( $T = 4$  K,  $t_{ox} = 1$  nm,  $t_{box} = 25$  nm,  $t_{si} = 10$  nm). After Aouad et al. [41].



**Figure 29.** Drain current vs. front gate voltage  $V_g$ : Experimental (red solid line) and modeled with IS (dashed blue line) and modeled without IS (green dashed line) for  $V_b = 4$  V and 0 V at  $T = 4.2$  K.



**Figure 30.** Experimental (red solid line) and modeled (dashed blue line) back channel mobility  $\mu_{eff}$  vs. front channel inversion charge density  $N_{inv1}$  for  $V_b = 4$  V at  $T = 4.2$  K. model parameters:  $A = 0.45$ ,  $b = 0.55$  and  $c = 1.5 \times 10^{12}/\text{cm}^2$ .

through an additional explicit dependence of the back channel mobility with the front inversion charge density of the form,  $\mu_{eff2,IS} = \mu_{eff2} \cdot [a + b \cdot \exp.(-N_{inv1}/c)]$ , with  $a$ ,  $b$  and  $c$  being fitting parameters (**Figure 30**). By this way, the drain current can reasonably be well modeled as shown in **Figure 29** (dashed blue line), inferring the crucial role of remote inter-subband scattering in the back channel mobility.

## 6. Basic circuit operation at cryogenic temperatures

Although operational cryo-CMOS circuits have been demonstrated down to 30 mK [17, 30, 68–70], unfortunately no mature models are yet available to accurately predict the behavior of passive and active devices at cryogenic temperatures [71, 72]. Due to this lack of compact models at cryogenic temperatures, designers are faced to a blind-design procedure, which reduces the optimization of cryogenic integrated circuits [12, 30, 32, 58, 73–75]. Using the extensive electrical characterizations of single FDSOI transistors at cryogenic temperatures, it is however possible to already design efficient circuits.

Among them oscillators are essential building blocks in many digital and analog circuits. They are required for example to generate a clock signal in the control

circuit of quantum computers [30, 76], and so must be also efficient at cryogenic temperature. Here we have electrically characterized ring oscillator (RO) fabricated from 28 nm-FDSOI technology [30, 77]. **Figure 31a** shows the delay per stage of a 101-stages RO as a function of temperature from 300 K down to 4.2 K. Without any back-biases applied on the MOSFETs composing the inverter stages, decreasing the temperature results in slowing down the RO. This can be explained by the threshold voltage shift at cryogenic temperature, which leads to a decrease of the effective current evaluated from the single characteristics of NMOS and PMOS transistors.

The effective drive current  $I_{EFF}$ , which is a measure of the current drive of the MOSFET during switching and correlates well to circuit delay, can be defined for a single inverter as [78],

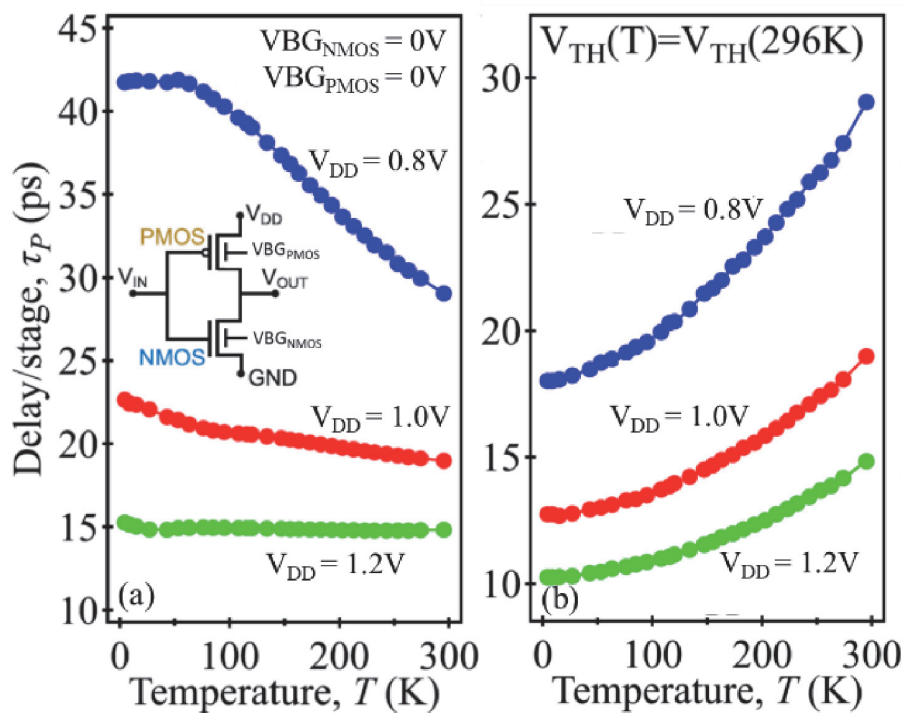
$$I_{EFF} = \left( \frac{1}{I_{EFF,NMOS}} + \frac{1}{I_{EFF,PMOS}} \right)^{-1} \quad (15)$$

with

$$I_{EFF,NMOS/PMOS} = \frac{(I_H + I_L)}{2} \quad (16)$$

where

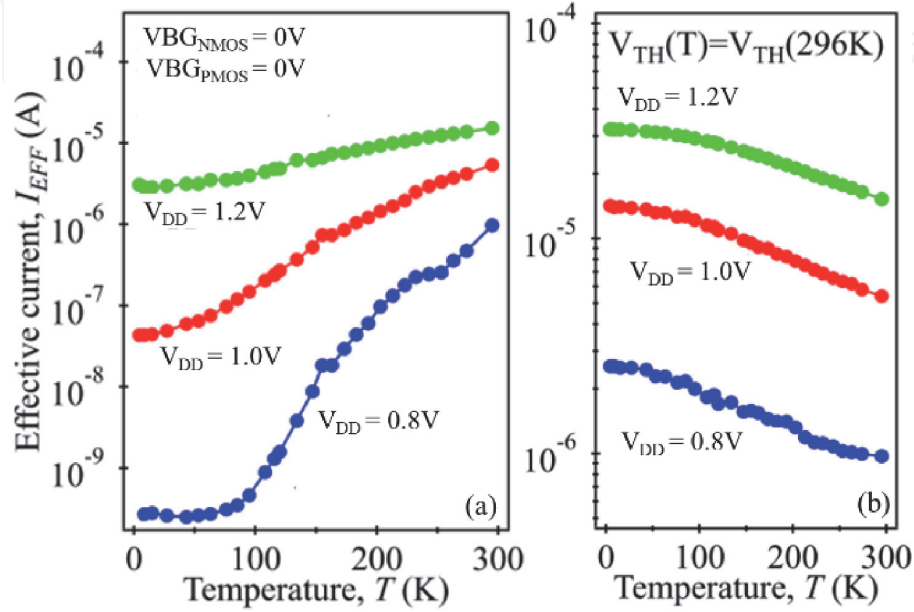
$$\begin{aligned} I_H &= I_{DS}(V_{GS} = V_{DD}, V_D = V_{DD}/2) \\ I_L &= I_{DS}(V_{GS} = V_{DD}/2, V_D = V_{DD}) \end{aligned} \quad (17)$$



**Figure 31.**

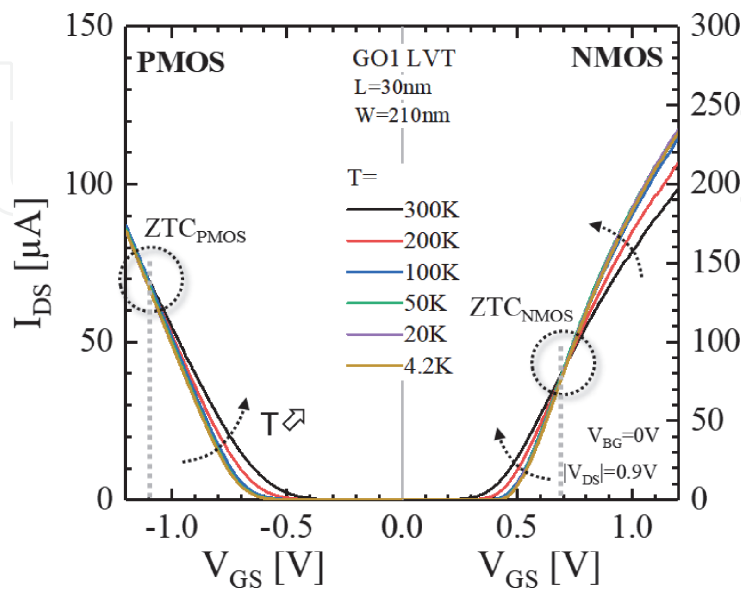
(a) Delay per stage versus temperature of a 101-stages RO ( $L = 34$  nm,  $W_{NMOS} = 420$  nm,  $W_{PMOS} = 600$  nm) for different supply voltages  $V_{DD} = 0.8$ ,  $1$ , and  $1.2$  V showing the RO slowing down due to the increase of  $V_{TH}$  at low temperature. (b) Delay per stage versus temperature for  $V_{DD} = 0.8$ ,  $1$ , and  $1.2$  V in the case of compensated  $V_{TH}$ . The RO speeds up at low temperature due to the carrier mobility enhancement (from Bohuslavskyi et al. [77]).

**Figure 32a** shows the evolution of  $I_{EFF}$  as a function of temperature, in the case where no  $V_{BG}$  is applied. We observed that  $I_{EFF}$  decreases with temperature, and this decrease is stronger as  $V_{DD}$  is decreased (3 decades degradation from 300 K to 4.2 K for  $V_{DD} = 0.8$  V). This  $I_{EFF}$  variation is linked with the temperature dependence of  $I_{DS}$ - $V_{GS}$  curves. A zero-temperature coefficient point (ZTC), corresponding to a gate voltage for which the drain current exhibits no temperature dependence, is systematically observed on the measured  $I_{DS}$  vs.  $V_{GS}$  curves, as illustrated in **Figure 33** and already evidenced in **Figures 4** and **17** [79]. For  $|V_{GS}| < |V_{ZTC}|$  the drain current decreases as  $T$  decreases ( $\partial I_{DS}/\partial T|_{V_{GS} = cte} > 0$ ), whereas for



**Figure 32.**

(a) Effective current  $I_{EFF}$  measured on single NMOS and PMOS transistors ( $L = 34$  nm,  $W_{NMOS} = 210$  nm,  $W_{PMOS} = 300$  nm) for different supply voltages  $V_{DD} = 0.8, 1$ , and  $1.2$  V; the effective current decreases as the temperature is reduced. (b)  $I_{EFF}$  versus temperature for  $V_{DD} = 0.8, 1$ , and  $1.2$  V in the case of compensated  $V_{TH}$ ; in that case the effective current increases as the temperature is reduced (from Bohuslavskyi et al. [77]).



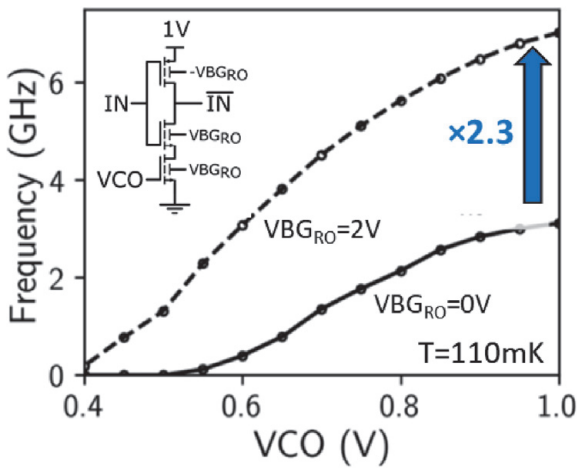
**Figure 33.**

(a) Drain current  $I_{DS}$  measured on single NMOS and PMOS transistors ( $L = 30$  nm,  $W_{NMOS} = W_{PMOS} = 210$  nm) as a function of gate voltage  $V_{GS}$  for different temperature from 300 K down to 4.2 K. A zero temperature coefficient (ZTC) point for which the drain current ( $I_{DS}$ ) is independent of the temperature is evidenced for NMOS and PMOS.

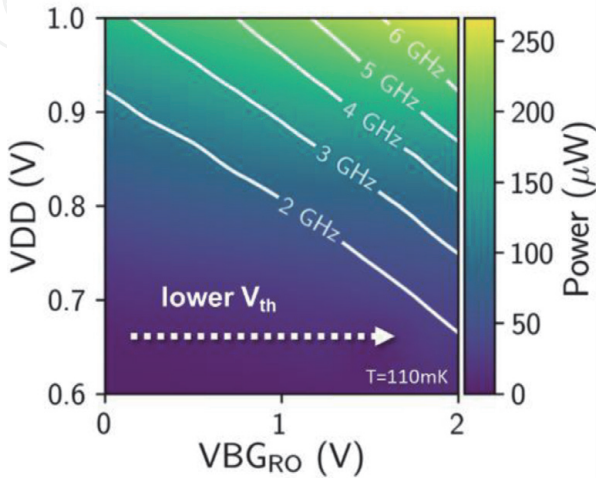
$|V_{GS}| > |V_{ZTC}|$  the drain current exhibits an opposite temperature behavior ( $\partial I_{DS} / \partial T|_{V_{GS} = cte} < 0$ ).

It is worth noticing that for the pMOS the ZTC point is located at higher  $|V_{GS}|$  ( $\approx 1.1$  V) compared to the nMOS devices ( $\approx 0.7$  V). The  $I_{EFF}$  temperature dependence is mainly driven by the region with positive T-dependence  $\partial I_{DS} / \partial T|_{V_{GS} = cte}$ , i.e. for  $|V_{GS}|$  below  $|V_{ZTC}|$ .

If a back bias  $V_{BG}$  is applied, it is possible to shift the threshold voltage back to its room temperature value (**Figure 6**). In that configuration, the drain current  $I_{DS}$  increases with the temperature decrease whatever  $V_{GS}$  and  $V_{DS}$  values, due to mobility and saturation velocity improvement with T decrease at a given  $|V_{GS} - V_{TH}|$  overdrive gate voltage (see **Section 2.4**). Consequently, the effective current  $I_{EFF}$  follows the same trend with respect to T (**Figure 32b**). Thus a correctly chosen forward back bias on NMOS and PMOS will lead to a speed-up of the RO as T decreases (**Figure 31b**). At a given temperature, the back biasing  $V_{BG}$  allows to tune the frequency as illustrated in **Figure 34**. Finally by playing with the supply voltage  $V_{DD}$  and  $V_{BG}$  it is also possible to manage power consumption and performance [30, 77]. It has been illustrated at 110mK on a VCO RO (**Figure 35**) where back bias allows switching from low power mode (e.g. 27  $\mu$ W at 2GHz) to high performance mode (e.g. 6.9GHz for 268  $\mu$ W).



**Figure 34.** Oscillating frequency as a function of VCO voltage for a VCO RO ( $L = 28$  nm). Forward Back-biasing increases maximal frequency (from Guevel et al. [30]).



**Figure 35.** Power as a function of supply voltage  $V_{DD}$  and back bias voltage  $V_{BGRO}$  ( $L = 28$  nm). Forward back-biasing decreases power for same frequency (from Guevel et al. [30]).

## 7. Summary and conclusions

A review of recent results obtained on 28 nm FDSOI transistors operated down to deep cryogenic temperatures has been presented. First, the main device electrical properties in terms of gate capacitance and charge control and drain current transfer characteristics have been discussed along with the temperature dependence of the major MOSFET parameters (threshold voltage, subthreshold swing and mobility). Then, the self-heating phenomena were characterized in details, providing valuable information about the actual device temperature versus power dissipation, as well as the thermal resistance that limits the heat dissipation in the FDSOI structure, especially at low temperature. The matching properties have then been studied owing to threshold voltage and drain current statistical variability analysis, revealing that the mismatch in FDSOI transistors only increases of about 30–40% at deep-cryogenic temperatures. Besides, Poisson-Schrodinger simulations have been carried out with success down to zero Kelvin, giving access to valuable information about the gate charge control in FDSOI structures versus temperature, and, providing physical insight to the development of compact model mandatory for FDSOI circuit design at deep cryogenic temperatures. Finally, the operation of elementary circuits such as ring oscillators and voltage controlled oscillators has been demonstrated in terms of inverter delay and clock frequency down to deep-cryogenic temperatures.

This work highlights the powerful advantage of FDSOI over bulk technology, led by the back biasing capability. It offers in particular an efficient way to manage power consumption and performance, thus mitigating thermal effects, which are crucial aspects in cryo-electronics.

## Acknowledgements

This work was partially supported by the French Authorities within the frame of NANO2022 project, and by the ERC Synergy QuCube (Grant No. 810504 — QUCUBE — ERC-2018-SyG), and EU H2020 RIA project SEQUENCE (Grant No. 871764).

## Author details


Mikaël Cassé<sup>1</sup> and Gérard Ghibaudo<sup>2\*</sup>

<sup>1</sup> Université Grenoble Alpes, CEA-LETI, Minatec, Grenoble, France

<sup>2</sup> Université Grenoble Alpes, IMEP-LAHC, Minatec, Grenoble, France

\*Address all correspondence to: ghibaudo@minatec.inpg.fr

## IntechOpen

© 2021 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the Creative Commons Attribution License (<http://creativecommons.org/licenses/by/3.0>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited. 

## References

- [1] R. R. Green, "MOSFET operation at 4.2 K," *Review of Scientific Instruments*, vol. 39, no. 10, pp. 1495–1497, 1968, doi: 10.1063/1.1683144.
- [2] C. G. Rogers, "MOST's at cryogenic temperatures," *Solid-State Electronics*, vol. 11, no. 11, pp. 1079–1091, 1968, doi: 10.1016/0038-1101(68)90130-5.
- [3] W. E. Howard and F. F. Fang, "Low temperature effects in Si FETs," *Solid-State Electronics*, vol. 8, no. 1, pp. 82–83, 1965, doi: [https://doi.org/10.1016/0038-1101\(65\)90011-0](https://doi.org/10.1016/0038-1101(65)90011-0).
- [4] K. v. Klitzing, G. Dorda, and M. Pepper, "New Method for High-Accuracy Determination of the Fine-Structure Constant Based on Quantized Hall Resistance," *Phys. Rev. Lett.*, vol. 45, no. 6, pp. 494–497, Aug. 1980, doi: 10.1103/PhysRevLett.45.494.
- [5] R. K. Kirschman, "Cold electronics: an overview," *Cryogenics*, vol. 25, no. August 1984, pp. 115–122, 1985, doi: 10.1016/0011-2275(85)90036-0.
- [6] E. A. Gutiérrez, J. Deen, and C. Claeys, *Low temperature electronics: physics, devices, circuits, and applications*. Academic Press, 2000.
- [7] F. Balestra and G. Ghibaudo, *Device and Circuit Cryogenic Operation for Low Temperature Electronics*. 2001.
- [8] J. M. Hornibrook *et al.*, "Cryogenic Control Architecture for Large-Scale Quantum Computing," vol. 024010, pp. 1–9, 2015, doi: 10.1103/PhysRevApplied.3.024010.
- [9] E. Charbon *et al.*, "Cryo-CMOS for Quantum Computing," *IEEE International Electron Devices Meeting (IEDM)*, pp. 343–346, 2016, doi: 10.1109/ICRC.2017.8123682.
- [10] X. Xue *et al.*, "CMOS-based cryogenic control of silicon quantum circuits," 2020, [Online]. Available: <http://arxiv.org/abs/2009.14185>.
- [11] J. P. G. van Dijk *et al.*, "Impact of Classical Control Electronics on Qubit Fidelity," *Physical Review Applied*, vol. 12, no. 4, p. 1, 2019, doi: 10.1103/PhysRevApplied.12.044054.
- [12] J. C. Bardin *et al.*, "Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, 2019, doi: 10.1109/JSSC.2019.2937234.
- [13] E. Charbon, "Cryo-CMOS Electronics for Quantum Computing Applications," in *Proceedings of European Solid-State Device Research Conference*, 2019, pp. 1–6.
- [14] D. J. Reilly, "Challenges in Scaling-up the Control Interface of a Quantum Computer," *IEDM Technical Digest. IEEE International Electron Devices Meeting*, pp. 745–750, 2019.
- [15] R. M. Incandela, L. Song, and H. A. R. Homulle, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society*, vol. 6, no. January, pp. 996–1006, 2018, doi: 10.1109/JEDS.2018.2821763.
- [16] S. J. Pauka *et al.*, *A Cryogenic Interface for Controlling Many Qubits*. arXiv:1912.01299v1, 2019.
- [17] B. Patra *et al.*, "A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for  $4 \times 32$  Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers: Visuals," 2020.

- [18] F. Sebastiano *et al.*, “Cryo-CMOS Interfaces for Large-Scale Quantum Computers,” in *IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 525–528.
- [19] F. Balestra and G. Ghibaudo, “Physics and performance of nanoscale semiconductor devices at cryogenic temperatures,” *Semiconductor Science and Technology*, vol. 32, no. 2, 2017, doi: 10.1088/1361-6641/32/2/023002.
- [20] B. Dierickx, L. Warmerdam, E. R. Simoen, J. Vermeiren, and C. Claeys, “Model for hysteresis and kink behavior of MOS transistors operating at 4.2 K,” *IEEE Transactions on Electron Devices*, vol. 35, no. 7, pp. 1120–1125, 1988, doi: 10.1109/16.3372.
- [21] E. Simoen, B. Dierickx, L. Warmerdam, J. Vermeiren, and C. Claeys, “Freeze-Out Effects on NMOS Transistor Characteristics at 4.2 K,” *IEEE Transactions on Electron Devices*, vol. 36, no. 6, pp. 1155–1161, 1989, doi: 10.1109/16.24362.
- [22] F. Balestra and G. Ghibaudo, “Brief review of the MOS device physics for low temperature electronics,” *Solid-State Electronics*, vol. 37, no. 12, pp. 1967–1975, 1994.
- [23] T. Lu, Z. Li, C. Luo, J. Xu, W. Kong, and G. Guo, “Characterization and Modeling of 0.18 $\mu\text{m}$  Bulk CMOS Technology at sub-Kelvin Temperature,” *IEEE Journal of the Electron Devices Society*, vol. 8, no. June, pp. 1–1, 2020, doi: 10.1109/jeds.2020.3015265.
- [24] A. Rhouni, O. Gevin, X. de la Broïse, J. L. Sauvageot, V. Revéret, and L. Rodriguez, “First-ever test and characterization of the AMS standard bulk 0.35  $\mu\text{m}$  CMOS technology at sub-kelvin temperatures,” *Journal of Physics: Conference Series*, vol. 834, p. 012005, May 2017, doi: 10.1088/1742-6596/834/1/012005.
- [25] R. M. Incandela, L. Song, H. A. R. Homulle, F. Sebastiano, E. Charbon, and A. Vladimirescu, “Nanometer CMOS Characterization and Compact Modeling at Deep-Cryogenic Temperatures,” no. 10, pp. 58–61, 2017.
- [26] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschiroto, and C.ENZ, “Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing,” in *Proceedings of European Solid-State Device Research Conference*, 2017, pp. 62–65, doi: 10.1109/ESSDERC.2017.8066592.
- [27] B. Cretu, D. Boudier, E. Simoen, A. Veloso, and N. Collaert, “Assessment of DC and low-frequency noise performances of triple-gate FinFETs at cryogenic temperatures,” *Semiconductor Science and Technology*, vol. 31, no. 12, 2016, doi: 10.1088/0268-1242/31/12/124006.
- [28] M. Shin *et al.*, “Low temperature characterization of 14nm FDSOI CMOS devices,” in *International Workshop on Low Temperature Electronics (WOLTE)*, Grenoble, France, 2014, pp. 29–32, doi: 10.1109/WOLTE.2014.6881018.
- [29] H. Bohuslavskyi *et al.*, “28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing,” in *IEEE Silicon Nanoelectronics Workshop (SNW)*, 2017, pp. 143–144, doi: 10.23919/SNW.2017.8242338.
- [30] L. L. Guevel *et al.*, “A 110mK 295  $\mu\text{W}$  28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot: Visuals,” 2020.
- [31] L. Nyssens *et al.*, “28-nm FD-SOI CMOS RF Figures of Merit down to 4.2 K,” *IEEE Journal of the Electron Devices Society*, vol. 8, no. June, pp. 646–654, 2020, doi: 10.1109/JEDS.2020.3002201.

- [32] S. Bonen *et al.*, “Cryogenic Characterization of 22-nm FDSOI CMOS Technology for Quantum Computing ICs,” *IEEE Electron Device Letters*, vol. 40, no. 1, pp. 127–130, 2019, doi: 10.1109/LED.2018.2880303.
- [33] H. J. Park, M. Bawedin, H. G. Choi, and S. Cristoloveanu, “Kink effect in ultrathin FDSOI MOSFETs,” *Solid-State Electronics*, vol. 143, pp. 33–40, 2018, doi: <https://doi.org/10.1016/j.sse.2017.12.002>.
- [34] C. Enz, A. Beckers, and F. Jazaeri, “Cryo-CMOS Compact Modeling,” *IEEE International Electron Devices Meeting (IEDM)*, no. 871764, pp. 529–532, 2020.
- [35] J.-P. Noel *et al.*, “Multi-VT UTBB FDSOI Device Architectures for Low-Power CMOS Circuit,” *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2473–2482, 2011.
- [36] M. Kantner and T. Koprucki, “Numerical simulation of carrier transport in semiconductor devices at cryogenic temperatures,” *Optical and Quantum Electronics*, vol. 48, no. 12, p. 543, Nov. 2016, doi: 10.1007/s11082-016-0817-2.
- [37] S. S. Sesnic and G. R. Craig, “Thermal Effects in JFET and MOSFET at Cryogenic Temperatures,” *IEEE Transactions on Electron Devices*, vol. 19, no. 8, pp. 933–942, 1972.
- [38] D. P. Foty and S. L. Titcomb, “Thermal Effects in n-Channel Enhancement MOSFET’s Operated at Cryogenic Temperatures,” *IEEE Transactions on Electron Devices*, vol. 34, no. 1, pp. 107–113, 1987, doi: 10.1109/T-ED.1987.22892.
- [39] N. Planes *et al.*, “28nm FDSOI technology platform for high-speed low-voltage digital applications,” in *Symposium on VLSI Technology, Digest of Technical Papers*, 2012, vol. 33, no. 4, pp. 133–134, doi: 10.1109/VLSIT.2012.6242497.
- [40] B. Cardoso Paz *et al.*, “Electrostatics and channel coupling on 28 nm FD-SOI for cryogenic applications,” in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, 2020, p. 1.
- [41] M. Aouad, S. Martinie, T. Poiroux, and G. Ghibaudo, “Poisson-Schrodinger simulation of inversion charge in FDSOI MOSFET down to 0K – Towards compact modeling for cryo CMOS application,” in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Caen, France, 2020, p. 1.
- [42] T. A. Karatsori, G. Ghibaudo, C. Dimitriadis, and C. Theodorou, “Influence of AC signal oscillator level on effective mobility measurement by split C-V technique in MOSFETs,” *Electronics Letters*, vol. 52, 2016, doi: 10.1049/el.2016.1715.
- [43] B. Cardoso Paz *et al.*, “Performance and Low-Frequency Noise of 22-nm FDSOI down to 4.2 K for Cryogenic Applications,” *IEEE Transactions on Electron Devices*, vol. 67, no. 11, 2020, doi: 10.1109/TED.2020.3021999.
- [44] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, vol. 25. 2002.
- [45] B. Cardoso Paz *et al.*, “Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing,” in *Symposium on VLSI Technology, Digest of Technical Papers*, 2020, p. TN2.1.
- [46] E. Arnold, “Disorder-induced carrier localization in silicon surface inversion layers,” *Applied Physics Letters*, vol. 25, no. 12, pp. 705–707, 1974, doi: 10.1063/1.1655369.

- [47] H. Bohuslavskyi *et al.*, “Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs Described With Band Broadening,” *IEEE Electron Device Letters*, vol. 40, no. 5, pp. 784–787, 2019, doi: 10.1109/LED.2019.2903111.
- [48] G. Ghibaudo, M. Aouad, M. Cassé, S. Martinie, T. Poiroux, and F. Balestra, “On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature,” *Solid-State Electronics*, vol. 170, no. April, p. 107820, 2020, doi: 10.1016/j.sse.2020.107820.
- [49] B. Cardoso Paz, “Front and back channels coupling and transport on 28 nm FD-SOI MOSFETs down to liquid-He temperature,” *Solid State Electronics*, 2021.
- [50] M. Cassé *et al.*, “Evidence of 2D intersubband scattering in thin film fully depleted silicon-on-insulator transistors operating at 4.2 K,” *Applied Physics Letters*, vol. 116, p. 243502, 2020, doi: 10.1063/5.0007100.
- [51] B. M. Tenbroek, M. S. L. Lee, W. Redman-white, R. J. T. Bunyan, and M. J. Uren, “Self -Heating Effects in SOI MOSFET’s and their measurement by small signal conductance techniques,” *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2240–2248, 1996.
- [52] C. Xu, S. K. Kolluri, and K. Endo, “Analytical Thermal Model for Self-Heating in Advanced FinFET Devices With Implications for Design and Reliability,” *IEEE Trans on Computer-Aided Design Int. Circ. Syst.*, vol. 32, no. 7, pp. 1045–1058, 2013.
- [53] C. Prasad, L. Jiang, D. Singh, M. Ag, J. Thomas, and P. Vandervoorn, “Self-heat Reliability Considerations on Intel’s 22nm Tri i-Gate Technology,” in *IEEE International Reliability Physics Symposium (IRPS)*, 2013, pp. 1–5.
- [54] C. Prasad, S. Ramey, and L. Jiang, “Self-heating in advanced CMOS technologies,” in *IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 6A–4.1–6A–4.7, doi: 10.1109/IRPS.2017.7936336.
- [55] K. Triantopoulos *et al.*, “Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K,” *IEEE Transactions on Electron Devices*, vol. 66, no. 8, 2019, doi: 10.1109/TED.2019.2919924.
- [56] P. G. Mautry and J. Trager, “Self-heating and Temperature Measurement in Sub- $\mu$ m-MOSFETs,” *ESSDERC ’89: 19th European Solid State Device Research Conference*, pp. 675–678, 1989.
- [57] T. Takahashi, T. Matsuki, T. Shinada, Y. Inoue, and K. Uchida, “Direct evaluation of self-heating effects in bulk and ultra-thin BOX SOI MOSFETs using four-terminal gate resistance technique,” *IEEE Journal of the Electron Devices Society*, vol. 4, no. 5, pp. 365–373, 2016, doi: 10.1109/JEDS.2016.2568261.
- [58] A. Beckers, F. Jazaeri, and C. Enz, “Cryogenic MOS Transistor Model,” *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018, doi: 10.1109/TED.2018.2854701.
- [59] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, “Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures,” *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 996–1006, 2018, doi: 10.1109/JEDS.2018.2821763.
- [60] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, “Design-oriented Modeling of 28 nm FDSOI CMOS Technology down to 4.2 K for Quantum Computing,” *2018 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS)*,

pp. 1–4, Mar. 2018, doi: 10.1109/  
ULIS.2018.8354742.

[61] P. A. 't Hart, J. P. G. van Dijk, M. Babaie, E. Charbon, A. Vladimircscu, and F. Sebastiano, "Characterization and Model Validation of Mismatch in Nanometer CMOS at Cryogenic Temperatures," in *2018 48th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2018, pp. 246–249, doi: 10.1109/ESSDERC.2018.8486859.

[62] B. Cardoso Paz *et al.*, "Integrated Variability Measurements of 28 nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications," in *IEEE International Conference on Microelectronic Test Structures*, 2020, vol. 2020-May, pp. 8–12, doi: 10.1109/ICMTS48187.2020.9107906.

[63] H. Bohuslavskyi *et al.*, "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs described with Band Broadening," *IEEE Electron Device Letters*, pp. 1–1, 2019, doi: 10.1109/LED.2019.2903111.

[64] A. Beckers, F. Jazaeri, and C. Enz, "Revised theoretical limit of the subthreshold swing in field-effect transistors," *arXiv:1811.09146 [cond-mat]*, Nov. 2018, Accessed: Aug. 08, 2019. [Online]. Available: <http://arxiv.org/abs/1811.09146>.

[65] J. Mazurier, O. Weber, F. Andrieu, C. L. Royer, O. Faynot, and M. Vinet, "Variability of planar Ultra-Thin Body and Buried oxide (UTBB) FDSOI MOSFETs," in *2014 IEEE International Conference on IC Design Technology*, May 2014, pp. 1–4, doi: 10.1109/ICICDT.2014.6838617.

[66] E. G. Ioannidis, C. G. Theodorou, S. Haendler, E. Josse, C. A. Dimitriadis, and G. Ghibaudo, "Impact of Source – Drain Series Resistance on Drain Current Mismatch in Advanced Fully Depleted SOI n-MOSFETs," *IEEE Electron Device Letters*, vol. 36, no. 5,

pp. 433–435, 2015, doi: 10.1109/  
LED.2015.2411289.

[67] A. P. Gnädinger and H. E. Talley, "Quantum mechanical calculation of the carrier distribution and the thickness of the inversion layer of a MOS field-effect transistor," *Solid-State Electronics*, vol. 13, no. 9, pp. 1301–1309, 1970, doi: [https://doi.org/10.1016/0038-1101\(70\)90027-4](https://doi.org/10.1016/0038-1101(70)90027-4).

[68] S. R. Ekanayake, T. Lehmann, A. S. Dzurak, R. G. Clark, and A. Brawley, "Characterization of SOS-CMOS FETs at low temperatures for the design of integrated circuits for quantum bit control and readout," *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 539–547, 2010, doi: 10.1109/TED.2009.2037381.

[69] S. J. Pauka *et al.*, "Characterizing Quantum Devices at Scale with Custom Cryo-CMOS," *Physical Review Applied*, vol. 13, no. 5, p. 1, 2020, doi: 10.1103/PhysRevApplied.13.054072.

[70] I. D. Conway Lamb *et al.*, "An FPGA-based instrumentation platform for use at deep cryogenic temperatures," *Review of Scientific Instruments*, vol. 87, no. 1, p. 014701, 2016, doi: 10.1063/1.4939094.

[71] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. D. Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures ☆," *Solid State Electronics*, vol. 159, no. 688539, pp. 106–115, 2019, doi: 10.1016/j.sse.2019.03.033.

[72] C. Enz, A. Beckers, and F. Jazaeri, "Cryo-CMOS Compact Modeling," in *IEEE International Electron Devices Meeting (IEDM)*, 2020, no. 871764.

[73] E. D. Buchanan, D. J. Benford, J. B. Forgione, S. H. Moseley, and E. J. Wollack, "Cryogenic applications of

commercial electronic components,”  
Cryogenics, vol. 52, no. 10, pp. 550–556,  
2012, doi: 10.1016/j.  
cryogenics.2012.06.017.

[74] E. Schriek, F. Sebastiano, and E.  
Charbon, “A Cryo-CMOS Digital Cell  
Library for Quantum Computing  
Applications,” IEEE Solid-State Circuits  
Letters, vol. 3, pp. 310–313, 2020, doi:  
10.1109/LSSC.2020.3017705.

[75] J. P. G. van Dijk *et al.*, “A Scalable  
Cryo-CMOS Controller for the  
Wideband Frequency-Multiplexed  
Control of Spin-Qubits and  
Transmons,” IEEE Journal of Solid-State  
Circuits, vol. 55, no. 11, pp. 2930–2946,  
2020.

[76] J. Gong, Y. Chen, F. Sebastiano, E.  
Charbon, and M. Babaie, “A 200dB  
FOM 4-5GHz Cryogenic Oscillator with  
an Automatic Common-Mode  
Resonance Calibration for Quantum  
Computing Applications:  
Visuals,” 2020.

[77] H. Bohuslavskyi *et al.*, “Cryogenic  
Characterization of 28-nm FD-SOI Ring  
Oscillators With Energy Efficiency  
Optimization,” IEEE Transactions on  
Electron Devices, vol. 65, no. 9,  
pp. 3682–3688, 2018.

[78] M. H. Na, E. J. Nowak, W. Haensch,  
and J. Cai, “The effective drive current  
in CMOS inverters,” *IEEE International  
Electron Devices Meeting (IEDM)*,  
pp. 121–124, 2002, doi: 10.1109/  
IEDM.2002.1175793.

[79] K. Triantopoulos, M. Cassé, L.  
Brunet, P. Batude, G. Reimbold, and G.  
Ghibaudo, “Self-heating assessment and  
cold current extraction in FDSOI  
MOSFETs,” San Francisco, 2017, doi:  
10.1109/S3S.2017.8309239.